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Test Methods for Switching Energy Loss Associated with Output Capacitance Hysteresis in Semiconductor Power Devices

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TEST METHODS FOR SWITCHING ENERGY LOSS ASSOCIATED WITH OUTPUT CAPACITANCE HYSTERESIS IN SEMICONDUCTOR POWER DEVICES

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Foreword

This document was drafted by JEDEC JC-70.1 GaN and JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittees consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use in the power semiconductor and related power electronic industries and provides guidelines for a series of test methods and circuits to be used for measuring the switching energy loss due to output capacitance hysteresis in semiconductor power devices. The selection of a specific test method and circuit among those proposed by this document remains at user's discretion depending on the requirements in terms of accuracy, simplicity, cost, time, compatibility, or any other criteria.

Introduction

Switching energy loss in power transistors has been usually idealized to near-zero in soft-switched power circuits like resonant or zero-voltage switching converters. This assumption follows the approach that all the energy stored in the transistor output capacitance (C_{OSS}) is recovered at the end of one cycle. In modern soft-switched converters, the increase in switching frequencies has evidenced an incomplete C_{OSS} energy recovery that is related to mechanisms other than channel or forward conduction.

Differently, in hard-switched power circuits, the process of C_{OSS} charge and discharge in power transistors is typically counted to contribute to the switching energy losses as the total energy stored in the output capacitance (E_{OSS}) is eventually dissipated in the channel as a Joule heat. In its turn, E_{OSS} is normally inferred from C_{OSS} measurements in accordance with JEDEC standards [1], [2] and other standards [3], [4]. In all these standards there is a lack of information regarding the test circuit and methodology to extract the energy from charge or capacitances. Moreover, these standards are based on small-signal measurements, which means that the capacitance measurement between terminals of a semiconductor device is carried out with an impedance analyzer that uses a sinusoidal signal with high-frequency (100 kHz-1 MHz) and small amplitude (~100 mV).

In [5] it was demonstrated that C_{OSS} extracted by large-signal and small-signal techniques may differ in power transistors, thus exhibiting a hysteresis effect in the large-signal. In fact, the process of charging and discharging C_{OSS} when a transistor is held in off-state may imply a non-negligible loss of energy. Analogously, power rectifiers are also susceptible to show C_{OSS} hysteresis and energy loss by charging and discharging their anode-to-cathode capacitance (C_{AK}) without an intermediate forward conduction process [6]. The aforementioned energy loss for power transistors and diodes is named in this document as $E_{OSS,H}$ indifferently of device type.

TEST METHODS FOR SWITCHING ENERGY LOSS ASSOCIATED WITH OUTPUT CAPACITANCE HYSTERESIS IN SEMICONDUCTOR POWER DEVICES

(From JEDEC Board Ballot JCB-24-10, formulated under the cognizance of JC-70.1 GaN and JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittees.)

1 Scope

The test methods in this document describe a means of measuring the switching losses related to output capacitance hysteresis in semiconductor power devices. The test methods can be normally applied to the following discrete packaged devices:

a) Silicon power devices –diodes, JFETs, MOSFETs.
b) SiC power devices – diodes, JFETs, MOSFETs, cascodes
c) GaN power devices – diodes, MOSFETs, eHEMTs, dHEMTs, cascodes

This document does not exclude other type of transistors and discrete or integrated power devices in other semiconductor materials. The methodologies covered herein are valid at the wafer level for technology characterization, with proper consideration of the probe connections and their impacts on results.

2 Terms, Definitions and Letter Symbols

DUT	Device Under Test
ZVS	Zero Voltage Switching
V_{IN}	input supply voltage
L	inductance
R	resistance
C	capacitance
f	frequency
i_D	drain current of DUT, time-varying
i_L	current through inductor, time-varying
$V_{DS(OFF)}$	drain to source voltage of DUT in OFF-state, dc component
$V_{GS(ON)}$	gate to source voltage of DUT in ON-state, dc component
$V_{GS(OFF)}$	gate to source voltage of DUT in OFF-state, dc component
v_{DS}	drain to source voltage of DUT, time-varying
v_{GS}	gate to source voltage of DUT, time-varying
t_r	rise time of the signal measured
t_f	fall time of the signal measured
I_{IN}	input current in a test circuit
I_{OUT}	output current in a test circuit
C_{OSS}	output capacitance
E_{OSS}	total energy stored in output capacitance
$E_{OSS,H}$	energy loss due to C_{OSS} hysteresis
T_J	junction temperature
T_C	case temperature
T_{REF}	reference temperature
P_D	dissipated power
R_{th}	thermal resistance

3 Test Circuits

3.1 Generic Test Circuit

In order to measure $E_{OSS,H}$ in semiconductor power devices, the conceptual scheme represented in Figure 1 is recommended. In this scheme, the DUT is a power rectifier or a power transistor that is held in off-state during the charging and discharging process without any intermediate on-state or concurrent channel current. With the objective to ensure a total absence of channel conduction in transistors, the gate and source terminals are electrically shorted or connected to a negative voltage with a low-inductive connection. Under these conditions, the DUT is represented by a two-terminal device with its output capacitance (C_{OSS} or C_{AK}) defined between these two terminals.

As indicated in Figure 1, the two DUT terminals are connected to a test circuit that generates a single or a periodical voltage excitation for charging and discharging the DUT output capacitance. This voltage signal may have an arbitrary shape, nonetheless rectangular and sinusoidal voltage waveforms are preferable to match the stimulus of certain applications. A test circuit can apply the voltage excitation to a single DUT but there is also the possibility to test multiple DUTs at the same time by merely parallelizing or by using dedicated topologies.

It is important that, at least during the time interval where $E_{OSS,H}$ is calculated, the electrical excitation applied to the DUT does not activate forward conduction in the power rectifier or any type of first or third quadrant conduction for the case of power transistors (e.g., conduction of parasitic diode highlighted in blue in Figure 1). In addition, the maximum voltage during the electrical excitation (v_{MAX}) must never reach the power rectifier or power transistor avalanche voltage or any other voltage limit that involves a significant increase of the leakage current. Anyone of these mechanisms would originate additional losses and, therefore, the impossibility to properly measure $E_{OSS,H}$ as an isolated physical quantity.

As per the impact of the package parasitics, as long as their action does not enable any one of the mentioned additional losses, they are not relevant in the test circuits and methods described here.

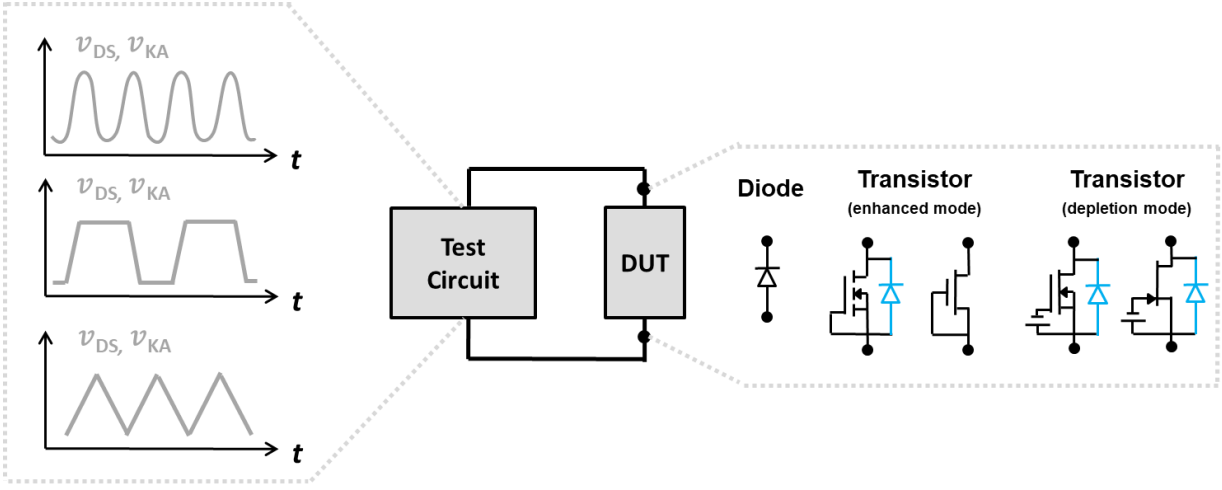

Figure 1 — Conceptual Scheme of a Test Circuit to Measure $E_{OSS,H}$ in Semiconductor Power Devices

3.2 Sawyer-Tower Test Circuits

A more specific form for the generic circuit in 3.1 is a test circuit constituted by a signal generator, a charge integrator and a DUT. This circuit arrangement, schematically described in Figure 2, is commonly known as Sawyer-Tower test circuit. Several variants of Sawyer-Tower test circuit have been reported in technical and scientific literature for testing semiconductor power devices.

Figure 3a shows the most widely used variant, referred here as Standard Sawyer-Tower test circuit. As main features, the charge integrator is a reference capacitor (C_{REF}) and the signal generator is mainly composed of a power amplifier to eventually apply a high-voltage sinusoidal excitation between the two terminals of the DUT. Due to the programmability of the power amplifier, this circuit allows a high degree of flexibility and automation for testing $E_{OSS,H}$ at different signal frequencies and amplitudes.

Figure 3b depicts the Half-Bridge Sawyer-Tower test circuit. Differently from the Standard case, the signal generator is built with a half-bridge circuit. This allows to replicate the rectangular voltage waveform seen in most of the soft-switching power circuits, like LLC resonant converters, phase-shifted ZVS full-bridge converters and active clamp flybacks, among others. A key feature of the rectangular voltage waveform is the slew rate, which is adjustable by means of the inductance L_O, the half-bridge equivalent capacitance, the operation frequency and/or the external voltage V_{IN}.

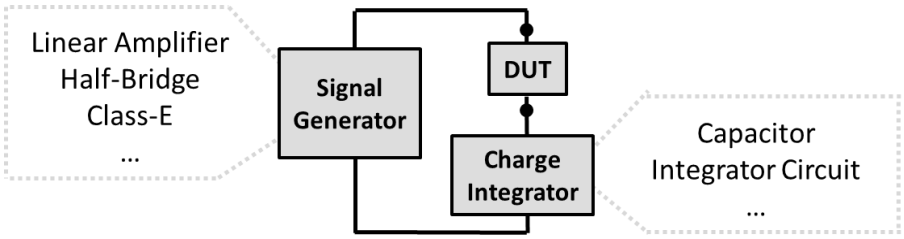

Figure 2 — Conceptual Scheme of the Sawyer-Tower Test Circuit

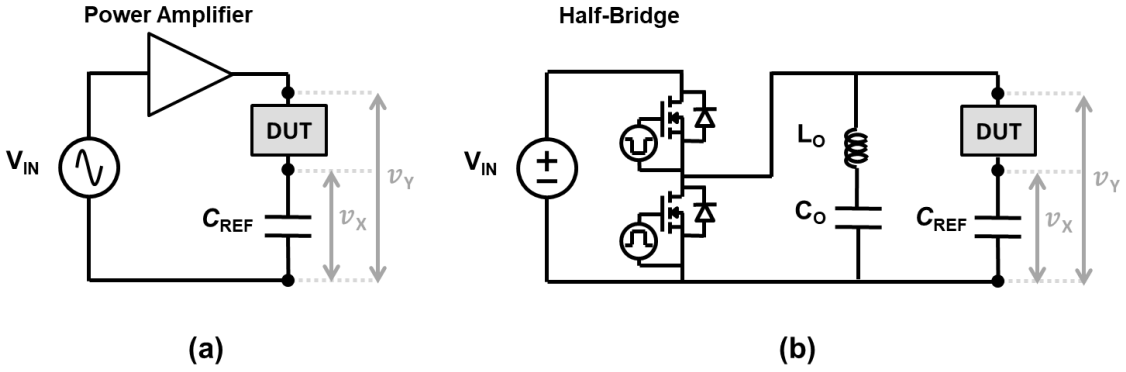

Figure 3 — Schematic Representation of (a) Standard Sawyer-Tower Test Circuit [7, 8, 9] and (b) Half-Bridge Sawyer-Tower Test Circuit [9, 10]

3.2 Sawyer-Tower Test Circuits (cont'd)

In both Standard and Half-Bridge Sawyer-Tower test circuits, the selection of C_{REF} is crucial for the measurement precision. C_{REF} must be a low-loss linear capacitor within the confines of the operating conditions including the range of frequency, positive and negative voltage slew-rate, voltage magnitude, and temperature used during the measurement. More concretely, it is required a C_{REF} with a substantially lower dissipation factor than the DUT and with a constant capacitance. These capacitor features can be achieved by using a dielectric material having constant and real permittivity, low equivalent series resistance, low parasitic inductance, and small leakage current. C_{REF} forms a voltage divider with DUT's C_{OSS}, subsequently C_{REF} must be small enough to provide a measurable voltage but large enough to keep most of the voltage v_Y dropped across the DUT. Typical values for C_{REF} are approximately five to ten times the value of DUT's C_{OSS} at $V_{DS(OFF)}$ = 0 V.

3.3 Other Test Circuits

There are a large variety of test circuits other than Sawyer-Tower that have been reported in literature to measure $E_{OSS,H}$ in semiconductor power devices. Most of these circuits omit an element for charge integration but still fit in the generic description of 3.1. Despite Sawyer-Tower being superior in terms of accuracy, other circuits may offer additional advantages and may be a better alternative depending on the DUT type and on the measuring conditions.

The Non-Linear Resonance or Unclamped Inductive Switching test circuit in Figure 4a is used to measure $E_{OSS,H}$ in power transistors [11, 17, 18, 19, 20]. It works by the principle that DUT's C_{OSS} is charged when the inductive load L_1 is discharged. L_1 becomes initially charged when the DUT is in on-state whereas C_{OSS} is charged after the DUT is turned-off. V_{IN} needs to be positive to allow charging L_1 but it will remain relatively low with respect to the v_{DS} maximum amplitude (v_{MAX}), thus enabling to sweep v_{DS} through a wide range. Aside from being a relatively simple test circuit, another advantageous feature is the possibility to extract $E_{OSS,H}$ by averaging over multiple cycles (in steady-state conditions) or from a single cycle, where the DUT self-heating is eliminated.

The test circuits in Figure 4c and Figure 4d were reported in [5, 13] and [12], respectively. These test circuits stimulate the DUT with a rectangular voltage waveform. The ZVS test circuit in Figure 4c is capable to test two DUTs consecutively, whereas the resistive load switch test circuit in Figure 4d allows to tune the slew rate by means of resistances. Some resonant circuits, like power circuits based on RF amplifiers in [6], stimulate the DUT with a periodical voltage signal that is neither rectangular nor sinusoidal (Figure 4b).

3.3 Other Test Circuits (cont'd)

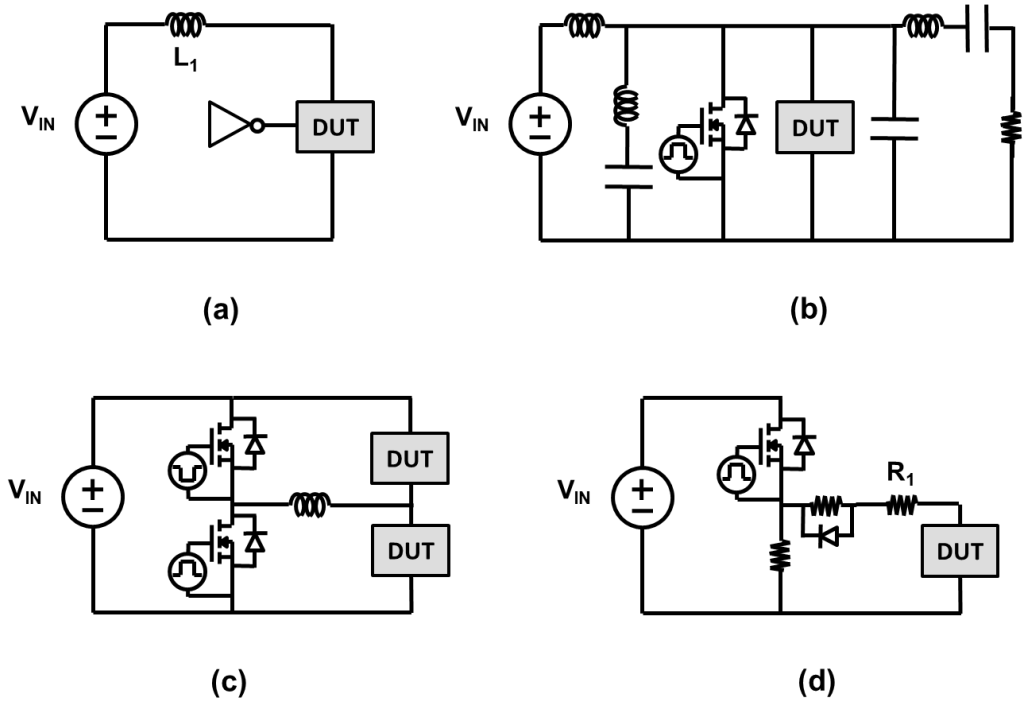

Figure 4 — Schematic Representation of (a) Non-Linear Resonance or Unclamped Inductive Switching Test Circuit [11, 17, 18, 19, 20], (b) Resonant Power Circuit in [6], (c) ZVS Test Circuit [5, 13], (d) Resistive Load Switch Test Circuit Proposed in [12]

4 Test Methods

4.1 Electrical Test Methods

In the Sawyer-Tower test circuit, the method to measure $E_{OSS,H}$ is based on the principle that the charge stored in the series capacitor C_{REF} is the same as the charge stored in C_{OSS} of the DUT (Q_{OSS}). This allows an indirect measurement by following the next steps:

- record the scaled v_Y and v_X waveforms and plot v_Y - v_X to obtain v_{DS} or v_{AK} (Figure 5a),
- calculate the charge Q_{REF} (equal to Q_{OSS}) stored in C_{REF} by means of the formula $Q_{REF} = v_X$ x C_{REF} (Figure 5b), and
- integrate v_{DS} with respect to Q_{OSS} for each switching cycle, from zero to Q_{MAX} (Q_{MAX} is Q at v_{MAX}), to obtain the energy difference between a charging and discharging cycle.

$$E_{\mathrm{OSS,H}} = \int_0^{Q_{\mathrm{MAX}}} v_{\mathrm{DS}}(Q_{\mathrm{OSS}})dQ_{\mathrm{OSS}} + \int_{Q_{\mathrm{MAX}}}^0 v_{\mathrm{DS}}(Q_{\mathrm{OSS}})dQ_{\mathrm{OSS}}$$

When sensing high voltage at the MHz range of frequency it is advised to add a small capacitor between the probe and the measured point (v_Y) to attenuate the signal and prevent probe derating. In such a case, a preliminary step should be added to the previous ones to determine the attenuation ratio for v_Y. Deskew and matching of passive probes is also very important to minimize errors. The need for time alignment of both voltage probes measuring v_Y and v_X is even more critical the higher the excitation voltage slew-rate and/or frequency. Optionally, a verification test may be done to ensure that the probes have equal impulse response and negligible delay mismatch by the following the procedure described in [10]:

- connect v_Y and v_X sensing probes to a voltage node with a high voltage slew-rate and/or frequency.
- compare v_Y and v_X waveforms captured by each probe to verify their overlap with minimal delay.
- replace the DUT with a second low-loss reference capacitor with a capacitance value similar to that of the DUT C_{OSS}, and
- verify the response is linear and has good overlap between the charging and discharging sections of the trace.

In the Non-Linear Resonance test circuit, there are several methods to calculate $E_{OSS,H.}$ A first method requires sensing v_{DS} during one or more pulses. Assuming the resonance in the main LC loop (L = L_1 in Figure 4a), $E_{OSS,H}$ is calculated by

$$E_{\mathrm{OSS,H}} = \frac{1}{2L_1}\left({S_1}^2 - {S_2}^2\right) = \frac{1}{2L_1}\left(\left(\int_{t_0}^{t_1} v_{\mathrm{DS}}(t)dt\right)^2 - \left(\int_{t_1}^{t_2} v_{\mathrm{DS}}(t)dt\right)^2\right)$$

where $S_{1,2}^2/2L_1$ are the energies during the time that v_{DS} ramps up and down, respectively (Figure 6a). The setup for this test is very similar to the one used for unclamped inductive switching test and there is also the possibility to be carried out in repetitive mode [17]. A second method to measure E_{OSS} can also rely on sensing the inductor current (i_L) in a half-cycle resonance in either a single pulse or repetitive mode [17, 18, 19]. $E_{OSS,H}$ is calculated by subtracting the conduction loss of parasitic components from the total loss in a half-cycle resonance.

4.1 Electrical Test Methods (cont'd)

$$E_{\mathrm{OSS,H}} = L\left(I_{max}^2 - I_{min}^2\right)/2 - (I_{max}/2)^2 R_{\mathrm{P}} T$$

where I_{max} and I_{min} are the maximum and minimum i_L in a half resonance cycle (Figure 6a), R_P is the total equivalent series resistance of parasitic components such as the load inductor, shunt resistor and bus capacitor, and T is the period of the half-cycle resonance.

Alternatively, by measuring i_L at the beginning and end of each pulse, $E_{OSS,H}$ can be directly determined as the energy difference at times t_0 ($E_0 = (1/2).L.i_L(t_0)^2$) and t_2 ($E_2 = (1/2).L.i_L(t_2)^2$), along one cycle of the resonance [20]. The energy loss in the inductor is equal to $2\pi/Q_F$, where Q_F is the inductor quality factor, that needs to be as high as possible.

$$E_{\mathrm{OSS,H}} = (1 - 2\pi/Q_{\mathrm{F}})(E_0 - E_2)$$

In the test circuits from Figure 4c and Figure 4d, the method to measure $E_{OSS,H}$ requires sensing the voltage drop between the two DUT terminals and the current at one of the DUT terminals. As a matter of example, the i_D or i_K sensing in the circuit of Figure 4d is done by resistor R_1. Once v_{DS} and i_D are captured (Figure 6b) $E_{OSS,H}$ is calculated by

$$E_{\mathrm{OSS,H}} = \int_{t_0}^{t_1} v_{\mathrm{DS}}(t) i_{\mathrm{D}}(t) dt + \int_{t_1}^{t_2} v_{\mathrm{DS}}(t) i_{\mathrm{D}}(t) dt$$

where t_1 and t_2 are times selected in a stable region of the waveform where the slew rate (dv_{DS}/dt) is close to zero. In the case that the voltage sensing would include the inductors appearing in circuits depicted in Figure 4b and Figure 4c, the losses in these inductors need to be accounted for.

The specifications for the required test conditions will depend on the test circuit, however the list below covers the most important test conditions.

- Off-state voltage (or its maximum value).
- Switching frequency (f).
- Slew rate for turn-off (v_{DS} rise, C_{OSS} charged).
- Slew rate for turn-on (v_{DS} fall, C_{OSS} discharged).
- Junction temperature (T_J).

Due to the different material dependencies for $E_{OSS,H}$, there is no general rule to define a worst case for the aforementioned test conditions.

4.1 Electrical Test Methods (cont'd)

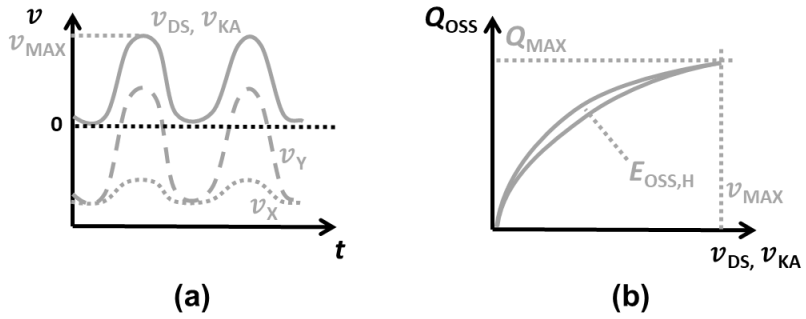

Figure 5 — Schematic Example of (a) Sensed Waveforms and (b) Calculated Q_{OSS} Curves Measured from a Standard Sawyer-Tower Test Circuit

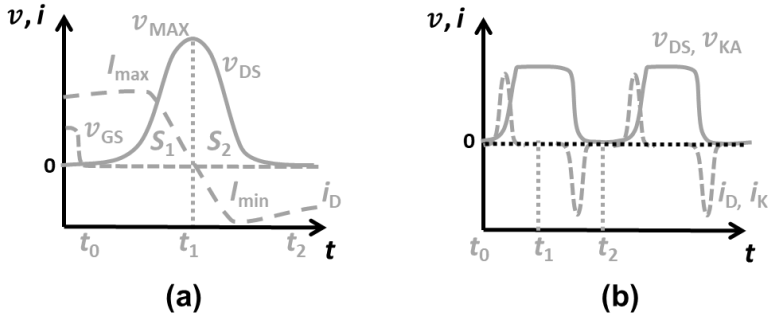

Figure 6 — Schematic Example of Sensed Waveforms from (a) Non-Linear Resonance Test Circuits and (b) Test Circuits in Figure 4c and Figure 4d

4.2 Calorimetric Test Methods

By using a test circuit with a periodical voltage signal applied to the DUT for a long time, there is the possibility to extract $E_{OSS,H}$ with calorimetric test methods.

The continuous excitation of the DUT can be implemented by any test circuit that is able to generate a continuous and repetitive v_{DS} excursion at a constant frequency f, such as those shown in Figure 1.

One option is to perform a steady-state calorimetric measurement, where the test circuit is operated for sufficient time such that the system is in thermal steady-state and equilibrium. For this case, the primary equation to interpret the results is

$$T_C - T_{REF} = R_{th} P_D$$

where $T_C - T_{REF}$ is the temperature difference between the DUT and a reference value (e.g., ambient temperature), R_{th} is the thermal resistance, and $P_D$is the dissipated losses within the DUT. When using the Sawyer Tower as a test circuit [11,14], then the DUT is the only significant source of loss in the system. If there are more loss sources that are thermally coupled with the DUT in the circuit, then $T_C - T_{REF}$ and P_D will become vectors, and R_{th} is a matrix that considers the cross coupling between all devices that are sourcing losses. One example of a cross-coupled source of loss could be a half-bridge that is located physically near to the DUT, which may be used to excite the DUT rather than a power amplifier.

The first step for any calorimetric method is to measure R_{th}. One way to do this is to insert several different known power losses P_D, while measuring the resulting $T_C - T_{REF}$. With the measured data of $T_C - T_{REF}$ and P_D, the characteristic thermal resistance R_{th} of the test circuit can be calculated. This is an important step, as the accuracy of the extracted R_{th} will determine the accuracy of the final results [15, 16]. It is recommended to measure several operating points in thermal steady-state to obtain R_{th}, rather than relying on a single test result to calculate this critical value.

Once R_{th} is characterized, the final power dissipation can be calculated by inverting the thermal impedance matrix with calorimetric test data as follows:

$$P_D = {R_{th}}^{-1}(T_C - T_{REF})$$

Finally, $E_{OSS,H}$ can be calculated by

$$E_{OSS,H} = \frac{P_D}{f}$$

As an alternative to steady-state measurements, transient calorimetric methods can be used [13,15,16]. Instead of waiting for the test circuit to reach thermal equilibrium, the thermal transient response is modelled by an RC thermal network. Although this is a more complicated approach, it offers the advantage that the loss measurements can be performed faster, as there is no need to wait until thermal equilibrium is reached.

It is useful to employ a calorimetric $E_{OSS,H}$ measurement as a validation of electric measurements, such as in [11], where both the Sawyer-Tower method and a calorimetric method are used. Calorimetric methods are also recommended to measure $E_{OSS,H}$ in real application circuits that cannot allow proper optimization for an electrical $E_{OSS,H}$ measurement, as it is the case in the power circuit represented in Figure 4b [6].

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