JEDEC STANDARD

Standard for Description of 2.5 V CMOS Logic Devices

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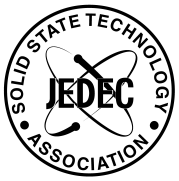

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STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES

(Formerly JEDEC Board Ballot JCB-99-50, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Purpose

To provide a standard for 2.5-V nominal supply-voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Scope

This standard defines dc interface parameters and test loading for a CMOS digital logic family based on 2.5-V (nominal) power supply levels and 2.5-V input tolerance.

3 Terms and definitions

For the purpose of this document, the following term and definition apply.

3.1 Prefixes

Prefixes "54" or "74" immediately preceding family name indicate the operating temperature range. For example, 54XXX refers to the Military (MIL) version of devices which are specified over the temperature range of –55 ºC to 125 ºC. 74XXX refers to the Commercial (COM'L) version of devices which are specified over –40 ºC to 85 ºC.

4 Standard specification

4.1 Absolute maximum ratings

Table 1 — Absolute maximum ratings over operating free-air temperature range (see Note 1)

Supply voltage range, V_{DD}	–0.5 V to 3.6 V
Input voltage range, V_I: Except I/O ports	–0.5 V to V_{DD} + 0.5 V
I/O ports (see Note 2)	–0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O (see Note 2)	–0.5 V to V_{DD} + 0.5 V
Voltage range applied to any output in the high-impedance state or power-off state, V_O	–0.5 V to V_{DD} + 0.5 V
Storage temperature range, T_{STG}	–65 ºC to 150 ºC

NOTES

1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2 This value is limited to 3.6 V maximum.

4.2 Recommended operating conditions

Table 2 — Recommended operating conditions (see Note 1)

			Min	Max	Unit
V_{DD}	Supply voltage	Operating	1.8	2.7	V
		Data retention only	1.2		
V_{IH}	High-level input voltage	V_{DD} = 2.3 V to 2.7 V (see Note 2)	1.7	V_{DD} + 0.3	V
		1.8 V ≤ V_{DD} < 2.3 V (see Note 3)	0.7 × V_{DD}	V_{DD} + 0.3	
V_{IL}	Low-level input voltage	V_{DD} = 2.3 V to 2.7 V (see Note 2)	–0.3	0.7	V
		1.8 V ≤ V_{DD} < 2.3 V (see Note 3)	–0.3	0.2 × V_{DD}	
V_I	Input voltage		0	V_{DD}	V
V_O	Output voltage		0	V_{DD}	V
Δt / Δv	Input transition rise or fall rate (see Note 4)		0	10	ns/V
T_A	Operating free-air temperature	54 series	–55	125	°C
		74 series	–40	85	

NOTES

1 Unused control inputs must be held high or low to prevent them from floating.

2 Normal range operating conditions per JESD8-5

3 Wide range operating conditions per JESD8-5

4 As measured between 0.7 V and 1.7 V

4.3 DC specifications

Table 3 — Electrical characteristics over recommended operating free-air temperature range

Parameter	Test Conditions		V_{DD}	Min	Max	Unit
V_{OH}	I_{OH} = –100 µA		1.8 V	1.6		V
	I_{OH} = –1 mA,	V_{IH} = 1.7 V	2.3 V	2		
	I_{OH} = –8 mA,	V_{IH} = 1.7 V	2.3 V	1.8		
V_{OL}	I_{OL} = 100 µA		1.8 V		0.2	V
	I_{OL} = 1 mA,	V_{IL} = 0.7 V	2.3 V		0.4	
	I_{OL} = 8 mA,	V_{IL} = 0.7 V	2.3 V		0.6	
I_I	$V_I = V_{DD}$ or GND		2.7 V		±10	µA
I_{BHL} (see Note 1)†	V_I = 0.7 V		2.3 V	45		µA
I_{BHH} (see Note 2)†	V_I = 1.7 V		2.3 V	–45		µA
I_{BHLO} (see Note 3)†	V_I = 0 to V_{DD}		2.7 V	500		µA
I_{BHHO} (see Note 4)†	V_I = 0 to V_{DD}		2.7 V	–500		µA
I_{OZ} (see Note 5)†	$V_O = V_{DD}$ or GND		2.7 V		±10	µA
I_{DD}	$V_I = V_{DD}$ or GND,	I_O = 0	2.7 V		20	µA

† Specification only for components with optional bus hold.

NOTES

1 The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

2 The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{DD} and then lowering it to V_{IH} min.

3 An external driver must source at least I_{BHLO} to switch this node from low to high.

4 An external driver must sink at least I_{BHHO} to switch this node from high to low.

5 For I/O ports, the parameter I_{OZ} includes the input leakage current.

5 Test circuit and switching waveforms

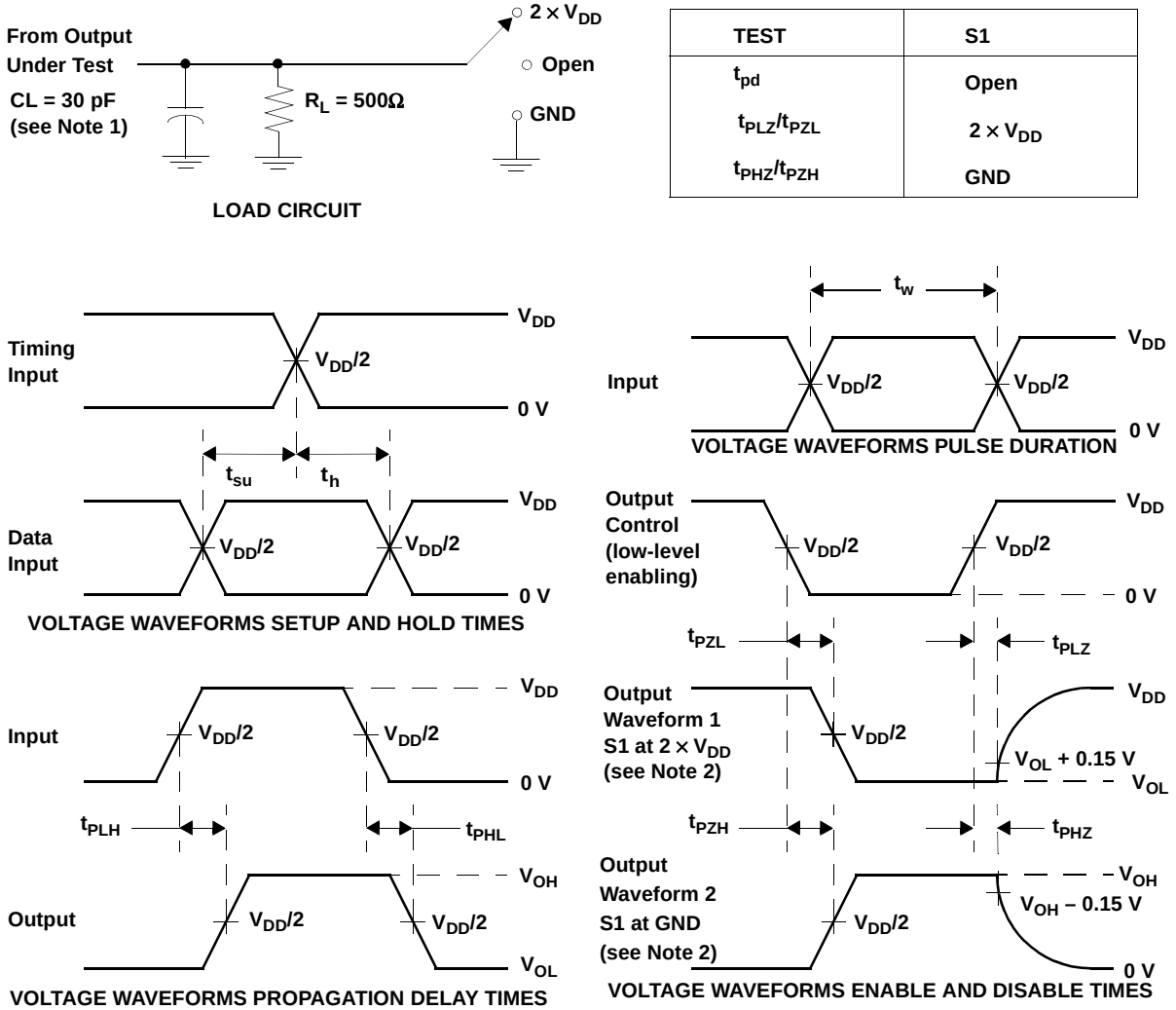


Figure 1 — Parameter Measurement Information (V_{DD} = 1.8 V to 2.7 V)

NOTES

1 CL includes probe and jig capacitance.

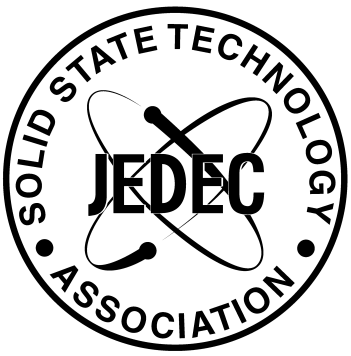
2 Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

3 All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2$ ns, $t_f \leq 2$ ns, measured from 10% to 90%, unless otherwise specified.

4 The outputs are measured one at a time with one transition per measurement.

6 Reference to other applicable JEDEC standards and publications

JESD8-5: *2.5 V ± 0.2 V (Normal Range), and 1.8 V to 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits.*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