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Test Method for Continuous-Switching Evaluation of Gallium Nitride Power Conversion Devices

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TEST METHOD FOR CONTINUOUS-SWITCHING EVALUATION OF GALLIUM NITRIDE POWER CONVERSION DEVICES

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Foreword

This document was drafted by JEDEC JC-70.1 GaN Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use in the GaN power semiconductor and related power electronic industries and provides guidelines for test methods and circuits to be used for continuous-switching tests of GaN power conversion devices.

Introduction

In previous literature, tests methods to evaluate maximum power ratings and Safe Operating Area (SOA) have been proposed for power transistors [1], [2]. However, all these tests ignore the switching transient, thus focusing on a time interval with fixed v_{DS} and i_D values (normally a single pulse). In this sense, typical SOA graphs like the one illustrated in Figure 1 do not represent i_D-v_{DS} trajectories during a switching event.

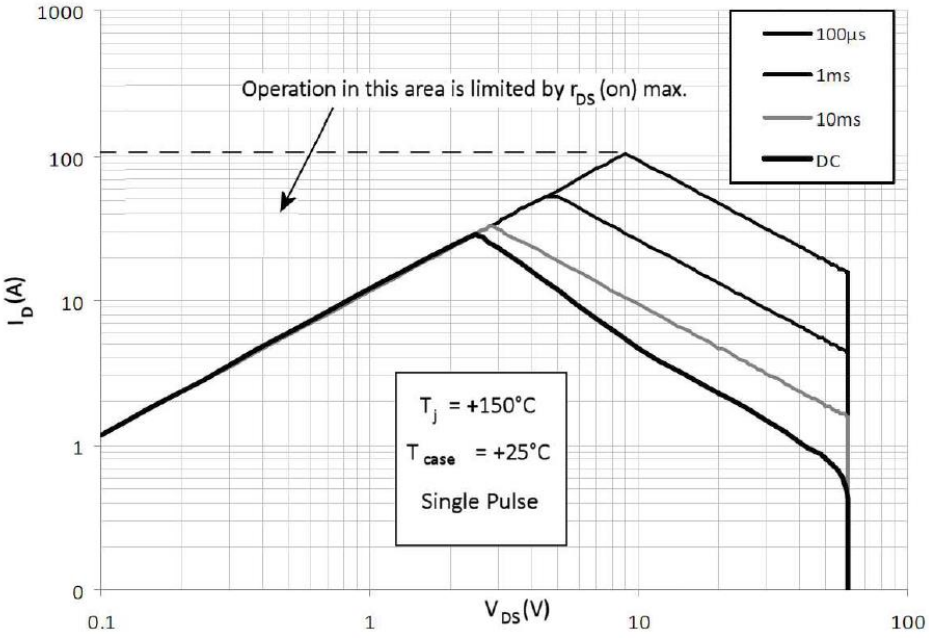

Figure 1 — Safe Operating Area (SOA) for a conventional power transistor. [1]

Introduction (cont'd)

This kind of SOA is not sufficient to design fast switching converters. Since GaN lateral power transistors have small input and output capacitances, their switching is generally very fast. GaN devices switch in the order of nanoseconds. Although this means that the self-heating effect is smaller in such a fast switching transition, imposing higher v_{DS} and i_D on GaN power transistors simultaneously during multiple switching events can cause the transistors to experience electrical stress. Therefore, characterization of switching operating conditions in addition to conventional SOA is necessary for GaN power transistors.

When switching the devices multiple times in continuous operation, this stress is repeated, and it can result in cumulated degradation over time, which can affect the switching reliability [3]. While most of the time "hard-switching" causes more stress than "soft-switching" [4], GaN devices are also targeted for higher-frequency applications which utilize soft-switching topologies. Accordingly, safe switching of a GaN power transistors strongly depends on the intended application profile.

This document describes test methods and gives advice on test circuits to be used for continuous-switching. JEP180 describes how to use these circuits to determine switching reliability.

TEST METHOD FOR CONTINUOUS-SWITCHING EVALUATION OF GALLIUM NITRIDE POWER CONVERSION DEVICES

(From JEDEC BoD Ballot JCB-20-60, formulated under the cognizance of the JC-70.1 Subcommittee on GaN Power Electronic Conversion Semiconductor Standards.)

1 Scope

This method describes a means of electrically operating GaN power switching devices in a continuous-switching circuit and determining dynamic switching waveforms and I-V loci for the continuous-switching test. The test method can be applied to the following:

a) GaN enhancement- and depletion-mode discrete power devices
b) GaN integrated power solutions

A packaged device-under-test (DUT) typically exhibits a more realistic stress profile than a wafer-level test by including the interactions with parasitic elements as well as cumulative self-heating and mechanical effects. However, the methodologies covered herein are valid at the wafer level for technology characterization, with proper consideration of the probe connections and their impacts on results.

This document is not intended to cover the underlying mechanisms of device degradation or failure but gives a general guidance on circuits and test methods that may be used to implement stress procedures and define stress conditions, such as JEP180. This test method may be used for any high speed power switching device.

2 Normative references

JEDEC JEP173, *Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices, Version 1.0,* January 2019

JEDEC JEP180, *Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices, Version 1.0,* February 2020

3 Terms, definitions and letter symbols

DUT	Device Under Test
CCM	Continuous Conduction Mode
DPT	Double Pulse Test
ZVS	Zero Voltage Switching
SOA	Safe Operating Area
PFC	Power Factor Correction
ACF	Active Clamp Flyback
V_{DD}	supply voltage
L	inductance
R	resistance
C	capacitance
$I_{D(ON)}$	drain current of DUT in ON-state, dc component
i_D	drain current of DUT, time-varying
i_L	current through inductor, time-varying
$V_{DS(ON)}$	drain to source voltage of DUT in ON-state, dc component
$R_{DS(ON)}$	drain to source resistance of DUT in ON-state
$V_{DS(OFF)}$	drain to source voltage of DUT in OFF-state, dc component
$V_{GS(ON)}$	gate to source voltage of DUT in ON-state, dc component
$V_{GS(OFF)}$	gate to source voltage of DUT in OFF-state, dc component
v_{DS}	drain to source voltage of DUT, time-varying
v_{GS}	gate to source voltage of DUT, time-varying
t_r	rise time of the signal measured
t_f	fall time of the signal measured
f_{BW}	bandwidth frequency
I_{IN}	input current in a test circuit
I_{OUT}	output current in a test circuit
C_{OSS}	output capacitance
T_J	junction temperature
T_C	case temperature

4 Test circuits and waveforms

GaN power transistors are typically being targeted for both hard-switching and soft-switching topologies for power conversion applications. The test circuit to be used to evaluate the switching reliability must be appropriate for the target application. In considering the application profile, factors such as switching topology, frequency, voltage, operating current, and temperature should be considered.

Hard-switching conditions refer to the overlap of the drain voltage and channel current when the power device switches either from ON-to-OFF or OFF-to-ON states. Typical hard-switching topologies include totem-pole Power Factor Correction (PFC) boost converters, buck converters, motor control inverters, and single-ended flyback circuits.

Soft-switching conditions refer to conditions where there is no overlap of the drain voltage and channel current when the GaN power device switches between the ON- and OFF-states. Overlap between the drain voltage and drain current waveforms may still occur due to the commutation current of C_{OSS}, but this current does not flow through the channel in a soft-switching condition. Typical soft-switching topologies include Zero Voltage Switching (ZVS) converters, LLC converters, Active Clamp Flyback (ACF), etc. Soft-switching may also refer to the synchronous switch in a hard-switching topology, where its steady-state drain current is always negative.

Resistive-load switching, in which the overlap of voltage and current fall between the hard-switching and soft-switching conditions, is not typically seen in power electronic applications. However, the easier implementation of this switching type makes it attractive for device-level characterization and testing purposes.

As described above, current-voltage loci are the crux that determines the switching type. The loci of the above three switching types are explained in great detail in papers such as [4]. In the following, the continuous-switching methods for these switching types is covered.

4.1 Inductive and resistive switching methods

In order to select the appropriate electric test circuit to use for determining the i_D-v_{DS} locus of the GaN device, the application profile must first be carefully understood. The test circuit selected should closely replicate or exceed the switching stress for the switching locus type present in the application intended for the device. However, even if only hard-switching or soft-switching is selected as the primary evaluation vehicle, vendors may additionally characterize other switching stress profiles relevant to the actual operation, e.g., those occurring during transient periods or other less frequent events.

Figure 2 shows the circuit conventionally used for inductive-load double-pulse testing (DPT). As shown here, this test circuit is equivalent to a boost converter with the output tied to the input voltage source. Therefore, switching transition seen by the DUT is analogous to the hard-switching transistor in half-bridge topologies where an inductor is connected at the switch-node.

If a hard-switching application profile is determined to be the appropriate stress circuit, the inductive-load switching circuit in Figure 3(a) can be used. Here, the high-side switch can either be a GaN transistor or a free-wheeling diode, as long as the switching locus for the DUT closely resembles that of the application circuit. If a transistor is used for the high-side, its gate can be tied to its source to produce a diode-like operating mode, or it can be synchronously switched with appropriate dead time. This circuit is also equivalent to the DPT circuit in Figure 2, if the load resistance R is set to 0 Ω. However, when operated continuously, R may be adjusted to achieve a given $I_{D(ON)}$ for the desired operating conditions.

4.1 Inductive and resistive switching methods (cont'd)

Figure 3(b) shows an alternative test circuit for continuous inductive-load switching, a synchronous boost converter. In this configuration, the blocking voltage $V_{DS(OFF)}$ is equal to the output voltage across the resistive load R, and the average current $I_{D(ON)}$ is equal to the input current I_{IN}. If this circuit is operated in continuous conduction mode (CCM), with I_{IN} greater than the ripple-current amplitude, then the low-side DUT will experience a hard-switching turn-on and turn-off transition. In CCM, the high-side device could also be replaced by a free-wheeling diode, or its gate and source can be tied together, yielding a similar configuration to the high-side diode in Figure 3(a).

Figure 3(c) shows a buck converter with a half-bridge configuration. In this configuration, the DUT is soft-switching. The i_D-v_{DS} locus for soft-switching operation is important for resonant and soft-switching topologies, typically utilized to design compact power converters operated at high switching frequency. In the corresponding electric circuit, low-side (DUT) and high-side devices are switched in a complimentary manner while imposing a certain dead-time. The high-side device could be either hard-switching or soft-switching, depending on the amplitudes of I_{OUT} and the ripple current, as well as the dead-times. In CCM, the low-side DUT in a buck converter typically operates in reverse conduction mode, with soft-switching turn-on and turn-off transitions. However, clause 4.3 explains how the circuit could be used for two different stress types, depending on the operating conditions.

While it typically does not resemble the exact application, conditions implemented in most power conversion topologies, resistive-load switching can also be used, since it is convenient to implement and control. Figure 3(d) shows a resistive-load switching circuit. Although the locus is much smaller than that for inductive-load switching, the resistive-load switching is also beneficial in that the duty cycle can be varied with more flexibility than for inductive-load switching.

In all of these configurations, dynamic ON-state resistance can be measured by employing a clamp circuit as described in JEP173.

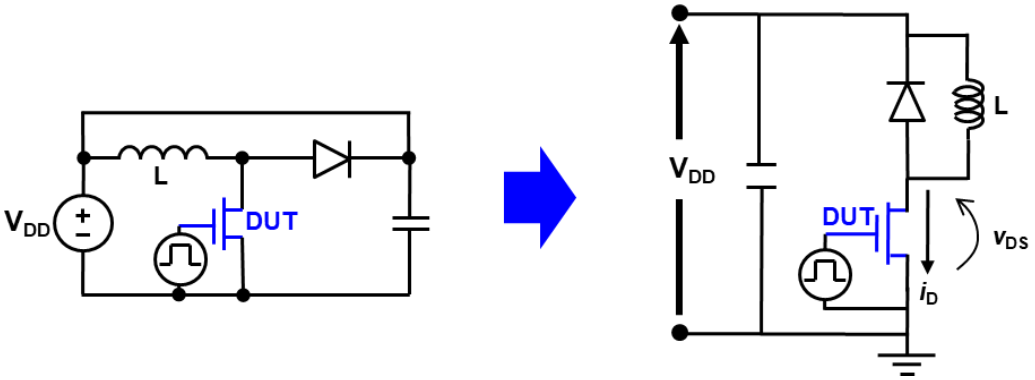

Figure 2 — Test circuit typically used for double-pulse testing which is equivalent to a boost converter with its output tied to the input voltage source.

4.1 Inductive and resistive switching methods (cont'd)

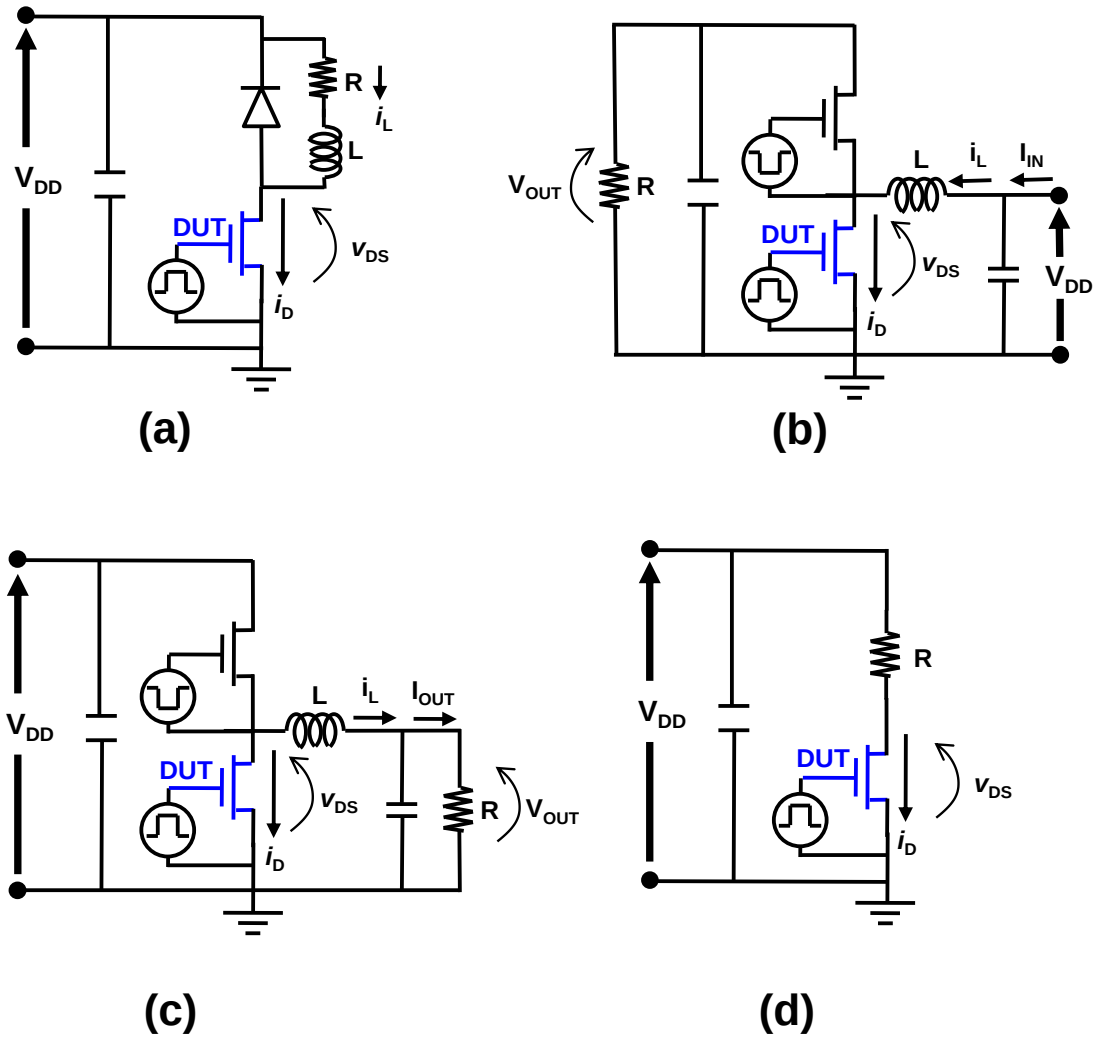

Figure 3 — Examples of circuits to provide continuous-switching operation with tunable i_D-v_{DS} locus: (a) inductive-load switching with a modified DPT circuit, (b) synchronous boost converter, (c) synchronous buck converter, (d) resistive-load switching circuit.

4.2 Capture of waveforms and i_D-v_{DS} loci

In order to measure the i_D-v_{DS} locus during the switching transient, the dynamic drain current i_D of the DUT must be measured with sufficiently high bandwidth and sampling rate. This current measurement often presents a challenge, as the current sensor may significantly impact the circuit behavior, and it may not be well-suited for continuous operation. In some cases, current sensors may not be readily available with the required bandwidth, or their insertion may add an unacceptable magnitude of parasitic inductance to the circuit. Therefore, two options are typically employed to capture the waveforms and locus: experimental capture (e.g., with a DPT) or a circuit simulation model with carefully tuned parasitics.

In a DPT, the DUT is switched twice to capture the waveforms for turn-on and turn-off transitions. Figure 2 shows a typical DPT circuit used for inductive-load switching, with waveforms as described in Figure 4(a). Since the DUT is switched only twice, the temperature rise of the DUT due to self-heating is limited, thus $T_J \approx T_C$, which may also be similar to the ambient temperature. When operated continuously with a resistor at the output, the circuits in Figure 3(a) and Figure 3(b) produce the waveforms shown in Figure 4(b). In continuous operation, the DUT may be affected by self-heating, in which case T_J may be higher than T_C and the ambient temperature of its environment. The locus should be captured at a T_J similar to the actual stress condition, which may require adjustment of the ambient temperature to compensate. When a current sensor is employed in the circuit to capture dynamic drain current (i_D), it is typically connected in series with the source of the low-side DUT. This position shares a common reference point with v_{DS} and v_{GS}, allowing all three measurements to use passive probes. Differential voltage probes can also be used if they provide sufficient bandwidth to capture the full spectrum of the switching waveforms. The bandwidth for all voltage and current measurements should be much higher than the equivalent frequency components of the signal measured, which can be estimated by the shortest rise or fall transition in the signal measured:

$$f_{eq} \approx 0.35 / \min(t_r, t_f) \tag{4.2.1}$$

In order to accurately capture detailed rise and fall waveforms, the measurement system should have a bandwidth several times higher than this equivalent frequency (e.g., 5x, 10x). The bandwidth of the oscilloscope and probe must both be considered when determining the measurement system bandwidth.

In a similar way, the sampling rate must be sufficiently high that the sampling interval is much smaller than the duration of the shortest rise or fall transition, in order to accurately capture the shape of the transition. Measurement with either too-low bandwidth or sampling rate will result in inaccurate waveforms and locus plots.

Proper connectivity of the probes to the test vehicle are also critical for accurate waveform capture. For example, long ground leads should be avoided, and Kelvin connections to all measurement points should be used where possible. Furthermore, the i_D and v_{DS} waveforms must also be accurately time-aligned in order to capture the switching locus by adjusting the deskew settings in the oscilloscope. Methodology for probe connections, time-alignment/deskew, and further test setup details for double-pulse testing may be found in [5], [6].

When measuring an accurate current waveform is not practical, the test circuit can instead be simulated in software such as purely SPICE or a combination between SPICE and finite-element/finite-volume methods [7], [8]. In this case, accurate simulation models must be available for the DUT and other components in the circuit. Parasitic circuit impedances must also be included in the simulation model, including stray inductances, capacitances, and resistances. These impedances must be precisely tuned to accurately represent the test circuit.

4.2 Capture of waveforms and i_D-v_{DS} loci (cont'd)

To verify the accuracy of either measured waveforms or simulation results, the voltage waveforms must be compared against those collected from the continuous-switching test circuit. The v_{DS} waveform of the DUT in continuous-switching should closely match measurements or simulations. Other voltage waveforms can also be compared for further verification, such as the v_{GS} of the DUT and the voltage across the high-side device.

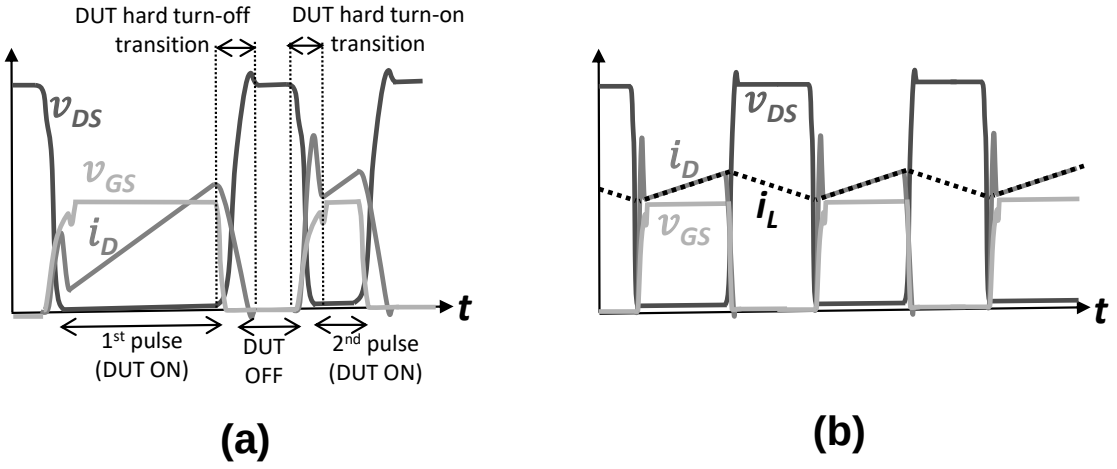

Figure 4 — Waveforms of v_{GS}, v_{DS}, and i_D in an inductive-load switching test, (a) DPT (b) continuous operation.

4.3 Examples of waveforms and i_D-v_{DS} loci

Figures 5(a) and 6(a) show the waveforms and locus of a hard-switching device in an inductive switching test, using the test circuits shown in Figure 3(a) or 3(b). The locus and waveforms corresponds to the switching transitions of a high-side DUT in a buck converter or low-side DUT in a boost converter. In this test condition, the inductor current during the DUT turn-on transition ($I_{D(ON)}$) is an important parameter for specifying the switching stress.

Figures 5(b) and 6(b) show the waveforms and locus of the synchronous switch in a half-bridge topology, in which the steady-state drain current $I_{D(ON)}$ is always negative. This locus corresponds to the test circuit in Figure 3(c) when operating in CCM, with the resistance R selected to produce an output current I_{OUT} that is greater than the ripple-current amplitude. If the dead-time is long enough for v_{DS} of the low-side device to fall to 0 V before it turns on, then this device will be soft-switching. Otherwise, it may experience a partially hard-switching turn-on transition.

Figures 5(c) and 6(c) show the waveforms and locus of a soft-switching device in a resonant topology. This test can also be performed using the circuit in Figure 3(c), but the resistance R is selected to produce an output current I_{OUT} that is below the ripple-current amplitude. In this operating condition, $I_{D(ON)}$ oscillates between positive and negative currents during each on-state. The circuit can be operated as a resonant topology with 50% duty cycle by neglecting the load resistor entirely, thereby setting I_{OUT} to 0 A [9].

4.3 Examples of waveforms and i_D-v_{DS} loci (cont'd)

Figures 5(d) and 6(d) show the waveforms and locus with a resistive load. Unlike the case for inductive-load switching, there is no current spike in the switching waveform, and the locus curve is much smaller. In some cases, a capacitor may be added in parallel with the resistor R, which will change the shape of the locus and waveform.

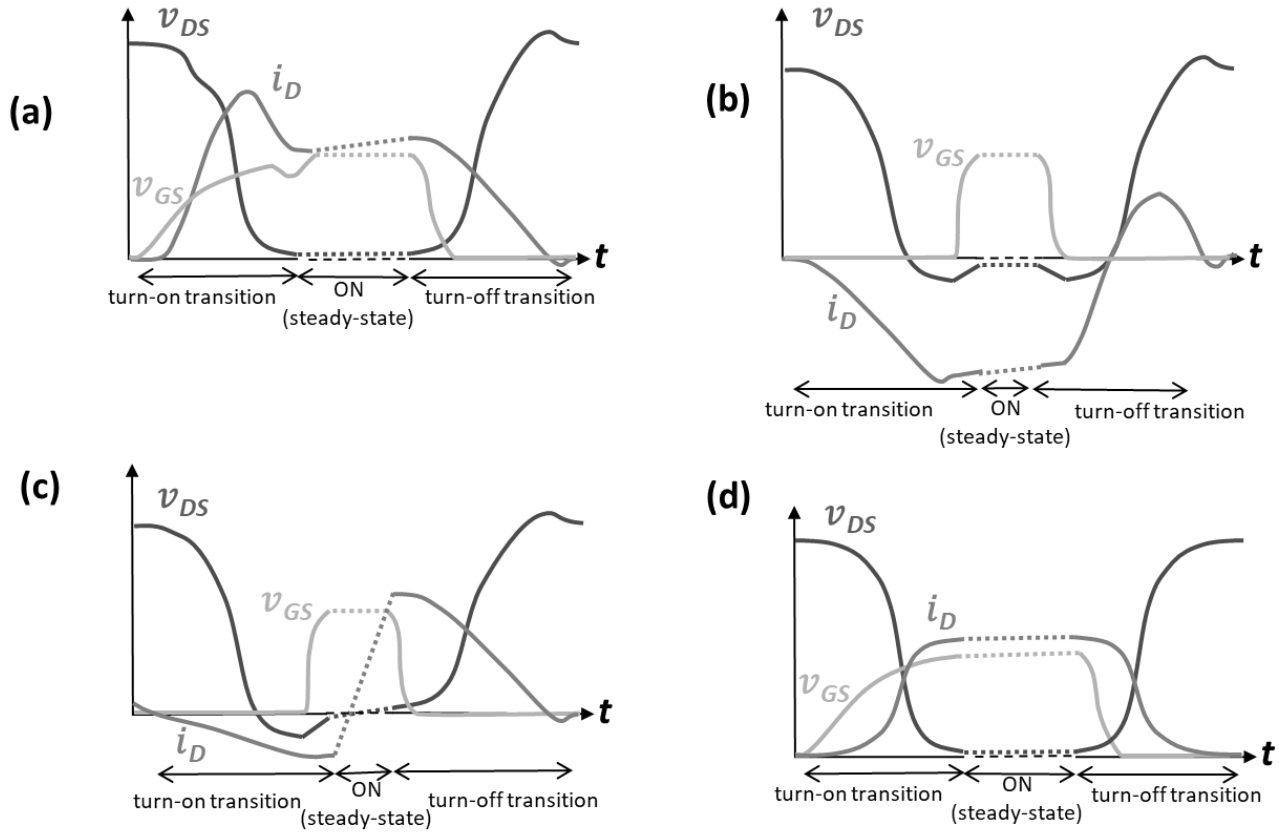

Figure 5 — Simplified examples of time-domain waveforms for DUT operation in circuits, (a) inductive-load switching with hard-switched turn-on and turn-off, e.g., high-side in a buck converter or low-side in a boost converter, (b) soft-switched (ZVS) turn-on and turn-off transitions, e.g., low-side in a CCM buck converter with inductive load, (c) switching in a resonant topology with soft-switched (ZVS) turn-on and hard-switched turn-off transitions, (d) resistive-load switching.

4.3 Examples of waveforms and i_D-v_{DS} loci (cont'd)

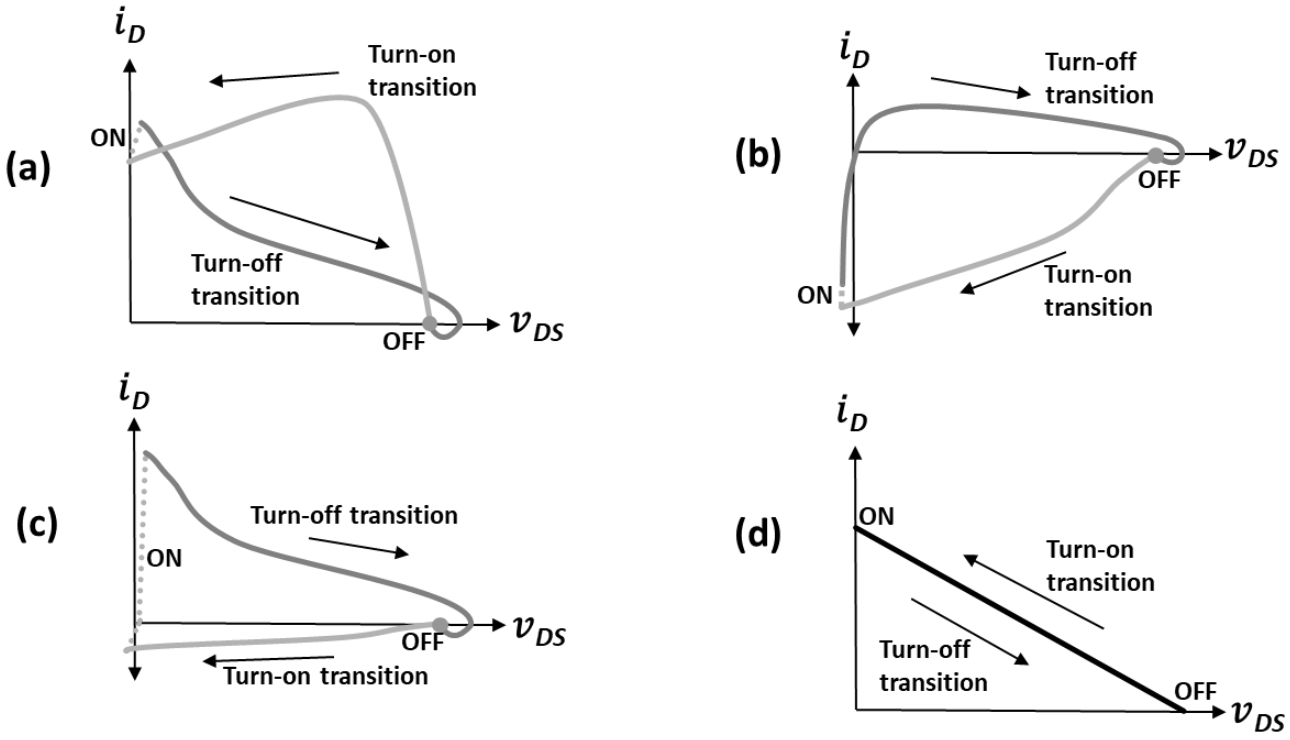

Figure 6 — Switching locus plots corresponding to the time-domain waveforms in Figure 5

5 Measurement considerations

The impact of self-heating on the DUT electrical parameters must be considered when they are measured in–situ during continuous-switching. Choosing a low turn-on duty cycle in the test method may allow the DUT junction temperature T_J to be very similar to its case temperature T_C and surrounding ambient temperature. Additionally, the DUT temperature can be directly monitored with a temperature sensor, a thermal camera or similar method.

If in-situ monitoring is not possible, it is recommended that the continuous-switching test is interrupted intermittently to check that the DUT electrical parameters remain within their normal values according to JEP180.

During all of the continuous mode operating tests, it is recommended to note the time stamps at which the measurements are performed once the test begins for appropriate interpretation of results over time.

The impact of any connected measurement equipment during the continuous-switching test should be considered and minimized when possible.

6 References

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