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Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices, Version 1.0

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DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GAN HEMT BASED POWER CONVERSION DEVICES

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Foreword

This document was drafted by JEDEC JC-70.1 GaN Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies. The early on efforts for this document development were started in 2016 in GaN Standards for Power Electronic Conversion Devices Working Group (GaNSPEC DWG). GaNSPEC DWG was an independent working body that later transitioned into JC-70.1 in 2017 and consisted of industry experts along with academic scholars located around the globe.

This document is intended for use in the GaN power semiconductor and related power electronic industries, and provides guidelines for measuring the dynamic ON-resistance of GaN power devices.

Introduction

Gallium Nitride (GaN) lateral power High Electron Mobility Transistor (HEMT) conducts through a two-dimensional electron gas (2DEG) in ON-state operation. Due to the various stress conditions that the device encounters during power electronic switching applications, some charge may get trapped in specific regions of the transistor structure. This leads to an increased ON-resistance when operated in a switching environment and is known as dynamic ON-resistance. Increased dynamic ON-resistance translates to higher power loss, thereby reducing overall system efficiency.

The test methods provided in this document can be used as a guideline for measuring dynamic ON-resistance of GaN power device, focused on lateral HEMT technologies. These three test methods may be applied for datasheet, process control, technology development, final tests and other usage.

DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GAN HEMT BASED POWER CONVERSION DEVICES

(From JEDEC Board Ballot JCB-18-55, formulated under the cognizance of the JC-70.1 Subcommittee on GaN Power Electronic Conversion Semiconductors.)

1 Scope

In general, dynamic ON-resistance testing is a measure of charge trapping phenomena in GaN power transistors. This publication describes the guidelines for testing dynamic ON-resistance of GaN lateral power transistor solutions. The test methods can be applied to the following:

a) GaN enhancement and depletion-mode discrete power devices [1]
b) GaN integrated power solutions
c) the above in wafer and package levels

Wafer level tests are recommended to minimize parasitic effects when performing high precision measurements. For package level tests, the impact of package thermal characteristics should be considered so as to minimize any device under test (DUT) self-heating implications.

The prescribed test methods may be used for device characterization, production testing, reliability evaluations and application assessments of GaN power conversion devices. This document is not intended to cover the underlying mechanisms of dynamic ON-resistance and its symbolic representation for product specifications.

2 Terms, definitions and letter symbols

DUT	Device Under Test
V_{DD}	Supply voltage
V_{DS}	Drain to Source Voltage of DUT
V_{GS}	Gate to Source Voltage of DUT
D1	Free-wheeling diode
L	Inductance
R	Resistance
C	Capacitance
I_D	Drain current of DUT in ON-state
$V_{DS(ON)}$	Drain to Source Voltage of DUT in ON-state
$R_{DS(ON)}$	Drain to Source Resistance of DUT in ON-state
$V_{DS(OFF)}$	Drain to Source Voltage of DUT in OFF-state
$V_{GS(ON)}$	Gate to Source Voltage of DUT in ON-state
$V_{GS(OFF)}$	Gate to Source Voltage of DUT in OFF-state
t_{off}	OFF-state pulse width
t_{on}	ON-state pulse width
$t_{m,on}$	measurement timing in ON-pulse
t_{dn}	Soft-switching delay time between the OFF and ON pulse or vice-versa, with n =1 or 2
f	Frequency
N	Number of pulses
T_C	CaseTemperature
P_{Peak}	Instantaneous Peak Power, applicable for only hard switching
E_{Pulse}	Energy dissipated per pulse, applicable for only hard switching

3 Test circuits and waveforms

GaN power transistors typically are being targeted for both hard and soft-switching topologies for power conversion applications.

Hard switching conditions refer to the overlap of the voltage and current waveforms when the power device switches either from ON-to-OFF or OFF-to-ON states. Typical hard-switching topologies include totem-pole Power Factor Correction (PFC) boost converters, buck converters, motor control inverter and single ended fly-back circuits.

Soft switching conditions refer to conditions where there is no or minimal overlap of the voltage and current waveforms when the GaN power device switches between the ON- and OFF-states. Typical soft-switching topologies include Zero Voltage Switching (ZVS) converters, LLC converters, Active Clamp Fly-back (ACF) etc.

Resistive load switching is another type that is not typically seen in the power electronic applications whose overlap of voltage and current waveforms fall in between the hard and soft switching types. However, the easier implementation of this switching type makes it attractive for the device level characterization and testing purposes.

As described above, current-voltage loci are the crux that determines the switching type. The loci of above three switching types are explained with great detail in here [2]. The following subsections cover the dynamic ON-resistance measurement methods for these three switching types.

3.1 Inductive and resistive switching methods

A hard-switching inductive and resistive loaded test vehicle that is analogous to what is generally termed the “double-pulse” tester in power electronic applications [3] is shown in Figure 1. Another depiction of the double-pulse tester is shown in Figure 2, which illustrates that the double-pulse tester is equivalent to a boost converter with the input tied to the output [4]; note that $R_{Load} = 0$ in this depiction.

3.1 Inductive and resistive switching methods (cont'd)

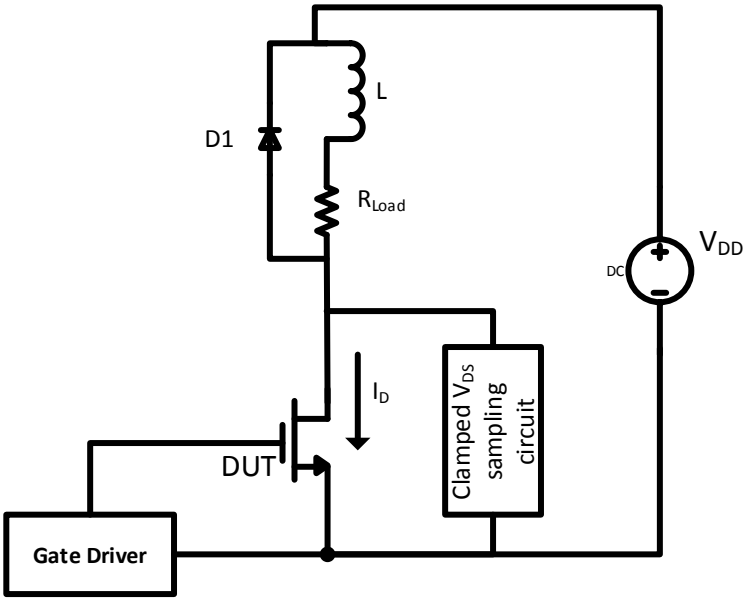


Figure 1 — Inductive-Resistive load "double-pulse" test circuit for hard-switching evaluation

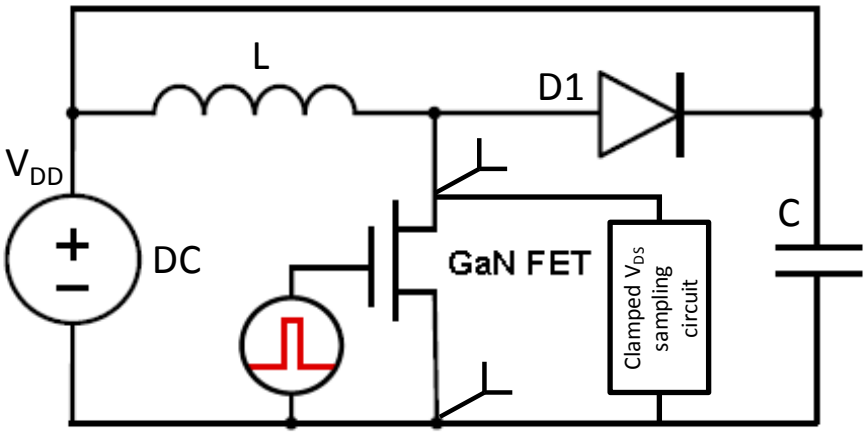


Figure 2 — Depiction of the hard-switching "double-pulse" test circuit (showing its similarity to a boost converter)

When a power transistor switches at high voltages, measuring the drain-to-source ON-state voltage with a passive probe in combination with an oscilloscope can be quite challenging, as the oscilloscope's dynamic-range precision may not be adequate. As an example, consider a device with an ON-state voltage of 0.5 V at 1 A of drain current switching from 400 V in the OFF-state. An 8-bit oscilloscope configured to measure the 400 V OFF-state voltage will have a resolution of 1.5625V (= $400/2^8$), which is not sufficient to measure the 0.5 V ON-state voltage. The measurable voltage has an error of more than 3 times the actual voltage in this example and this further increase to 30 times to detect a 10% dynamic ON-state voltage drift. To circumvent such problems, a circuit may be employed to clamp the high OFF-state voltage on a low-voltage measurement probe without compromising the ON-state voltage.

3.1 Inductive and resistive switching methods (cont'd)

Since the clamped sampling circuit reduces the voltage swing quite significantly on the measurement probe, the dynamic ON-state voltage of the power transistor can be effectively measured, from which its dynamic ON-resistance is calculated using Ohm's law. Some examples of voltage clamp sampling circuits are reported in [5-6].

It is to be noted that if R_{Load} = 0 in Figure1 (which makes the circuits of Figs. 1 and 2 identical), the circuit is nothing but a standard power electronics double-pulse or boost test circuit. The hard-switching circuits presented in Figs. 1 and 2 provide the flexibility of running tests either in single-pulse, double-pulse or continuous-pulse modes. They provide high impedance on the drain, which lowers Vds without the need for an additional synchronized tester resource. A high impedance may also be achieved by setting L=0 and using a high-value resistor making this a pure resistive switching. The single and double-pulse test modes are often advantageous in production environments where fast switching characterization is needed, whereas the continuous-pulse test mode is beneficial for longer-term device characterization and reliability evaluation. The flow chart for inductive and/or resistive switching load based measurement is presented in Figure3, and Figure 4 shows the representative hard-switching waveforms of a GaN power transistor in the Figure1, Figure2 test circuits when subjected to continuous gate pulses. In a pure resistive switching load test circuit, the DUT current in ON-state stays constant unlike the inductive load circuit where the current increases linearly with time. A high-performance clamp circuit design may be required to measure the drain-to-source dynamic ON-resistance in < 1 us after the device transitions from the OFF-state to the ON-state. The $R_{DS(ON)}$ is evaluated dynamically during the period when the transistor gate is ON as $R_{DS(ON)} = V_{DS(ON)}/I_D$.

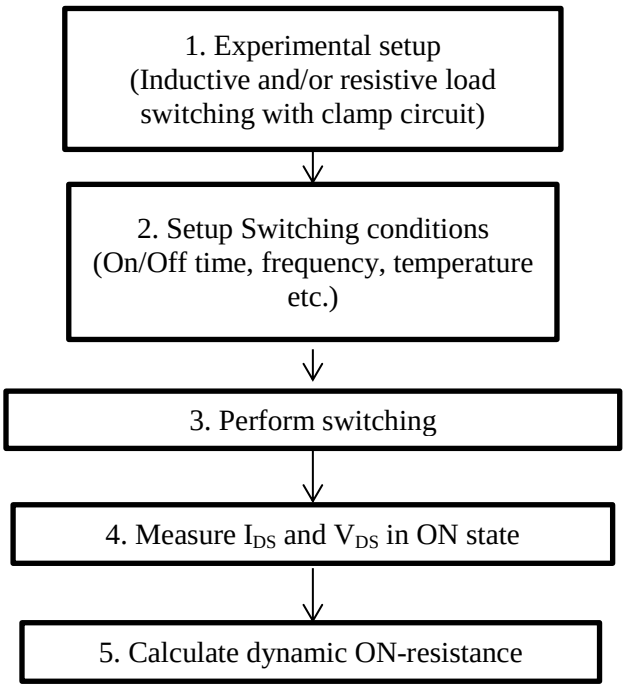


Figure 3 — Simplified flowchart for inductive and/or resistive switching based dynamic on-resistance test

3.1 Inductive and resistive switching methods (cont'd)

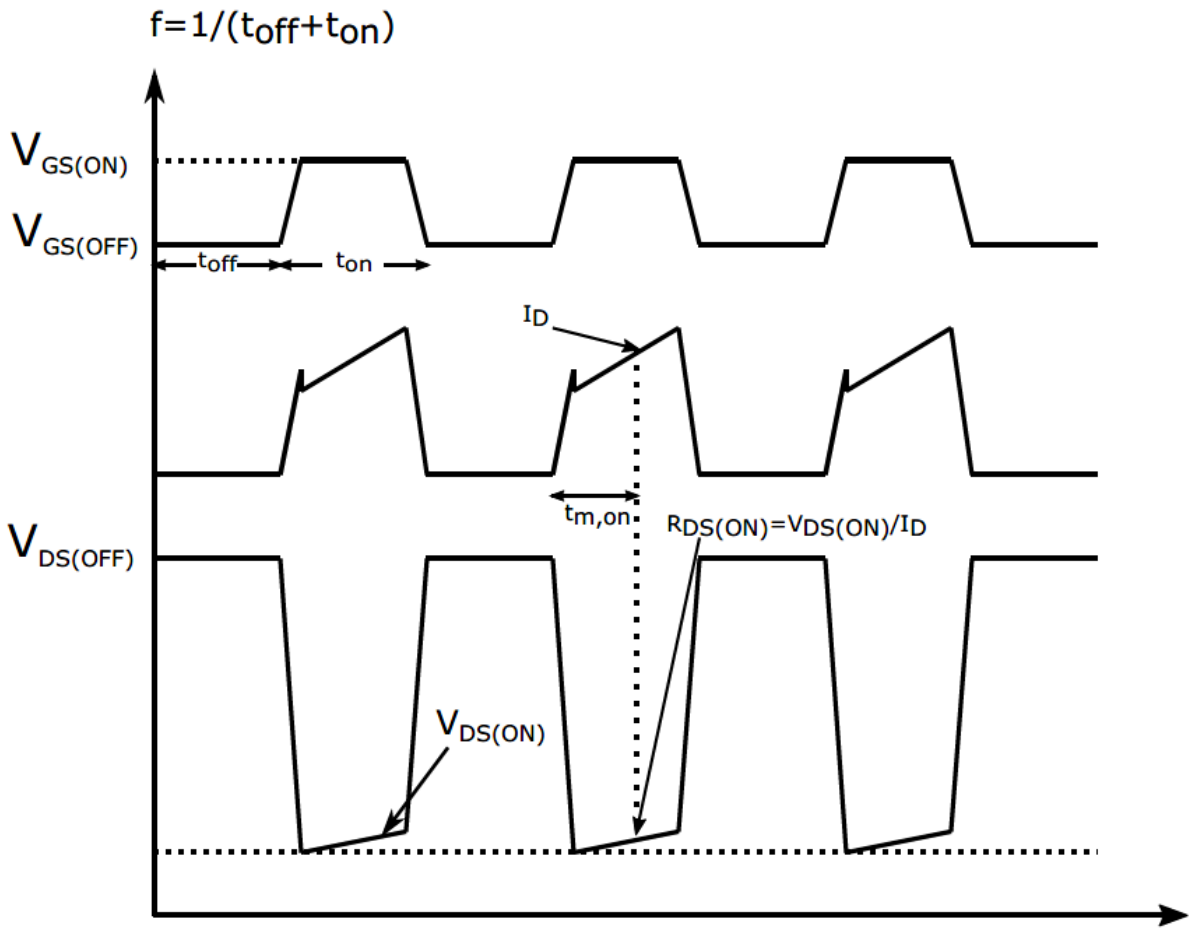


Figure 4 — Representative continuous-pulse hard-switching waveforms for measuring dynamic on-resistance using the test circuits in Figure 1 and Figure 2

3.2 Pulsed Current-Voltage (I-V) method

The pulsed I-V technique is analogous to soft switching, which is widely used in GaN RF electronics. This method involves pulsing the gate and drain voltage signals independently, and hence is branded as a classic “double pulse” technique in the RF world, thus potentially leading to confusion since this term is used in the power electronics world to refer to a hard-switching test, as discussed above. Using this approach, a few manufacturers have developed systems to fulfill power electronic requirements [7]. Figure5 and Figure6 provides simplified test setup and test flow respectively for soft switching.

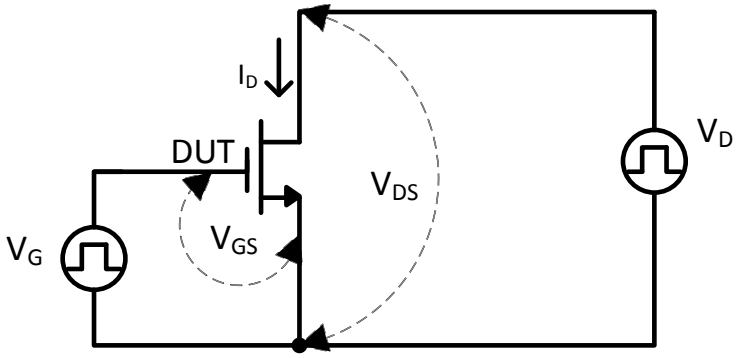


Figure 5 — Example test circuit for soft-switching on-resistance measurement
(the gate and drain terminals are pulsed with independent voltage signals)

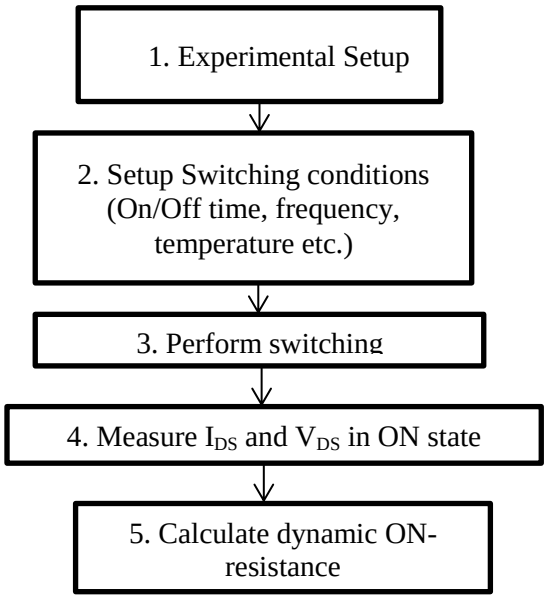
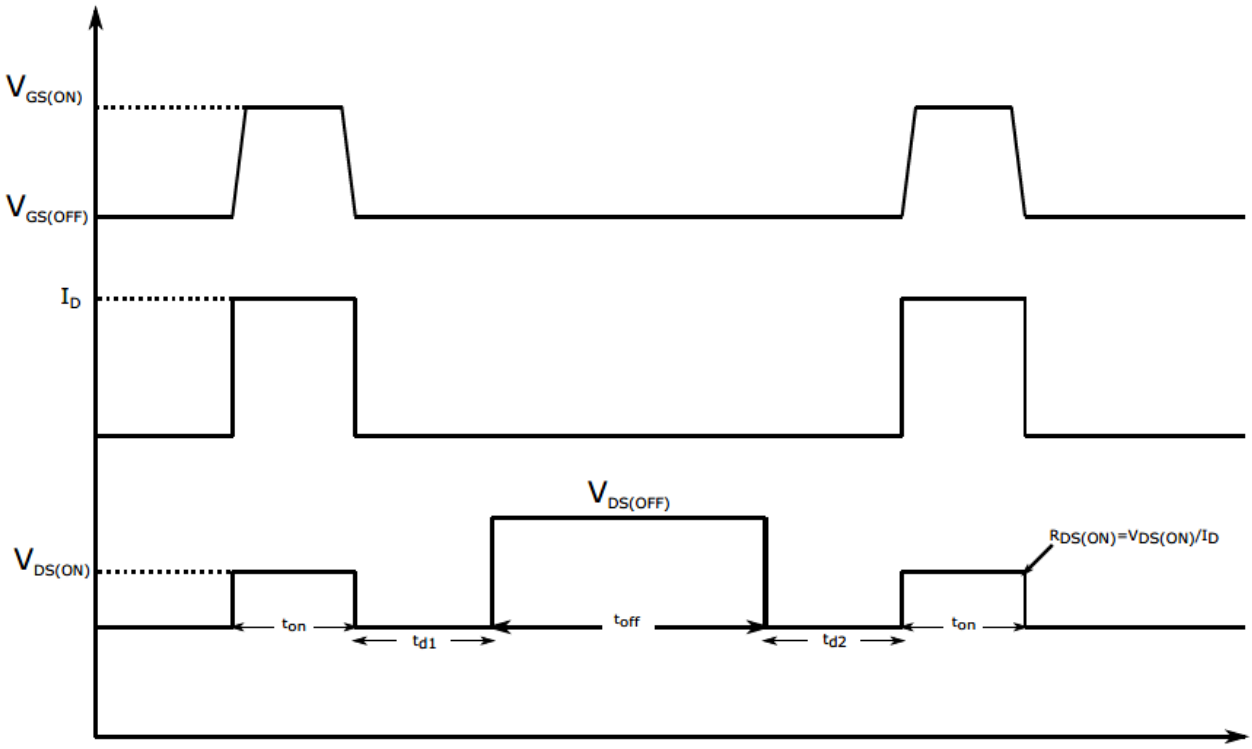


Figure 6 — Simplified flowchart for soft switching based dynamic on-resistance test

3.2 Pulsed Current-Voltage (I-V) method (cont'd)

As illustrated in Figure 7, the gate is initially pulsed ON while the drain is pulsed to a low value $V_{DS(ON)}$ such that the transistor is in the linear region of operation, where the ON-resistance may be evaluated as $R_{DS(ON)} = V_{DS(ON)}/I_D$. After a pause t_{d1} where gate and drain voltage are both zero, the drain is set to a high stress value while the gate remains OFF for a time t_{off}. Subsequently, after a second wait period t_{d2} where both gate and drain are again both zero, the ON-state gate and drain signals are repeated and the $R_{DS(ON)}$ is again measured. This measured $R_{DS(ON)}$ is compared to the initially measured value to see if any change has occurred due to the high drain voltage stress. This procedure may be repeated, with the drain sress voltage stepped to a higher value between each $R_{DS(ON)}$ measurement. Note that the stress time t_{off}, represents both the DC and pulsed states. As an example, the DC state can correspond to reliability stress time in qualification. On the other hand, the pulsed state may correspond to soft-switching applications. Similar methods may be employed with continuous switching of both gate and drain pulses with a definite frequency. The above described soft switching test methods may be applied for wafer and package level characterization, and reliability evaluations.



NOTE Measurement windows are interleaved with stress periods.

Figure 7 — Illustrative timing diagram for measuring dynamic ON-resistance under OFF-state stress in soft-switching mode.

4 Requirements

4.1 General parameter requirements

The list below in the tabular format provides the critical parameters whose numerical values are required to be recorded.

V_{DD}	Supply voltage
T_C	Case Temperature
I_D	Drain current of DUT in ON-state
t_{off}	OFF-state pulse width
t_{on}	ON-state pulse width
$t_{m,on}$	Measurement timing in ON-pulse
t_{dn}	Delay time between the OFF and ON pulse or vice-versa, with n = 1 or 2, applicable only for soft switching
f	Frequency
N	Number of pulses
P_{Peak}	Instantaneous Peak Power (optional), applicable only for hard switching
E_{Pulse}	Energy dissipated per pulse (optional), applicable only for hard switching

For a desired target DUT case temperature 'T_C', it is recommended to minimize self-heating effect to avoid any of its impact on dynamic ON-resistance measurement data. Choosing a low turn-on duty cycle in the test method will allow the case temperature to be very close to the DUT junction temperature.

During all the continuous mode operating tests, it is recommended to note down the time stamps at which the measurements are performed once the test begins for appropriate interpretation of results over time.

Provided that the test includes non-continuous switching such as the single-pulse mode or the traditional double-pulse test mode, it is required that individual ON and OFF pulse widths for such tests be specified.

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