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# Guidelines for Representing Switching Losses of SIC Mosfets in Datasheets

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# GUIDELINES FOR REPRESENTING SWITCHING LOSSES OF SIC MOSFETS IN DATASHEETS

## Contents

# GUIDELINES FOR REPRESENTING SWITCHING LOSSES OF SIC MOSFETS IN DATASHEETS

## Foreword

This document was formulated by JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use in the SiC power semiconductor and related power electronic industries, and provides guidelines for representation of switching losses and related measurement conditions on SC MOSFET device datasheets.

## Introduction

Switching losses are key parameters for evaluating power device performance, for benchmarking devices of different manufacturers and deciding on the suitability of a device in an application. Measurement and/or setup parameters can have a significant influence on the measured switching losses. Without clear definition of the methodology used, it is not possible to compare devices properly or, in some cases, even decide on its suitability for the target purpose.

The purpose of this document is to point out the factors that can influence switching losses for silicon carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and provide guidelines for a clean representation in datasheets.

# GUIDELINES FOR REPRESENTING SWITCHING LOSSES OF SIC MOSFETS IN DATASHEETS

(From JEDEC Board Ballot JCB-21-53, formulated under the cognizance of the JC-70.2 Subcommittee on SiC Power Electronic Conv. Semiconductor Standards.)

## 1 Scope

All power semiconductor devices incur switching losses that have to be taken carefully into account when evaluating and benchmarking device performance. For power transistors such as SiC MOSFETs, the losses include turn-on and turn-off losses. In case of SiC diodes, recovery losses also need to be included. In addition, losses originating from the device's internal capacitances need to be considered in application.

This document describes the impact of measurement and/or setup parameters on switching losses of power semiconductor switches; focusing primarily on SiC MOSFET turn-on losses. In terms of turn-off losses, the behavior of SiC MOSFETs is similar to that of existing silicon based power MOSFETs, and as such are adequately represented in typical datasheets. Therefore, the major focus of this representation guide is turn-on losses in SiC MOSFETs. The given methodology can be applied (in datasheets) for single devices, e.g., discrete packages, and parallel operated devices, e.g., power modules. It may also be applied in more complex topologies if topology specific specialties are taken into account.

## 2 Terms, definitions and letter symbols

| | |
|---|---|
| DUT | Device Under Test |
| FWD | Free-wheeling diode |
| $E_{ON}$ | Turn-on switching energy losses |
| $C_{GS}$ | Gate-source capacitance |
| $C_{GD}$ | Gate-drain capacitance |
| $C_{DS}$ | Drain-source capacitance |
| $C_{ISS}$ | Input capacitance |
| $C_{OSS}$ | Output capacitance |
| $C_{RSS}$ | Reverse-transfer capacitance |
| $V_{G,OFF}$ | Gate-source voltage applied to turn off the DUT |
| $V_{G,OFF,MIN}$ | Minimum value of $V_{GS,OFF}$ |
| $V_{G,OFF,MAX}$ | Maximum value of $V_{GS,OFF}$ |
| $V_{G,OFF,TYP}$ | Typical value of $V_{GS,OFF}$ |
| $V_{G,OFF,CHAR}$ | Recommended turn-off gate voltage in the datasheet |
| $V_{G,min}$ | Minimum turn-off gate voltage rating specified in the datasheet |
| $V_{GS,OFF(PASS)}$ | Gate-source voltage applied to turn off the passive switch |
| $Q_{RR}$ | Reverse recovery charge |
| $Q_C$ | Diode capacitive charge |
| $R_G$ | Gate resistance |
| $R_{G,TYP}$ | Typical gate resistance used for datasheet characterization tests |
| $V_T$ | Threshold voltage |
| dV/dt | Slew rate of drain-source voltage ($V_{DS}$) during DUT switching |

## 3 Description of switching losses in SiC MOSFETs

Switching losses for power transistors are typically measured under an inductive load in a double pulse circuit. In this measurement, during turn-on of the device under test (DUT), the free-wheeling diode (FWD) undergoes reverse recovery, and the reverse recovery current of the diode flows through the DUT and contributes to its turn-on energy loss ($E_{ON}$). As such, the reverse recovery behavior of the FWD can have a significant influence on the $E_{ON}$ of the DUT [1]. Therefore, the selection of the FWD and its operating conditions should be carefully considered for measuring $E_{ON}$ of SiC MOSFETs.

Focusing on device design, every power semiconductor switch has inherent capacitances that can be partly described as a capacitive equivalent network, as depicted in Figure 1.

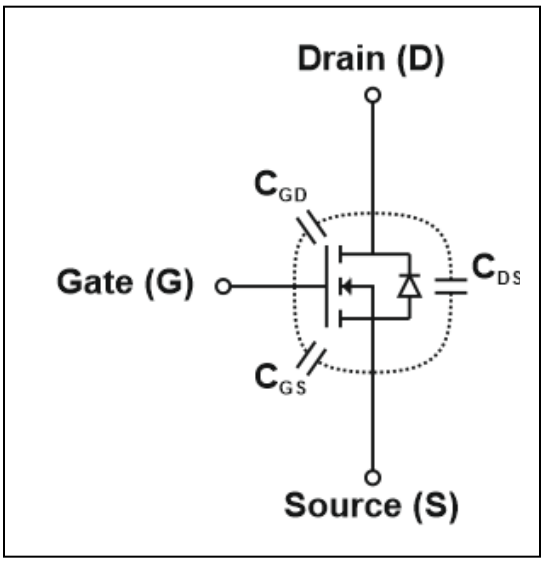



**Figure 1 — Schematic display of the macroscopic device capacitances exemplarily for a MOSFET**

- Input capacitance ($C_{ISS}$, i.e., $C_{GS} + C_{GD}$) characterizes the capacitive behavior in the gate circuit and is situated between gate and source and gate and drain.
- Output capacitance ($C_{OSS}$, i.e., $C_{DS} + C_{GD}$) characterizes the capacitive behavior in the load circuit, i.e., mainly the therein stored charges, and is situated between drain and source and gate and drain.
- Reverse transfer capacitance ($C_{RSS}$, i.e., $C_{GD}$) characterizes the capacitive coupling between load circuit and gate circuit and is situated between drain and gate.

During operation, any dV/dt in the gate circuit is transferred to the load circuit via the reverse transfer capacitance and vice versa. While dV/dt in the gate circuit is typically small, i.e., in the range of 100 V/µs, for SiC based power semiconductor switches, dV/dt in the load circuit can reach values of 50 kV/µs or even higher. A dV/dt in the load circuit forces a current flow to the gate via the reverse transfer capacitance. This forced (displacement) current has to be compensated by the gate driver via the gate resistor to keep the actual switching state. If the forced current is undercompensated, the power semiconductor switch alters its switching state temporarily and switches parasitically. After the gate driver compensates the forced current, the power semiconductor switch re-establishes its target switching state or comes back to the external applied gate voltage. This parasitic switching is an unintended switching event which can result in additional losses or, in the worst case, a device destruction if a bridge short circuit is triggered by this.

## 3 Description of switching losses in SiC MOSFETs (cont'd)

Several factors can favor or inhibit parasitic switching such as:

- Device design (primarily the ratio of gate-drain charge ($Q_{GD}$) to gate-source charge ($Q_{GS}$)),
- Topology,
- Switching slope, and
- Gate circuit including gate driver and gate impedance.

The impact of parasitic switching on losses depends on the circuit topology. For simple topologies like buck/booster stages or single switches, parasitic switching is induced by the power semiconductor switch itself, e.g. in a booster stage, a high positive dV/dt during turn-off is transferred via $C_{RSS}$ to the gate. As the resulting induced gate voltage is counteracting the turn-off switching event, higher turn-off losses may occur in case of large resistive and/or inductive elements in the gate circuit, which is a well understood behavior in power MOSFETs. If switching losses are determined properly, parasitic effects lead to higher but reasonable switching losses. Knowing details on switching slope, measurement setup, and gate-driver setup, allows verifying datasheet values.

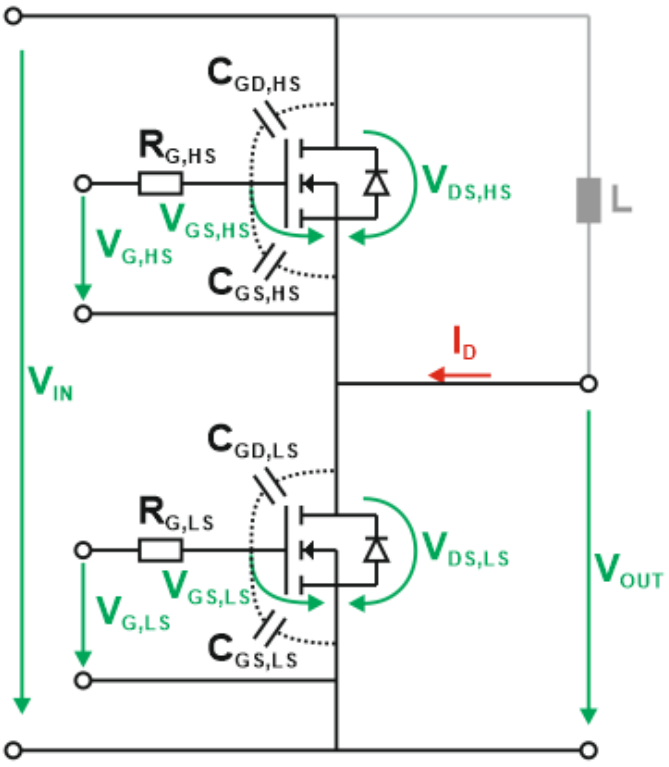
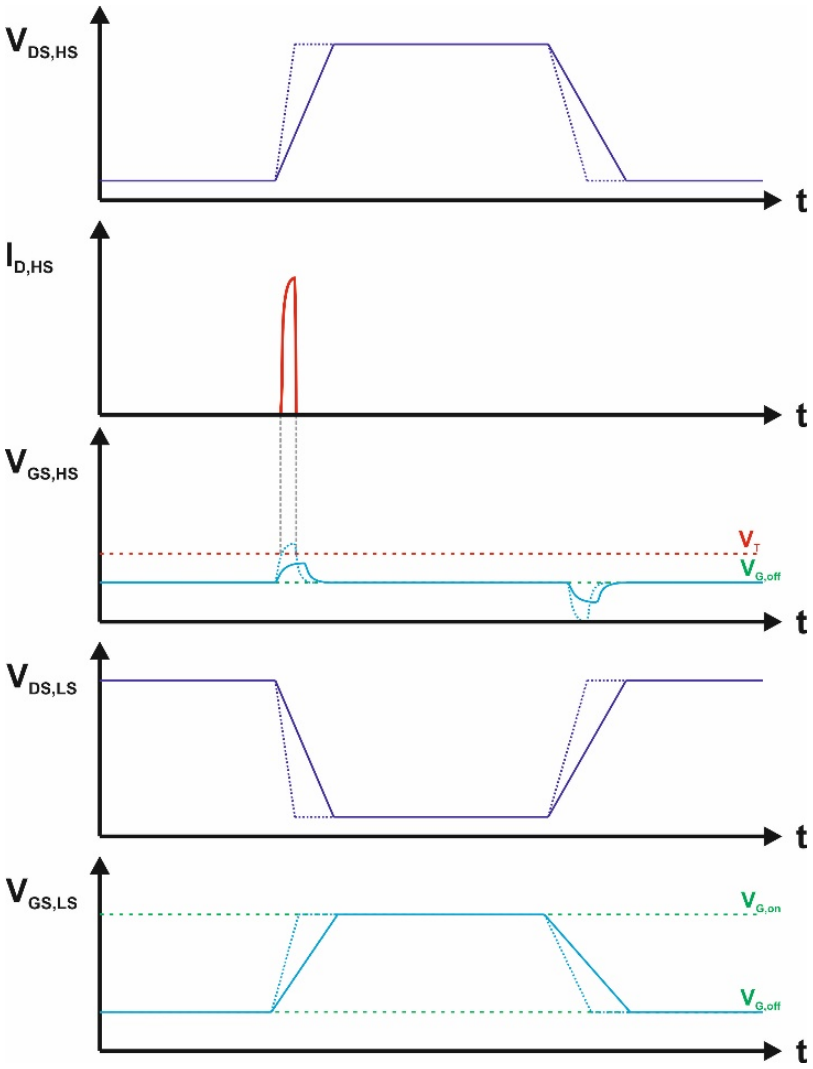



**Figure 2 — Schematic display of a half bridge structure utilizing MOSFETs on high side system (HS) and low side system (LS)**

## 3 Description of switching losses in SiC MOSFETs (cont'd)




NOTE Parasitic effects like over voltage peaks and/or impact of negative inductive feedback in the gate circuit are not shown.

**Figure 3 — Schematic display of transient waveforms in a half-bridge topology for high side system (HS) and low side system (LS is the active device)**

For a more complex topology, e.g., a half bridge (as shown in Figure 3, with exemplary waveforms in Figure 4), identical effects occur for the active power semiconductor switch, and the passive power semiconductor switch can switch parasitically as well. During turn-on of the active device, a negative dV/dt occurs at the output. For the passive device, this negative dV/dt results in a positive dV/dt in its load circuit that is transferred via $C_{RSS}$ on the passive device's gate. Depending on the resulting dV/dt, gate circuit, and capacitances of the passive device itself, a parasitic turn on can be induced, i.e., the passive device is conducting for a short period of time during the turn-on of the active device. As worst case consequence, a bridge short circuit could occur and the active device might be destroyed. Typically, parasitic turn-on increases switching losses of the active power semiconductor switch and induces additional switching losses for the passive power semiconductor switch.

## 3 Description of switching losses in SiC MOSFETs (cont'd)

For an active power semiconductor switch, Figure 4 exemplarily shows this increase of $E_{ON}$ up to a factor of two if $V_{G,off}$ is varied. These losses are neither considered nor specified in datasheets explicitly but are essential for the estimation of device's temperatures or power efficiency. It should be noted that applying a negative gate voltage may cause a small change in the threshold voltage of a SiC MOSFET, which can impact switching losses. This effect has been discussed in detail in previous JEDEC publications on $V_T$ measurement and bias-temperature instability (BTI) of SiC MOSFETs [2, 3].

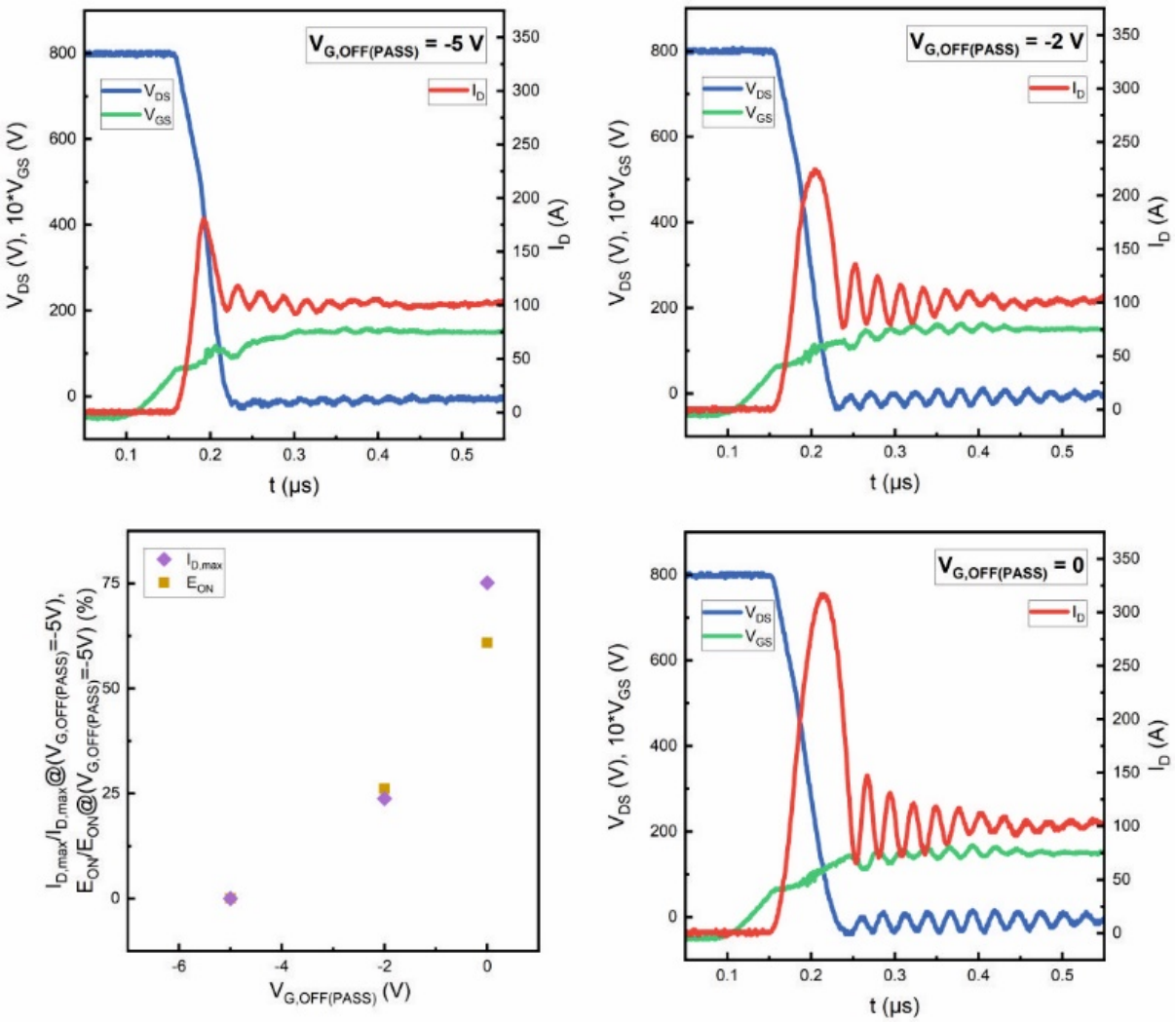



**Figure 4 — Exemplary switching curve for a SiC MOSFET during reverse recovery, showing increasing impact of parasitic turn-on of the passive switch on the high-side turn-on losses**

## 3 Description of switching losses in SiC MOSFETs (cont'd)

There are two common choices for the FWD for $E_{ON}$ measurement in SiC MOSFETs: (a) SiC Schottky Barrier Diode (SBD), and (b) the intrinsic body diode of a SiC MOSFET, often the same device as the DUT (active device). The reverse recovery charge ($Q_{RR}$) of a SiC SBD is primarily the capacitive charge ($Q_C$) of the diode (if operated in unipolar mode), and is largely independent of operating conditions like current and temperature. However, for a MOSFET body diode, its $Q_{RR}$ can depend on a number of factors, including gate voltage of the FWD device, temperature, load current, and current commutating slope (dI/dt). The $Q_{RR}$ of the body diode is influenced by the gate voltage through two mechanisms:

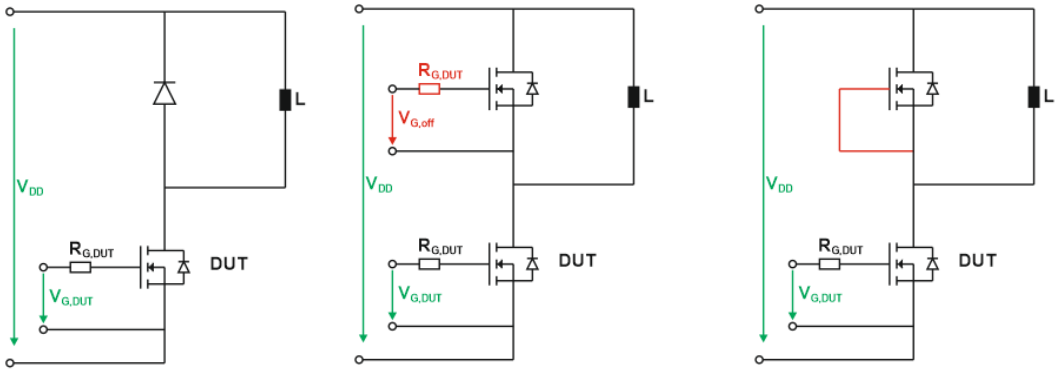
- Parasitic turn-on: As described previously, during the turn-on of the DUT (active switch), the channel of the FWD MOSFET can turn on because of positive dV/dt and feedback capacitance ($C_{RSS}$) between drain and gate of the MOSFET. This leads to additional current flow, which increases $E_{ON}$ of the DUT. This effect is especially important to consider for SiC MOSFETs because these devices are operated under higher dV/dt conditions, have lower threshold voltages (due to effects such as drain induced barrier lowering) and generally offer less negative gate voltage ratings than comparable silicon technologies like IGBTs. Parasitic turn-on can be prevented by applying a negative gate voltage on the FWD MOSFET's gate or by connecting the gate to the source through a low gate impedance, provided that the internal gate resistance of the MOSFET is also low.

- Current flow through channel during body diode forward operation: Depending on the gate voltage, a part of the diode current can flow through the MOS channel of the FWD MOSFET [4]. This channel current does not contribute to the carrier-stored part of $Q_{RR}$. If the MOS channel is turned off by applying a more negative gate voltage, a higher proportion of the current can flow through the junction body diode, which can increase stored charge and $Q_{RR}$. This effect is especially important at high junction temperatures in SiC MOSFETs because of the strong dependence of anode injection efficiency on temperature.

It should be noted that the parasitic switching effect also occurs in silicon based devices like MOSFETs or IGBTs. However, while Si based superjunction MOSFETs can switch at quite high dV/dt values, hard switching in half bridges/inverters are typically not part of their field of application; and buck or booster applications are less critical as explained above. For Si based IGBTs, although hard switching in inverter circuits is the major field of application, these devices are typically not switched at high dV/dt values in the range of 50 kV/µs or above. In addition, Si based IGBTs are characterized and operated with typical gate driver voltages of ±15 V which reduces the probability of parasitic effects significantly. Consequently, the limited range of gate driver voltages, large dV/dt, and operation in hard switching inverter circuits makes it necessary to consider parasitic effects for SiC based power semiconductor switches and provide a methodology of representation in datasheets.

## 4 Representation Guide

As outlined above, turn on measurement of a SiC MOSFET is strongly influenced by the choice and operating conditions of the FWD. Therefore, it is important that the choice of FWD and its operating conditions are documented in the turn on measurement in a device datasheet.
For single power semiconductor switches, a drawing of the characterization setup should be displayed, as shown in Figure 5. In this drawing, the devices used for characterization are indicated and, if a passive switch is situated in the free-wheeling path, the voltages at the passive switch's gate should be specified.




NOTE The figure includes free-wheeling path; here from left-hand side to right-hand side: distinct free-wheeling diode anti-parallel to load inductance, actively controlled MOSFET with inherent body diode as free-wheeling path, and gate-source shorted MOSFET, i.e., by an ideal Miller clamping, with inherent body diode as free-wheeling path. Relevant information on devices used and/or gate driver circuit of the high side system is highlighted in red color.

**Figure 5 — Sketch of a characterization setup**

In any configuration that contains an application relevant free-wheeling path, e.g., a booster stage or half bridge, no additional information on the characterization setup is required. In this case, the commutation will be performed as in the final application, i.e., either via a free-wheeling diode or passive device's body diode or passive device's channel. As the interacting parameters are manifold, a graph and/or table should be included. This graph (examples depicted in Figure 6) and/or table should provide the following information:

- Turn on losses or total losses, i.e., sum of turn on losses and turn off losses, versus the active switch's gate resistor or dV/dt, and
- Turn on losses or total losses, i.e., sum of turn on losses and turn off losses, versus the passive switch's off state gate voltage.

This information can also be combined in a single graph by displaying losses versus off state gate voltage for different gate resistor values or vice versa.

As the applied DC link voltage and the switched load current control the dV/dt, minimum representation of graphs is given for the typical DC link voltage and typical load current used for the device's characterization. The device temperature should be 25 °C and the maximum operating temperature.

## 4 Representation Guide (cont'd)

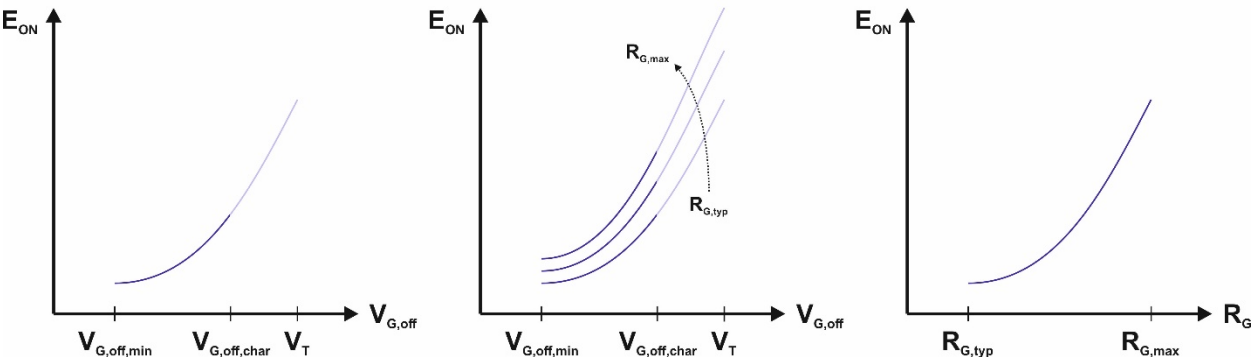



**Figure 6 — Exemplary and schematic drawings.**

As off-state gate voltage and gate resistor are fundamental factors for turn-on losses, the following ranges should be covered:

- Off-state gate voltage ($V_{G,off}$) needs to be considered at minimum two points:
  - $V_{G,off,typ} = V_{G,off,char}$ with the minimum applied gate voltage during switching/characterization as displayed in the datasheet
  - $V_{G,off,min} = V_{G,min}$ (the minimum recommended operating gate voltage as specified in the datasheet)

As $V_{G,off,max}$ is limited by the threshold voltage ($V_T$), off-state gate voltages larger than the gate-source threshold voltage at the corresponding device temperature should not be considered. If $V_{G,off,char}$ is smaller than $V_T$, the corresponding graph shall cover the range from $V_{G,min}$ to $V_{G,off,char}$.

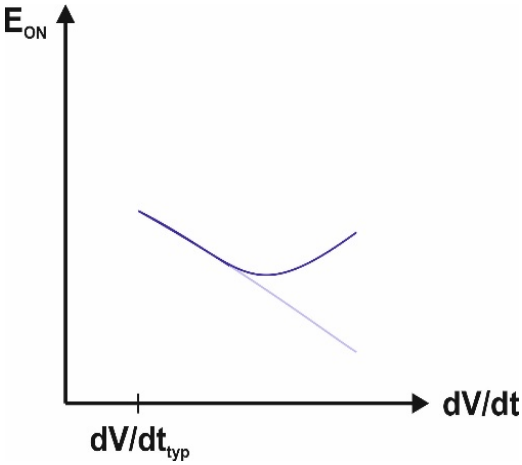
- Gate resistor ($R_G$) needs to be considered at minimum one point:
  - $R_{G,typ} = R_{G,char}$ with the gate resistor during switching/characterization as displayed in the datasheet

As switching losses are typically displayed from $R_{G,typ}$ to $10 \times R_{G,typ}$, the maximum $R_G$ displayed in the datasheet could also be considered.

If current controlled gate driver designs are used, gate resistor may not be the correct fundamental factor. In such cases, $R_G$ should be substituted by turn on dV/dt, i.e., $dV/dt_{typ}$ (example depicted in Figure 7). A suitable range of dV/dt should be considered; comparable to a given $R_G$ range.

Within this methodology, it is assumed that the same gate drivers, off-state voltages, and gate resistors are used for both active and passive power semiconductor switches. If this is not the case, the operating conditions of the passive power semiconductor switch must be specified in terms of $V_{G,OFF,TYP(PASS)}$ and $R_{G,TYP(PASS)}$.

## 4 Representation Guide (cont'd)




NOTE The semi-transparent line indicates $E_{ON}$ vs. dV/dt without parasitic turn-on.

**Figure 7 — Exemplary and schematic drawing**

As an alternative, a limited set of switching loss measurements may be provided which imposes a lower testing burden but still provides insight into the effect of parasitic turn-on. This set of measurements can be performed as follows:

$E_{ON}$ can be specified under three FWD choices:

a. Using a SiC SBD of similar current rating as the FWD. In this case, parasitic turn-on effect is completely eliminated and only the $Q_C$ of the diode primarily contributes to the $E_{ON}$ of the DUT.
b. Using the DUT's body diode as the FWD with negative gate voltage (maximum recommended negative gate-drive voltage provided by the manufacturer). This minimizes the likelihood of parasitic turn-on occurring, and only includes the body diode $Q_{RR}$ of the FWD.
c. Using the DUT's body diode as the FWD with zero gate voltage. This condition would represent the worst case parasitic turn-on effect, and may increase the $E_{ON}$ of the DUT.

For small SiC MOSFETs where the device capacitance and switching losses are small, the switching waveforms can also be influenced by parasitic capacitance from the circuit board or load inductance. In such cases, an estimate of the parasitic capacitance in the measurement circuit should be specified in the datasheet.

## 5 References

[1] K. Sobe, T. Basler and B. Klobucar, "Characterization of the parasitic turn-on behavior of discrete CoolSiC MOSFETs", Proc. PCIM, 2019.

[2] JEDEC JEP183, *Guidelines for measuring the threshold voltage (VT) of SiC MOSFETs*

[3] JEDEC JEP184, *Guideline for evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion*

[4] V. Pala, E. Van Brunt, S. H. Ryu, B. Hull, S. Allen, J. Palmour and A. Hefner, "Physics of Bipolar, Unipolar and Intermediate Conduction Modes in Silicon Carbide MOSFET Body Diodes", Proc. ISPSD, 2016, pp. 227-230

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