JEDEC STANDARD

POD135 - 1.35 V Pseudo Open Drain I/O

JESD8-21C.01

(Revision of JESD8-21C, JUNE 2019)

JUNE 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by

3103 North 10th Street

Suite 240 South

Arlington, VA 22201-2107

PRICE: Contact JEDEC

Printed in the U.S.A.

This page intentionally left blank

POD135 - 1.35V PSEUDO OPEN DRAIN I/O

(From JEDEC Board Ballot JCB-19-13, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the DC and AC single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.35V Pseudo Open Drain I/Os. The 1.35 V Pseudo Open Drain interface, also known as POD135, is primarily used to communicate with GDDR5 or GDDR5M SGRAM devices.

Multiple Classes of POD135 are expected to reside within the family of POD135 interfaces in order to accommodate various device and market applications. The various classes standardized within the context of POD135 are documented in the appendices of this document (e.g., POD135/Class A, POD135/Class B, etc).

The core of this standard defines documents the subset of values common to all Classes of POD135 and documents specification items left to definition within a specific Class as denoted by CDV which is defined as Class Dependent Value.

The values specific to each particular class of POD135 are found in the annexes. See specific Class tables for further details. (Note it does not follow that all specification values defined in a given Class are necessarily different from the matching parameter in other Class within POD135. Multiple Classes may reuse a given specification value if appropriate to the Class requirements.)

Classes were not part of the original POD135 specification. With the addition of Classes the original POD135 values remain unchanged and grouped as POD135/Class A and POD135/Class C. The updates to the specification are included in POD135/Class B and POD135/Class D. As other devices or market applications are defined, they may use one of the already defined Class(es) or define a new Class.

2 Core POD135 Interface Standard

Table 1 — DC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
Device Supply Voltage	VDD	1.3095	1.35	1.3905	V	1
Output Supply Voltage	VDDQ	1.3095	1.35	1.3905	V	1
Reference Voltage	VREF	CDV		CDV	V	2, 6
Reference Voltage for DQ and DBI_n pins	VREFD	CDV		CDV	V	2, 7
Reference Voltage for DQ and DBI_n pins	VREFD2	CDV		CDV	V	2, 7
External Reference Voltage for address and command	VREFC	CDV		CDV	V	3, 7
DC Input Logic HIGH Voltage	VIH (DC)	CDV			V	6
DC Input Logic LOW Voltage	VIL (DC)			CDV	V	6
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	CDV			V	7
DC Input Logic LOW Voltage for address and command	VILA (DC)			CDV	V	7
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD	VIHD (DC)	CDV			V	7
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD	VILD (DC)			CDV	V	7
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD2	VIHD2 (DC)	CDV			V	7
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD2	VILD2 (DC)			CDV	V	7
Input Logic HIGH Voltage for RESET_n, SEN, MF	VIHR	CDV			V	7
Input Logic LOW Voltage for RESET_n, SEN, MF	VILR			CDV	V	7
Input logic HIGH voltage for EDC1/2 (x16 mode detect)	VIHX	CDV			V	7
Input logic LOW voltage for EDC1/2 (x16 mode detect)	VILX			CDV	V	7
Input Leakage Current Any Input 0V <= V_{IN} <= VDDQ (All other pins not under test = 0V)	Il				µA	
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz				µA	
Output Logic LOW Voltage	VOL (DC)			0.56	V	

NOTE 1 GDDD5 SGRAM devices are designed to tolerate PCB designs with separate VDD and VDDQ power regulators.

NOTE 2 AC noise in the system is estimated at 50 mV pk-pk for the purpose of DRAM design.

NOTE 3 External VREFC is to be provided by the controller as there is no other alternative supply.

NOTE 4 DQ/DBI_n input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).

NOTE 5 ADD/CMD input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).

NOTE 6 Applicable to an interface with a single VREF for the device.

NOTE 7 Applicable to an interface with multiple VREF pins and levels

2 Core POD135 Interface Standard (cont'd)

Table 2 — AC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage	VIH (AC)	CDV			V	1
AC Input Logic Low Voltage	VIL (AC)			CDV	V	1
AC Input Logic HIGH Voltage for address and command	VIHA (AC)	CDV			V	2
AC Input Logic LOW Voltage for address and command	VILA (AC)			CDV	V	2
AC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD	VIHD (AC)	CDV			V	2
AC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD	VILD (AC)			CDV	V	2
AC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD2	VIHD2 (AC)	VREFD2 + 0.36			V	2
AC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD2	VILD2 (AC)			VREFD2 - 0.36	V	2
NOTE 1 Applicable to an interface with a single VREF for the device. See Class C in Annex A. NOTE 2 Applicable to an interface with multiple VREF pins and levels. See Class A and B in Annex A.						

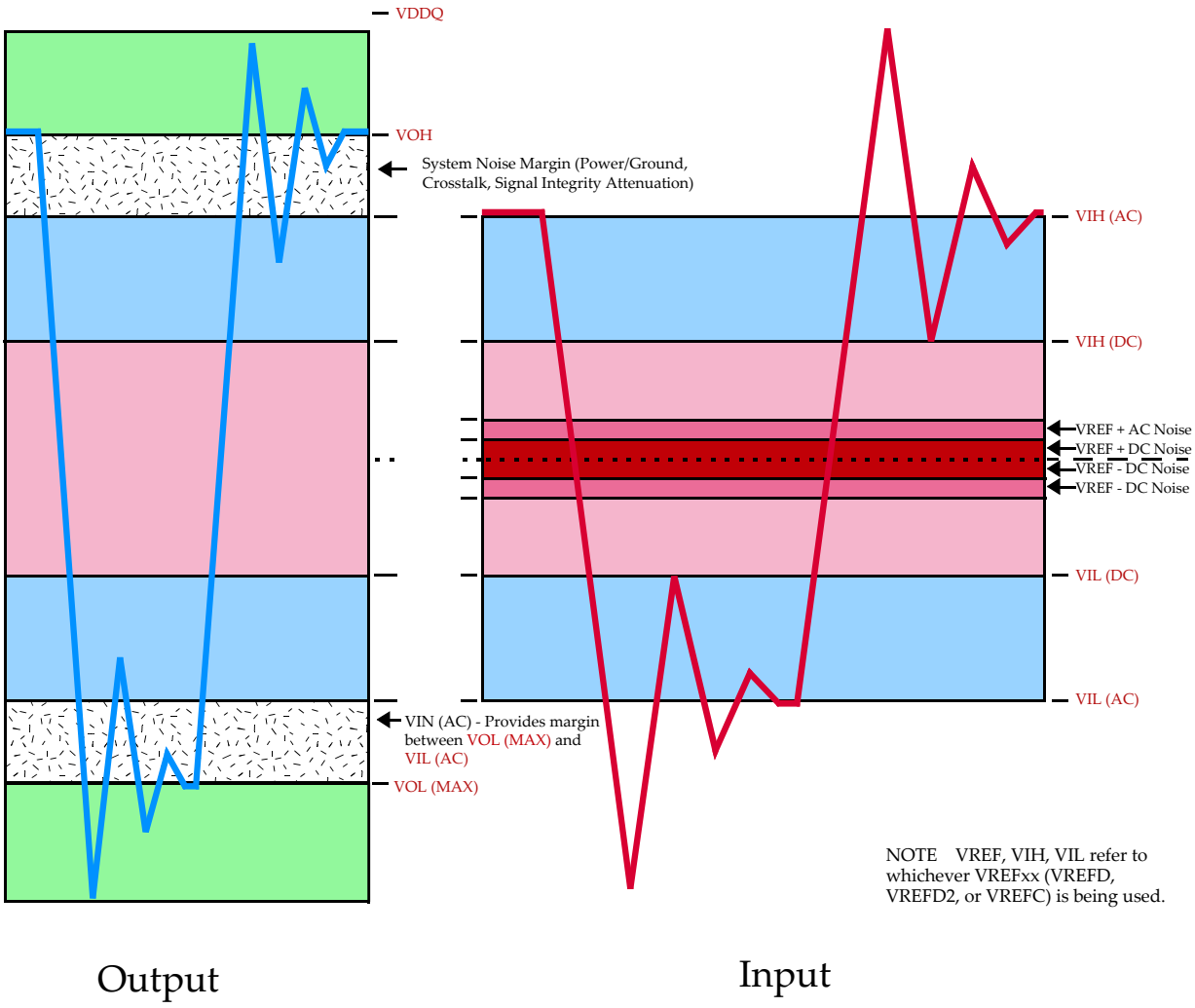


Figure 1 — Voltage Waveform

2 Core POD135 Interface Standard (cont'd)

Table 3 — Clock Input Operating Conditions

Parameter	Symbol	POD135		Unit	Note
		Min	Max		
Clock Input Mid-Point Voltage; CK_t and CK_c	VMP (DC)	VREFC - 0.10	VREFC + 0.10	V	1, 6
Clock Input Differential Voltage; CK_t and CK_c	VID or VIDCK (DC)	CDV		V	4, 6
Clock Input Differential Voltage; CK_t and CK_c	VID or VIDCK (AC)	CDV		V	2, 4, 6
Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (DC)	CDV		V	5, 7, 14
Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (AC)	CDV			2, 5, 7, 14
Clock Input Voltage Level; CK_t, CK_c, WCK_t and WCK_c single ended	VIN	-0.30	VDDQ + 0.30		
CK_t/CK_c Single ended slew rate	CKslew	2.7		V/ns	9
WCK_t/WCK_c Single ended slew rate	WCKslew	2.7		V/ns	10, 14
Clock Input Crossing Point Voltage; CK_t and CK_c	VIX or VIXCK (AC)	VREFC - 0.108	VREFC + 0.108	V	2, 3, 6
Clock Input Crossing Point Voltage; WCK_t and WCK_c	VIXWCK (AC)	VREFD - 0.09	VREFD + 0.09	V	2, 3, 7, 8, 14
Allowed time before ringback of CK/WCK below VIDCK/WCK(AC)	t_{DVAC}			ps	11, 12, 13, 14

NOTE 1 This provides a minimum of 0.845 V to a maximum of 1.045 V, and is nominally 70% of VDDQ with POD135. DRAM timings relative to CK_t/CK_c cannot be guaranteed if these limits are exceeded.

NOTE 2 For AC operations, all DC clock requirements must be satisfied as well.

NOTE 3 The value of VIXCK and VIXWCK is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.

NOTE 4 VIDCK is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is VREFC.

NOTE 5 VIDWCK is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either VREFD, VREFD2 or the internal VREFD. See Class A and B for the type of VREFD supported.

NOTE 6 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross.

NOTE 7. The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross.

NOTE 8 VREFD is either VREFD, VREFD2 or the internal VREFD. See Class A and B for the type of VREFD supported.

NOTE 9 The slew rate is measured between VREFC crossing and VIXCK(AC).

NOTE 10 The slew rate is measured between VREFD crossing and VIXWCK(AC).

NOTE 11 Figure 3 illustrates the exact relationship between (CK_t-CK_c) or (WCK_t-WCK_c) and VID(AC), VID(DC) and t_{DVAC}

NOTE 12 Ringback below VID(DC) is not allowed.

NOTE 13 t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of clock operating conditions and clock related parameters.

NOTE 14 Applicable to an interface with multiple VREF pins and levels (See Class A and B in Appendix A).

2 Core POD135 Interface Standard (cont'd)

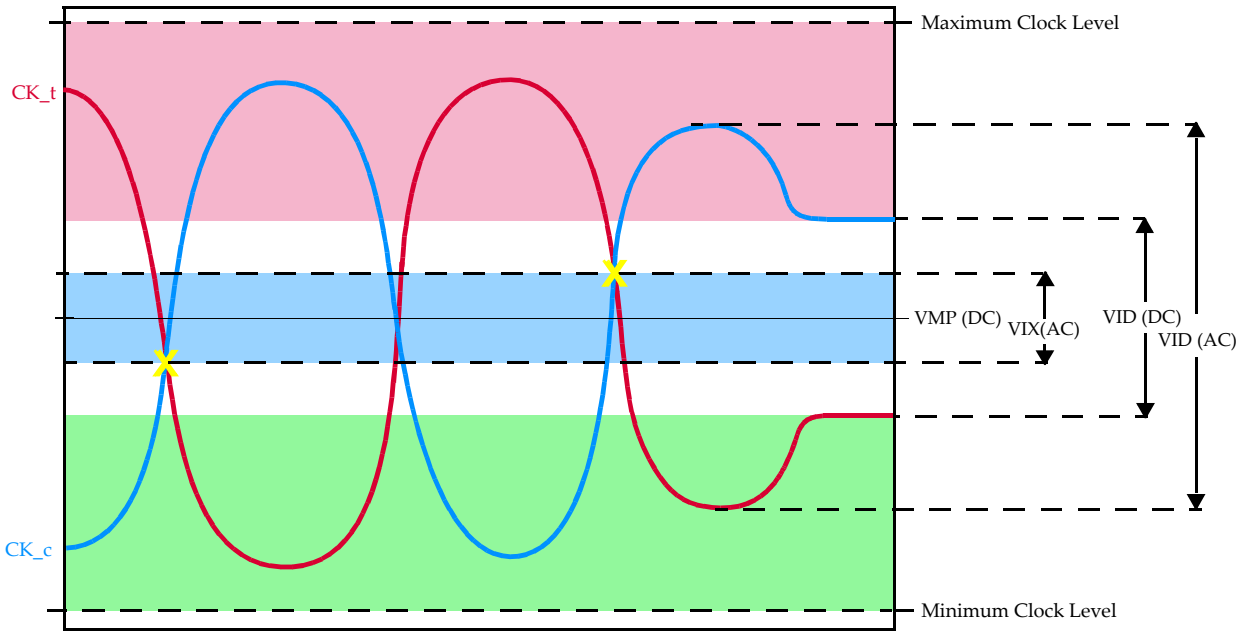


Figure 2 — Clock Waveform

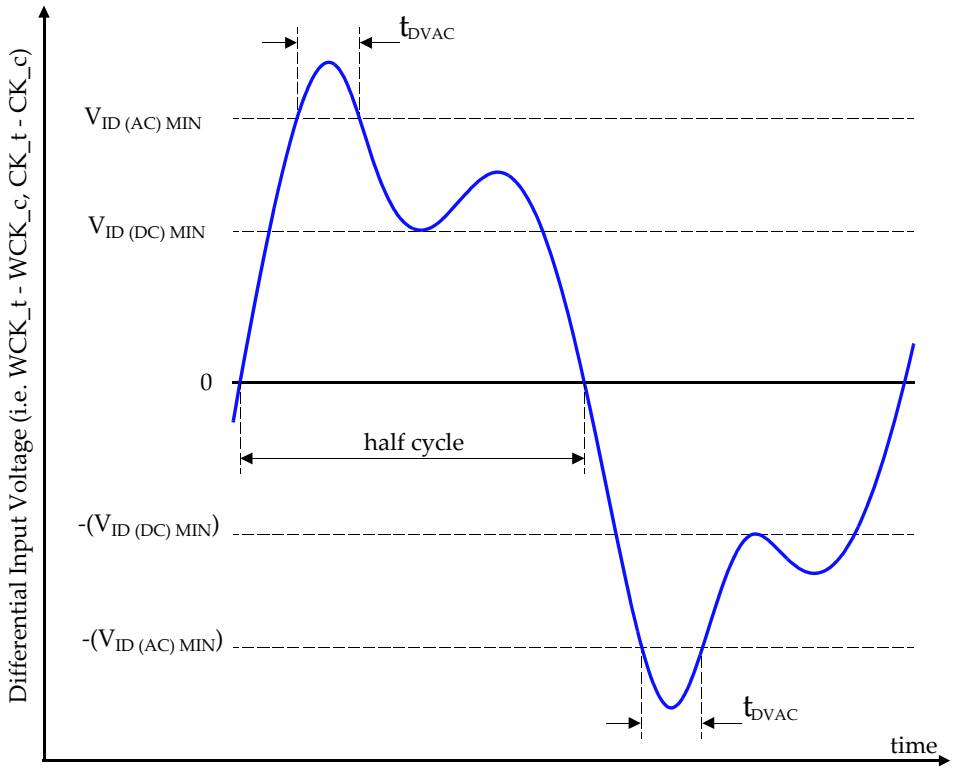


Figure 3 — Definition of Differential AC-swing and "Time Above AC-level" t_{DVAC}

2 Core POD135 Interface Standard (cont'd)

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.35 V (VDD/VDDQ)
2. Power the DRAM device and calibrate the output drivers and termination to eliminate process variation at 25 °C.
3. Reduce temperature to 10 °C recalibrate.
4. Reduce temperature to 0 °C and take the fast corner measurement.
5. Raise temperature to 75 °C and recalibrate
6. Raise temperature to 85 °C and take the slow corner measurement
7. Reiterate 2 to 6 with VDD/VDDQ 1.3095 V
8. Reiterate 2 to 6 with VDD/VDDQ 1.3905 V
9. All obtained Driver and Termination IV characteristics have to be bounded by the specified MIN and MAX IV characteristics

The values in Table 4 (Ideal with +/- 10% min/max) are targets for the designer and are not required to be met. Vendor datasheets should be consulted for further details. It is expected that the characteristics of the real curves will have some non-linearity as shown in Figure 6 and Figure 7. This may help to reduce the overall capacitance and boost performance. It is up to the designer to find the optimum combination of linearity and capacitance for best Rx and Tx performance.

Table 4 — 1.35 V I/O Impedances

Pull-Down Characteristic at 40 ohms			
Voltage (V)	**MIN (mA)**	**Ideal (mA)**	**MAX (mA)**
0.1	2.25	2.50	2.75
0.2	4.50	5.00	5.50
0.3	6.75	7.50	8.25
0.4	9.00	10.00	11.00
0.5	11.25	12.50	13.75
0.6	13.50	15.00	16.50
0.7	15.75	17.50	19.25
0.8	18.00	20.00	22.00
0.9	20.25	22.50	24.75
1.0	22.50	25.00	27.50
1.1	24.75	27.50	30.25
1.2	27.00	30.00	33.00
1.3	29.25	32.50	35.75
1.35	30.15	33.75	37.12

Pull-Up/Termination Characteristic at 60 ohms			
Voltage (V)	**MIN (mA)**	**Ideal (mA)**	**MAX (mA)**
0.1	-1.50	-1.67	-1.83
0.2	-3.00	-3.33	-3.67
0.3	-4.50	-5.00	-5.50
0.4	-6.00	-6.67	-7.33
0.5	-7.50	-8.33	-9.17
0.6	-9.00	-10.00	-11.00
0.7	-10.50	-11.67	-12.83
0.8	-12.00	-13.33	-14.67
0.9	-13.50	-15.00	-16.50
1.0	-15.00	-16.67	-18.33
1.1	-16.50	-18.33	-20.17
1.2	-18.00	-20.00	-22.00
1.3	-19.50	-21.67	-23.83
1.35	-20.25	-22.50	-24.75

2 Core POD135 Interface Standard (cont'd)

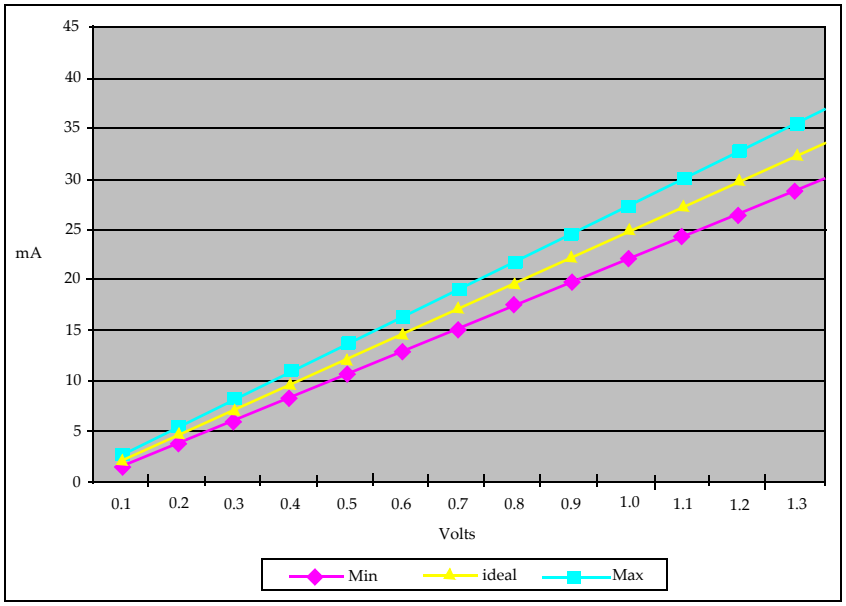


Figure 4 — Target Pull Down Characteristic at 40 ohms

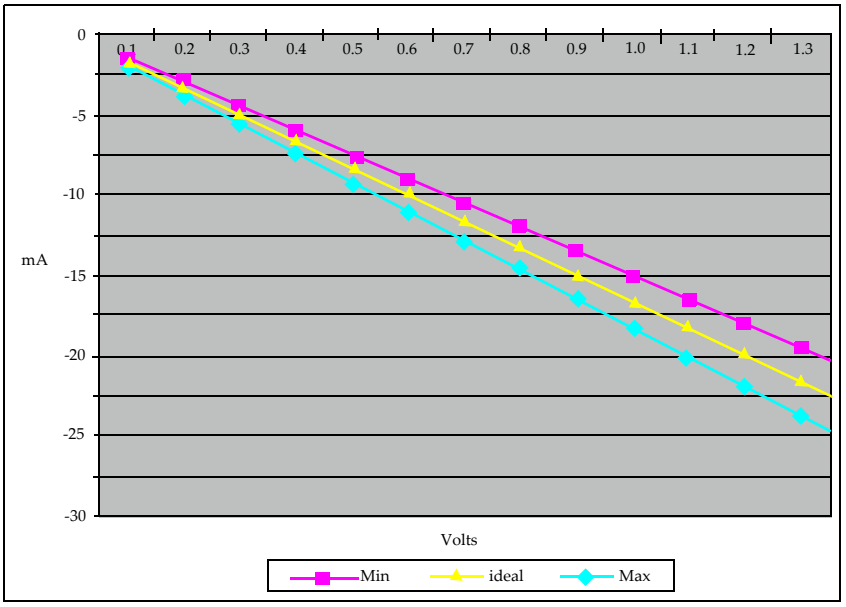


Figure 5 — Target Pull Up/Termination Characteristic at 60 ohms

2 Core POD135 Interface Standard (cont'd)

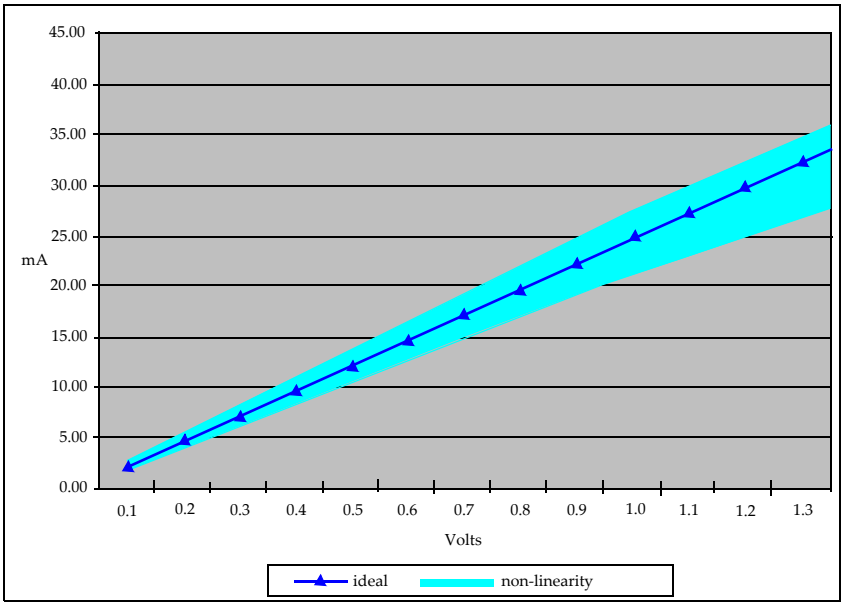


Figure 6 — Example of Non-linearity, Pull Down Characteristic at 40 ohms

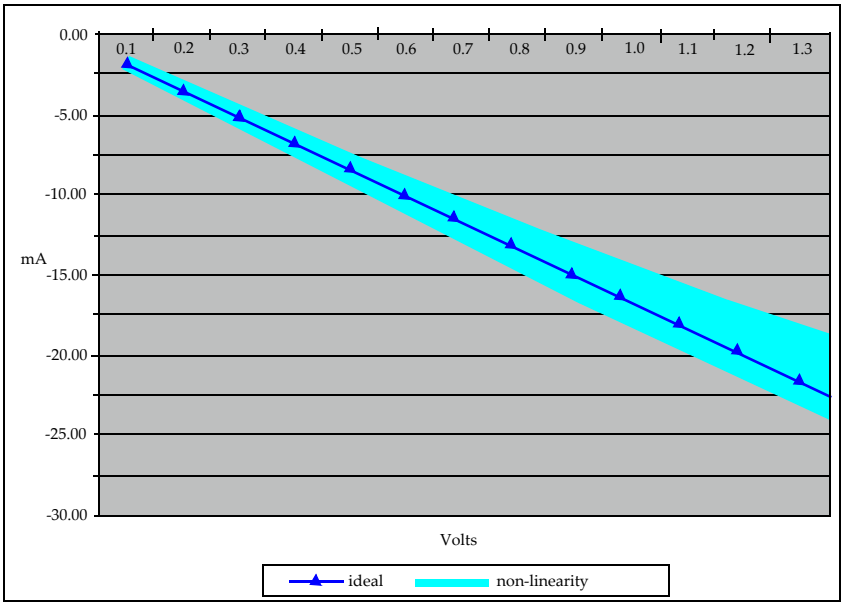


Figure 7 — Example of Non-linearity, Pull Up/Termination Characteristic at 60 ohms

3 Additional Background Information

The POD I/O system is optimized for small systems with data rates exceeding 2.0 Gbps. The system allows a single Initiator to control one or two Target devices in the case of GDDR5. The POD driver uses a 40/60 Ohm output impedance that drives into a 60 Ohm equivalent terminator tied to VDDQ. Single, dual and quad load systems are shown as follows:

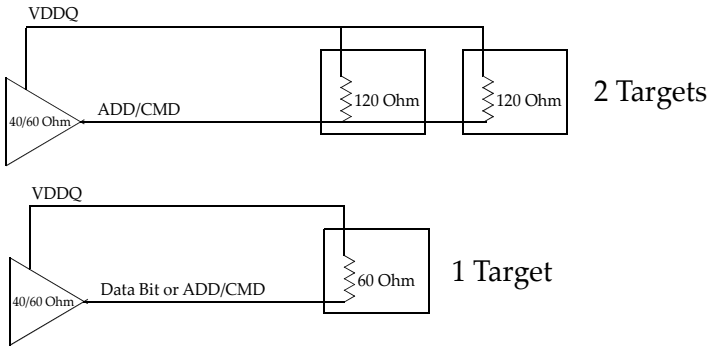


Figure 8 — System Configurations

The POD Initiator I/O cell is comprised of a 40/60 ohm driver and a terminator of 60 ohms. The Initiator POD cell's terminator is disabled when the output driver is enabled. The basic cell is shown in Figure 9.

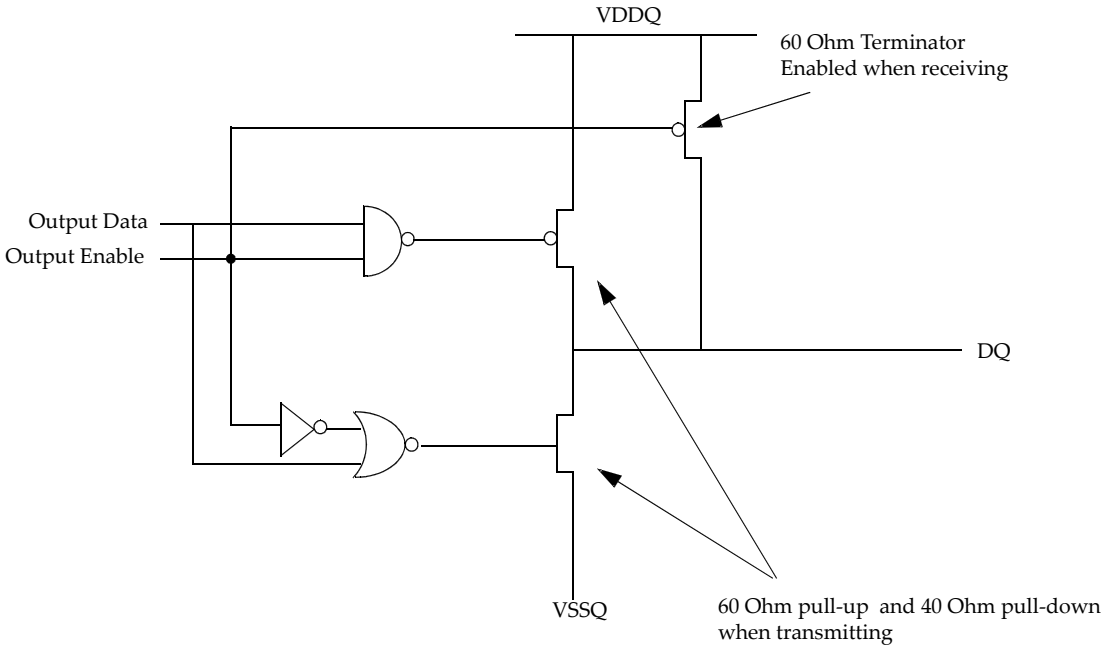


Figure 9 — Initiator I/O Cell

3 Additional Background Information (cont'd)

The POD Target I/O cell is comprised of a 40/60 ohm driver and programmable terminator of 60 or 120 ohms for GDDR5. The Target POD cell's terminator is disabled when the output driver is enabled or any other Target output driver is enabled. The basic cell is shown in Figure 10.

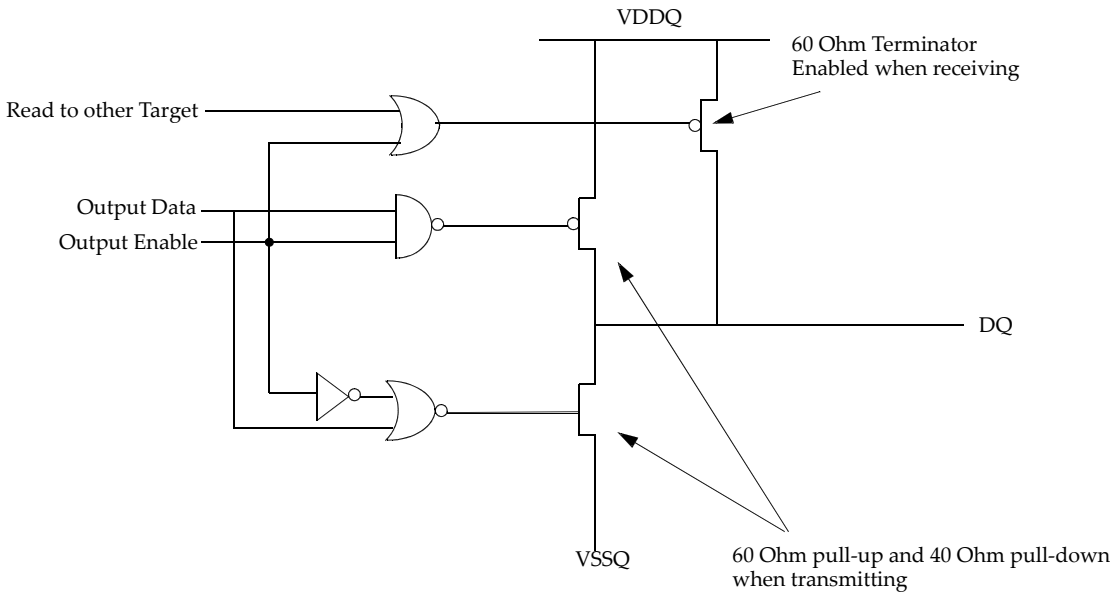


Figure 10 — Target I/O Cell

The POD Initiator and Target I/O cells are intended to have their driver and terminators combined together to minimize the area needed to implement the cell and reduce input capacitance. For GDDR5 this is possible by using three 120 ohm driver/terminator sub cells that are connected in parallel. The combinations used are as follows.

Table 5 — POD I/O Sub Cells, 120 ohm Based

Number of 120 ohm Sub Cells Enabled	Resulting Impedance	Use
1	120 ohms	2 Target loads or
2	60 ohms	1 Target load or Initiator terminator
3	40 ohms	Initiator or Target Driver

To ensure that the target impedance is achieved the POD I/O cell is designed to be calibrated to an external 1% precision resistor.

The following procedure may be used to calibrate the cell:

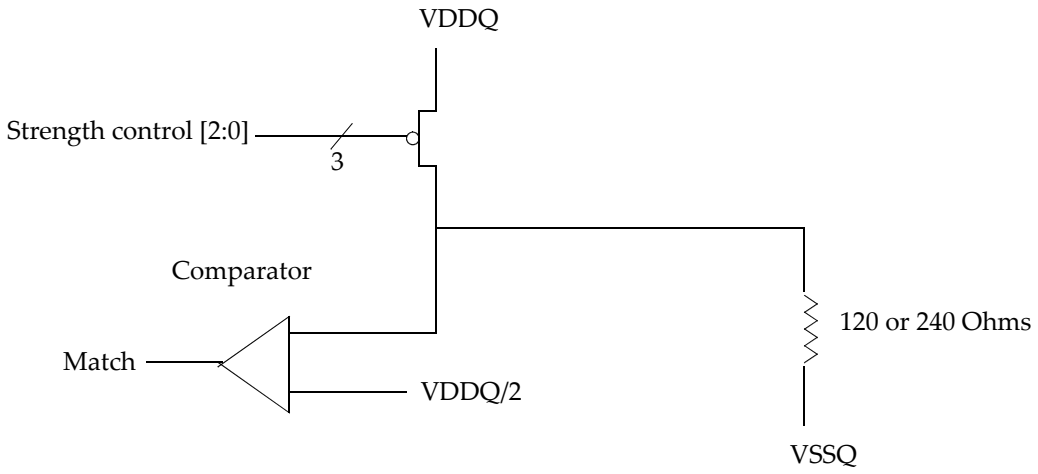
1.) First calibrate the PMOS device against a 120 ohm resister to VSS via the ZQ pin as illustrated in Figure 11.

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VDDQ/2
- PMOS device is calibrated to 120 ohms

3 Additional Background Information (cont'd)

2.) Then calibrate the NMOS device against the calibrated 120 ohm PMOS device as illustrate in Figure 12.

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than VDDQ/2
- NMOS device is now calibrated to 120 ohms



When Match PMOS leg is calibrated to 120 ohms

Figure 11 — PMOS Calibration

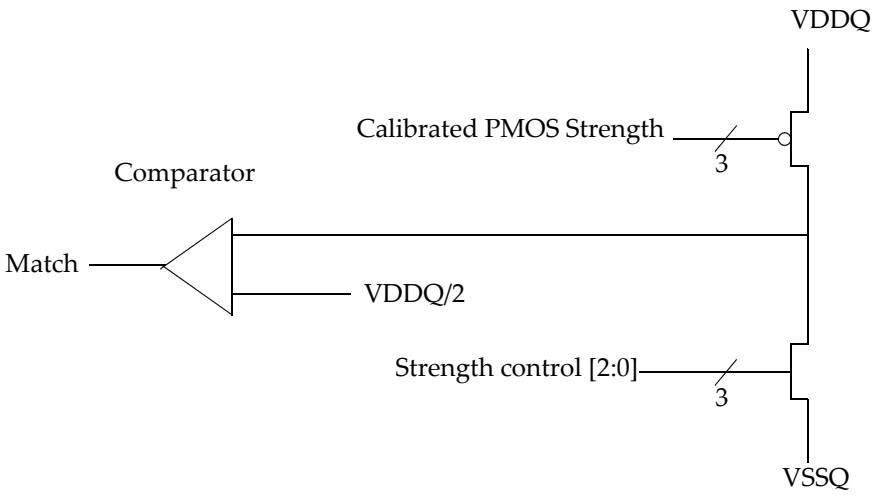


Figure 12 — MOS Calibration

Annex A — POD135 Classes

A.1 POD135/Class A

POD135/Class A is intended for GDDR5 devices (JESD212). Class A devices may have either external VREFD, VREFD2 or internal VREFD.

Table 6 — Class A DC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
Reference Voltage for DQ and DBI_n pins	VREFD	0.69 * VDDQ		0.71 * VDDQ	V	1, 2, 8
Reference Voltage for DQ and DBI_n pins	VREFD2	0.49 * VDDQ		0.51 * VDDQ	V	1, 2, 3, 8
External Reference Voltage for address and command	VREFC	0.69 * VDDQ		0.71 * VDDQ	V	4, 8
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	VREFC + 135			V	8
DC Input Logic LOW Voltage for address and command	VILA (DC)			VREFC - 0.135	V	8
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD	VIHD (DC)	VREFD + 0.09			V	8
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD	VILD (DC)			VREFD - 0.09	V	8
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD2	VIHD2 (DC)	VREFD2 + 0.27			V	8
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD2	VILD2 (DC)			VREFD2 - 0.27	V	8
Input logic HIGH voltage for EDC1/2 (x16 mode detect)	VIHX	VDDQ - 0.3			V	7, 8
Input logic LOW voltage for EDC1/2 (x16 mode detect)	VILX			0.30	V	7, 8

NOTE 1 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 2 Source of Reference Voltage and control of Reference Voltage for DQ and DBI_n pins is determined by VREFD, Half VREFD, Auto VREFD, VREFD MERGE and VREFD Offsets mode registers.
NOTE 3 VREFD Offsets are not supported with VREFD2.
NOTE 4 External VREFC is to be provided by the controller as there is no other alternative supply.
NOTE 5 DQ/DBI_n input slew rate must be greater than or equal to 2.7V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).
NOTE 6 ADD/CMD input slew rate must be greater than or equal to 2.7V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
NOTE 7 VIHX and VILX define the voltage levels for the receiver that detects x32 or x16 mode with RESET_n going High.
NOTE 8 Applicable to an interface with multiple VREF pins and levels.

Table 7 — Class A AC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage for address and command	VIHA (AC)	VREFC + 0.18			V	1
AC Input Logic LOW Voltage for address and command	VILA (AC)			VREFC - 0.18	V	1
AC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD	VIHD (AC)	VREFD + 0.135			V	1
AC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD	VILD (AC)			VREFD - 0.135	V	1

NOTE 1 Applicable to an interface with multiple VREF pins and levels.

A.1 POD135/Class A (cont'd)

Table 8 — Class A Clock Input Operating Conditions

Parameter	Symbol	POD135		Unit	Note
		Min	Max		
Clock Input Differential Voltage; CK_t and CK_c	VIDCK (DC)	0.198		V	2, 4
Clock Input Differential Voltage; CK_t and CK_c	VIDCK (AC)	0.36		V	1, 2, 4
Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (DC)	0.18		V	3, 5, 6
Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (AC)	0.27			1,3, 5, 6

NOTE 1 For AC operations, all DC clock requirements must be satisfied as well.

NOTE 2 VIDCK is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is VREFC.

NOTE 3 VIDWCK is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either VREFD, VREFD2 or the internal VREFD.

NOTE 4 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross.

NOTE 5 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross.

NOTE 6 Applicable to an interface with multiple VREF pins and levels.

A.2 POD135/Class B

POD135/Class B is intended for GDDR5M devices (JESD228). Class B devices may have either internal VREFD or VREFD2.

Table 9 — Class B DC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
Internal Reference Voltage for DQ and DBI_n pin(s)	VREFD	0.69 * VDDQ		0.71 * VDDQ	V	1, 2, 6
Internal Reference Voltage for DQ and DBI_n pin(s)	VREFD2	0.49 * VDDQ		0.51 * VDDQ	V	1, 2, 6
External Reference Voltage for address and command	VREFC	0.69 * VDDQ		0.71 * VDDQ	V	3, 6
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	VREFC + 0.10			V	6
DC Input Logic LOW Voltage for address and command	VILA (DC)			VREFC - 0.10	V	6
DC Input Logic HIGH Voltage for DQ and DBI_n pin(s) with VREFD	VIHD (DC)	VREFD + 0.09			V	6
DC Input Logic LOW Voltage for DQ and DBI_n pin(s) with VREFD	VILD (DC)			VREFD - 0.09	V	6
DC Input Logic HIGH Voltage for DQ and DBI_n pin(s) with VREFD2	VIHD2 (DC)	VREFD2 + 0.27			V	6
DC Input Logic LOW Voltage for DQ and DBI_n pin(s) with VREFD2	VILD2 (DC)			VREFD2 - 0.27	V	6
Input Logic HIGH Voltage for RESET_n, MF, DBI_n input for Device ID assignment at power-up (x8 only)	VIHR	VDDQ - 0.50			V	6
Input Logic LOW Voltage for RESET_n, MF, DBI_n input for Device ID assignment at power-up (x8 only)	VILR			0.30	V	6

NOTE 1 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 2 Reference Voltage for DQ and DBI_n pins is determined by Half VREFD and VREFD Offsets mode registers.
NOTE 3 External VREFC is to be provided by the controller as there is no other alternative supply.
NOTE 4 DQ/DBI_n input slew rate must be greater than or equal to 2.7V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).
NOTE 5 ADD/CMD input slew rate must be greater than or equal to 2.7V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
NOTE 6 Applicable to an interface with multiple VREF pins and levels.

Table 10 — Class B AC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage for address and command	VIHA (AC)	VREFC + 0.125			V	1
AC Input Logic LOW Voltage for address and command	VILA (AC)			VREFC - 0.125	V	1
AC Input Logic HIGH Voltage for DQ and DBI_n pin(s) with VREFD	VIHD (AC)	VREFD + 0.125			V	1
AC Input Logic LOW Voltage for DQ and DBI_n pin(s) with VREFD	VILD (AC)			VREFD - 0.125	V	1

NOTE 1 Applicable to an interface with multiple VREF pins and levels.

A.2 POD135/Class B (cont'd)

Table 11 — Class B Clock Input Operating Conditions

Parameter	Symbol	POD135		Unit	Note
		Min	Max		
Clock Input Differential Voltage; CK_t and CK_c	VIDCK (DC)	VIHA (DC) - VILA (DC)		V	2, 4
Clock Input Differential Voltage; CK_t and CK_c	VIDCK (AC)	VIHA (AC) - VILA (AC)		V	1, 2, 4
WRITE Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (DC)	VIHD (DC) - VILD (DC)		V	3, 5, 6
WRITE Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (AC)	VIHD (AC) - VILD (AC)			1, 3, 5, 6

NOTE 1 For AC operations, all DC clock requirements must be satisfied as well.

NOTE 2 VIDCK is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is VREFC.

NOTE 3 VIDWCK is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either internal VREFD or VREFD2.

NOTE 4 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross.

NOTE 5 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross.

NOTE 6 Applicable to an interface with multiple VREF pins and levels.

A.3 POD135/Class C

POD135/Class C is intended for point-to-point connections with a single VREF

Table 12 — Class C DC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
Reference Voltage	VREF	0.69 * VDDQ		0.71 * VDDQ	V	1, 2
DC Input Logic HIGH Voltage	VIH (DC)	VREF + 0.108			V	2
DC Input Logic LOW Voltage	VIL (DC)			VREF - 0.108	V	2

NOTE 1 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 2 Applicable to an interface with a single VREF for the device.

.

Table 13 — Class C AC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage	VIH (AC)	VREF + 0.18			V	1
AC Input Logic Low Voltage	VIL (AC)			VREF - 0.18	V	1

NOTE 1 Applicable to an interface with a single VREF for the device.

Table 14 — Class C Clock Input Operating Conditions

Parameter	Symbol	POD135		Unit	Note
		Min	Max		
Clock Input Differential Voltage; CK_t and CK_c	VID (DC)	0.198		V	2, 3
Clock Input Differential Voltage; CK_t and CK_c	VID (AC)	0.36		V	1, 2, 3

NOTE 1 For AC operations, all DC clock requirements must be satisfied as well.
NOTE 2 VID is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is VREF.
NOTE 3 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross.

A.4 POD135/Class D

POD135/Class D is primarily intended for GDDR6 devices (JESDxxx). Class D devices have either external or internal V_{REFC} or V_{REFC2} for CA, and internal V_{REFD} or V_{REFD2} for data.

Table 15 — Class D DC Operating Conditions

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
Pump voltage	V_{PP}	1.746	1.8	1.908	V	2
Reference voltage: DQ and DBI_n pins	V_{REFD}		$0.7 * V_{DDQ}$ or $0.725 * V_{DDQ}$		V	3, 4
	V_{REFD2}		$0.5 * V_{DDQ}$		V	3, 4, 5
Reference voltage: CA pins	V_{REFC}	$0.69 * V_{DDQ}$		$0.71 * V_{DDQ}$	V	6
	V_{REFC2}	$0.49 * V_{DDQ}$		$0.51 * V_{DDQ}$	V	6, 7
DC input logic HIGH voltage with V_{REFC}: CA	$V_{IHA}(DC)$	$V_{REFC} + 0.135$			V	
DC input logic LOW voltage with V_{REFC}: CA	$V_{ILA}(DC)$			$V_{REFC} - 0.135$	V	
DC input logic HIGH voltage with V_{REFC2}: CA	$V_{IHA2}(DC)$	$V_{REFC2} + 0.27$			V	
DC input logic LOW voltage with V_{REFC2}: CA	$V_{ILA2}(DC)$			$V_{REFC2} - 0.27$	V	
DC input logic HIGH voltage with V_{REFD}: DQ and DBI_n	$V_{IHD}(DC)$	$V_{REFD} + 0.09$			V	
DC input logic LOW voltage with V_{REFD}: DQ and DBI_n	$V_{ILD}(DC)$			$V_{REFD} - 0.09$	V	
DC input logic HIGH voltage with V_{REFD2}: DQ and DBI_n	$V_{IHD2}(DC)$	$V_{REFD2} + 0.27$			V	
DC input logic LOW voltage with V_{REFD2}: DQ and DBI_n	$V_{ILD2}(DC)$			$V_{REFD2} - 0.27$	V	
RESET_n and Boundary Scan input logic HIGH voltage; EDC and CA input logic high voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{IHR}	$0.8 * V_{DDQ}$			V	8
RESET_n and Boundary Scan input logic LOW voltage; EDC and CA input logic low voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{ILR}			$0.2 * V_{DDQ}$	V	8
Clock input differential voltage: CK_t, CK_c	$V_{IDCK}(DC)$	0.198			V	9, 11
Clock input differential voltage: WCK_t, WCK_c	$V_{IDWCK}(DC)$	0.18			V	10, 12

NOTE 1 GDDR6 SGRAMs are designed to tolerate PCB designs with separate V_{DD} and V_{DDQ} power regulators.

NOTE 2 DC bandwidth is limited to 20 MHz.

NOTE 3 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.

NOTE 4 The reference voltage for DQ and DBI_n pins is generated internally, and its values are determined by the Half VREFD and VREFD Level mode register bits. The typical V_{REFD} level depends on the selected data termination value (48 Ohm or 60 Ohm); see Mode Register 6 (MR6) for details.

NOTE 5 Programmable VREFD levels are not supported with V_{REFD2}.

NOTE 6 The reference voltage source (external or internal) is determined at power-up; the reference voltage level is determined by Half VREFC and the VREFC Offset mode register bits.

NOTE 7 Programmable VREFC offsets are not supported with V_{REFC2}.

NOTE 8 V_{IHR} and V_{ILR} apply to boundary scan input pins TDI, TMS and TCK. V_{IHR} and V_{ILR} apply to EDC and CA inputs at reset when latching default device configurations. V_{IHR} and V_{ILR} also apply to CA, CABI_n, CKE_n, CK, DQ, DBI_n, EDC and WCK inputs when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.

NOTE 9 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.

NOTE 10 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.

NOTE 11 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC Timings table.

NOTE 12 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table.

A.4 POD135/Class D (cont'd)

Table 16 — Class D AC Operating Conditions (For Design only[6])

Parameter	Symbol	POD135			Unit	Note
		Min	Typ	Max		
AC input logic HIGH voltage with V_{REFC}: CA	$V_{IHA}(AC)$	V_{REFC} + 0.18			V	
AC input logic LOW voltage with V_{REFC}: CA	$V_{ILA}(AC)$			V_{REFC} - 0.18	V	
AC input logic HIGH voltage with V_{REFC2}: CA	$V_{IHA2}(AC)$	V_{REFC} + 0.36			V	
AC input logic LOW voltage with V_{REFC2}: CA	$V_{ILA2}(AC)$			V_{REFC} - 0.36	V	
AC input logic HIGH voltage with V_{REFD}: DQ and DBI_n	$V_{IHD}(AC)$	V_{REFD} + 0.135			V	
AC input logic LOW voltage with V_{REFD}: DQ and DBI_n	$V_{ILD}(AC)$			V_{REFD} - 0.135	V	
AC input logic HIGH voltage with V_{REFD2}: DQ and DBI_n	$V_{IHD2}(AC)$	V_{REFD2} + 0.36			V	
AC input logic LOW voltage with V_{REFD2}: DQ and DBI_n	$V_{ILD2}(AC)$			V_{REFD2} - 0.36	V	
Clock input differential voltage: CK_t, CK_c	$V_{IDCK}(AC)$	0.36			V	1, 2, 4
Clock input differential voltage: WCK_t, WCK_c	$V_{IDWCK}(AC)$	0.27				1, 3, 5

NOTE 1 For AC operations, all DC clock requirements must be satisfied as well.

NOTE 2 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.

NOTE 3 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.

NOTE 4 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC Timings table.

NOTE 5 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table.

NOTE 6 The AC Operating conditions are for design only and are valid on the silicon at the input of the receiver. They are not intended to be measured.

Annex B — (Informative) Differences Between Revisions

This annex briefly describes most of the changes made to entries that appear in this standard, JESD8-21C.01, compared to its predecessor, JESD8-21C (June 2019). Some punctuation changes are not included.

Clause	Description of Change
Editorial, Terminology update.	

B.1 Differences between JESD8-21C and JESD8-21B (March 2018)

Clause	Description of Change
Annex A.4	Reference voltage (V_{REFD}, V_{REFD2}) for DQ and DBI_n pins for POD135/Class D (GDDR6) changed

This page intentionally left blank