JEDEC STANDARD

POD125 - 1.25 V Pseudo Open Drain I/O

JESD8-30A.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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POD125 - 1.25 V PSEUDO OPEN DRAIN I/O

(From JEDEC Board Ballot JCB-19-12, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the DC and AC single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.25 V Pseudo Open Drain I/Os.

The 1.25 V Pseudo Open Drain interface, also known as POD125, is primarily used to communicate with GDDR6 SGRAM devices.

Multiple Classes of POD125 are expected to reside within the family of POD125 interfaces in order to accommodate various device and market applications. The various classes standardized within the context of POD125 are documented in the appendices of this document (e.g., POD125/Class A).

The core of this standard documents the subset of values common to all Classes of POD125 and documents specification items left to definition within a specific Class as denoted by CDV which is defined as Class Dependent Value.

The values specific to each particular class of POD125 are found in the annexes. See specific Class tables for further details.

NOTE It does not follow that all specification values defined in a given Class are necessarily different from the matching parameter in other Class within POD125. Multiple Classes may reuse a given specification value if appropriate to the Class requirements.

2 Core POD125 Interface Standard

Table 1 — DC Operating Conditions

Parameter	Symbol	POD125			Unit	Notes
		Min	Typ	Max		
Device Supply Voltage	V_{DD}	1.2125	1.25	1.2875	V	1
Output Supply Voltage	V_{DDQ}	1.2125	1.25	1.2875	V	1
Reference voltage: DQ and DBI_n pins	V_{REFD}	CDV		CDV	V	3, 4
	V_{REFD2}	CDV		CDV	V	3, 4, 5
Reference voltage: CA pins	V_{REFC}	CDV		CDV	V	6
	V_{REFC2}	CDV		CDV	V	6, 7
DC input logic HIGH voltage with V_{REFC}: CA	V_{IHA}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFC}: CA	V_{ILA}(DC)			CDV	V	8
DC input logic HIGH voltage with V_{REFC2}: CA	V_{IHA2}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFC2}: CA	V_{ILA2}(DC)			CDV	V	8
DC input logic HIGH voltage with V_{REFD}: DQ, DBI_n	V_{IHD}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFD}: DQ, DBI_n	V_{ILD}(DC)			CDV	V	8
DC input logic HIGH voltage with V_{REFD2}: DQ, DBI_n	V_{IHD2}(DC)	CDV			V	8
DC input logic LOW voltage with V_{REFD2}: DQ, DBI_n	V_{ILD2}(DC)			CDV	V	8
RESET_n and boundary scan input logic HIGH voltage; EDC and CA input logic high voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{IHR}	CDV			V	8
RESET_n and boundary scan input logic LOW voltage; EDC and CA input logic low voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{ILR}			CDV	V	8
Input leakage current (any input 0V <= V_{IN} <= V_{DDQ}; all other signals not under test = 0V)	I_L				µA	
Output leakage current (outputs are disabled; 0V <= V_{OUT} <= V_{DDQ})	I_{OZ}				µA	
Output logic LOW voltage	VOL(DC)			0.52	V	
Single ended clock input voltage level: CK_t, CK_c, WCK_t, WCK_c	V_{IN}	-0.30		V_{DDQ} + 0.30		13
Clock input mid-point voltage: CK_t, CK_c	V_{MP}(DC)	V_{REFC} - 0.10		V_{REFC} + 0.10	V	9, 12
Clock input differential voltage: CK_t, CK_c	V_{IDCK}(DC)	CDV			V	10, 12
Clock input differential voltage: WCK_t, WCK_c	V_{IDWCK}(DC)	CDV			V	11, 14

NOTE 1 GDDR6 SGRAMs are designed to tolerate PCB designs with separate V_{DD} and V_{DDQ} power regulators.
NOTE 2 DC bandwidth is limited to 20 MHz.
NOTE 3 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 4 The reference voltage source and control for DQ and DBI_n pins are determined by Half V_{REFD} and V_{REFD} Level mode register bits.
NOTE 5 Programmable V_{REFD} levels are not supported with V_{REFD2}.
NOTE 6 The reference voltage source (external or internal) is determined at power-up; the reference voltage level is determined by Half V_{REFC} and the V_{REFC} Offset mode register bits.
NOTE 7 Programmable V_{REFC} offsets are not supported with V_{REFC2}.
NOTE 8 V_{IHR} and V_{ILR} apply to boundary scan input pins TDI, TMS and TCK. V_{IHR} and V_{ILR} apply to EDC and CA inputs at reset when latching default device configurations. V_{IHR} and V_{ILR} also apply to CA, CABI_n, CKE_n, CK, DQ, DBI_n, EDC and WCK inputs when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.
NOTE 9 This provides a minimum of 0.775 V to a maximum of 0.975 V, and is normally 70% of V_{DDQ}. DRAM timings relative to CK_t cannot be guaranteed if these limits are exceeded.
NOTE 10 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
NOTE 11 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.
NOTE 12 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC Timings table.
NOTE 13 Use V_{IHR} and V_{ILR} when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.
NOTE 14 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table.

2 Core POD125 Interface Standard (cont'd)

Table 2 — AC Operating Conditions (For Design Only[11])

Parameter	Symbol	POD125			Unit	Notes
		Min	Typ	Max		
AC input logic HIGH voltage with V_{REFC}: CA	$V_{IHA}(AC)$	CDV			V	
AC input logic LOW voltage with V_{REFC}: CA	$V_{ILA}(AC)$			CDV	V	
AC input logic HIGH voltage with V_{REFC2}: CA	$V_{IHA2}(AC)$	CDV			V	
AC input logic LOW voltage with V_{REFC2}: CA	$V_{ILA2}(AC)$			CDV	V	
AC input logic HIGH voltage with V_{REFD}: DQ, DBI_n	$V_{IHD}(AC)$	CDV			V	
AC input logic LOW voltage with V_{REFD}: DQ, DBI_n	$V_{ILD}(AC)$			CDV	V	
AC input logic HIGH voltage with V_{REFD2}: DQ,DBI_n	$V_{IHD2}(AC)$	CDV			V	
AC input logic LOW voltage with V_{REFD2}: DQ,DBI_n	$V_{ILD2}(AC)$			CDV	V	
Clock input differential voltage: CK_t, CK_c	$V_{IDCK}(AC)$	CDV			V	1, 3, 5
Clock input differential voltage: WCK_t, WCK_c	$V_{IDWCK}(AC)$	CDV				1, 4, 6
Clock input crossing point voltage; CK_t, CK_c	$V_{IXCK}(AC)$	V_{REFC} - 0.10		V_{REFC} + 0.10	V	1, 2, 5
Clock input crossing point voltage: WCK_t, WCK_c	$V_{IXWCK}(AC)$	V_{REFD} - 0.09		V_{REFD} + 0.09	V	1, 2, 6, 7
Allowed time before ring back of CK/WCK below $V_{IDCK}(AC)/V_{IDWCK}(AC)$	t_{DVAC}				ps	8, 9, 10

NOTE 1 For AC operations, all DC clock requirements must be satisfied as well.
NOTE 2 The value of V_{IXCK} and V_{IXWCK} is expected to equal 70% V_{DDQ} for the transmitting device and must track variations in the DC level of the same.
NOTE 3 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
NOTE 4 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.
NOTE 5 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC Timings table.
NOTE 6 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table.
NOTE 7 V_{REFD} is either V_{REFD} or V_{REFD2}
NOTE 8 Figure 3 illustrates the exact relationship between (CK_t - CK_c) or (WCK_t - WCK_c) and $V_{ID}(AC)$, $V_{ID}(DC)$ and t_{DVAC}.
NOTE 9 Ring back below $V_{ID}(DC)$ is not allowed.
NOTE 10 t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of clock operating conditions and clock related parameters.
NOTE 11 The AC Operating conditions are for DRAM design only and are valid on the silicon at the input of the receiver. They are not intended to be measured.

2 Core POD125 Interface Standard (cont'd)

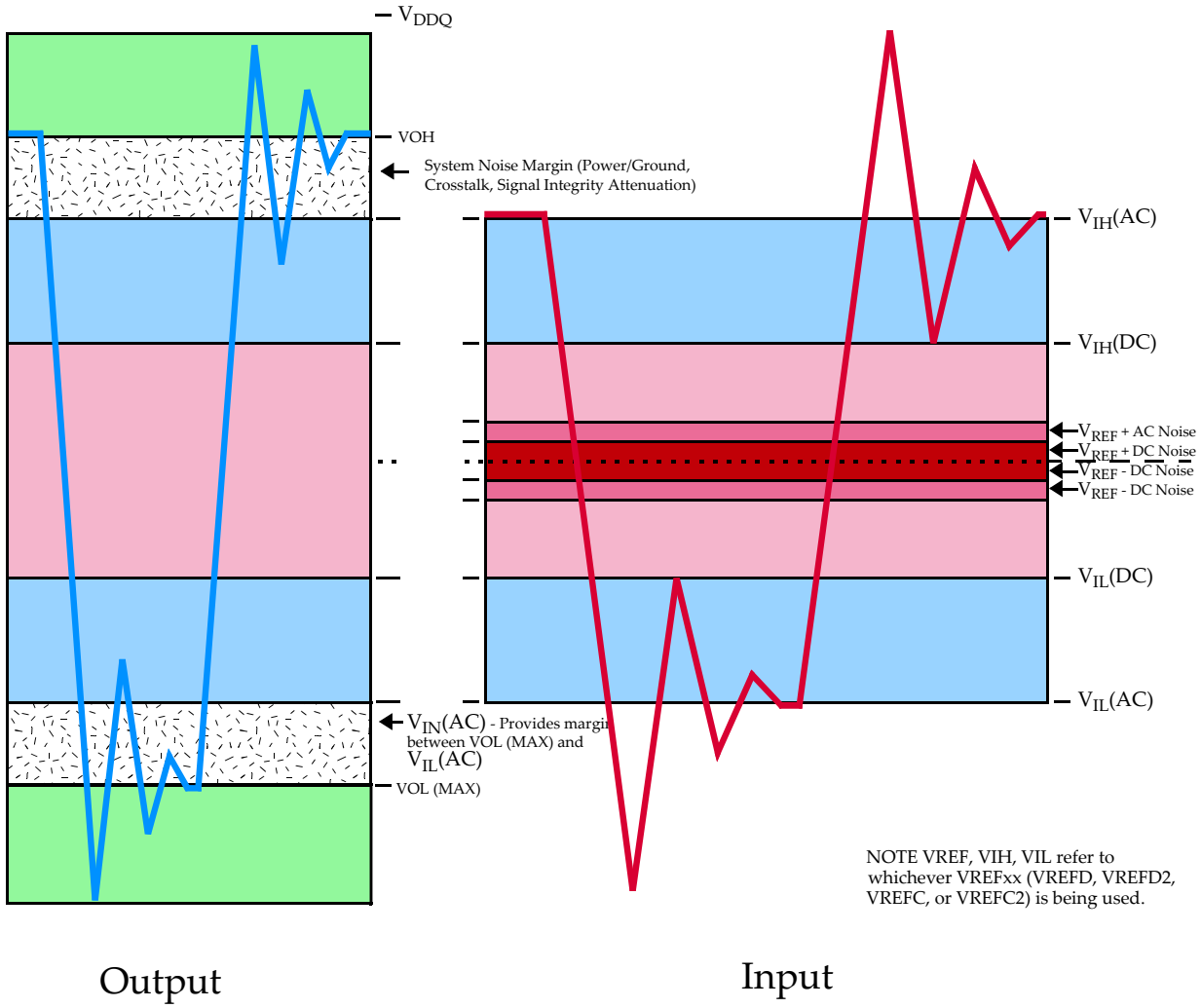


Figure 1 — Voltage Waveform

2 Core POD125 Interface Standard (cont'd)

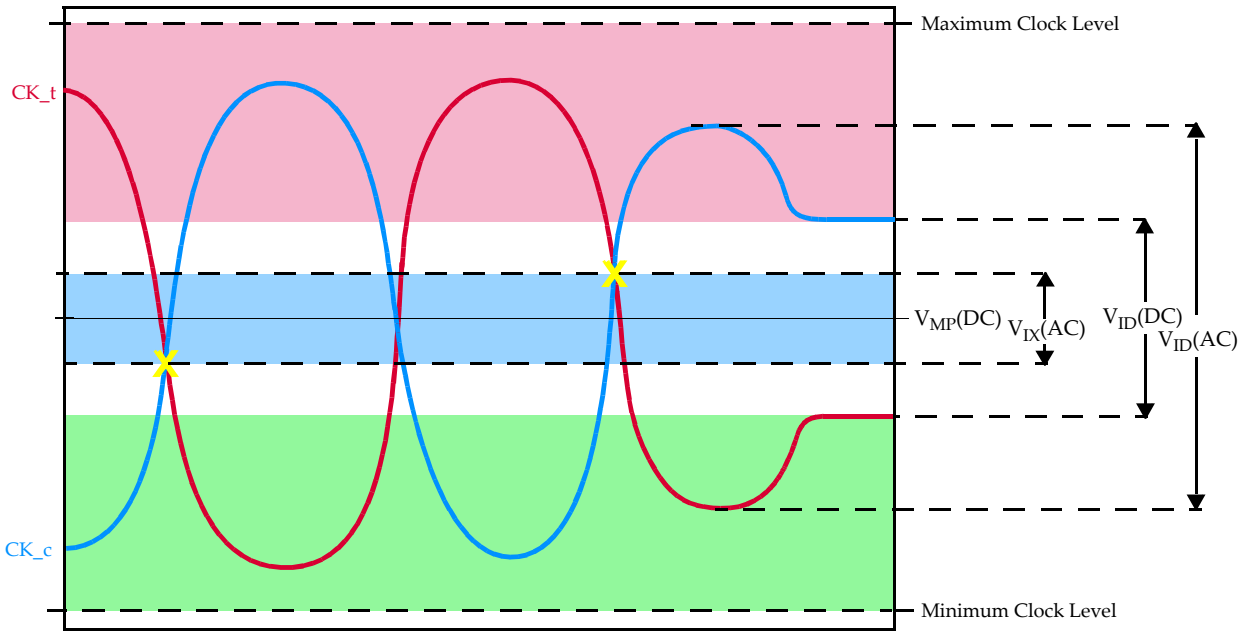


Figure 2 — Clock Waveform

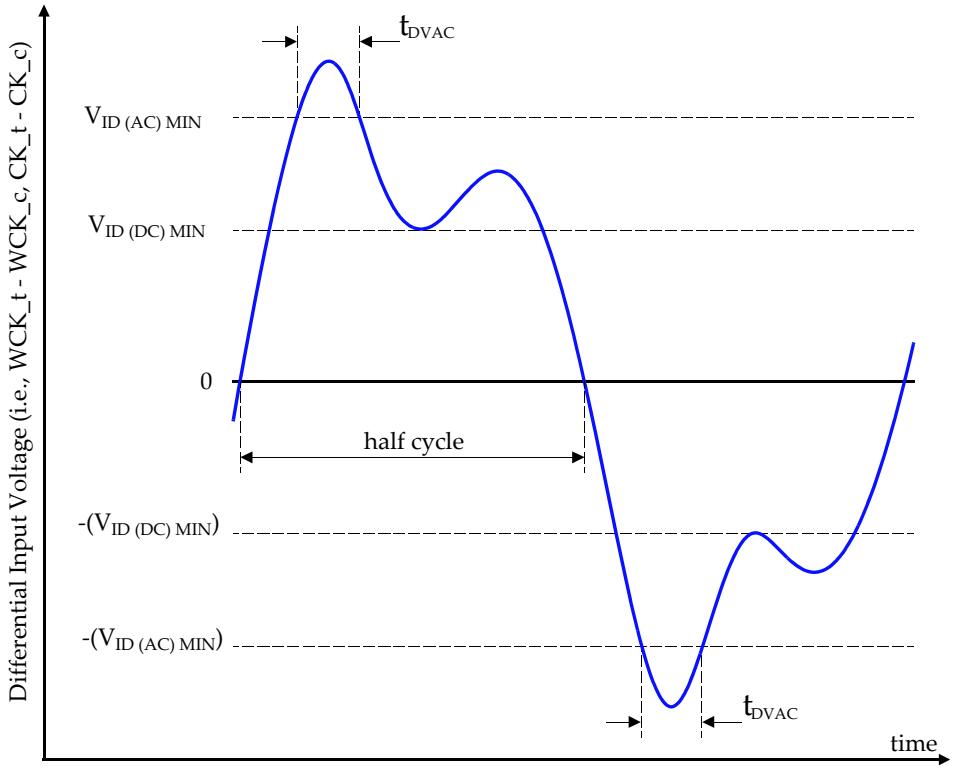


Figure 3 — Definition of Differential AC-Swing and "Time above AC-Level" t_{DVAC}

2 Core POD125 Interface Standard (cont'd)

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.25 V (V_{DD}/V_{DDQ})
2. Power the device and calibrate the output drivers and termination to eliminate process variation at 25 °C.
3. Reduce temperature to 10 °C and recalibrate.
4. Reduce temperature to 0 °C and take the fast corner measurement.
5. Raise temperature to 75 °C and recalibrate
6. Raise temperature to 85 °C and take the slow corner measurement
7. Reiterate 2 to 6 with V_{DD}/V_{DDQ} 1.2125 V
8. Reiterate 2 to 6 with V_{DD}/V_{DDQ} 1.2875 V
9. All obtained driver and termination IV characteristics have to be bounded by the specified MIN and MAX IV characteristics.

The following values (ideal with +/- 10% min/max) are targets for the designer and are not required to be met. Vendor datasheets should be consulted for further details. It is expected that the characteristics of the real curves will have some non-linearity as shown in Figure 6 and Figure 7. This may help to reduce the overall capacitance and boost performance. It is up to the designer to find the optimum combination of linearity and capacitance for best RX and TX performance.

Table 3 — 1.25V I/O Impedances

Pull-Down Characteristic at 40 Ohm			
Voltage (V)	**MIN (mA)**	**Ideal (mA)**	**MAX (mA)**
0.1	2.25	2.50	2.75
0.2	4.50	5.00	5.50
0.3	6.75	7.50	8.25
0.4	9.00	10.00	11.00
0.5	11.25	12.50	13.75
0.6	13.50	15.00	16.50
0.7	15.75	17.50	19.25
0.8	18.00	20.00	22.00
0.9	20.25	22.50	24.75
1.0	22.50	25.00	27.50
1.1	24.75	27.50	30.25
1.2	27.00	30.00	33.00
1.25	28.125	31.25	35.375

Pull-Up/Termination Characteristic at 60 Ohm			
Voltage (V)	**MIN (mA)**	**Ideal (mA)**	**MAX (mA)**
0.1	-1.50	-1.67	-1.83
0.2	-3.00	-3.33	-3.67
0.3	-4.50	-5.00	-5.50
0.4	-6.00	-6.67	-7.33
0.5	-7.50	-8.33	-9.17
0.6	-9.00	-10.00	-11.00
0.7	-10.50	-11.67	-12.83
0.8	-12.00	-13.33	-14.67
0.9	-13.50	-15.00	-16.50
1.0	-15.00	-16.67	-18.33
1.1	-16.50	-18.33	-20.17
1.2	-18.00	-20.00	-22.00
1.3	-18.75	-21.835	-22.915

2 Core POD125 Interface Standard (cont'd)

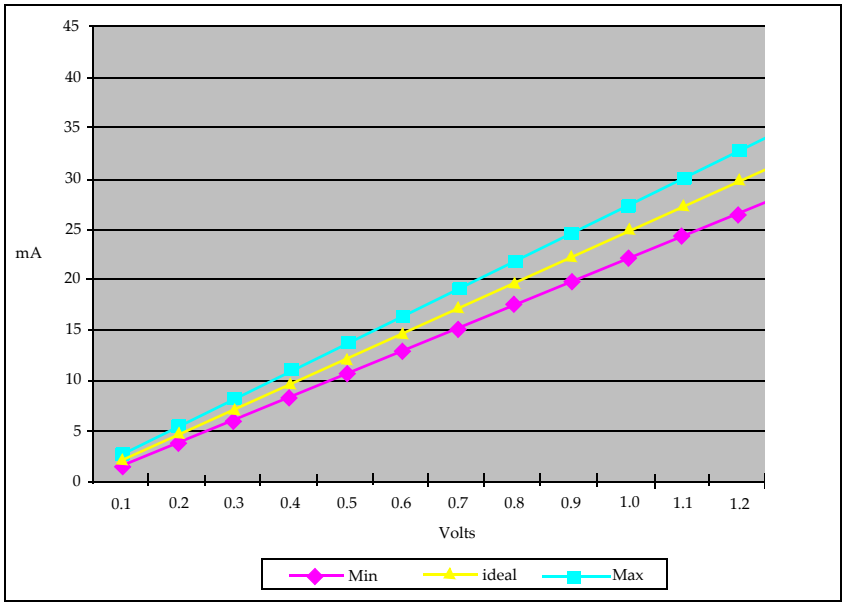


Figure 4 — Target Pull-Down Characteristic at 40 Ohm

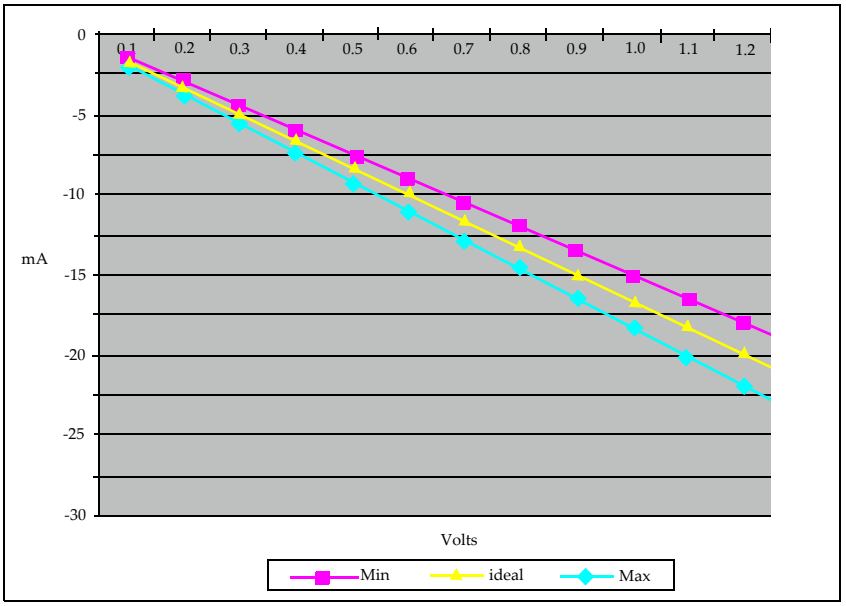


Figure 5 — Target Pull-Up/Termination Characteristic at 60 Ohm

2 Core POD125 Interface Standard (cont'd)

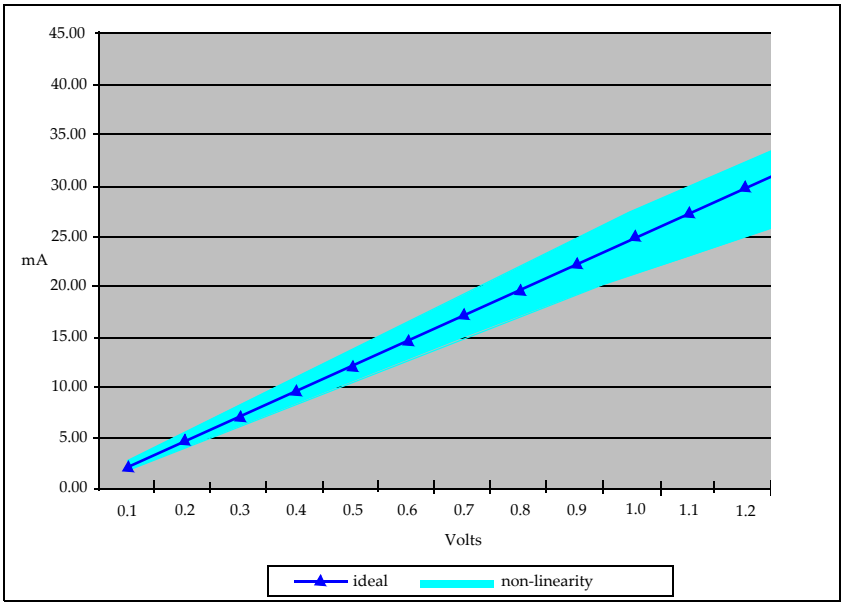


Figure 6 — Example of Non-Linearity, Pull-Down Characteristic at 40 Ohm

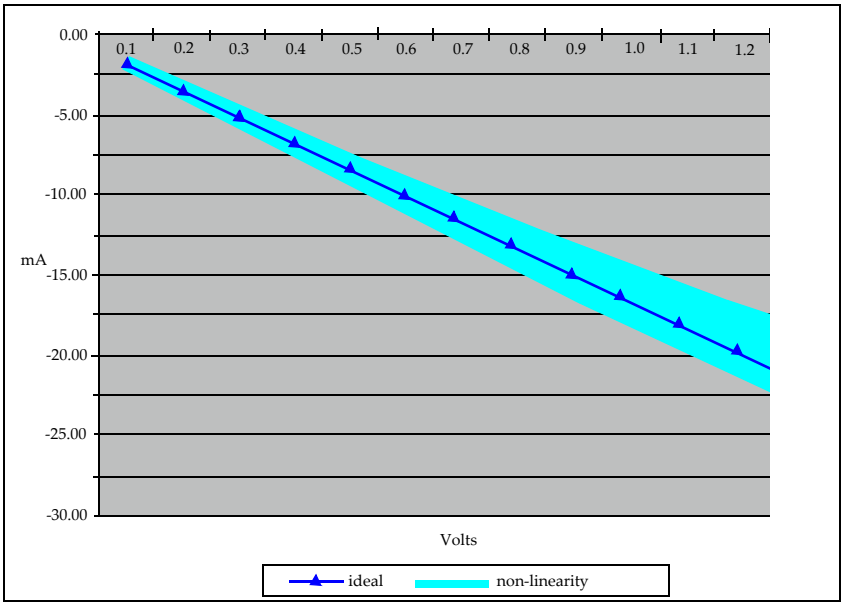


Figure 7 — Example of Non-Linearity, Pull-Up/Termination Characteristic at 60 Ohm

3 Additional Background Information

The POD I/O system is optimized for small systems with very high data rates. The system allows a single Initiator to control one or two Targets in the case of GDDR6. The POD driver uses either a 60/40 ohm output impedance that drives into a 60 ohm equivalent terminator tied to V_{DDQ} or a 48/40 ohm output impedance that drives into a 48 ohm equivalent terminator tied to V_{DDQ}. Single and dual load systems are shown as follows:

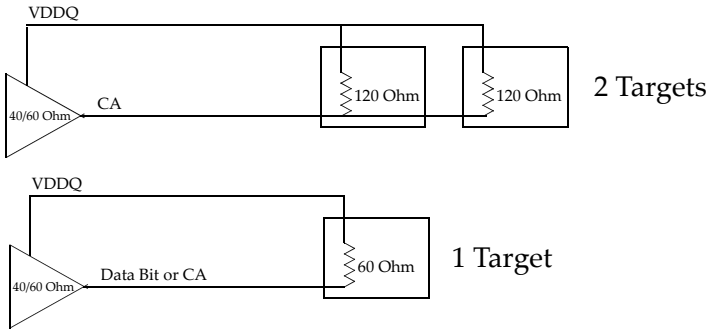


Figure 8 — System Configurations

The POD Initiator I/O cell is comprised of a 60/40 ohm driver and a terminator of 60 ohms or a 48/40 ohm driver and a terminator of 48 ohms. The Initiator POD cell's terminator is disabled when the output driver is enabled. The basic cell is shown in Figure 9.

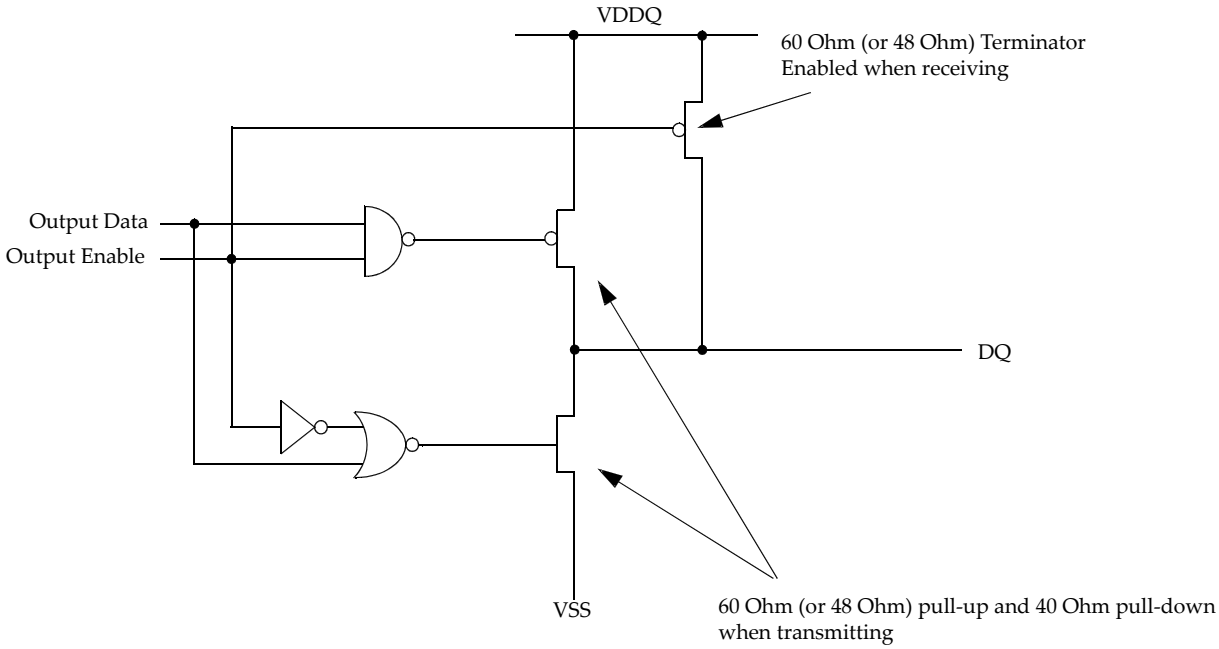


Figure 9 — Initiator I/O Cell

3 Additional Background Information (cont'd)

The POD Target I/O cell is comprised of a 60/40 ohm driver and programmable terminator of 60 ohms or 120 Ohms for GDDR6 or a 48/40 ohm driver and programmable terminator of 48 ohms or 120 ohms for GDDR6. The Target POD cell's terminator is disabled when the output driver is enabled or any other Target output driver is enabled. The basic cell is shown in Figure 10.

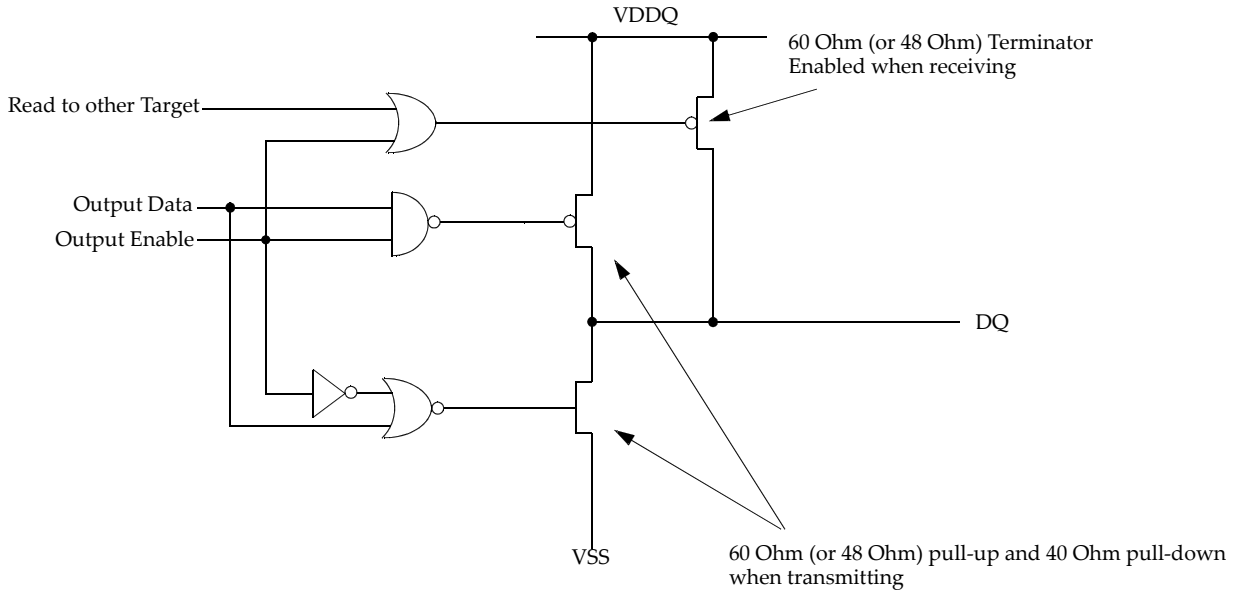


Figure 10 — Target I/O Cell

The POD Initiator and Target I/O cells are intended to have their driver and terminators combined together to minimize the area needed to implement the cell and reduce input capacitance. For GDDR6 this is possible by using three 120 ohm driver/terminator sub cells that are connected in parallel to result in a 60/40 Ohm driver and programmable terminator of 60 ohms or 120 ohms. The combinations used are as follows:

Table 4 — POD I/O Sub-Cells, 120 Ohm Based

# of 120 Ohm Sub-Cells Enabled	Resulting Impedance	Use
1	120 ohms	2 Target loads
2	60 ohms	1 Target load or Initiator terminator
3	40 ohms	Initiator or Target Driver

To ensure that the target impedance is achieved the POD I/O cell is designed to be calibrated to an external 1% precision resistor.

The following procedure may be used to calibrate the cell:

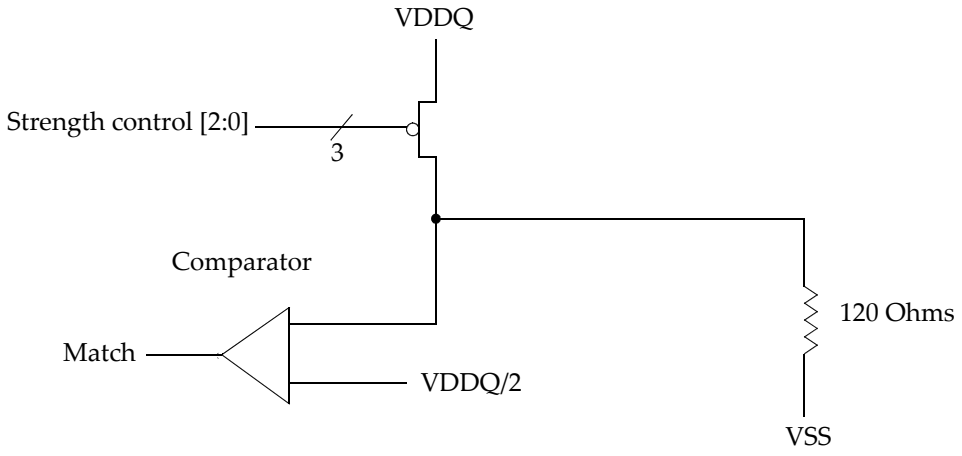
1.) First calibrate the PMOS device against a 120 ohm resistor to V_{SS} via the ZQ pin as illustrated in Figure 11.

- Set strength control to minimum setting,
- Increase drive strength until the comparator detects data bit is greater than $V_{DDQ}/2$,
- PMOS device is calibrated to 120 ohms.

3 Additional Background Information (cont'd)

2.) Then calibrate the NMOS device against the calibrated 120 Ohm PMOS device as illustrated in Figure 12.

- Set strength control to minimum setting,
- Increase drive strength until the comparator detects data bit is less than $V_{DDQ}/2$,
- NMOS device is now calibrated to 120 ohms.



When Match PMOS leg is calibrated to 120 ohms

Figure 11 — PMOS Calibration

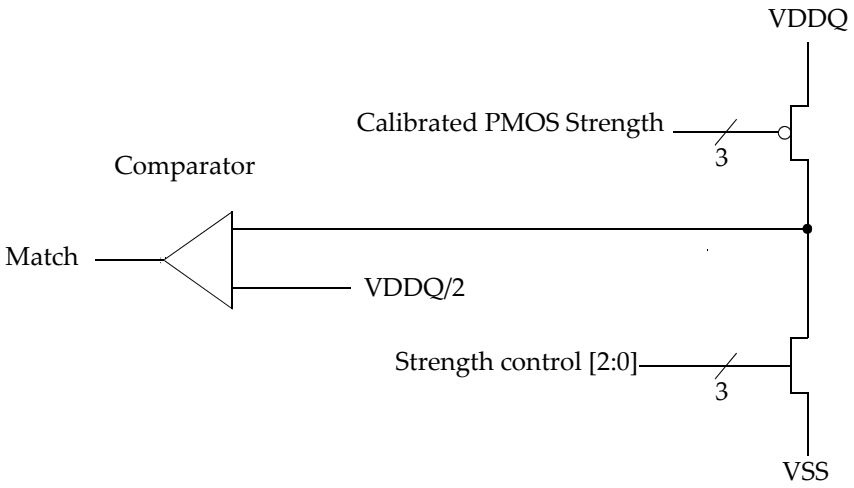


Figure 12 — NMOS Calibration

Annex A — POD125 Classes

A.1 POD125/Class A

POD125/Class A is intended for GDDR6 SGRAM devices (JESD250). Class A devices have either external or internal V_{REFC} or V_{REFC2} for CA, and internal V_{REFD} or V_{REFD2} for data.

Table 5 — Class A DC Operating Conditions

Parameter	Symbol	POD125			Unit	Notes
		Min	Typ	Max		
Reference voltage: DQ and DBI_n pins	V_{REFD}		0.7 * V_{DDQ} or 0.725 * V_{DDQ}		V	3, 4
	V_{REFD2}		0.5 * V_{DDQ}		V	3, 4, 5
Reference voltage: CA pins	V_{REFC}	0.69 * V_{DDQ}		0.71 * V_{DDQ}	V	6
	V_{REFC2}	0.49 * V_{DDQ}		0.51 * V_{DDQ}	V	6, 7
DC input logic HIGH voltage with V_{REFC}: CA	V_{IHA}(DC)	V_{REFC} + 0.125			V	8
DC input logic LOW voltage with V_{REFC}: CA	V_{ILA}(DC)			V_{REFC} - 0.125	V	8
DC input logic HIGH voltage with V_{REFC2}: CA	V_{IHA2}(DC)	V_{REFC2} + 0.25			V	8
DC input logic LOW voltage with V_{REFC2}: CA	V_{ILA2}(DC)			V_{REFC2} - 0.25	V	8
DC input logic HIGH voltage with V_{REFD}: DQ, DBI_n	V_{IHD}(DC)	V_{REFD} + 0.085			V	8
DC input logic LOW voltage with V_{REFD}: DQ, DBI_n	V_{ILD}(DC)			V_{REFD} - 0.085	V	8
DC input logic HIGH voltage with V_{REFD2}: DQ, DBI_n	V_{IHD2}(DC)	V_{REFD2} + 0.25			V	8
DC input logic LOW voltage with V_{REFD2}: DQ, DBI_n	V_{ILD2}(DC)			V_{REFD2} - 0.25	V	8
RESET_n and boundary scan input logic HIGH voltage; EDC and CA input logic high voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{IHR}	0.8 * V_{DDQ}			V	8
RESET_n and boundary scan input logic LOW voltage; EDC and CA input logic low voltage for x16/x8 mode, PC vs. 2-channel mode, CK and CA ODT select at reset	V_{ILR}			0.2 * V_{DDQ}	V	8
Clock input differential voltage: CK_t, CK_c	V_{IDCK}(DC)	0.18			V	9, 11
Clock input differential voltage: WCK_t, WCK_c	V_{IDWCK}(DC)	0.165			V	10, 12

NOTE 1 GDDR6 SGRAMs are designed to tolerate PCB designs with separate V_{DD} and V_{DDQ} power regulators.
NOTE 2 DC bandwidth is limited to 20 MHz.
NOTE 3 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 4 The reference voltage for DQ and DBI_n pins is generated internally, and its values are determined by the Half VREFD and VREFD Level mode register bits. The typical V_{REFD} level depends on the selected data termination value (48 ohm or 60 ohm); see Mode Register 6 (MR6) for details.
NOTE 5 Programmable V_{REFD} levels are not supported with V_{REFD2}.
NOTE 6 The reference voltage source (external or internal) is determined at power-up; the reference voltage level is determined by Half VREFC and the VREFC Offset mode register bits.
NOTE 7 Programmable VREFC offsets are not supported with V_{REFC2}.
NOTE 8 V_{IHR} and V_{ILR} apply to boundary scan input pins TDI, TMS and TCK. V_{IHR} and V_{ILR} apply to EDC and CA inputs at reset when latching default device configurations. V_{IHR} and V_{ILR} also apply to CA, CABI_n, CKE_n, CK, DQ, DBI_n, EDC and WCK inputs when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.
NOTE 9 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
NOTE 10 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.
NOTE 11 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC Timings table.
NOTE 12 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table.

A.1 POD125/Class A (cont'd)

Table 6 — Class A AC Operating Conditions (For Design Only)

Parameter	Symbol	POD125			Unit	Notes
		Min	Typ	Max		
AC input logic HIGH voltage with V_{REFC}: CA	V_{IHA}(AC)	V_{REFC} + 0.165			V	
AC input logic LOW voltage with V_{REFC}: CA	V_{ILA}(AC)			V_{REFC} - 0.165	V	
AC input logic HIGH voltage with V_{REFC2}: CA	V_{IHA2}(AC)	V_{REFC} + 0.333			V	
AC input logic LOW voltage with V_{REFC2}: CA	V_{ILA2}(AC)			V_{REFC} - 0.333	V	
AC input logic HIGH voltage with V_{REFD}: DQ, DBI_n	V_{IHD}(AC)	V_{REFD} + 0.125			V	
AC input logic LOW voltage with V_{REFD}: DQ, DBI_n	V_{ILD}(AC)			V_{REFD} - 0.125	V	
AC input logic HIGH voltage with V_{REFD2}: DQ,DBI_n	V_{IHD2}(AC)	V_{REFD2} + 0.333			V	
AC input logic LOW voltage with V_{REFD2}: DQ,DBI_n	V_{ILD2}(AC)			V_{REFD2} - 0.333	V	
Clock input differential voltage: CK_t, CK_c	V_{IDCK}(AC)	0.333			V	1, 2, 4
Clock input differential voltage: WCK_t, WCK_c	V_{IDWCK}(AC)	0.25				1, 3, 5

NOTE 1 For AC operations, all DC clock requirements must be satisfied as well.

NOTE 2 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.

NOTE 3 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.

NOTE 4 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC Timings table.

NOTE 5 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table.

Annex B — (Informative) Differences Between JESD8-30A.01 and JESD8-30A

This annex briefly describes most of the changes made to entries that appear in this standard, JESD8-30A.01, compared to its predecessor, JESD8-30A (June 2019). Some punctuation changes are not included.

Clause	Description of Change
	Editorial changes only to update terminology

B.1 Differences between JESD8-30A and JESD8-30 (September 2017)

Clause	Description of Change
Annex A.1	Reference voltage (V_{REFD}, V_{REFD2}) for DQ and DBI_n pins for POD125/Class A (GDDR6) changed

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