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Design for Testability Guidelines

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Design For Testability

Guidelines

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JEDEC

Committee on Semicustom Integrated Circuits

DESIGN FOR TESTABILITY GUIDELINES

TABLE OF CONTENTS

NOTE: Two chapters are in the process of completion and will be included in a future edition:

1) Packaging Impact on Design For Testability

2) Fault Detection, Fault Coverage, Fault Simulation and Testability Analysis

DESIGN FOR TESTABILITY GUIDELINES

CHAPTER 1

INTRODUCTION

(From JEDEC Council Ballot JCB-87-46, formulated under the cognizance of JC44 Committee on Semicustom Integrated Circuits.)

The concern most often voiced by Application Specific Integrated Circuit (ASIC) users is that of testability. Many vendors have taken steps to try to minimize the concerns of their customers but, to date, each company has instituted its own policies and the customers have seen little to ease their confusion. This document is composed of inputs from many IC manufacturers and some IC users. It is intended to bring together a coherent approach to designing for testability. It is not intended as a specification, nor is it to be interpreted as the only way to design. It should, rather, be used as guidance (as the title implies) when designs are being initiated.

As the reader progresses through this guide he will notice that there is no list of authors and no company labels are shown. This was not done to slight the authors or minimize the contributions that they and their companies made. It was done, instead, to try to emphasize the broad base of contributors and companies who support these guidelines.

The second section of this guide contains definitions for most of the terms commonly used with reference to designing for testability. These definitions are the result of industry-wide discussion and, as such, represent the consensus of the industry.

Several topics will be covered. Perhaps the item that leads to the most discussion is Fault Simulation. This technique enables design engineers to evaluate their test patterns (input stimulus and expected output values) to determine whether these patterns will detect faults (errors in the circuitry) that may occur during either the design or processing stages. A fault simulator uses fault models, such as a node shorted to power (stuck-at-one) or a node shorted to ground (stuck-at-zero), and compares the response of a fault-free circuit with the response of a faulty circuit after applying test patterns supplied by the design engineer. If the response of the fault-free circuit is different than the response of the faulty circuit, then the test patterns have detected the fault. By faulting all the nodes in the circuit, the fault simulator will produce the test pattern fault coverage (the percentage of faults detected vs. total faults tested). The higher the fault coverage, the better the

test pattern will separate a faulty circuit from a fault-free circuit. By analyzing which faults have not been detected by the current set of test patterns, additional test patterns can be generated by the design engineers in order to detect the faults which were missed. Many vendors recommend greater than 90 percent fault coverage.

Designing testability into any circuit will affect the hardware to some degree. Additional logic will most probably have to be included for any of the methods outlined in this guide. This additional logic will increase the amount of silicon required to implement the design and therefore increase the cost. The savings from enhanced testability do not usually show up until the testing cost of the part and its end system are analyzed. These costs include the labor required to generate the test vectors, the computer time to evaluate the vectors, and the actual time required to test the part. Depending on how the additional circuitry is implemented, the ac performance of the part may be degraded. Each of these factors will also be discussed.

The final section of this guide is a bibliography of documents that the reader may want to investigate. While this list is extensive, it is by no means all-inclusive. The reader is encouraged to do some follow-up investigation after finishing this document.

DESIGN FOR TESTABILITY GUIDELINES

CHAPTER 2

TERMS AND DEFINITIONS

1. Node:

The end-point of a branch in a network or a point at which two or more branches meet.

2. Fault:

A defect that may cause a failure in the circuit operation and/or timing.

NOTE:
Subclassifications of faults may not be mutually exclusive.

2.1 Parametric Fault:

A fault in a circuit that causes failure to meet ac or dc specifications but does not cause functional failure.

2.2 Functional Fault:

A fault that causes improper logical operation of a circuit.

2.2.1 Combinational Fault:

A functional fault that is not affected by the sequence of the input stimuli.

2.2.2 Sequential Fault:

A functional fault that is affected by the sequence of the input stimuli.

3. Stuck-at-0 Fault:

A fault in a digital circuit characterized by a node remaining at a logic low (0) state regardless of changes in input stimuli.

3.1 Stuck-at-1 Fault:

A fault in a digital circuit characterized by a node remaining at a logic high (1) state regardless of changes in input stimuli.

DESIGN FOR TESTABILITY GUIDELINES

4. Short Circuit Fault:

A fault in a circuit that alters the number of nodes by connecting two or more nodes together.

4.1 Open Circuit Fault:

A fault in a circuit that alters the number of nodes by breaking a node into two or more nodes.

5. Test Vector:

A single instance of input stimuli and expected output responses.

6. Test Pattern:

A set of test vectors.

7. Test Program:

A test pattern and instructions suitable for use on Automatic Test Equipment.

Note:
A test program may be used to perform functional and parametric (ac, dc, or other) tests.

8. Detectable Fault:

A functional fault for which a test pattern can be created that will always cause the effects of the fault to be observable at an externally accessible node.

8.1 Detected Fault:

A functional fault that causes effects that are observed at an externally accessible node when the circuit is exercised by the existing test pattern.

8.2 Undetected Fault:

A functional fault that causes effects that are not observed at an externally accessible node when the circuit is exercised by the existing test pattern.

DESIGN FOR TESTABILITY GUIDELINES

9. Undetectable Fault:

A functional fault for which no test pattern can be created that will cause the effects of the fault to be observable at an externally accessible node.

10. Test-Pattern Fault Coverage:

The ratio of the total number of detected faults to the total number of detectable faults.

11. Fault detectability Ratio:

The ratio of detectable faults to the sum of detectable and undetectable faults.

12. Fault Grading:

The process of determining the test-pattern fault coverage of a circuit.

13. Fault-Tolerant Design:

A design approach to enhance the ability of a circuit to remain operational after the occurrence of a fault.

Note:
Fault-tolerant design techniques may impact fault detection.

14. Controllability:

The ability of a node to be established at specific logic state(s) by applying stimuli to the circuit's externally accessible node(s).

15. Observability:

The ability to determine the logic state(s) of a node at the circuit's externally accessible node(s).

16. Circuit Initialization:

A sequence of stimuli that set internal nodes of a circuit to a predictable state.

DESIGN FOR TESTABILITY GUIDELINES

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DESIGN FOR TESTABILITY GUIDELINES

CHAPTER 3

STRUCTURED AND NON-STRUCTURED APPROACHES TO DESIGNING FOR TESTABILITY

Design For Testability (DFT) refers to a design approach that enables thorough testing of a system with minimal effort and maximum coverage. A circuit is termed testable when the testing effort involved is minimal compared to the design and manufacturing efforts. The key concepts in DFT are controllability and observability. (See definitions in Chapter 2.) The purpose of the various DFT techniques is to increase the ability to control/observe internal nodes from external inputs/outputs.

Some states of a circuit are buried in logic and cannot easily be controlled or observed by external pins. This makes the generation of test vectors more time consuming and usually results in more test vectors being generated. This problem can be addressed by adding special test pins that increase the controllability or observability of these states. If extra pins are not available, on-chip test logic can be used to test portions of the circuit while it is operating in a test mode. Input combinations that cannot occur during the normal operation of the circuit can be used to place the circuit in the test mode. On-chip test circuitry can also be used to partition the circuit into logical subsystems that can be tested in parallel. Testing smaller logical subsystems simplifies the task of test vector generation. Because the logical subsystems operate in parallel, these test vectors may be merged together, resulting in reduced test time on the tester.

To help solve the testing problem there are two basic approaches prevalent in the industry. The first approach is categorized as ad hoc or nonstructured and the second approach is categorized as a structured approach. The nonstructured techniques are the ones that can be applied to a given product, but are not directed at solving the general problem of testing sequential logic. Non-structured techniques usually provide specific solutions at lower cost than structured approaches would, but without the general applicability. The structured techniques tend to solve the general problem with design methodology and lend themselves more easily to design automation.

The implementation of a structured approach to DFT begins with the design process. Most structured techniques rely on the "shift register" method which connects all memory elements (latches,

flip-flops) into a shift register and uses each element as pseudo-input/output for testing purposes. Converting sequential logic into combinational circuits simplifies test pattern generation and reduces test development costs. There are a number of DFT techniques used by VLSI chip designers; three are briefly discussed below.

ISOLATION OF FUNCTIONAL BLOCKS

One of the simplest methods of designing testability into a circuit is to partition the functional blocks such that each may be individually tested as a separate unit. In an integrated circuit, only the nodes at the external pins can be controlled and observed directly. In order to isolate the functional blocks of the chip, internal nodes must be made controllable and observable from the external pins. Additional logic such as multiplexers may have to be added to perform this function. This, in turn, will increase gate count. If the design is implemented in gate arrays, enough extra logic may be required as to force the use of the next larger array. In cell based designs, each added gate will increase die size. The total number of internal signals that must be isolated will dictate the exact amount of additional logic that will have to be added. If extra package pins are available, internal signals may be brought directly to the outside world for observation at no additional cost. If package pins are not available, however, bringing internal signals out will force the use of a larger package. Costs will vary with the package selection.

Any added logic will have an effect on the ac performance of the circuit. If the added logic is to be placed in a critical timing path, a trade off will result between performance and testability.

DESIGN FOR TESTABILITY GUIDELINES

SCAN DESIGN

There are many varieties of scan design and each has its own impact on the hardware. All of these techniques ease the problem of testability by making the circuit appear to be structured as a combinational network. The nature of scan design makes it very easy to control and observe every bi-stable element in the circuit. This discussion will be limited to the following scan design methods:

Level Sensitive Scan Design (LSSD)
Scan Path
Random Access Scan
Two Port Flip-Flop

It should be noted that several of these methods have very restrictive design rules and force a specific design methodology.

LEVEL SENSITIVE SCAN DESIGN (LSSD)

The LSSD method (developed and trademarked by IBM) represents one of the best known and most successful approaches. "Level sensitive" refers to constraints requiring logic subsystems to be insensitive to ac characteristics such as rise time, fall time and minimum circuit delays. LSSD requires that the designer adhere to a very strict set of design rules. These eliminate many possible test problems and ease the automatic generation of test vectors. All bi-stable elements in the circuit must be implemented as level sensitive latches.

The key element in this design is the "Shift Register Latch" (SRL) as shown in Figure 3-1a. The SRL is a level sensitive device that does not contain hazards or race conditions. Figure 3-1b shows that the SRL includes a system input (D), clock (C), external scan-in input (SI), two nonoverlapping clocks (A and B), and scan-out output (SO). Latches L1 and L2 function in a master/slave configuration during the test mode while L1 also functions as a storage element during the system mode.

Interconnecting several SRLs gives the circuit a scan capability and reduces the testing of a sequential circuit to the testing of a combinatorial circuit (Figure 3-1c). The functional operation of combinatorial logic can be tested independent of any timing considerations other than adequately slowing the clock. This method permits partitioning a large network into manageable segments for which tests are easily generated. The number of test

patterns required is reduced since multiple portions of the circuit are tested simultaneously.

There are a number of negative factors associated with the LSSD approach. First, the SRLs are 2-3 times as complex as simple latches. The silicon overhead to implement the SRLs is in the range of 4 to 20 percent. However, this overhead can be reduced if the L2 latches can also be utilized to perform system functions. Up to four additional pins are required to implement LSSD, which could affect the circuit size and the package selection. By making functional use of some primary input/outputs required to operate the SRLs, the number of extra pins can be reduced.

The LSSD structured design approach for DFT eliminates or alleviates some of the problems in designing and testing VLSI chips at a reasonable cost.

SCAN PATH

The scan path method is very similar to the LSSD approach, but differs in the latch design and clock mechanism. The basic concept involves serially shifting test data into the internal memory elements and scanning out the test results. This allows initialization of all the internal memory elements to desired states and permits the contents of the buried registers to be easily examined.

The storage element consists of a latch or D flip-flop clocked by CP with a multiplexer at the input, as shown in Figure 3-2. The multiplexer inputs D and T1 represent the system and test data inputs selected by the TEST ENABLE (TE) input signal. The Q output of one flip-flop then feeds the SI input of the next flip-flop. This is done until the SCAN ring is formed. Some vendors offer macro cell libraries including latches and flip-flops with built-in scan circuitry. Scan path testing also requires three additional pins (Test Input, Test Enable and Test Output). Automatic test pattern generators exist which can achieve very high fault coverage using any of the methods discussed. There are some disadvantages however. Adding logic into the data path limits the speed at which the circuit can be clocked. The hardware overhead is related to the number of registers, since each requires a two to one multiplexer. Additional routing must be included for the select signal which connects to each register and for the interconnection of the scan data path.

Experimental results show that the scan path method reduces test generation time by an order of magnitude. The additional

circuitry required to implement this scheme ranges from 5 to 15 percent.

RANDOM ACCESS SCAN

Random access scan requires a very similar latch to those used in LSSD or scan path methods, with the exception that a decode input has been added. Rather than connect the scan registers into a serial shift register, the scan registers are individually addressable. The scan data input lines are all tied in common. A decoder must be included in the circuit design in order to get the data into the scan registers. A similar approach must be used to get the data from the scan registers to the outside world. The hardware overhead is approximately the same as for other methods. However, because of the large number of decode lines to be routed the routing overhead is quite high. There is no fixed order in which the data must be loaded or unloaded. If only a few register states change from one test vector to another, only those registers that change must be written. A reduction in test vector length may be an advantage.

DUAL PORT FLIP FLOPS

The dual port flip flop is very similar in concept and implementation to Stanford scan path designs. Rather than place a two to one multiplexer at the D input of the register, which adds extra delay to the data path, two data inputs to the latch section are included. No select signal is used as the selection of data is performed by clocking one of two clocks. If the normal system clock is pulsed, data present at the D input is latched into the register. If the scan clock is pulsed, data at the scan data input is latched into the register. The actual circuit area for implementation is approximately the same as for Stanford scan path. Routing penalty is also similar because a second clock must be routed rather than a test mode pin. The advantage of no AC speed penalty is a plus for this method.

BUILT-IN LOGIC BLOCK OBSERVATION (BILBO)

The previously mentioned techniques require external equipment to generate and apply the test vectors to the circuit. The BILBO technique, shown in Figure 3-3, includes test vector generation and response evaluation on the chip. Such an approach allows a minimum of both tester intervention and test overhead in terms of dedicated test I/O pins. The response of a circuit to a given stimulus gets fed to a Linear Feedback Shift Register (LFSR). The

input data is divided by the response and the remainder corresponds to the cyclic code. The cyclic code represents the signature that corresponds to the test input, which enables comparing the code with a predetermined correct signature value.

BILBO can operate in four different modes:
a) Latch mode
b) Shift mode
c) Multiple-input Signature register
d) Reset mode

The BILBO approach permits functionally converting the system flip-flops to a linear feedback shift register, keeping the overhead low. This technique saves both off-line test generation time and test application time. BILBO needs, at most, two pins: one for setting the chip in the test mode and another for reading the go/no-go information from the signature register.

The overhead in terms of silicon real estate is about 5 to 15 percent and there is some loss of performance due to delays in the Exclusive-OR gates.

BUILT-IN TEST (BIT) AND BUILT-IN SELF-TEST (BIST)

There are many types of built in test and built in self tests circuits. Some of the methods use portions of the system circuitry for self oscillation test or polynomial generation. These require very little hardware overhead, but their test coverage is based upon probability rather than exhaustive coverage. An advantage is that these methods allow in-system test with little difficulty.

GOOD ENGINEERING PRACTICES TO ENHANCE TESTABILITY

Logic Design With Testability in mind

Test program development and debugging can be very time consuming and costly unless designers consider test issues during the logic design phase. Due to the increased complexity of VLSI chips, it is not feasible for test engineers to independently develop and debug test programs. The responsibility now lies with

logic designers to design logic such that it is easy to test and requires a reduced set of vectors to thoroughly test the device.

Various techniques can be applied to ensure that a design is testable. Such techniques essentially improve controllability, observability and predictability of a design. Some of these techniques are fairly simple and can be implemented with minimum overhead, and they aid in the development and debugging of the circuit and its test program. A brief description of some testability guidelines is given below.

1. Initialize the circuit to a known state

The entire circuit should be initializable to a known state without requiring knowledge of the current state. In order to easily predict the output of a circuit, all the latches and flip-flops must have set or reset capability. Circuits that never need to be set to a particular state during normal operation, such as frequency dividers (Figure 3-4a), still require a set/reset capability. The tester needs to know how many pulses to apply before the first pulse appears on the output, and this depends on the initial state of the circuit. A power-on clear mechanism, which initializes the circuit in the actual system configuration, may not be an adequate test initialization implementation. Although this function must also be tested, the tester loses many of its utility programs if initialization is performed only in this manner and overall testing suffers dramatically. By adding the special set or reset signal, the circuit can be directly set into a known state and the tester is guaranteed that the first pulse will appear after a known number of cycles and all of the tester's utility programs will still be intact.(Figure 3-4b).

2. Avoid asynchronous circuitry

For asynchronous systems, changes in the output state depend on circuit delays that are a function of wafer processing. Due to the variation in process parameters, there is no guarantee as to when an output will change state. (It may be at the end of one cycle or at the beginning of another.) Since the test vectors must be determined before the test is started, it is very difficult to keep the tester synchronized with the circuit. Therefore, testing of asynchronous circuitry is difficult and costly (and in some cases, impossible).

In an asynchronous SR Latch, for example Figure 3-5a, set and reset signals can change state at any time, causing the output to change state at any time during any period. The output transition

is dependent on the delays that create the set and reset signals. Addition of the clock (Figure 3-5b) ensures that if the set or reset signal changes state, the output will change only after the next clock transition.

3. Allow internal clocks to be bypassed from the circuit's inputs

On-chip oscillator circuitry or other periodic pulse generating circuitry makes synchronization of the tester and the circuit very difficult (Figure 3-6a). By allowing these clock signals to be bypassed and generated by the tester, the tester is automatically synchronized with the circuit (Figure 3-6b). It is desirable to output any bypassed clock signal as a circuit test.

4. Allow counters and dividers to be bypassed

Bypassing sequential circuits decreases the number of test vectors required to test the device and reduces the test time. The sequential circuitry is tested once and then is bypassed while the rest of the circuit is being tested.

When 10 latches are used to divide a 1 MHz clock signal down to 1 kHz, the tester has to apply 1000 test vectors for each 1 kHz pulse (Figure 3-7a). However, when bypass circuitry is available, the divider can be tested once and then bypassed. The remainder of the circuit can be tested with each test vector creating a 1 kHz pulse (Figure 3-7b).

5. Partition circuitry that has more than 8 bits of cascaded latches

The number of vectors required to step through all the bits in cascaded latches is two to the power of the number of bits that are cascaded. A 24 bit counter would require 16 million vectors to count through its sequence (after initialization), resulting in a ridiculous amount of time and cost for testing (Figure 3-8a). After partitioning the counter into 3 groups of 8 bits, 768 vectors are required to test the counter, each group requiring 256 vectors, (Figure 3-8b). The circuit used to partition the counter can pass the count signal forward to the output or can be used directly to set the second or the third section of the partitioned circuitry.

6. Provide direct access to the control inputs of each functional module

DESIGN FOR TESTABILITY GUIDELINES

By applying a stimulus directly to a module without passing the simulator through complex circuitry, the number of test vectors can be minimized.

To stimulate functional module 3 (Figure 3-9a), signals must propagate through modules 1 and 2. If modules 1 and 2 contain sequential circuitry, a large number of vectors will be required to stimulate the inputs of module 3. By allowing module 3 to receive its signals either from module 2 (bypassing module 1) or directly from the circuit inputs, the number of test vectors required to test the device can be reduced (Figure 3-9b).

7. Provide direct access to observe the outputs of each functional module

The response for a particular module can be observed at the circuit output without propagating it through other complex modules.

When trying to observe the response of functional module 1 (Figure 3-10a), the response must propagate through modules 2 and 3. If modules 2 and 3 contain sequential circuitry, a large number of vectors will be required to observe the response from module 1 at the output of the circuit. By allowing module 1 to feed directly to the circuit output, the response values can be observed with a reduced set of test vectors (Figure 3-10b).

8. Avoid nesting of sequential circuits

In sequential circuits, the next state is a function of the present state and current stimulus while the present state is determined by the stimulus applied previously. Therefore, multiple patterns need to be applied to control or observe the sequential circuit. The length of the test pattern increases dramatically if one sequential circuit feeds back to another sequential circuit. This is also known as nesting of sequential circuitry.

In the example, (Figure 3-11a) many vectors are required to stimulate the modules or to pass the response to the rest of the circuit. By partitioning the sequential circuits and breaking the feedback paths, controllability and observability can be improved (Figure 3-11b).

DESIGN FOR TESTABILITY GUIDELINES

9. Allow redundant circuitry to be tested

Redundant circuitry is often included to improve reliability or fabrication yields. Access must be provided to allow both portions of circuitry to be tested separately to ensure that they both work.

Figure 3-12a shows a circuit with redundancy. To insure that input B is noticed at the output whenever it goes high, this circuit was designed with multiple paths for signal B to reach the output. This redundancy makes it impossible to test for the short to ground, as shown. By adding steering logic, both signal paths can be stimulated separately to insure that they are functioning correctly (Figure 3-12b).

10. Watch out for signals that reconverge

Signals that fan out in multiple directions from a single source and later reconverge at the inputs to a functional module can create logic hazards and untestable circuits.

The circuit shown in Figure 3-13a is hazard-free but has an untestable fault. When signal B or C is HIGH, signal A can change state without causing a spike on the output. If B and C are both HIGH, the output of G4 will remain HIGH regardless of the value of G2. Therefore a short at the output of G2 will not be detected. By breaking the reconvergent path of the signal A, as shown in Figure 3-13b, and by making the test input LOW, the output of G2 can be tested. This additional circuitry greatly enhances the testability of the circuit.

DESIGN FOR TESTABILITY GUIDELINES

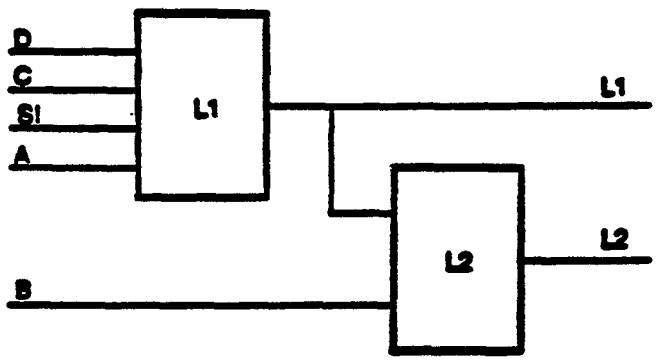
SUMMARY

This chapter has presented several methods of designing testability into circuits. An attempt was made to focus on the subjects of chip size and performance impacts. Only general methods were discussed, as methods vary from vendor to vendor, causing each to have a different effect on the hardware.

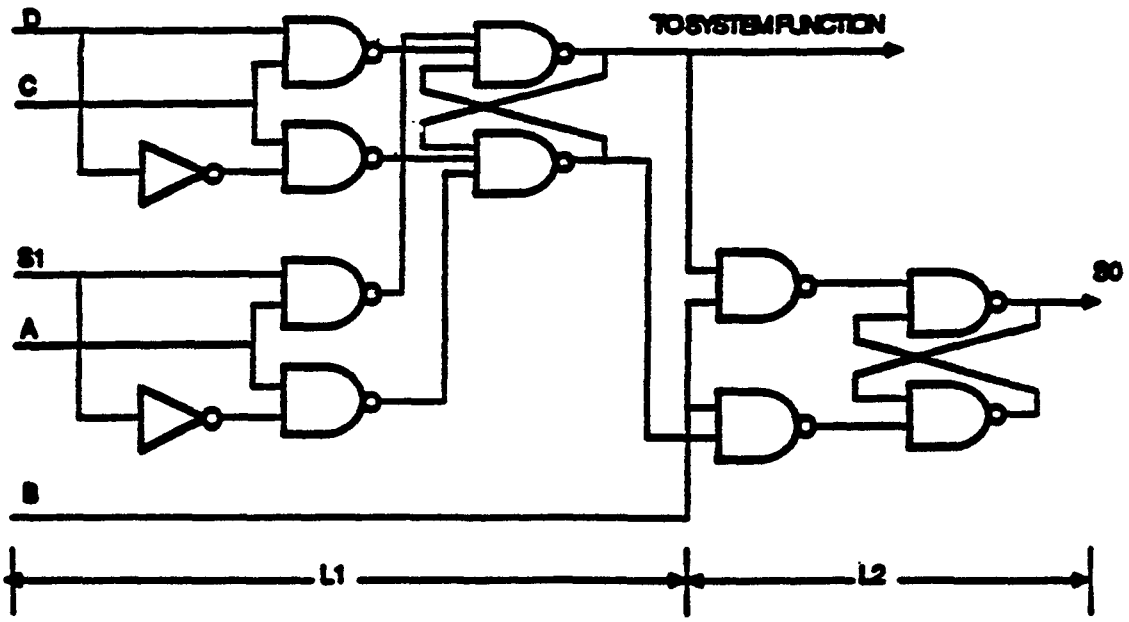
DESIGN FOR TESTABILITY GUIDELINES

Figure 3-1
Shift Register Latch (SRL)

3-1a. Symbolic representation

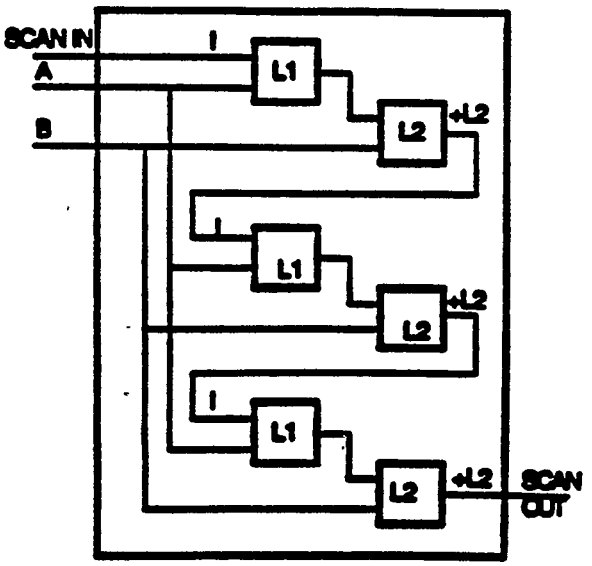


3-1b. Gate level implementation



DESIGN FOR TESTABILITY GUIDELINES

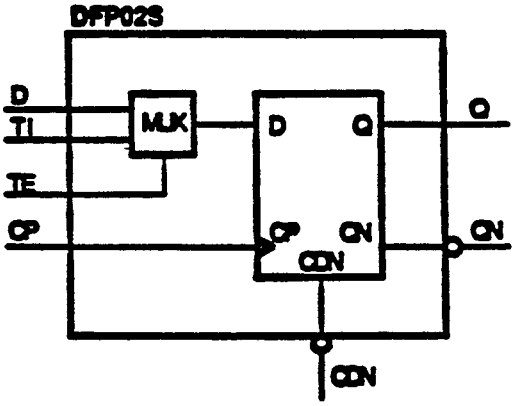
3-1c. Circuit interconnection



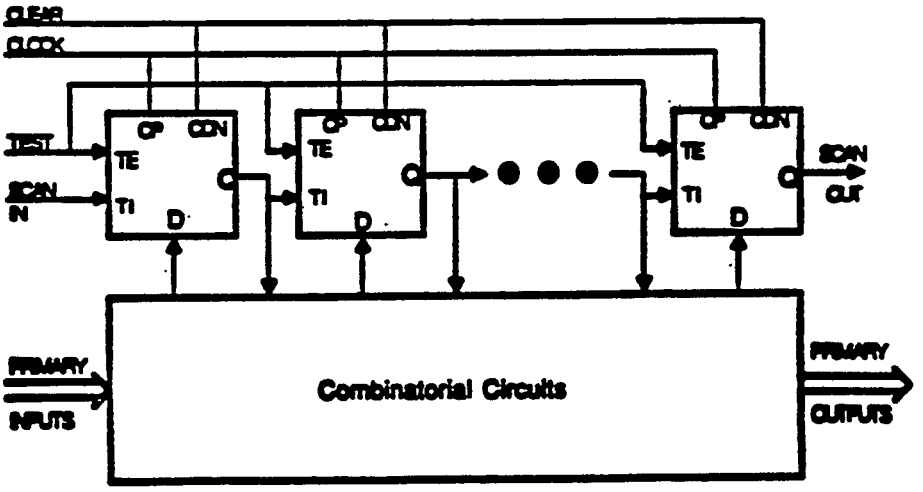
DESIGN FOR TESTABILITY GUIDELINES

Figure 3-2
Scan Path Implementation

3-2a. D Flip-flop with scan



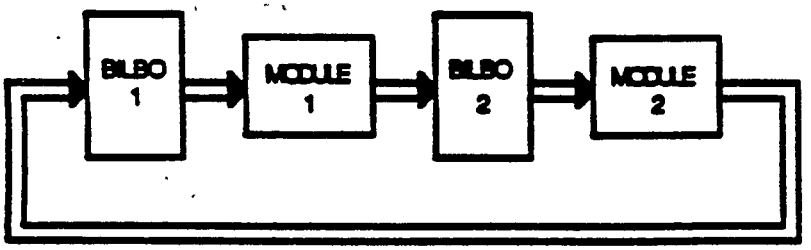
3-2b. Circuit implementation



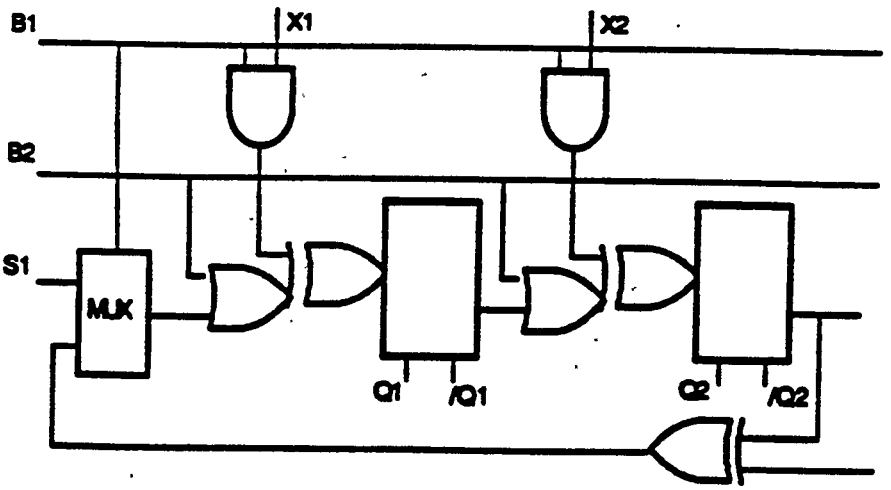
DESIGN FOR TESTABILITY GUIDELINES

Figure 3-3
BILBO Implementation

3-3a. BILBO Implementation for combinatorial network



3-3b. BILBO Operating modes



DESIGN FOR TESTABILITY GUIDELINES

Figure 3-4
SET/RESET capability

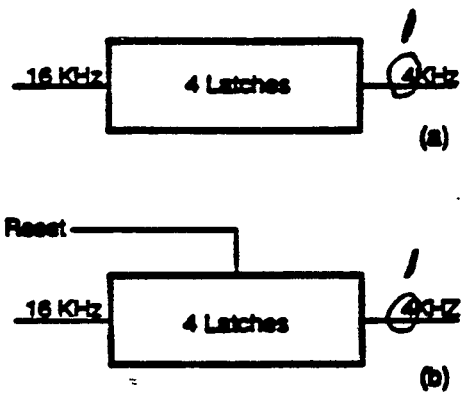
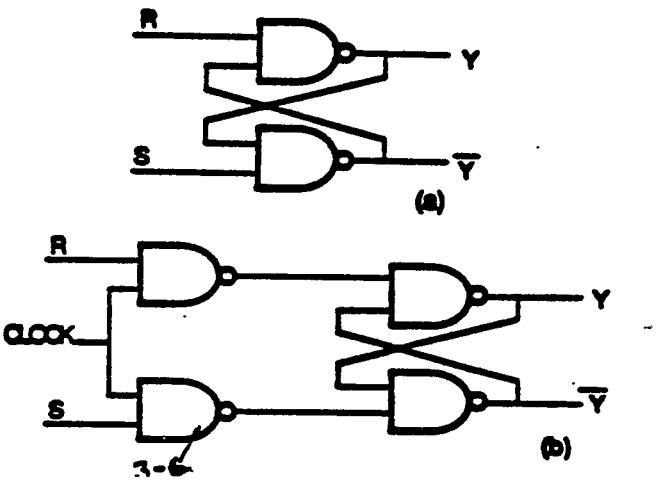
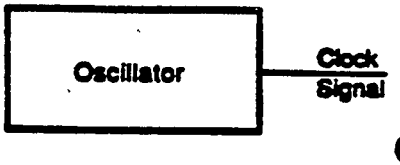


Figure 3-5
Asynchronous SR Latch

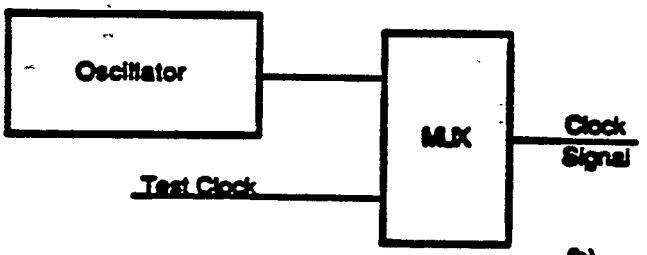


DESIGN FOR TESTABILITY GUIDELINES

Figure 3-6
Bypass internal clock



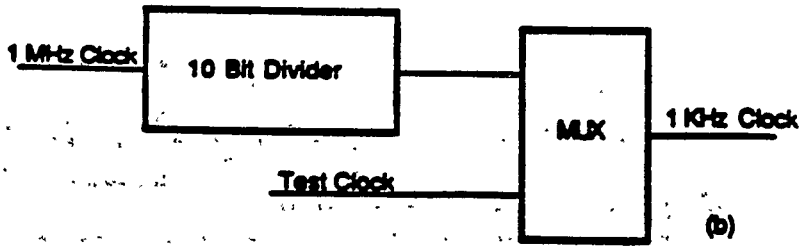
(a)



(b)

Figure 3-7
Bypass internal registers

(a)



(b)

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Figure 3-8
Partition long chain of sequential circuits

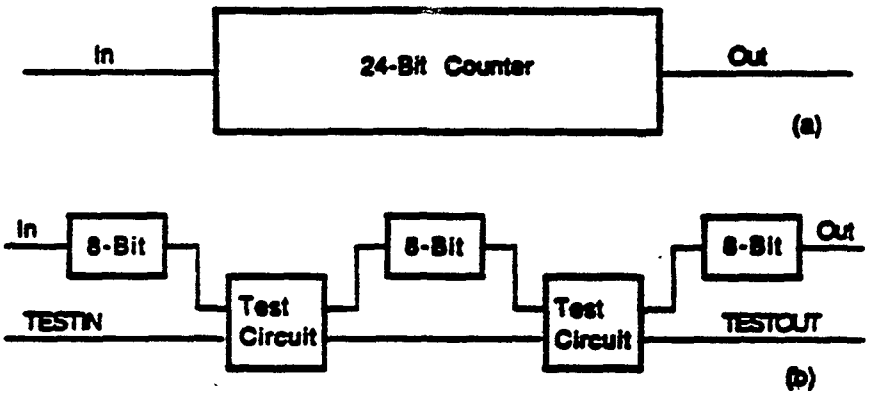

Figure 3-9
Direct access of functional module

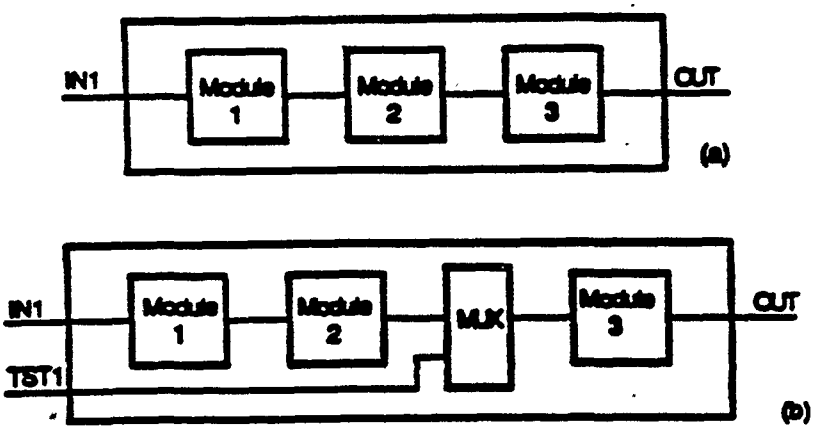

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Figure 3-10
Observing functional modules

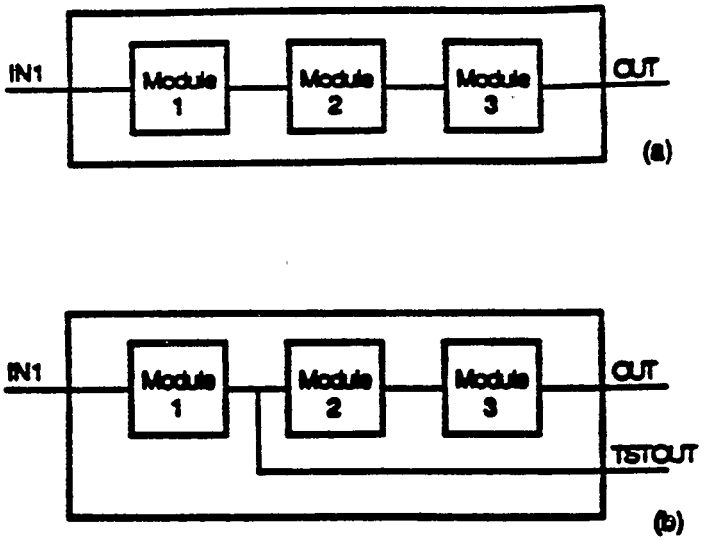

Figure 3-11
Nesting of sequential circuits

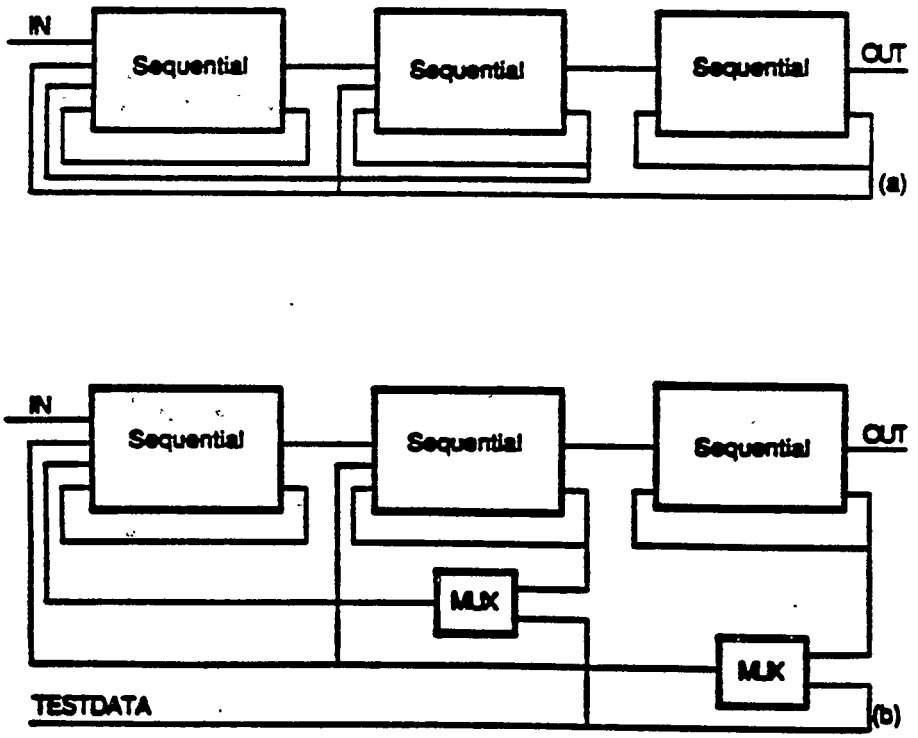

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Figure 3-12
Redundant circuitry

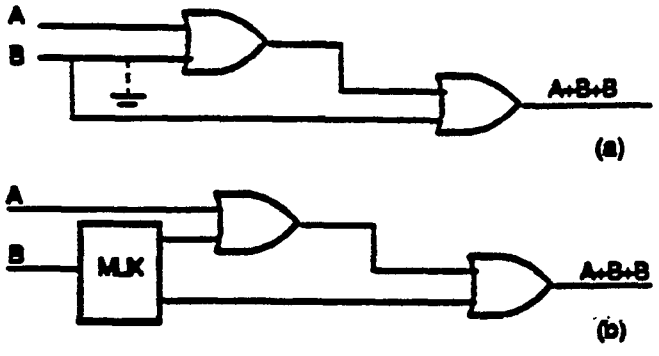
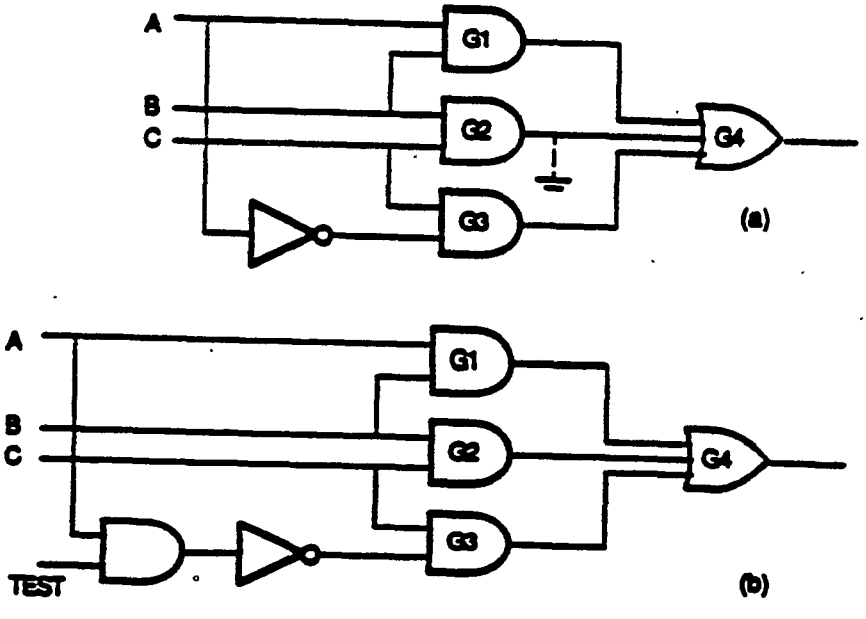


Figure 3-13
Reconverging Signals



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CHAPTER 4

ISOLATION TECHNIQUES FOR MEGACELL/MEMORY/ANALOG STRUCTURES IN SEMICUSTOM IC'S TO ENHANCE TESTABILITY

This chapter addresses a technique for isolating large circuit blocks in Semicustom IC's, in order to reduce the complexity and cost associated with performing functional testing of the chip. For the purpose of illustration, this discussion assumes that the chip to be tested contains the following large blocks:

* RAM
* ROM
* Random logic circuit
* Microprocessor
* Analog circuit (A/D converters)

In general, when these blocks are used together on a chip, a bus architecture would be employed. If it were not, a more complex testing circuit would be needed.

Figure 4-1 is a block diagram containing the blocks listed above. Clocking circuitry has been omitted in the interest of simplicity. The inputs to the Pipeline Register/Scan Register contain both Scan-in and Test Control signals. These are the only 2 additional testing signals required. The outputs of this register consist of control and address signals connected to the Control and Address Bus, data signals connected to the Data Bus, and a control signal connected to the multiplexer for the A/D converters. The Primary Input/Primary Output (PI/PO) and Primary Input (PI) lines are directly accessible from outside the circuit. The Pipeline Register/Scan Register serves the dual purpose of a conventional pipeline register during normal operation and a scan-in register during testing. This register may, in fact, be very wide (40 bits, for example). The multiplexer for the A/D converters may consist of transmission gates. The other two blocks are the Signature Analyzer (SA) and Decoders.

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Once the architecture described above has been implemented, the following steps can be used for testing. It should be noted that the steps are independent and sequencing (after Step 1) can be arranged for convenience.

1. Set the Test Control Signal to Test Mode.

2. Microprocessor test: Scan in a word that instructs the microprocessor to perform a specific operation and send the result to the signature analyzer. Additional words can be scanned in to perform various operations. Knowledge of the control words causes predictable responses from the microprocessor. The Decoder circuitry should contain "good" signatures to be compared with the output of the Signature Analyzer. This will determine if the microprocessor is working correctly. A linear feed-back shift register could be used to design the Signature Analyzer.

3. ROM test: Scan words in that enable the ROM and allow the contents to be read out one byte at a time. The contents of the ROM can be monitored and compressed in the Signature Analyzer. Results of the analysis would determine the functionality.

4. RAM test: Scan words in that enable the RAM. Conventional RAM testing methods can be employed because address and data lines are directly connected to the RAM and other circuit blocks are disabled.

5. Random logic test: Scan in a random logic test word. Use conventional random logic testing methods. Scan registers may provide assistance in this area.

6. A/D converter test: Scan in a word that enables the multiplexer. Apply analog inputs to the A/D converters, one input at a time. The digitized analog inputs can be read out via the data bus and compared with predicted values.

With reference to performance degradation, data shows that a typical transmission gate contributes about 1.3k ohms and 0.5 picofarad. In one typical application the output slew rate may degrade to 67% and the propagation delay may increase by 33%.

The hardware overhead of this technique is reflected in the Signature Analyzer, Decoder, and the modifications to make the pipeline register serve a dual purpose. Only one Signature Analyzer is needed, since it can serve each of the other blocks. However, a separate Decoder will be needed for each block.

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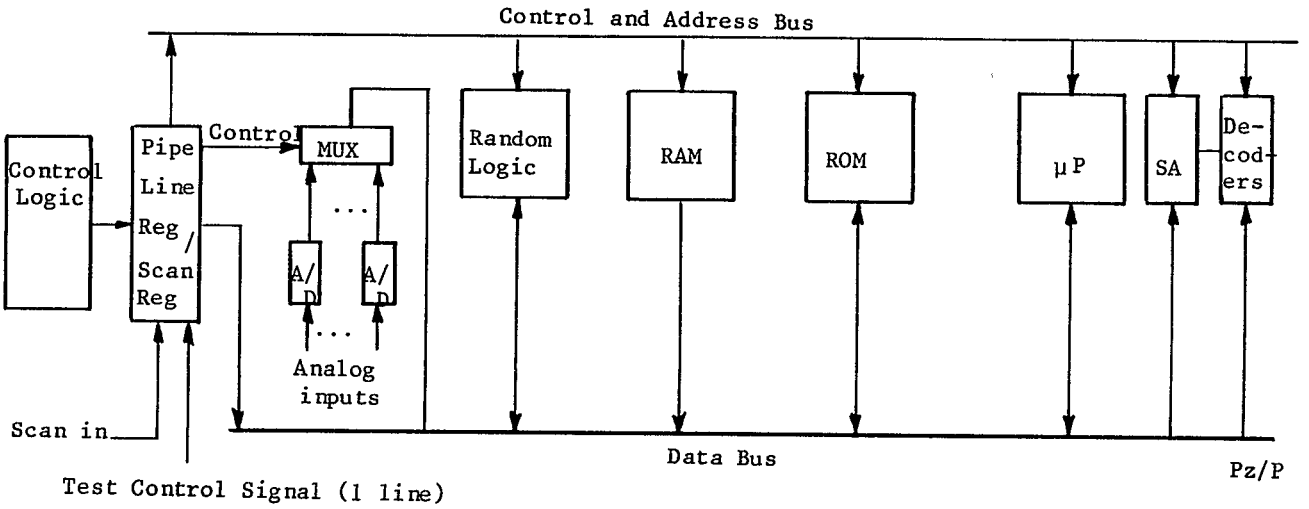
FIGURE 4-1
BLOCK DIAGRAM OF ISOLATED LARGE CIRCUIT BLOCKS



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CHAPTER 5

AUTOMATIC TEST PATTERN GENERATION

This chapter discusses an increasingly popular test methodology called Automatic Test Generation (ATG). It is the intent of this discussion to provide a practical overview of today's circuit design environment and the way ATG integrated into this environment. Three ATG approaches for sequential circuits (full scan, partial scan, and non-scan) will be discussed. Important testing and debugging implications of using the ATG approach will also be presented.

The circuit design environment has evolved dramatically over the past few years, providing computing power and software to aid in almost every phase of the design process. Schematic capture, simulation, test extraction, and layout represent the essential backbone software programs for a complete design system. Semiconductor process technology has kept pace, permitting implementation of extremely complex logic systems on a single chip. This has resulted in an increase in the difficulty of chip testing.

Much of the added testing difficulty is due to higher density and fixed I/O count. Packing more logic onto one circuit greatly increases the gate to I/O ratio and decreases the accessability to that logic. Allowing a reasonable number of I/O signals to be used for testing can considerably ease the testing process. These test signals can be used to add controllability and/or observability to the circuit in a variety of ways. However, for a great many designs it is not possible to set aside the desired number of dedicated test pins due to pinout constraints. In any case, the task of generating a complete and efficient test program must be accomplished.

Most often, designers specify a functional simulation, and the test program is automatically extracted from the functional simulation results. Fault grading tools allow the designer to grade his test program by calculating a fault coverage percentage. The designer may then add to the test program to increase the fault coverage to an acceptable level. The automation of this "test generation" process is the subject of this chapter.

An integrated design environment begins with network entry (as shown in Figure 5-1) and proceeds with electrical rules checking and simulation. During the design process it is often necessary

to modify the network to correct errors and enhance the circuit. Once the design has been solidified, the process of test generation must be accomplished. It is important that testing considerations be addressed early in the design phase so test generation becomes a task of implementing the predefined testing plan. The designer should decide upon a target percentage for fault coverage as soon as possible, as a very high percentage may require the adoption of certain circuit design methods. It is possible that during the ATG phase, additional test points will be required to achieve the target percentage. If this is the case, the network will have to be modified and resimulated. For this reason, it is important in terms of efficiency and effectiveness that the ATG software be integrated into the design environment. ATG tools require the circuit description at a gate or transistor level, all circuit timing information, any pre-generated functional test patterns and any user specified parameters. The software will then use this information to follow a flow similar to that shown in Figure 5-2.

In this example, the first step is to check the circuit for adherence to any scan design rules imposed by the ATG tool. Fault simulation is then performed with the optional user generated functional patterns. All faults detected by these patterns are tagged and eliminated from the ATG process. Any remaining undetected faults are passed to the ATG algorithm where one fault is selected. Fault simulation is rerun to check the effects of generating the input patterns necessary to check the fault under consideration, and identify any additional undetected faults that may have been detected by this pattern. Iteration of this process continues until the desired fault coverage is achieved. Fault simulation, as an intermediate step, checks the targeted fault as well as all other undetected faults, thus reducing the number of ATG iterations.

DESIGN FOR TESTABILITY GUIDELINES

PATH SENSITIZATION

Test pattern generation programs use a variety of methods to achieve essentially the same test generation capability. The definition of a good test for a fault is an input combination which produces an incorrect output when the fault under consideration is present in the circuit. Thus, the presence of the fault can be observed at the outputs. Path sensitization is one such method of generating a test for a fault. The general procedure is:

1.) Select a fault (such as node "stuck at one").
2.) Assign the faulty wire a value opposite to the fault condition (such as node at "zero").
3.) Choose a path from the fault to a circuit output.
4.) Sensitize this path by assigning logic values to gate inputs along the path such that the faulty signal is passed to the circuit output.
5.) Obtain the test to detect the fault by determining the network inputs which will produce the desired values on gate inputs along the sensitized path.

Some variations on this path sensitization method are the Boolean Differences Method, the D-Algorithm, and the Truth Table Comparison Method. All of the above are effective methods for generating tests for faults in most combinational circuitry (without reconvergent fanout). However, they are not effective tools for ATG in sequential circuits. This has led to the development of a set of design rules to simplify test generation in sequential circuits. Level-sensitive scan design (LSSD) is one such design methodology that imposes design restrictions that allow the circuit to be forced into a test mode in which the ATG methods above can be used to generate tests for faults.

Another approach is that of random vector generation. This method has straightforward applications for some combinational circuitry but has not been effectively extended to sequential circuitry. Certain combinational circuits lend themselves nicely to this approach while others do not. By evaluating some simple circuit parameters such as the number of primary inputs, the number of levels of logic, and the average fan-in, a measure of circuit resistance to random ATG can be made. The number of random vectors required to reach the desired coverage can then be estimated based on this resistance factor.

DESIGN FOR TESTABILITY GUIDELINES

FULL SCAN DESIGNS

By far, the most popular ATG methodology follows a full scan approach. This calls for the circuit to follow rigid design rules that allow the circuit to be placed in a test mode such that all logic storage elements are connected to shift registers, breaking up the combinational circuitry. When this method is used, the circuit is placed in the test mode and a test pattern is shifted in, thereby defining all internal storage states. The circuit is then taken out of the test mod packages

DESIGN FOR TESTABILITY GUIDELINES

TESTING AND DEBUGGING CONSIDERATIONS

There are several types of problems that can cause a semiconductor circuit to fail. These include logic design and layout errors as well as mask and wafer fabrication defects. When performing test pattern generation, the design engineer must first determine the strategy of testing for all possible problems.

It is very important to remember that ATG patterns should only be used to test for non-consistent faults relating to the manufacturing process. Although ATG patterns may be an efficient tool for indicating the presence of a defect, they generally provide no information relative to the nature and location of the defect. Consequently, ATG patterns are not useful to the designer who is involved in the debugging process. Most ATG packages provide a cross reference listing that shows which faults are detected in each vector. This information may be of little use, however, because many faults may be detected in each vector and isolating the specific fault may be impossible.

It is also important to note that, in general, using a scan type design and an ATG test methodology will yield a much larger (longer) test program than will a functional test methodology. For example, a 6000 gate design, assuming 20% sequential circuitry, will have approximately 300 latches. Assuming that 532 test vectors per latch will achieve greater than 97% fault coverage, the tester program will require almost 160,000 tester cycles. In contrast, it is usually possible to achieve greater than 80% fault coverage when operating the circuit in a functional mode with fewer than 10,000 tester cycles. In order to accommodate the long test programs resulting from ATG, the tester environment should provide for scan test capability such that once a pattern is presented, the tester can automatically shift it into the scan chain.

A straightforward method of avoiding debugging and pattern-length problems is to begin the test program with a thorough functional test. ATG patterns can then be added to increase fault coverage to an acceptable level. Most ATG systems accept manually generated vector input. In this way, a fault grade of the functional patterns can be done before proceeding with automatic test generation. Then the remaining undetected faults can be worked on by the ATG system.

DESIGN FOR TESTABILITY GUIDELINES

CONCLUSION

When embarking on an ATG methodology, the designer must consider many aspects of the total design environment:

* Integration of the ATG system into the design environment
* Adherence to circuit design rules pertaining to scan capability in the tester environment, if necessary
* Maintaining a functional test generation plan for debugging and critical path testing

Considering all of these items before adopting any particular ATG implementation should minimize any problems that might occur later.

DESIGN FOR TESTABILITY GUIDELINES

Figure 5-1
Typical Design Flow

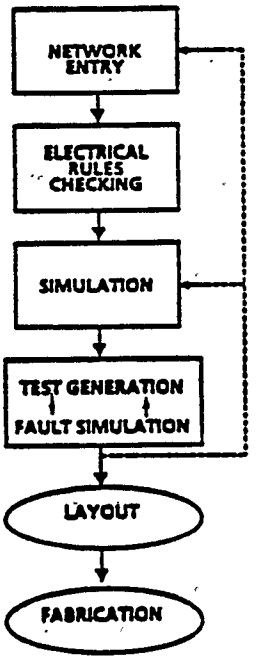

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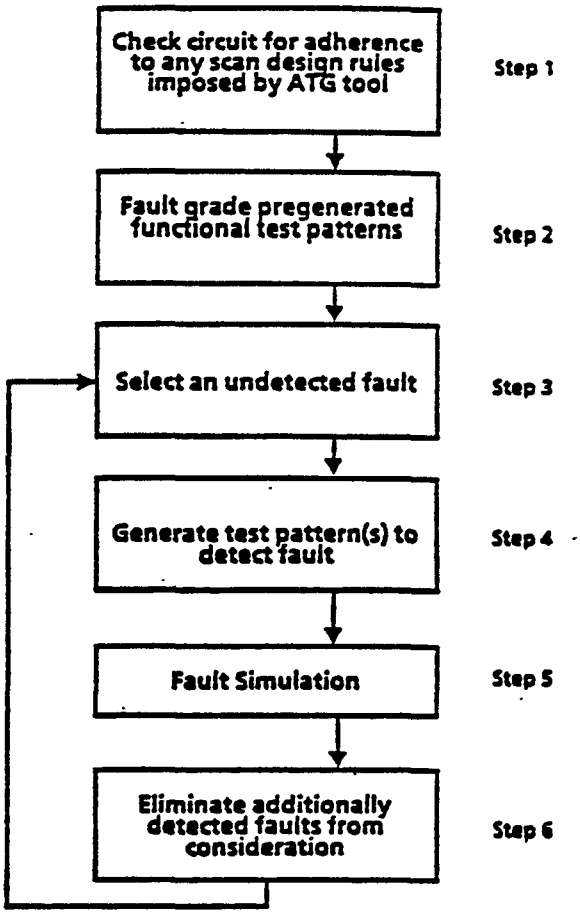
Figure 5-2
Typical ATG Flow



DESIGN FOR TESTABILITY GUIDELINES

CHAPTER 6

TEST PROGRAM GENERATION FROM SIMULATION FILES

A logic truth table is used to electrically verify the functionality of an integrated circuit and thereby check for the presence of manufacturing defects. This truth table is referred to as a test pattern, and a test vector is defined as a line in the truth table where one or more inputs or outputs changes state. Each vector is stored in a single word of the tester's main memory, and the pattern to be applied to the DUT is loaded into the tester's local memory. If the number of vectors exceeds the size of the local memory, two or more memory loads controlled by the CPU would be required, thus increasing the test time. Minimizing the number of test vectors is desirable not only to reduce the test run time, but also to reduce simulation and fault grading times.

Logic simulators allow system designers to control and observe the behavior of all nodes in a circuit, if so desired. Furthermore, the designer can monitor propagation delays through internal circuitry in response to a change in input stimuli.

Neither one of these features is available in Automated Test Equipment (ATE) used to screen integrated circuits. Access to internal nodes is not possible, and propagation delays need to be measured from inputs to outputs of the device. Testing a semicustom chip is performed by applying binary patterns (input vectors) to stimulate the logic inputs and then comparing the actual output states to the response that was predicted during the simulation process.

In general, the phase relationship and sequence of input stimuli applied to an integrated circuit to test the functionality and performance of the device are somewhat different than the simulation patterns used to verify the logic design. These differences are, for the most part, due to the inherent characteristics of testing equipment used to evaluate logic devices.

Testers are synchronous systems that require all input vectors to be changed at fixed points within the test cycle. Figure 6-1 is a diagram of the phase relationship of input and output data with respect to the test cycle for a sample test pattern. Normally, with the exception of primary clocks, input signals can change only at the beginning of each test cycle.

DESIGN FOR TESTABILITY GUIDELINES

The number of primary clocks that can be applied to the Device Under Test (DUT) is a function of the number of timing generators available in the tester. By programming these timing generators, one can select multiple clocks as well as their timing relationship with respect to the test cycle.

The duration of the test cycle varies from system to system and determines the upper limit of frequency at which a device can be tested. Typically, however, there are other constraints that require the testing frequency to be much lower than the capabilities of the tester.

One of the constraints is that all transitions at the outputs of the device must become stable within the same test cycle. Therefore, the maximum propagation delay from input to output of the DUT determines the maximum frequency at which it can be tested.

Another factor influencing the maximum testing frequency is called cycle slip. In some cases, the exact system cycle in which an output signal becomes valid is not critical to the system operation. It is, however, very important to the tester. Testing systems compare the output states to the expected responses on a cycle-by-cycle basis by activating strobe signals (see Figure 6-1) which, in turn, enable a set of comparators connected to the output channels. If output responses were to slip from one test cycle to the next, the device will fail even though it may be fully functional at the system level.

In order to avoid these problems, many semiconductor manufacturers test the functionality of the devices at a relatively low (1 MHz) tester frequency. The dynamic performance of the circuit is verified by selective measurement of propagation delays representative of the overall switching characteristics of the device.

Pin skew within the tester is another phenomenon closely related to cycle slip. Pin skew is defined as the phase shift among the input signals due to the differences in propagation delays within the pin electronics of the tester hardware. If the input signals feeding the data and the clock inputs of a flip flop change at different times, for example, they could cause the circuit to assume the wrong state, and the part will fail.

To prevent this from happening, input signals that must preserve their phase relationships should not be changed on the same test cycle.

DESIGN FOR TESTABILITY GUIDELINES

Test patterns can be greatly compacted by using bursts of clock signals when no other inputs or outputs change state within a test cycle. Figure 6-2 shows an example where clock bursting could be used to minimize the length of a test pattern.

There are cases where outputs might change state when the device is clocked a number of times but the output responses might not be of interest. In those cases the system designer should make the vendor aware of the presence of non-interesting outputs in order to take advantage of the clock bursting technique, thereby allowing compression of the test vector set.

Properly documented test vectors should contain input signals and expected output responses as observed during simulation. For any circuit containing sequential logic, test vectors typically consist of two parts:

1) An initialization step, where all memory or storage elements are set to a known state by exercising the device clock, data, and reset pins.

2) The actual test pattern used to stimulate output pins.

Though test pattern formats may vary among manufacturing companies, Figure 6-3 shows a typical generic test pattern.

Bidirectional pins must have the state of both the input and output signals listed separately. Interpretation of the information will be enhanced if the order of the input pins matches the order of the corresponding output pins. The tester will monitor the pin when the output is enabled, and will drive the pin when it is in the high impedance state.

If a device contains internal three-state busses, the designer must arrange the enable logic so that the busses are always driven (not left in a high impedance state). Furthermore, internal buss contention must be avoided to ensure that the state of the buss propagated to the device output pins during the test sequence will match the expected response from the simulation files.

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Figure 6-1
Sample synchronous pattern for use during functional test

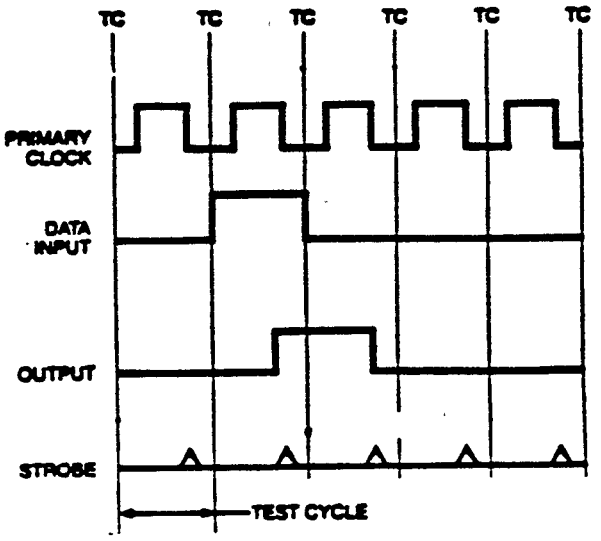

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Figure 6-2
Example of a clock burst cycle used to compress the length of the functional test pattern

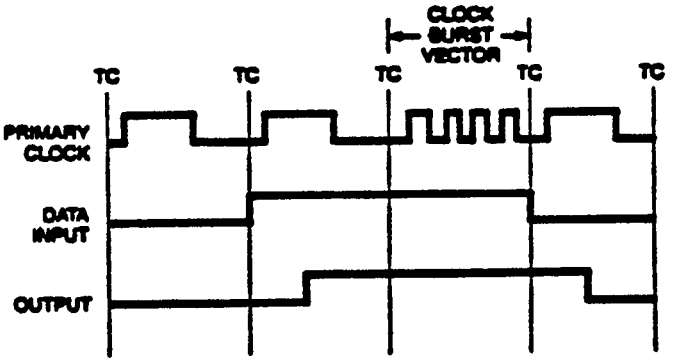

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Figure 6-3
Sample test pattern format

```
INPUT VECTORS;
SIG0,SIG1,SIG2,SIG3,SIG4,SIG5,SIG6,SIG7,
IDAT1,IDAT2,IDAT3,IDAT4,IDAT5,IDAT6;


OUTPUT SIGNALS;
SUM,CARRY,O0,O1,O2,O3,O4,O5,O6,O7,
ODAT1,ODAT2,ODAT3,ODAT4,ODAT5,ODAT6;
```

INPUTS;	OUTPUTS;
10010101xxxxxx	xxxxxxxxxxxxxx
10100101xxxxxx	xxxx000000001001
10001010xxxxxx	00011000010010001
01010010xxxxxx	10010100101100001
01001010xxxxxx	10010101001100001
10010100xxxxxx	01010010010010010
01001010xxxxxx	01001010010010001
10010010xxxxxx	10011110111101000
11011010xxxxxx	10110110101100000
00001111xxxxxx	00001010000000001
00010100xxxxxx	01001010001010001
11110010xxxxxx	01010111011010000
10100101xxxxx1	10101010101100oz
10010101xxxx01	10101001010000zz
10001010xxx110	10001010010102zzz
10010010xx0101	10010001010022zzz
10000100x10010	10000101001zzzzz
10010101010101	10010010102zzzzz
10010010100101	10010010102zzzzz
10010010010101	00101001002zzzzz
00101000110101	00010100102zzzzz
10001010100011	01001010012zzzzz
10000101011011	00000101012zzzzz
10001010101010	00001010102zzzzz
10001010110101	10000010102zzzzz
10001000010101	00010100102zzzzz
10001000110100	10010001012zzzzz
00100100101011	01010010102zzzzz
10010100101011	01010101102zzzzz
10101100101010	00101010102zzzzz
00101101010101	01010101002zzzzz
00101001000101	10101010102zzzzz

DESIGN FOR TESTABILITY GUIDELINES

CHAPTER 7

ENHANCING DC PARAMETRIC AND BOARD LEVEL TESTING

SYSTEM LEVEL TEST CONSIDERATIONS IN MULTI-CHIP/MULTI-MODULE SEMICUSTOM IC DESIGNS

The discussion in this chapter will be concerned with design methods for assuring the functionality of multiple semi-custom integrated circuits (or Application Specific Integrated Circuits, ASIC's) when they are combined on the circuit board. Although the method presented here is not currently known to be required in any ASIC design system, it is presented as one possible technique to be used by those system designers who want to improve manufacturability.

Two current limitations of production board testers define the requirements of such a design and test methodology. First, because of limited pattern memory, current board testers provide for only a few hundred to a few thousand test vectors. A good fault graded test pattern for one ASIC design may itself be several thousand vectors in length. Second, if an ASIC (or any) component cannot be isolated out of the board environment, it must be back driven by the board tester. This may unduly stress the component. In the case of a CMOS component, back driving may also lead to latchup induced failures due to injected current.

These board tester limitations place several requirements on design and test methodology for ASIC components. First, due to the limited number of vectors available at test, a small (low number of vectors) test for all ASIC components is required. Second, to avoid the stress of backdriving, component isolation of all ASIC components must be provided.

To ensure good fault coverage and yet keep the ASIC component test vector set for circuit board test small, internal fault detection must be performed on the component prior to board test. This important testing methodology should be two-fold. The production test pattern for the component must yield a high fault score for all single stuck-at faults. Using this proven production test pattern, all ASIC components should be tested by the ASIC vendor before shipping to the customer.

DESIGN FOR TESTABILITY GUIDELINES

Assuming that this internal fault detection has already taken place, the size of tests to verify that all I/O cells and connections are good must still be kept small. Utilization of a set of testable I/O cells by all ASIC designs would allow detection of the primary manufacturing failure modes:

* Blown input buffers due to electrostatic discharge

* Blown I/O buffers due to latchup failures

* Bad solder joints and/or socket connections

These cells should also allow all I/O buffers to be placed in a high impedance state, with a minimal number of vectors, to provide component isolation.

A special set of three I/O buffers is required to minimize the number of test vectors required to verify functionality and simplify the dc parametric testing of all input and output buffers. Figure 7-1 shows these three special I/O buffers. Figure 7-2 shows a summary of the I/O Buffer Logic States.

The first of these is a dedicated "-I/O TEST ENABLE" input buffer. If this signal is driven to a logic "0", the state of the output buffers is controlled by signals from the other two special buffers, "+I/O TEST OUTPUT ENABLE" and "+I/O TEST DATA". If this "-I/O TEST ENABLE" signal is driven to a logic "1", or not driven, the state of the output buffers is controlled by the functional data and output enable signals for each buffer.

The second special buffer is a multiplexed "+I/O TEST OUTPUT ENABLE" input buffer. It can be used as a normal input buffer. If "- I/O TEST ENABLE" is active (logic "0"), this input buffer controls the output enable of all of the output buffers. A logic "0" at this input causes all the output buffers to be placed in a high impedance state. A logic "1" causes all of the output buffers to be driven with the value given by the "+ I/O TEST DATA" signal.

The third special buffer is a dedicated "+ I/O TEST DATA" buffer. If "- I/O TEST ENABLE" is inactive (logic "1"), this signal is an output that indicates the Exclusive OR sum of all the inputs except "- I/O TEST ENABLE". If "- I/O TEST ENABLE" is active (logic "0") and + I/O TEST ENABLE" is active (logic "1"), this signal acts as an input that determines whether a logic "1" or "0" will be driven on all of the output buffers.

DESIGN FOR TESTABILITY GUIDELINES

With the above special buffers in place, testing the remaining I/O buffers is simplified. For example, all inputs can be Exclusive OR'd together such that regardless of the state of the other buffers, changing any single output will cause a change of state of the "I/O TEST DATA" output. Therefore, if there are N buffers it will take only (2*N) vectors to verify the functionality of all input buffers. In addition, dc parametric testing of input buffers for Vih and Vil is simplified.

Also, all output buffers can be controlled to either high impedance, logic "1", or logic "0", independent of the internal state of the chip. This means that only three input vectors are required to verify functionality of all output buffers. DC parametric testing of output buffers for Voh versus Ioh and Vol versus Iol is also simplified as well. Figure 7-3 illustrates this testing using the three I/O buffers.

In summary, design and test methodology required to assure system level testability of ASIC's should include the following:

* Special, easily testable three-stateable I/O buffers designed on all ASIC's.

* Vendor's production test pattern must yield a high fault score for all single stuck-at faults.

ON-CHIP TESTABILITY FEATURES

The use of on-chip testability features is intended to allow circuit designers an inexpensive, efficient, and simple method of performing dc parametric tests. In addition, features, such as a ring oscillator, can be added to allow the ac performance of the chip to be monitored. These simple tests are accomplished by dedicating three test pins on each circuit, and placing a multiplexer in front of each output buffer. Figure 7-4 shows a block diagram of the on-chip test features used by one gate array manufacturer. A few points should be noted regarding this diagram. First, the multiplexers in front of the output buffers are built directly into the peripheral structure of the chip. They are not constructed using the core transistors of the gate array. This significantly reduces the propagation delay through the output buffers. A similar approach is taken with the input buffers on the three test pins. Thus, by building the test structures directly into the silicon instead of by using metalization, performance of the device is optimized.

DESIGN FOR TESTABILITY GUIDELINES

Table 7-1 is a truth table detailing the on-chip test functions. There are three dedicated test pins TESTN, TOEN, and TDAT. By setting them all to a logical "1" the chip functions in the normal operation mode. When test enable (TESTN) or test output enable (TOEN) is set to a logical "0" the chip is placed in the test mode. To illustrate this approach, note that when TESTN=TOEN="0" it is possible to test Vol, Voh, Iol, and Ioh for every output buffer in two test cycles. Other parametric tests can be performed in a similar manner.

A ring oscillator has been included to determine the ac performance of the chip. This allows easy and direct access to the part in order to ensure that the process is within expected limits. The ring oscillator is also useful for performing correlation with the manufacturer's data at incoming inspection.

DESIGN FOR TESTABILITY GUIDELINES

Figure 7-1
Special input/output buffers

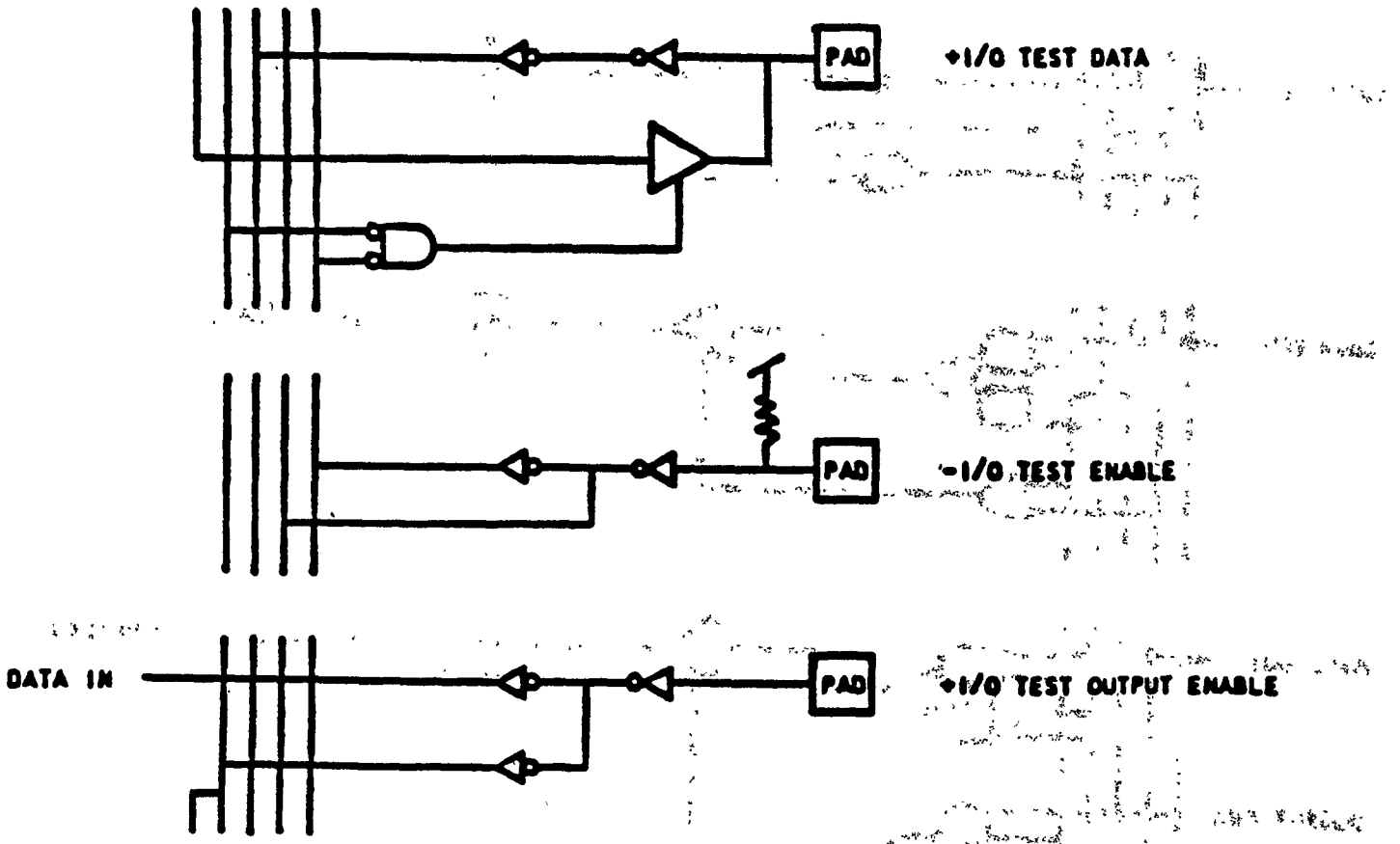
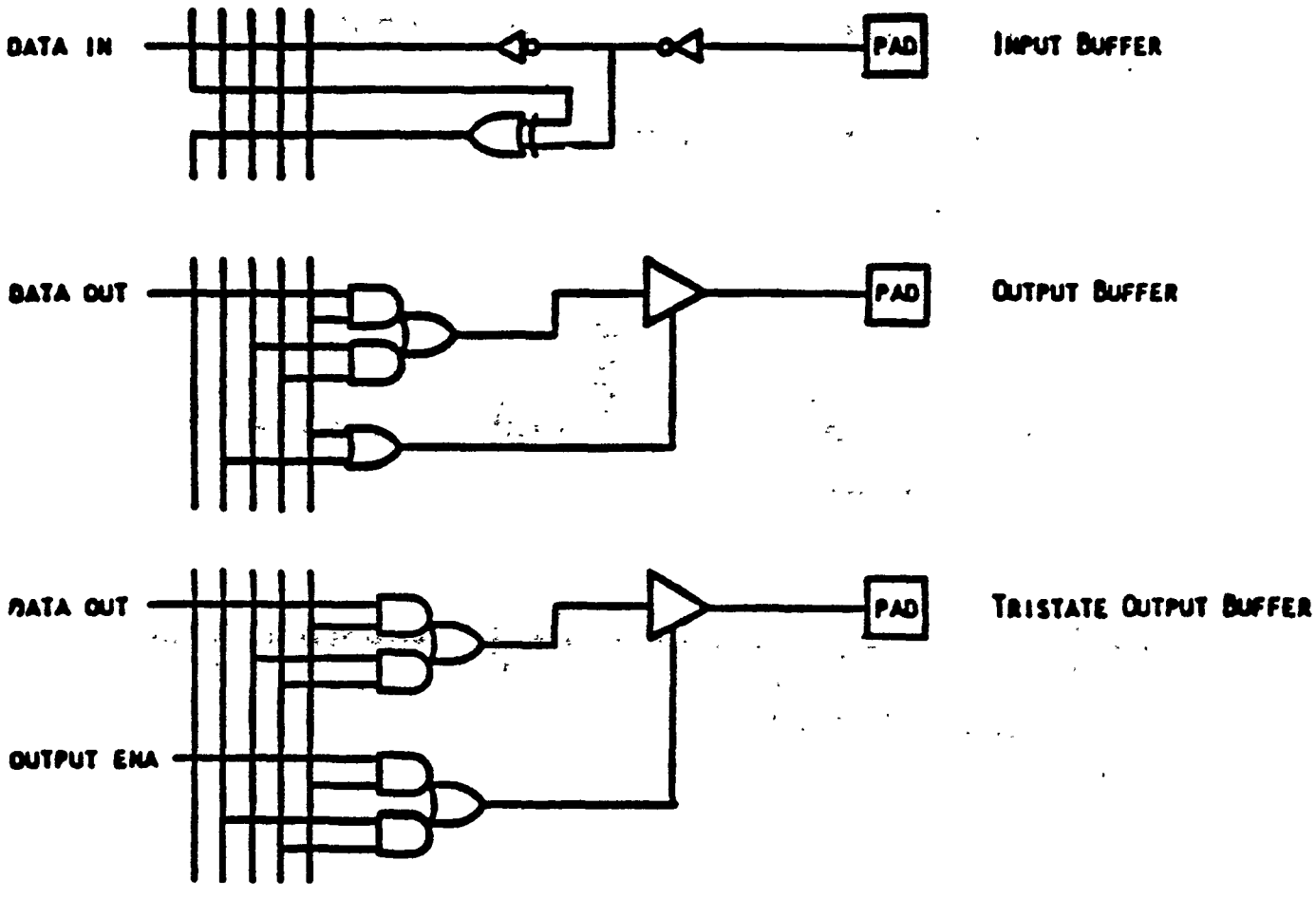


Figure 7-2
I/O Buffer Logic States

-I/O TEST ENAB.	+I/O TEST OUT ENAB.	+I/O TEST DATA	DATA OUT
INPUT: 0	INPUT: 0	HI-Z STATE	HI-Z
	INPUT: 1	INPUT: 0	OUT: 0
		INPUT: 1	OUT: 1
INPUT: 1	PIN USED AS A NORMAL INPUT BUFFER.	PIN USED AS AN OUTPUT. INDICATES EX-OR SUM OF INPUTS.	OUT: NORMAL LOGIC FUNCTION.

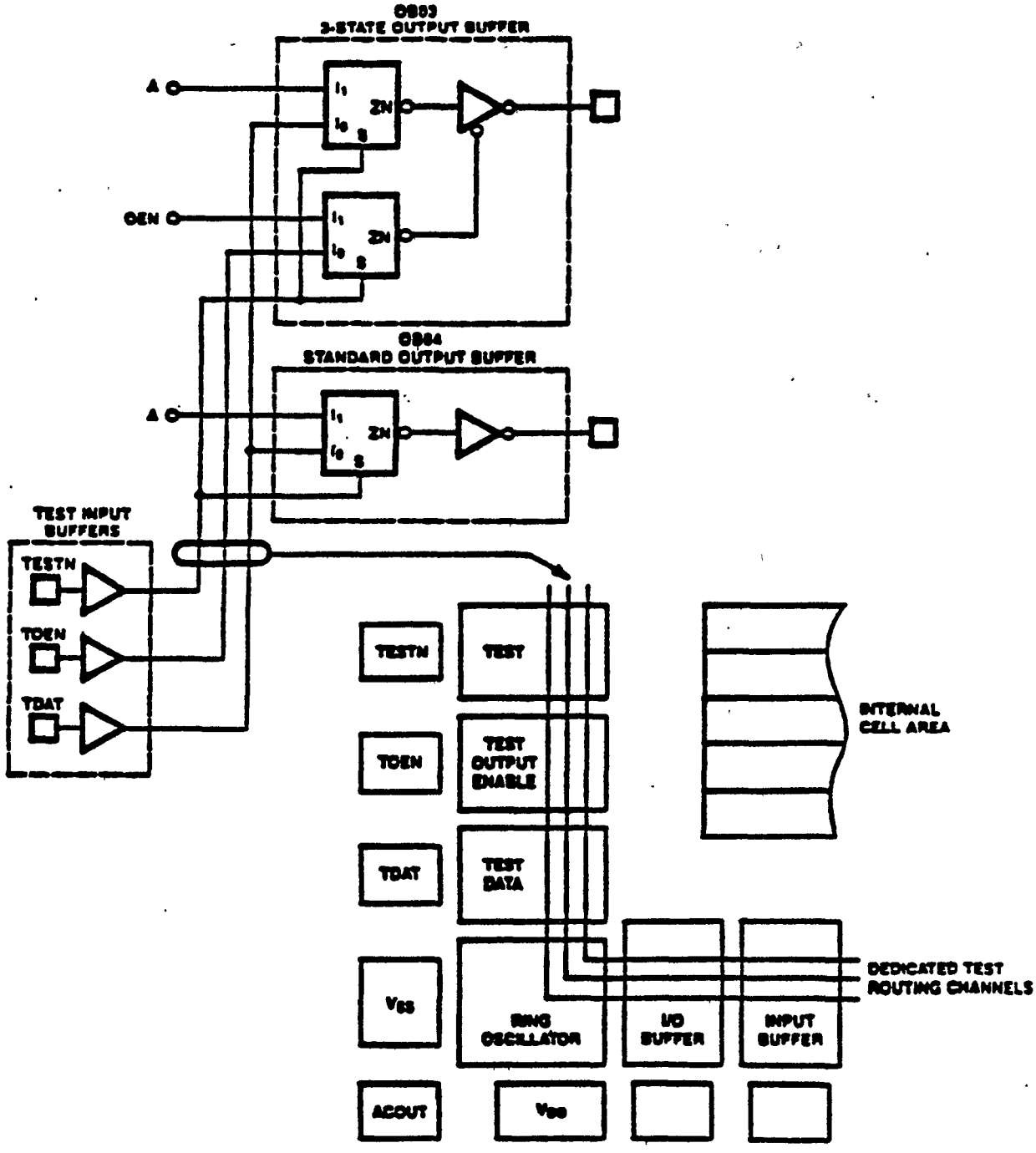
DESIGN FOR TESTABILITY GUIDELINES

Figure 7-3
Testable Input/output Buffer Example



DESIGN FOR TESTABILITY GUIDELINES

Figure 7-4
ON-CHIP TEST DIAGRAM



DESIGN FOR TESTABILITY GUIDELINES

TABLE 7-1
Truth Table for On-chip Testability Features

TEST TYPE	TESTN	TOEN	TDAT	TESTS ACOUT PERFORMED	DESCRIP.
DC PARAMETRIC	0	0	0	DISAB Vol,Iol	TEST DATA
	0	0	1	DISAB Voh,Ioh	ON OUTS
AC MONITOR	0	1	0	ENAB RING OSC	OUTS IN
DC PARAMETRIC	0	1	0	DISAB LEAKAGE	AC MODE
DC PARAMETRIC	0	1	1	DISAB SBY CURRENT	STATIC PWR
USER DEFINED	1	0	0	DISAB	
	1	0	1	DISAB	
	1	1	0	DISAB	
NORMAL	1	1	1	DISAB	NORMAL OP

DESIGN FOR TESTABILITY GUIDELINES

CHAPTER 8

SUMMARY AND CONCLUSION

This document has made an attempt to bring to the reader a brief overview of the necessity for designing with testability as a primary goal. It has also presented short descriptions of some of the more popular methods available with which to achieve this goal.

The application of these methods will vary from company to company and from circuit to circuit. No attempt should be made to suggest that there is only one correct method to use when designing testable circuits. Company policies or contract restrictions may favor particular approaches, and this document is not intended to contradict those policies.

When DFT is maintained as a goal, the designer, his company and the ultimate customer all will be rewarded. The designer will have fewer problems to solve at the time of test. The company will have to spend less time generating test programs and debugging those programs and the circuit. The customer will benefit through improved delivery and shorter incoming inspection cycles.

There is still, however, no such thing as a free lunch. DFT is not without its price. Chip layouts will be more complex. In some cases, they may even operate at slightly lower clock rates. These will be the challenges that will require the judicious use of DFT techniques and good engineering judgment.

As circuits continue to grow in complexity, DFT will move from the status of a design goal to that of an absolute necessity. VLSI and larger circuits with embedded processors and/or memories must be capable of being completely tested if any assurance of quality is to be provided. DFT techniques will continue to improve with time, as will the computer programs that automatically generate test programs to work with those techniques. The future will most certainly be technically challenging (and rewarding) for the circuit design and the design automation tool development communities.

DESIGN FOR TESTABILITY GUIDELINES

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APPENDIX A

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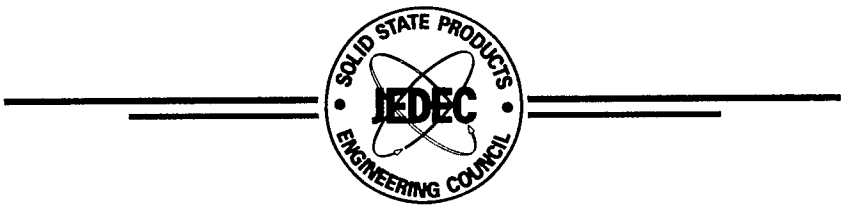
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