JEDEC STANDARD

Low Frequency Power Transistors

JESD10

JANUARY 1976 (Reaffirmed: SEPTEMBER 1981, OCTOBER 2002)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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JEDEC STANDARD No. 10

LOW FREQUENCY
POWER TRANSISTORS

Formerly JEDEC Suggested Standard No. 10

Published January, 1976

Reaffirmed September, 1981

Prepared by

JEDEC JC-25 Committee on Low Frequency Power Transistors

FOREWORD

The material in this document was developed by the Committee on Low Frequency Power Transistors (JC-25) of the Joint Electron Device Engineering Councils (JEDEC), and has been approved by the JEDEC Council for issuance as a JEDEC Suggested Standard.

The products under the jurisdiction of the Committee, and to which the document is primarily directed, include all power transistors, power Darlingtons, and similar single-chip devices capable of dissipating 2.5 W or more of power, and rated to operate at frequencies less than 3 MHz and to have gain band-width products less than 300 MHz.

This document is intended for the use of both transistor suppliers and users. It includes the test methods which are specified in the Committee's registration formats and are used for establishing and verifying the maximum ratings, safe operating conditions, and electrical characteristics of low frequency power transistors registered by JEDEC. It also includes accepted practices for making thermal characteristic tests of these transistors. Pertinent more to the interests of suppliers is a part on procedures for having transistors registered by JEDEC, and a part on military specifications used as procurement documents by the United States Government for purchasing semiconductor devices. Of more general interest is a users guide with sections on transistor failure modes, effects of temperature on electrical parameters, and hints for trouble shooting transistor circuits. The terms, with their definitions, and the letter symbols used in the document are listed in a separate part.

The document is issued in the form of a suggested standard while experience is gained with its use to determine if it should be adopted as an EIA-NEMA recommended standard.

Suggested Standard for

Low Frequency Power Transistors

ABBREVIATED TABLE OF CONTENTS

PART I

TERMS, DEFINITIONS AND LETTER SYMBOLS

PART 1

TERMS, DEFINITIONS AND LETTER SYMBOLS

CONTENTS

PART 1

TERMS, DEFINITIONS, AND LETTER SYMBOLS

1.1 INTRODUCTION

This part consists of a listing of letter symbols, terms, and definitions which are used in other parts of this document, and some which are included for general information. Omitted from the list, however, are some special letter symbols of limited application whose use and definition are sufficiently close in the document to avoid the necessity of being included.

While the primary source for this listing is JEDEC Publication No. 77-A, the listing and the JC-25 JEDEC registration formats are recommended as more specialized reference material and have overriding authority where any conflicts may occur.

References to definitions which are provided in JEDEC Publication 77-A are included in parentheses after the definition. Reference to the source of other definitions used are also included as appropriate.

The letter symbols used consist of primary symbols and secondary or subscript symbols. Upper-case letters indicate dc, average, rms, or maximum values while lower-case letters indicate instantaneous values of a quantity which varies with time

Descriptive information concerning letter symbols used are abbreviated and added in subscript, sometimes in parentheses. The abbreviations used are as follows: *M* and *PK* for maximum or peak value, *AV* for average value, *max* for maximum value, *min* for minimum value, and *on* for the value while the transistor is in its conducting state.

Multiple terminals connected to electrodes of the same type, such as the bases of a Darlington device, are identified by adding a number following and in line with each terminal designation in accordance with terminal numbering in EIA Standard RS-321B. For example, V_{EB1} is the voltage between the emitter and base terminal number 1.

1.2 TERMS AND DEFINITIONS

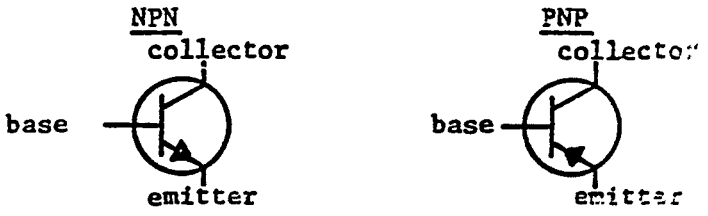
Term	*Definition*
base (B, b)*	A region which lies between an emitter and collector of a transistor and into which minority carriers are injected. (Ref. 60 IRE 28.S.
breakdown.	A phenomenon occurring in a reverse-biased semiconductor junction, the initiation of which is observed as a transition from a region of high small-signal resistance to a region of substantially lower small-signal resistance for an increasing magnitude of reverse current. (Ref. RS-282 par. 1.38).

Term	*Definition*
breakdown region	A region of the volt-ampere characteristic beyond the initiation of breakdown for an increasing magnitude of reverse current. (Ref RS-282 par. 1.37).
breakdown voltage.	The voltage measured at a specified current in a breakdown region. (Ref MIL-S-19500D Par. 20.3).
collector (C, c)*.	A region through which a primary flow of charge carriers leaves the base. (Ref. 60 IRE 28.S1).
electrode	An electrical and mechanical contact to a region of a semiconductor device. (Ref. RS-282 par. 1.06).
emitter (E, e)*	A region from which charge carriers that are minority carriers in the base are injected into the base. (Ref. 60 IRE 28.S1).
junction, collector.	A semiconductor junction normally biased in the high-resistance direction, the current through which can be controlled by the introduction of minority carriers into the base. (Ref. 60 IRE 28.S1).
junction, emitter	A semiconductor junction normally biased in the low-resistance direction to inject minority carriers into the base. (Ref. 60 IRE 28.S1).
open-circuit	A circuit in which halving the magnitude of the terminating impedance does not produce a change in the parameter being measured greater than the required accuracy of the measurement. (Ref MIL-S-19500D par. 20.8).
reverse current.	The current that flows through a semiconductor junction in the reverse direction.

*NOTE: Reference to base, collector, emitter symbolism (B, b, C, c, E, c) refers to the device terminals connected to those regions.

Term	*Definition*
reverse direction	The direction of higher resistance to steady direct-current flow through a semiconductor junction. (Ref. RS-282 par. 1.20).
saturation	A base-current and a collector-current condition resulting in a forward-biased collector junction. (Ref. JEDEC Publ. 77-A, p. D1.)
second breakdown	A condition of the transistor, resulting from a lateral current instability, in which the electrical characteristics are determined principally by the spreading resistance of a thermally maintained current constriction. The initiation of second breakdown is observed as a decrease in the voltage sustained by the collector. JC-25 NOTE: Second breakdown differs from thermal failure in that its initiation can not be predicted from low voltage thermal resistance measurements. Unless the current and duration in second breakdown are limited the high junction temperature at the current constriction will result in failure, usually as a collector-to-emitter short-circuit. Second breakdown can occur at positive, negative, or zero base current.
semiconductor device	A device whose essential characteristics are due to the flow of charge carriers within a semiconductor. (Ref. RS-282 par. 1.09).
semiconductor junction . . . . . (commonly referred to as junction)	A region of transition between semiconductor regions of different electrical properties (e.g., n-n+, p-n, p-p+ semiconductors), or between a metal and a semiconductor. (Ref. RS-282 par. 1.0).
short-circuit.	A circuit in which doubling the magnitude of the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. (Ref. MIL-S-19500D par. 20.16).

Term	*Definition*
small-signal	A signal which when doubled in magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. (Ref. MIL-S-19500D par. 20.17).
static value	A non-varying value or quantity of measurement at a specified fixed point, or the slope of the line from the origin to the operating point on the appropriate characteristic curve. (Ref. IEEE #255 par. 2.2.1).
terminal	An externally available point of connection to one or more electrodes. (Ref. RS-282 par. 1.14).
thermal resistance (steady-state)	The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium. (Ref. IEEE #223).
transient thermal impedance	The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval causing the change of temperature difference. (Ref. IEEE #223).
transistor	An active semiconductor device capable of providing power amplification and having three or more terminals. (Ref. IEC #147-0 par. 0-2.8).
transistor, junction, multijunction type	A transistor having a base and two or more junctions.
	Graphic symbols for emitter, base, collector transistors: (Ref. ANSI Y32.2).
	NOTE: In the graphic symbols, the envelope is optional if no element is connected to the envelope.

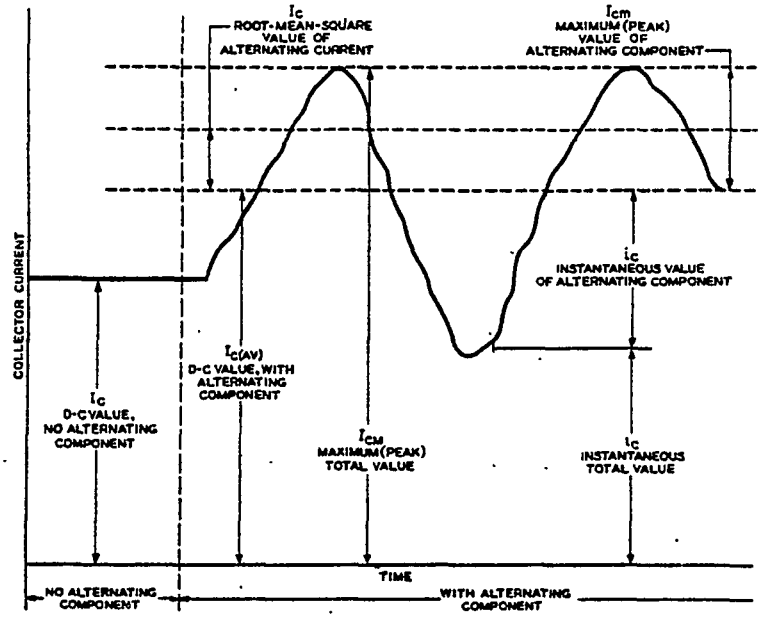


1.3 LETTER SYMBOLS, TERMS AND DEFINITIONS

Symbol	*Term*	*Definition*
C_{ibo}	open-circuit input capacitance	The capacitance measured across the input terminals (emitter and base) with the collector open-circuited for ac. (Ref. IEEE #255).
C_{obo}	open-circuit output capacitance	The capacitance measured across the output terminals (collector and base) with the input open-circuited to ac. (Ref. IEEE #255).
f_{hfe}	small-signal short-circuit forward current transfer ratio cutoff frequency (common-emitter)	The lowest frequency at which the magnitude of the small-signal short-circuit forward current transfer ratio is 0.707 of its value at a specified low frequency (usually 1 kHz or less). (Ref. IEEE #255).
f_T	transition frequency or frequency at which small-signal forward current transfer ratio (common-emitter) extrapolates to unity	The product of the modulus (magnitude) of the common-emitter small-signal short-circuit forward current transfer ratio, h_{fe}, and the frequency of measurement when this frequency is sufficiently high so that the modulus (magnitude) of h_{fe} is decreasing with a slope of approximately 6 dB per octave. (Ref. IEEE #255).
G_{PE}	large-signal insertion power gain (common-emitter)	The ratio, usually expressed in dB, of the signal power delivered to the load to the large-signal power delivered to the input.
h_{FE}	static forward current transfer ratio (common-emitter)	The ratio of the dc collector current to the dc base current. (Ref. MIL-S-19500D par. 30.28).
h_{fe}	small-signal short-circuit forward current transfer ratio (common emitter)	The ratio of the ac collector current to the small-signal ac base current with the collector short-circuited to the emitter for ac. (Ref. MIL-S-19500D par. 30.20).
h_{IE}	static input resistance (common-emitter)	The ratio of the dc base-emitter voltage to the dc base current. (Ref. MIL-S-19500D par. 30.29).
h_{ie}	small-signal short-circuit input impedance (common-emitter)	The ratio of the small-signal ac base-emitter voltage to the ac base current with the collector short-circuited to the emitter for ac. (Ref. MIL-S-19500D par. 30.24).

Symbol	*Term*	*Definition*
$I_m(h_{ie})$	imaginary part of the small-signal short-circuit input impedance, (common-emitter)	The ratio of the out-of-phase (imaginary) component of the small-signal ac base-emitter voltage to the ac base current with the collector terminal short-circuited to the emitter terminal for ac.
$R_e(h_{ie})$	real part of the small-signal short-circuit input impedance, (common-emitter)	The ratio of the in-phase (real) component of the small-signal ac base-emitter voltage to the ac base current with the collector terminal short-circuited to the emitter terminal for ac.
h_{oe}	small-signal open-circuit output admittance, (common-emitter)	The ratio of the ac collector current to the small-signal ac collector-emitter voltage with the base terminal open-circuited to the emitter for ac. (Ref. MIL-S-19500D par. 30.15).
$I_m(h_{oe})$	imaginary part of the small-signal open-circuit output admittance, (common-emitter)	The ratio of the ac collector current to the out-of-phase (imaginary) component of the small-signal collector-emitter voltage and with the base terminal open-circuited to the emitter for ac.
$R_e(h_{oe})$	real part of the small-signal open-circuit output admittance, (common-emitter)	The ratio of the ac collector current to the in-phase (real) component of the small-signal collector-emitter voltage and with the base-terminal open-circuited to the emitter for ac.
I_B, I_C, I_E	current, dc (base-terminal, collector-terminal, emitter-terminal)	The value of the dc current into the terminal indicated by the subscript.
I_b, I_c, I_e	current, rms value of alternating component (base-terminal, collector-terminal, emitter-terminal)	The root-mean-square value of alternating current into the terminal indicated by the subscript.
i_B, i_C, i_E	current, instantaneous total value (base-terminal, collector-terminal, emitter-terminal)	The instantaneous total value of alternating current into the terminal indicated by the subscript.

DIAGRAM ILLUSTRATING FOREGOING CURRENTS (Ref IEEE #255)



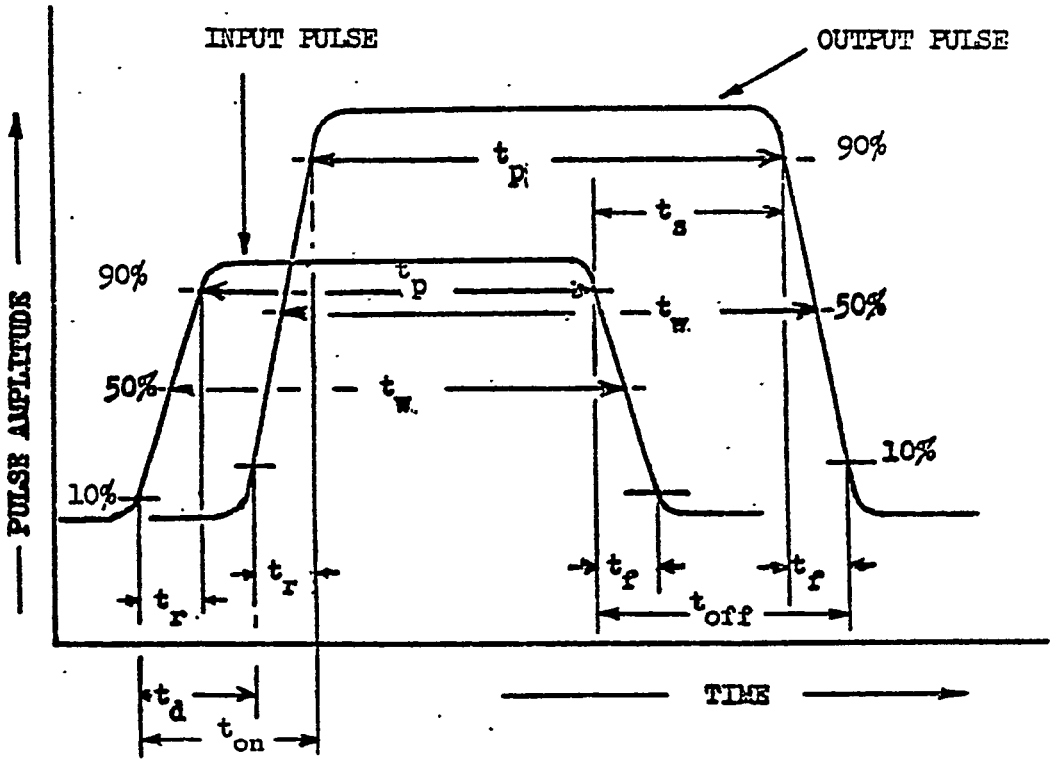
Symbol	*Term*	*Definition*
I_{CBO}	collector cutoff current, dc, emitter open	The dc current into the collector terminal when it is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited. (Ref IEEE #255).
I_{CEO}, I_{CER}, I_{CES}, I_{CEV}, I_{CEX}	collector cutoff current, dc (base open, resistance between base and emitter, base short-circuited to emitter, voltage between base and emitter, circuit between base and emitter)	The dc current into the collector terminal when it is biased in the reverse direction* with respect to the emitter terminal and the base terminal is (as indicated by the last subscript letter as follows): O = open-circuited. R = returned to the emitter terminal through a specified resistance. S = short-circuited to the emitter terminal. V = returned to the emitter terminal through a specified voltage. X = returned to the emitter terminal through a specified circuit. (Ref. IEEE #255) *For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for NPN transistors or negative for PNP transistors with respect to the emitter terminal.

Symbol	*Term*	*Definition*
I_{EBO}	emitter cutoff current, dc, collector open	The dc current into the emitter terminal when it is biased in the reverse direction with respect to the base terminal and the collector terminal is open-circuited. (Ref. IEEE #255).
P_{BE}	power input, dc (to the base, common-emitter)	The product of the dc input current and voltage with the common-emitter circuit configuration.
p_{BE}	power input; instantaneous total (to the base, common-emitter)	The product of the instantaneous input current and voltage with the common-emitter circuit configuration.
P_{OE}	large-signal output power (common-emitter)	The product of the large-signal ac output current and voltage with the common-emitter circuit configuration.
P_T	total nonreactive power input to all terminals	The sum of the products of the dc input currents and voltages, i.e. $V_{BE} \cdot I_B + V_{CE} \cdot I_C$ or $V_{BE} \cdot I_E + V_{CB} \cdot I_C$
p_T	nonreactive power input, instanteous total, to all terminals	The sum of the products of the instantaneous input currents and voltages.
Q	quality factor	2π times the ratio of the maximum stored energy to the energy dissipated per cycle at a given frequency. Note: The Q of an inductor at a frequency is the magnitude of the ratio of its reactance to its effective series resistance at that frequency. (IEEE std. 100-1972).
$r_b'C_c$	collector-base time constant	The product of the intrinsic base resistance and collector capacitance under specified small-signal conditions.
R_Θ (formerly Θ)	thermal resistance	Refer to thermal resistance (steady state) in 1.2.
$R_{\Theta CA}$	thermal resistance, case-to-ambient	The thermal resistance (steady-state) from the device case to the ambient.
$R_{\Theta JA}$ (formerly Θ_{J-A})	thermal resistance, junction-to-ambient	The thermal resistance (steady-state) from the semiconductor junction(s) to the ambient.

Symbol	*Term*	*Definition*
$R_{\Theta JC}$ (formerly Θ_{J-C})	thermal resistance, junction-to-case	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the case.
$R_{\Theta JM}$	thermal resistance, junction-to-mounting surface	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the mounting surface.
T_A	ambient temperature or free-air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces. (Ref. MIL-S-19500D par. 20.20.1).
T_C	case temperature	The temperature measured at a specified location on the case of a device. (Ref. MIL-S-19500D par. 20.20.2).
T_J	junction temperature	The temperature of the semiconductor junction.
T_{stg}	storage temperature	The temperature at which the device, without any power applied, is stored. (Ref. MIL-S-19500D par. 20.20.3).
t_d	delay time	The time interval from the point at which the leading edge of the input pulse has reached 10 percent of its maximum amplitude to the point at which the leading edge of the output pulse has reached 10 percent of its maximum amplitude. (Ref. MIL-S-19500D par. 20.11).
t_f	fall time	The time duration during which the trailing edge of a pulse decreases from 90 to 10 percent of its maximum amplitude. (Ref. MIL-S-19500D par. 20.12).
t_{off}	turn-off time	The sum of $t_s + t_f$.
t_{on}	turn-on time	The sum of $t_d + t_r$.
t_p	pulse time	The time duration from the point on the leading edge which is 90 percent of the maximum amplitude to the point on the trailing edge which is 90 percent of the maximum amplitude. (Ref. MIL-S-19500D par. 20.15).

Symbol	*Term*	*Definition*
t_r	rise time	The time duration during which the amplitude of the leading edge of a pulse increases from 10 to 90 percent of its maximum amplitude. (Ref. MIL-S-19500D par. 20.13).
t_s	storage time	The time interval from a point 90 percent of the maximum amplitude on the trailing edge of the input pulse to a point 90 percent of the maximum amplitude on the trailing edge of the output pulse. (Ref. MIL-S-19500D par. 20.14).
t_w	pulse average time	The time duration from the point on the leading edge which is 50 percent of the maximum amplitude to a point on the trailing edge which is 50 percent of the maximum amplitude. (Ref. MIL-S-19500D par. 20.10).

DIAGRAM ILLUSTRATING PULSE TIME SYMBOLOGY



Symbol	*Term*	*Definition*
$V_{(BR)CBO}$, (formerly BV_{CBO})	breakdown voltage collector-to-base, emitter open	The breakdown voltage between the collector terminal and the base terminal when the collector terminal is biased in the reverse direction with respect to the base terminal and the emitter terminal is open-circuited. (Ref. IEEE #255).
$V_{(BR)CEO}$, (formerly BV_{CEO})	breakdown voltage, collector-to-emitter with (base open,	The breakdown voltage between the collector terminal and the emitter terminal when the collector terminal is biased in the reverse direction* with respect to the emitter terminal and the base terminal is (as indicated by the last subscript letter as follows):
$V_{(BR)CER}$, (formerly BV_{CER})	resistance between base and emitter,	
$V_{(BR)CES}$, (formerly BV_{CES})	base short-circuited to emitter,	O = open-circuited. R = returned to the emitter terminal through a specified resistance. S = short-circuited to the emitter terminal. V = returned to the emitter terminal through a specified voltage. X = returned to the emitter terminal through a specified circuit.
$V_{(BR)CEV}$, (formerly BV_{CEV})	voltage between base and emitter,	(Ref. IEEE #255)
$V_{(BR)CEX}$ (formerly BV_{CEX})	circuit between base and emitter)	*For these parameters, the collector terminal is considered to be biased in the reverse direction when it is made positive for NPN transistors or negative for PNP transistors with respect to the emitter terminal.
$V_{(BR)EBO}$, (formerly BV_{EBO})	breakdown voltage, emitter-to-base, collector open	The breakdown voltage between the emitter and base terminals when the emitter terminal is biased in the reverse direction with respect to the base terminal and the collector terminal is open-circuited. (Ref. IEEE #255).
V_{BB}, V_{CC}, V_{EE}	supply voltage, dc (base, collector, emitter)	The dc supply voltage applied to a circuit connected to the reference terminal.
V_{BC}, V_{BE}, V_{CB}, V_{CE}, V_{EB}, V_{EC}	voltage, dc or average (base-to-collector, base-to-emitter, collector-to-base, collector-to-emitter, emitter-to-base, emitter-to-collector)	The dc voltage between the terminal indicated by the first subscript and the reference terminal (stated in terms of the polarity at the terminal indicated by the first subscript).

Symbol	*Term*	*Definition*
$V_{BE(sat)}$	saturation voltage, dc, base-to-emitter	The dc voltage between the base and emitter terminals for specified base-current and collector-current conditions which are intended to ensure that the collector junction is forward biased.
$V_{EB(fl)}$,	dc open-circuit voltage (floating potential) (emitter-to-base)	The dc open-circuit voltage (floating potential) between the emitter terminal and the base terminal when the collector terminal is biased in the reverse direction with respect to the base terminal. (Ref. IEEE #255)
V_{CBO}	collector-to-base voltage, dc, emitter open	The dc voltage between the collector terminal and the base terminal when the emitter terminal is open-circuited.
$V_{CE(sat)}$	saturation voltage, dc, collector-to-emitter	The dc voltage between the collector and the emitter terminals for specified saturation conditions. (Ref. IEEE #255)
V_{CEO},	collector-to-emitter voltage, dc, with (base open,	The dc voltage between the collector terminal and the emitter terminal when the base terminal is (as indicated by the last subscript letter):
V_{CER},	resistance between base and emitter,	O = open circuited.
V_{CES},	base short-circuited to emitter,	R = returned to the emitter terminal through a specified resistance.
V_{CEV},	voltage between base and emitter,	S = short-circuited to the emitter terminal.
V_{CEX}	circuit between base and emitter)	V = returned to the emitter terminal through a specified voltage.
		X = returned to the emitter terminal through a specified circuit.

Symbol	*Term*	*Definition*
$V_{CEO(sus)}$, $V_{CER(sus)}$, $V_{CES(sus)}$, $V_{CEV(sus)}$, $V_{CEX(sus)}$	sustaining voltage, collector-to-emitter with (base open, resistance between base and emitter, base short-circuited to emitter, voltage between base and emitter, circuit between base and emitter).	The collector-to-emitter breakdown voltage at relatively high values of collector current where the breakdown voltage is relatively insensitive to changes in collector current. The base terminal is (as indicated by the third subscript letter as follows): O = open circuited. R = returned to the emitter terminal through a specified resistance. S = short-circuited to the emitter terminal. V = returned to the emitter terminal through a specified voltage. X = returned to the emitter terminal through a specified circuit. NOTE: This would be the transient voltage between the collector and emitter terminals during switching with an inductive load from a forward-biased base-emitter to an external condition described by the third subscript letter.
V_{EBO}	emitter-to-base voltage, dc, collector open	The dc voltage between the emitter terminal and the base terminal with the collector terminal open-circuited.
$Z_{\Theta(t)}$ (formerly $\Theta_{(t)}$)	transient thermal impedance	Refer to transient thermal impedance in 1.2.
$Z_{\Theta JA(t)}$ (formerly $\Theta_{J-A(t)}$)	transient thermal impedance, junction-to-ambient	The transient thermal impedance from the semiconductor junction(s) to the ambient.
$Z_{\Theta JC(t)}$ (formerly $\Theta_{J-C(t)}$)	transient thermal impedance, junction-to-case	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

PART 2

REGISTRATION

PART 2

REGISTRATION

CONTENTS

PART 2

REGISTRATION

2.1 INTRODUCTION

This chapter describes established procedures that are followed in the assignment of semiconductor industry type designations to and registration of power transistors. These procedures are discussed from the standpoints of both administration by JEDEC and compliance by the device manufacturer.

The material in 2.2 on type assignments is taken from JEDEC Publication No. 15C (October 1971). However, the latest revision of this publication has overriding authority where any conflict may occur with the material contained here.

The material in 2.3 and 2.4 is taken from JEDEC Publication No. 74 (revised).

2.2 TYPE ASSIGNMENT

2.2.1 Introduction

This section describes the established administrative procedures that are followed in the orderly assignment of type designations to and registration of solid state devices. Technical standards concerning registration are not included.

The term "type designation" used here refers to the number assigned to a solid state device in accordance with the EIA-NEMA Standards for Designation System for Solid State Devices (EIA Standard RS-370, NEMA Publication No. 512). The term "type designation" may be applied to the original number assigned (without suffix) or to a number with a suffix letter. All procedures described here apply equally well to both the basic type designation and to the suffix letter designation unless otherwise stated (see 2.2.4 and 2.2.5).

2.2.2 Purpose and Intent

The purpose of the type designation and registration system is to facilitate the purchase and distribution of solid state devices by non-technical individuals. The registration procedures are designed to ensure that devices registered with the Council differ from each other in performance characteristics or physical dimensions.

The following is a partial list of the many ways in which the JEDEC registration system is useful to many segments of the electronics industry:

(1) A single number replaces the multiple house numbers that would be used where there are two or more manufacturers of a particular device. This advantage is of particular value to the larger consumer such as the government, because it means in most cases the procurement and supply of a single item, instead of multiple items.

(2) The existence of a nationally recognized designation encourages other manufacturers to make similar devices, thereby increasing and promoting competition.

(3) Types registered under the JEDEC system differ from each other in a significant manner in terms of performance characteristics or physical dimensions.

(4) Types registered under the JEDEC system can be more easily compared because defining characteristics of the specification must be based upon standard test conditions and registered according to standard formats (see 2.2.7).

(5) The publication of registration information through trade channels makes it easier for consumers to obtain second sources of supply.

(6) The specifications of registered devices carrying the authorized designations cannot be changed at will by the first or any subsequent manufacturer, thus promoting standardization and interchangeability.

(7) In many cases it provides a means for non-technical personnel of user procurement, and stock and maintenance operations to obtain the equivalent replacement parts.

(8) It provides a permanent record for future procurement in those cases where the original manufacturers no longer exist or make the type.

(9) It provides an identification system of parts which is of large benefit to the distributors and users of electronic parts. The JEDEC system permits reduction in the required number of parts in inventory.

Registration consists of the assignment of type designations to solid state devices in accordance with established rules, recording of the assignment and defining data, and the full dissemination of the information to the electronics industry.

Registration procedures and rules are established by JEDEC, which is sponsored jointly by EIA and NEMA. In any event, JEDEC neither assumes liability for, nor endorses the use of any products which bear its authorized registration number. The Council has as its primary objective the development of recommended standards in the field of solid state devices. An effective registration procedure is considered basic to the achievement of that objective.

It is the intent of these registration procedures to permit the assignment of discrete semiconductor device type designations not only to single solid state devices but also to combinations of solid state devices such as more than one transistor element, or diode elements and transistor elements within the same primary envelope. In each case, EIA Standard RS-370, "Designation System for Discrete Semiconductor Devices," governs.

2.2.3 Brief Outline of Registration Procedures

For detailed procedures see 2.2.4 and 2.2.5.

2.2.3.1 *Request*

The manufacturer furnishes to the Type Administrator defining data for a device in accordance with the applicable registration format and requests assignment of a type designation.

2.2.3.2 *Assignment*

The Type Administrator assigns a type designation and notifies the manufacturer of the assignment.

2.2.3.3 *Release (Public Announcement)*

Within one hundred and twenty (120) days after date of assignment, the Type Administrator announces the registration of the type by distributing the data to the manufacturers of solid state devices and to users.

2.2.3.4 *Correction Notice and Registration*

Once data on a type has been released, it is possible to change the defining data for that type only by either of two methods: a correction notice or a reregistration. In those cases where an error has been discovered in the data submitted, a correction notice may be filed only by the original sponsor or the Type Administrator within sixty (60) days after registration. Any device manufacturer may, at any time, propose a reregistration to change the registered values for a device. In order for the change to be adopted, however, there must be no opposition to the proposal from any other manufacturer of the device.

2.2.4 Detailed Procedures and Rules Governing Registration of Type Designations without Letter Suffix

2.2.4.1 *Application*

Any manufacturer of solid state devices, whether or not a member of EIA or NEMA, may request a type registration from the Type Administrator for a device the manufacturer is developing or manufacturing. Foreign manufacturers may also request type registrations. All applicants for type registrations will be charged a fee for the service.

The requirement that final registration data be made available to the Type Administrator in order to obtain a type registration makes it necessary for the manufacturer to defer his application until he is almost ready to market the device.

A request for registration must be made in writing by the manufacturer of the device. It must be accompanied by sufficient defining data to show that the device differs from any existing device for which a number has been assigned

by the Type Administrator. The data must be submitted in accordance with the applicable formats developed by the JEDEC Solid State Products Council. See 2.2.7, 2.2.8, and 2.2.9 for rules pertinent to development and use of formats. If these formats are not available, the information must meet the minimum requirements set by the Type Administrator. In any case, the Type Administrator shall be the sole authority for determining the adequacy of data submitted. Any appeal of the Type Administrator's determination shall be made in writing within thirty (30) days, in accordance with the procedures set out in 2.2.6.

Only one outline drawing will be allowed for a single type designation number (JEDEC 2N).

The data submitted shall be a typed original (or equivalent quality) on unfolded 8-1/2" by 11" plain white bond paper (no letterhead) specific instructions for data submission appear with each registration format. The data shall e mailed with suitable protection against creasing or bending. If the material is not received in condition suitable for reproduction, the Type Administrator reserves the right to return it to the sponsor notwithstanding delay and further costs to the sponsor.

Should the Type Administrator receive more than one application for a particular device, he shall assign the designation for the type to the manufacturer having the earliest time of receipt at the office of the Type Administrator. A manufacturer wishing to establish early receipt may make use of a telegram that furnishes adequate information for assignment. The telegram must be followed within fourteen (14) days by a letter supplying the information in the standard form, otherwise the application will be cancelled and the applicant so notified.

Any manufacturer filing subsequent to the first application will be furnished full information on the assignment, and the first manufacturer shall be informed of the disclosure.

2.2.4.2 *Assignment*

Upon receipt of the application for a type registration, the Type Administrator will make a search of existing type registrations to determine whether the applicant's device has sufficiently distinct characteristics to warrant the assignment of a new type designation. In determining discreteness or distinctness, the Type Administrator shall take into account major differences such as, but not limited to, different maximum ratings, new tests, different limits from those that have been applied to existing devices, physical changes, and any other characteristics that differ widely from already registered devices.

If additional data are deemed necessary by the Type Administrator to justify an assignment of a type number, he shall so inform the applicant. If the additional information is not given to the Type Administrator within fourteen (14) days, the applicant shall be notified that the application has been rejected and given reasons therefor.

In case the submitted data closely corresponds with that of a device already assigned a designation by the Type Administrator, the Type Administrator

shall reject the application in writing, giving the reasons therefor and supplying the type designation that is considered applicable. Any appeal of the Type Administrator's determination shall be made in writing within thirty (30) days in accordance with the procedures set out in 2.2.6.

In those cases where the Type Administrator's review indicates that an assignment is in order, the assignment will be recorded and a written notice for the assignment and authorization for use sent to the applicant.

Corrections or changes in the data may be submitted by the original applicant in the period prior to release. Changes are permissible only to the extent that the device characterization is not changed sufficiently to warrant a change in its type designation status. All changes or corrections must be authorized by the Type Administrator prior to their publication in association with a JEDEC type number and must have prior coordination with the other applicants to whom the designations may have been disclosed under the provisions of 2.2.4.1.

Should a manufacturer reverse a type designation and later decide that he will not market the device for which an authorized designation has been assigned and has not sold or publicly disclosed the device using that authorized designation, he may request cancellation of the assignment. The Type Administrator shall acknowledge the cancellation request and make record of the fact, but shall not make further use of the designation.

In making type designation assignments, the Type Administrator shall follow current JEDEC Standards, and the technical formats and guidance rules supplied by the JEDEC Solid State Products Council and its Committees. When all of this information is insufficient to cover a specific case, the Type Administrator may delay the application pending a decision from the appropriate JEDEC Committee. The Type Administrator shall notify the applicant of the delay and reason therefor.

2.2.4.3 *Release (Public Announcement)*

The Type Administrator shall release the registration data to the public as soon as he is authorized to do so by the manufacturer, who in turn does so when he is ready to market the device. If earlier authorization is not received, the Type Administrator shall automatically release the data one hundred and twenty (120) days after date of assignment. A delay may be requested for legitimate cause.

In those cases where a manufacturer publicly discloses data on an authorized type designation before he has requested the Type Administrator to release the data, the Type Administrator shall automatically release the data without waiting for the one hundred and twenty (120) day period to end. The Type Administrator will take such action only in those cases when he has been given conclusive evidence that disclosure has been made by the manufacturer. For purposes of this section, the term "disclosure" is meant to include the disclosure of an unreleased but authorized type designation and its data or use through advertising, general distribution of data sheets, listing of price lists, sampling, or other marketing steps. Disclosure as part of a government

contract for the development of a device is not considered to be disclosure within the meaning of this section.

In the case where an invitation-for-bid has been issued in connection with a government contract for a solid state type that has not been released, the Type Administrator shall use a procedure for effecting registration other than the one described in the preceding paragraph. The recipient of the invitation-for-bid shall supply details concerning the invitation and its source. The Type Administrator will then contact the sponsor of the unreleased type designation, informing him of circumstances which require the immediate release of data on the type.

The registration data is distributed by the Type Administrator to all known manufacturers of solid state devices, as well as to subscription lists of nonmanufacturers of devices. The information sheets making the announcement, which are known as releases, are summarized and listed in appropriate EIA and NEMA publications so that users and designers in all segments of the electronics industry are notified of the existence of the new device.

2.2.4.4 *Correction Notice and Reregistration*

After a type designation has been completely registered, one of the ways in which it is possible to change the defining data is by means of a correction notice. This can be filed only by the original sponsor or the Type Administrator and must be in the hands of the Type Administrator within sixty (60) days after the release date. Correction to registered data after sixty (60) days from date of release must be made through the reregistration procedure.

The correction notice process may be used when it is found that the registered data contains obvious incompatibilities, typographical errors, or ambiguities. The correction notice will be circulated to the same mailing list of those persons receiving the registration information, and it will clearly refer to the particular release involved.

A correction notice does not become effective until sixty (60) days after its release. During this period any manufacturer may object to the notice if he can show that the change is not truly an obvious error, incompatibility, or ambiguity. A single valid objection, if it cannot be reconciled by the Type Administrator with the proponent, will cause the correction notice to be cancelled.

The second way in which the defining data for a registered type may be changed is by means of reregistration. Reregistration may be proposed only by a manufacturer or the appropriate JEDEC Committee. In submitting data, the manufacturer should use the most current approved format. If absolutely necessary, he may use the format which was in effect at the time of registration of the device being reregistered.

A reregistration proposal should be limited to those changes or additions which do not affect unilateral interchangeability with the original version. Any proposed reregistration which, in the opinion of the Type Administrator, will affect unilateral interchangeability shall be rejected by the Type

Administrator. Examples of changes which affect unilateral interchangeability are relaxed package dimensions, relaxed electrical ratings or characteristics, etc. For dimensions and characteristics, increase of a maximum limit or reduction of a minimum limit constitutes a relaxation. For ratings (which imply device capability), reduction of an upper limit or increase of a lower limit constitures a relaxation. Manufacturers who believe unilateral interchangeability will not be affected have the prerogative of appealing the Type Administrator's decision as provided in 2.2.6.

Approved reregistration requests will be processed as follows. The Type Administrator shall distribute the reregistration proposal to the device manufacturers on the mailing list to receive copies of all semiconductor registrations. The reregistration release will instruct manufacturers having valid objections to the proposal to submit their comments in writing (oral comments are not acceptable) to the Type Administrator, so that he may receive them with sixty (60) days from the date of release.

If no written adverse comments to a reregistration proposal are received with the sixty (60) day period, the reregistration proposal becomes effective, superseding the original registration, and the industry shall be so notified by the Type Administrator.

In the event that adverse comments on the proposed registration are received and:

(1) if there is a possibility that the objections may be resolved, the Type Administrator shall issue a "Hold in Abeyance" notice at the end of the sixty day period.

(2) if attempts at reconciliation fail, the reregistration shall be cancelled and a cancellation notice sent to all recipients of the previous information.

(3) if the reconciliation results in a compromise, the previous proposal shall be cancelled and the new proposal submitted again for a sixty day approval by the industry.

(4) if the reconciliation results in the objectors' rescinding their negative comments, the Type Administrator shall issue a notice that the reregistration proposal has been accepted.

In those cases where the Type Administrator has rejected comments because he considers them to be not valid, he shall notify the objector of his action and inform the objector that he has thirty (30) days in which to file an appeal with the Council Secretary who, in turn, will notify the Type Administrator that an appeal has been filed. If no appeal is made within the specified period, the Type Administrator will proceed in accordance with the previous paragraphs.

2.2.5 Detailed Procedures and Rules Governing Registration of Type Designations with Suffix Letters

All of the preceding rules are applicable to the assignment of a type designation which contains a suffix letter, except as amended in the following paragraphs.

The applicability of suffix assignments, as opposed to a new designation, is outlined in EIA Standard RS-370. In general, a suffix designation can be applied to an improved version of an existing type if the improved version is unilaterally interchangeable with the prototype and all prior suffix versions. Exceptions exist for letters R and M; see EIA Standard RS-270.

The request and the accompanying information will not be treated as confidential information and will be circulated for approval to the recipients of solid state device registration releases in the same manner as a reregistration proposal (see 2.2.4.4).

In submitting the data, the manufacturer should use the current format. If absolutely necessary, he may use the format which was used for registration of the last suffix letter version (or the designation without suffix letter if no letter has been previously assigned).

If adverse comments on the assignment of the suffix letter are received by the Type Administrator within the sixty (60) day period, he shall refer the entire matter to the cognizant JEDEC Committee for guidance. When the JEDEC Committee votes on recommendations to be submitted to the Type Administrator, members whose companies are directly involved in the dispute shall be excluded from voting. The Type Administrator, preferably, or his designated alternate shall be present at the meeting when the JEDEC Committee discusses the matter he has referred to them. The Type Administrator shall make the decision on the registration of the suffix letter designation after considering the Committee's recommendations.

The Type Administrator shall inform the cognizant JEDEC Committee and the parties involved of his decision. If no adverse comments are received within thirty (30) days, then the notice of the assignment becomes effective. If adverse comments are received, then a status notice can be issued until all avenues of appeal are exhausted or the case dropped.

2.2.6 Appeal of the Type Administrator's Decisions

Decisions of the Type Administrator are subject to appeal to the JEDEC Solid State Products Council and to an Ad Hoc Arbitration Panel as provided herein. Decisions which may be appealed include those related to suffix letter registrations, correction notices, and reregistration proposals. Decisions on new type designations (that is, no suffix letter designations) may not be appealed although protests may be filed for the purpose of instituting corrective action on future assignments.

The right of appeal shall extend to any member of the industry having a product interest in, and adversely affected by, a decision of the Type Administrator. A notice of intent to appeal shall be sent by registered mail or telegram to the Type Administrator with a copy sent to the Council Secretary. Such notice shall be sent in time to reach the Type Administrator prior to the expiration of a period of thirty (30) days after the date of issuance of the notice of the Type Administrator's action.

Upon receipt of the notice of appeal, the Type Administrator shall immediately inform the manufacturer sponsoring the acting being appealed and the Chairman of the Council. The Type Administrator shall also publish a notice to industry informing them of receipt of the appeal and holding in abeyance the proposed action.

Upon receipt of the Type Administrator's notice, the Council Chairman shall immediately appoint an Appeal Panel of all, but not less than three, disinterested Council members, one to act as Chairman, to convene within twenty (20) days for the purpose of considering the appeal. Council members whose employers are either the sponsor or the appellant of the particular action being appealed may not serve on the Appeal Panel. If a full Appeal Panel cannot be convened from the Council members, the Chairman may appoint JC Committee chairmen or members to serve on the Appeal Panel.

Notices of the date, place, and time of the meeting of the Appeal Panel shall be given to all parties having an interest. Council Secretary shall serve as official recorder. The Appeal Panel shall consider all relevant facts and arguments before rendering a decision. Other pertinent data may be presented and the Appeal Panel shall decide whether the data is pertinent. Any question involving interpretation of procedure or the relevancy of fact or argument shall be referred to JEDEC legal counsel for appropriate ruling.

In the event the appellant is not satisfied with the decision of the Appeal Panel, he shall have the right to have the decision submitted to an Ad Hoc Arbitration Panel consisting of three qualified and disinterested parties. He shall have this right of appeal provided he and the other interested parties in the dispute agree in writing prior to appeal to accept the recommendations of the Ad Hoc Arbitration Panel and to waive any other right to redress. Notice of intent to exercise this right to review shall be made within three (3) working days of the Appeal Panel's decision to the Council Secretary. One member of the Ad Hoc Arbitration Panel shall be selected by the applicant, one member by the Council Chairman, and a third by mutual agreement of both. The Ad Hoc Arbitration Panel shall select one member to act as Chairman and shall hold a meeting to review the decision of the Appeal Panel at the earliest practicable time, but no later than fifteen (15) days after selection of the Panel.

After full consideration of the decision of the Appeal Panel, the Ad Hoc Arbitration Panel shall have the authority to confirm, reject, or modify such decision. The decision of the Ad Hoc Arbitration Panel shall be final.

2.2.7 Description of Registration Format

A format is intended to provide a uniform method of presentation of definition and performance of a JEDEC registered device. The Type Administrator uses the completed format to assure the uniqueness of the device for type assignment purposes. The registrant manufacturer uses the format to completely define a device to the degree which the formulating Committee and Council believe necessary to assure device interchangeability. Other potential manufacturers use the completed format and registration data to facilitate and assure device interchangeability. Solid state device users employ the completed registration data to select, compare, and define devices to achieve intended circuit performance. The format provides for a common language of understanding between supplier and user.

Each format provides for specific values of mechanical and electrical parameters in two categories. One is for mandatory parameters and the Type Administrator will not accept a proposed registration unless every such parameter is provided. The other is for additional parameters which the formulating Committee believes desirable for the further definition of a device intended for a normal application. Additional data not listed in a format is permissible if the registrant manufacturer believes it is necessary to further define the device and to assure interchangeability.

The Type Administrator must receive a properly completed registration format (see 2.2.2) in order to issue a JEDEC type number assignment. In the event an appropriate format has not been prepared by the JEDEC Committees, the Type Administrator, with advice from Council or Committee Chairmen, will determine what shall constitute an interim substitute format. A completed format characterizes a device by listing or referencing all mechanical outline dimensions and terminal identification, all essential electrical performance data and maximum ratings, all necessary test methods, and all appropriate parameter symbols which are believed necessary to assure device interchangeability. Each JEDEC product Committee originates formats for each device category over which it has been assigned responsibility. Each format is approved for circulation and use by the JEDEC Council. JEDEC Committees have the responsibility for maintaining and upgrading the technical content of formats such that they reflect the advancement of the technology of both design and manufacture. Mechanical and electrical parameters are to be listed as minimum, maximum, or rated values required to assure device interchangeability.

2.2.8 Use of a Format and JEDEC Registered Data

The solid state device manufacturer should use the JEDEC data for a registered device as the basis for his commercial data. Since the JEDEC registration data is industry property, each manufacturer who desires to produce and market that device must comply in every respect with the registered data. Commercial data describing that device must identify by asterisks all parameters which appear on the JEDEC registration. If a manufacturer believes it desirable, he may list additional defining data, such as performance curves or quality items, provided such additions do not affect interchangeability.

JEDEC type numbers should be used in the form in which they are assigned. In data presentation and in device marking, the JEDEC number should be kept separate and distinct and not make part of other identifying numbers, if such other numbers are present. Alterations in a JEDEC number should not be made for any purpose such as to indicate special selection, to modify characteristics, or to indicate interchangeability.

Specific examples of past practices which are considered to be in conflict with this policy are illustrated but not limited to the following:

Slash Branding:	JEDEC No./JEDEC No. JEDEC No./House No.
Unauthorized Suffix:	2N6000Z 2N6000-2 2N6000-TO-9 2N6000/TO-9

JEDEC Council reserves all rights to the use of its symbols. The Armed Services make use of JEDEC designations and are permitted to modify these designations by means of prefixes to indicate conformance with military specifications.

2.2.9 Test and Rating Methods Applied to JEDEC Data

Defining data on a format must be supported by sufficient reference or included information to assure an understanding of the test methods used in the measurement and interpretation of data and ratings. It is the responsibility of the formulating JEDEC Committee and Council to define as many of the following test methods, conditions, and other information, as appropriate for the device or format under consideration:

(1) Standard circuits for the measurement of electrical characteristics

(2) Standard circuits for life testing of semiconductor devices

(3) Standard mechanical tests (shock, vibration, etc.)

(4) Standard fixtures and gauges

(5) Standard failure defining criteria

(6) Standard time duration of test when applicable (hours, cycles, pulses, etc.)

(7) Standard definition of allowable number of defective units when absolutely necessary in the establishment of a rating.

There should be no question as to the intention behind, or interpretation of, any parameter or test listed on a format.

2.3 STANDARD VALUES FOR USE IN REGISTRATION

2.3.1 Introduction

This section contains lists of standard values which are recommended for use in power transistor device specifications and JEDEC Registration to JC-25 Formats. Good reasons should exist in those cases where values are used which are not included in these lists.

2.3.2 Standard Values for Ratings

(1) Voltage

(a) for $\leq$ 300 V: Rounded 13 series,[+]
(b) for > 300 V: increments of fifty volts.

(2) Current: Rounded 13 series.[+]

(3) Temperature: -273*, -250*, -200*, -175*, -150*, -125*, -100*, -65*, -55*, -40*, -25*, -10, 0*, +25*, +40, +55*, +70*, +85*, +100*, +110, +125*, +150*, +175*, +200*, +230, +250*, +300*, +350*, +400* °C. The temperatures indicated by an asterisk are preferred for use in new documents.

(4) Power: Rounded 13 series.[+]

2.3.3 Standard Values for Characteristics

(1) Gain (lower limit).

(a) for < 10: steps of 0.5
(b) for $\geq$ 10: Rounded 13 series[+]

(2) Gain (upper limit): Rounded 13 series[+]

(3) Frequency: Rounded 13 series.[+]

(4) Capacitance: Rounded 13 series.[+]

(5) Time, switching: Rounded 13 series.[+]

(6) Current, cutoff: Rounded 13 series.[+]

(7) Voltage, saturation: Rounded 13 series.[+]

[+] 1.0, 1.2, 1.5, 1.7, 2.0, 2.5, 3.0, 3.5, 4.0, 5.0, 6.0, 7.0, 8.0, $X10^n$; where n is an integral number.

2.4 MINIMUM DIFFERENCE STANDARD VALUES FOR DISCRETENESS OF REGISTRATION

2.4.1 Introduction

This section provides lists of minimum differences in ratings and characteristics that are recommended for use in determining if a transistor proposed for registration is descrete from those already registered.

Discreteness of any one rating or characteristic listed below on the basis of the minimum difference indicated is sufficient for transistor discreteness, provided that rating or characteristic is required by the registration format. Changes in ratings and characteristics not required in the registration format are not criteria for discreteness.

Most of the minimum differences indicated are given in terms of standard steps. A standard step refers to the steps in the series of standard values listed in section 2.3.

2.4.2 Minimum Differences for Ratings

(1) Voltage, collector-to-emitter (V_{CEO}, V_{CER}, V_{CES}, V_{CEX}): one standard step.

(2) Current, continuous collector (I_C): two standard steps.

(3) Power, continuous (P_T), and peak (P_{TM}):

(a) for $\leq$ 150 W: two standard steps,
(b) for $>$ 150 W: one standard step.

(4) Temperature, operating junction (T_J), and storage (T_{stg}): two standard steps.

2.4.3 Minimum Differences for Characteristics

(1) Current gain: dc (h_{FE}) and small-signal (h_{fe})

(a) for increase or decrease of both upper and lower limits: one standard step,
(b) for change in either upper or lower limit: two standard steps.

(2) Transition frequency (f_T), magnitude of small-signal current gain ($|h_{fe}|$), and output capacitance (C_{obo}): two standard steps each.

(3) Voltage, saturation ($V_{CE(sat)}$): three standard steps.

(4) Current, cutoff (I_{CEO}, I_{EBO}, I_{CBO}, I_{CEV}, I_{EB1}): two orders of magnitude.

(5) Time, storage (t_s): two standard steps.

PART 3

VERIFICATION TESTS

3.1 Maximum Ratings

PART 3

VERIFICATION TESTS

CONTENTS

PART 3

VERIFICATION TESTS

3.1 MAXIMUM RATINGS

3.1.1 Introduction

This section describes tests which are intended to verify the maximum ratings given in transistor registration formats; they are not tests for developing the maximum ratings nor are they for establishing performance or quality levels.

An npn transistor is shown as the transistor under test in the test circuits. These test methods will also apply to pnp devices by appropriate polarity changes in the test circuit elements. All circuit values specified in this section are nominal and should be maintained within equipment capabilities and good engineering practice. Also, suitable precautions should be taken against transient voltage spikes and oscillations.

Unless specified otherwise, the transistor case temperature should be maintained at approximately 25°C by use of an appropriate heat sink, when necessary.

3.1.2 Verification Criteria

To verify a given maximum rating for a transistor, the transistor shall be tested as described in the applicable subsection. This transistor shall still be capable of meeting all the electrical characteristics of the registration at the conclusion of the test procedure, after the transistor has been allowed to reach thermal equilibrium at 25°C.

3.1.3 Storage Temperature, Minimum - T_{stg} min.

3.1.3.1 *Test Conditions*

(1) Storage temperature at rated T_{stg} min.

(2) Test duration of six (6) hours at the rated T_{stg} min.

3.1.3.2 *Procedure*

The device under test is placed in a temperature-controlled enclosure either before or after the temperature in the enclosure has reached T_{stg} min.

3.1.4 Storage Temperature, Maximum - T_{stg} max.

3.1.4.1 *Test Conditions*

(1) Storage temperature at rated T_{stg} max.

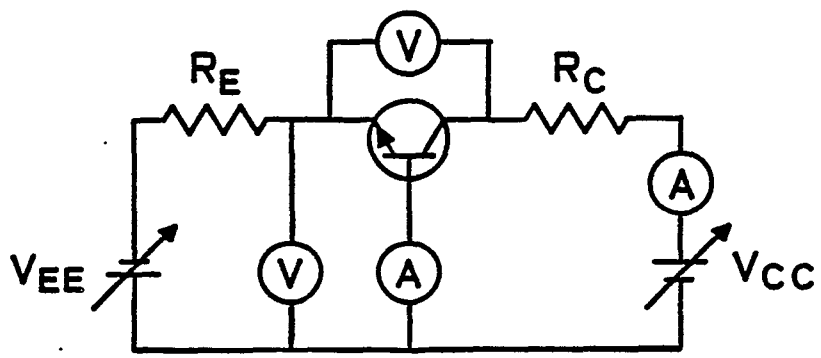
(2) Test duration of six (6) hours at the rated T_{stg} max.

3.1.4.2 *Procedure*

The device under test is placed in a temperature-controlled enclosure either before or after the temperature in the enclosure has reached T_{stg} max.

3.1.5 Junction Temperature, Maximum Operating - T_J (max.)

3.1.5.1 *Test Circuit and Conditions*



(1) $V_{CC} \sim 2V_{CE}$, $V_{EE} \sim 5V_{EB}$

(2) V_{CE} and the total power dissipation, P_T, must be specified. [Note that $P_T = V_{EB} \cdot I_B + V_{CE} \cdot I_C$.]

(3) The duration of the test shall be five (5) minutes, measured after thermal equilibrium is reached.

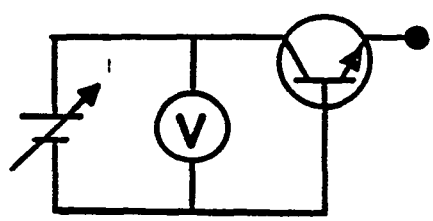
3.1.5.2 *Procedure*

Adjust the bias conditions to achieve the specified V_{CE} and P_T. In doing so, do not exceed the rated maximum values for I_B and V_{CEO} of the device. The case temperature, T_C, and P_T must be such that the junction temperature is equal to the maximum rated operating junction temperature calculated by:

$$T_J = T_C + \frac{P_T}{\text{Derating Factor (W/°C)}}.$$

3.1.6 Collector-to-Base Voltage, Maximum - V_{CBO}

3.1.6.1 *Test Circuit and Condition*



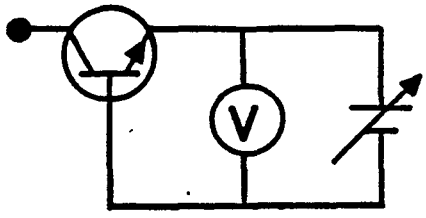
The duration of the test shall be one (1) minute.

3.1.6.2 *Procedure*

Adjust the bias supply to attain the specified V_{CBO}.

3.1.7 Emitter-to-Base Voltage, Maximum - V_{EBO}

3.1.7.1 *Test Circuit and Condition*



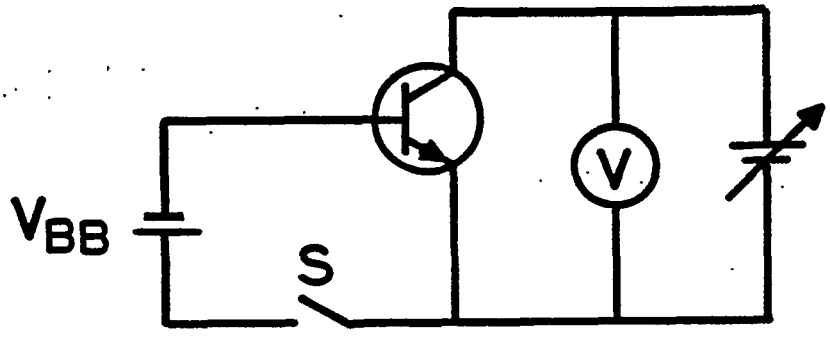
The duration of the test shall be one (1) minute.

3.1.7.2 *Procedure*

Adjust the bias supply to obtain the specified V_{EBO}.

3.1.8 Collector-to-Emitter Voltage, Maximum - V_{CEO}, V_{CEV}

3.1.8.1 *Test Circuit and Conditions*



(a) To verify the V_{CEO} rating, switch S is open; to verify the V_{CEV} rating, switch S is closed.
(b) V_{BB}, must be specified, if used.
(c) The duration of the test shall be one (1) minute.

3.1.8.2 *Procedure*

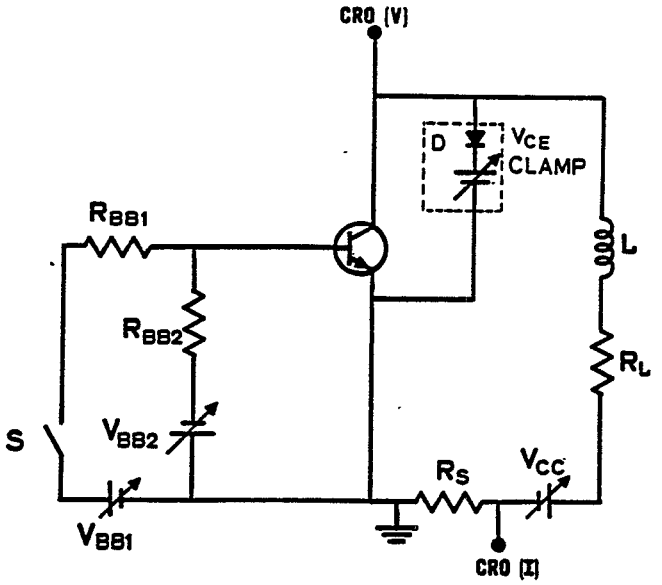
Adjust the bias supply to attain the specified rating voltage.

3.1.9 Collector-to-Emitter Sustaining Voltages, Maximum - $V_{CEX(sus)}$, $V_{CER(sus)}$, $V_{CEO(sus)}$

3.1.9 1 *Test Circuits and Conditions*

Either the inductive or the pulsed collector method may be used.

(1) Inductive Method



(a) The values of all circuit elements used must be specified. To verify the $V_{CER(sus)}$ rating, V_{BB2} is zero; to verify the $V_{CEO(sus)}$ rating, the reverse base drive circuit elements (R_{BB2} and V_{BB2}) are removed; and to verify the $V_{CEX(sus)}$ rating, R_{BB2} may be zero. The use of the V_{CE}-clamp is optional; however, if it is used, the characteristics or the registered type number of D, must be specified.

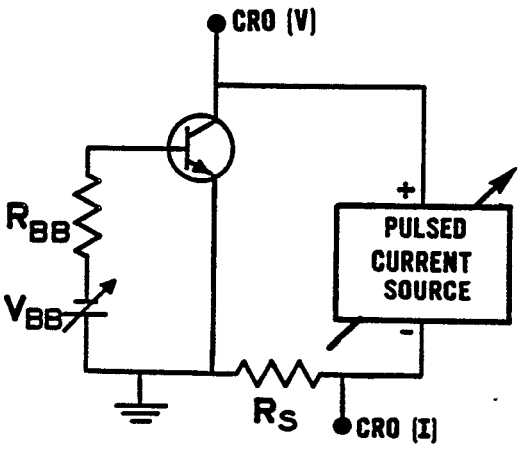
(b) $R_S \leq V_{CC}/(20\ I_C)$

(c) The collector current at the maximum rated value of V_{CE} must be specified.

(d) The on-off cycling rate (pulse repetition rate) of switch S must be specified.

(e) The test duration shall be long enough to make the readings of V_{CE} and I_C.

(2) Pulsed Collector Method



(a) The values of all circuit elements must be specified. To verify the $V_{CER(sus)}$ rating, V_{BB} is zero; to verify the $V_{CEO(sus)}$ rating, the reverse base drive circuit elements (R_{BB} and V_{BB}) are removed; and to verify the $V_{CEX(sus)}$ rating, R_{BB} may be zero.

(b) The collector current at the maximum rated value of V_{CE} must be specified.

(c) The pulse width and duty cycle of the collector current source must be specified.

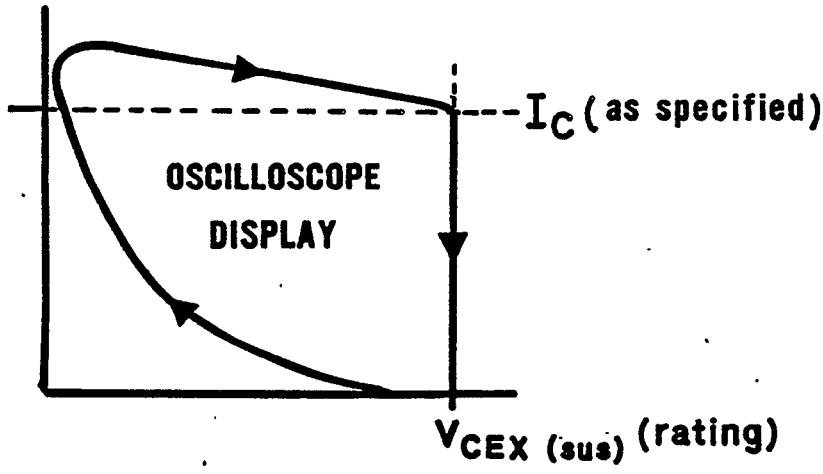
(d) The test duration shall be long enough to make the readings of V_{CE} and I_C.

3.1.9 2 *Procedures*

(1) Inductive Method

(a) Adjust the bias supplies to the specified test values.

(b) Increase the pulse width by increasing the time that switch S is closed, until the intersection of the specified collector current and V_{CE} rating is reached (see following illustration).

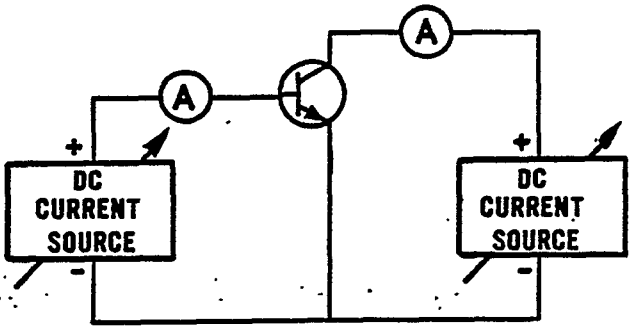


(2) Pulsed Collector Method

Adjust I_C to the specified value.

3.1.10 Collector Current, Maximum Continuous - I_C

3.1.10.1 *Test Circuit and Conditions*



(1) The base current, I_B, must be specified.

(2) Duration of the test at the rated value for I_C shall be five (5) minutes.

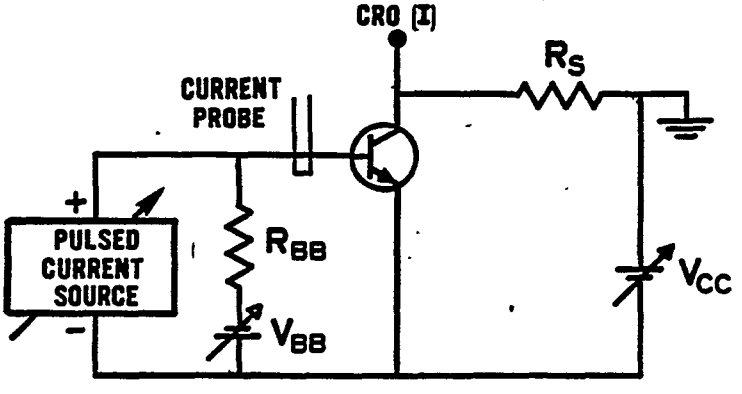
3.1.10.2 *Procedure*

(1) Increase the base drive to obtain the specified I_B.

(2) Increase the collector drive until the rated I_C is reached.

3.1.11 Collector Current, Maximum Pulsed - I_{CM}

3.1.11.1 *Test Circuit and Conditions*



(1) The amplitude, pulse width, and duty cycle of the pulsed current source shall be specified.

(2) V_{BB} and R_{BB} may be required to insure proper device turn-off.

(3) $R_S = V_{CC} / I_{CM}$

(4) The duration of the test shall be that time adequate to make the reading.

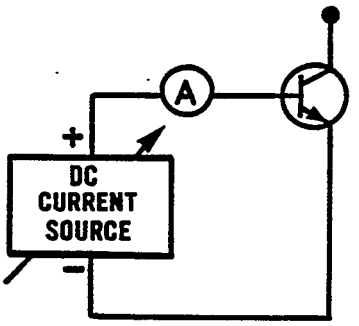
3.1.11.2 *Procedure*

(1) Adjust the pulse generator to obtain the specified drive pulse.

(2) Adjust V_{CC} to obtain the rated I_{CM}.

3.1.12 Base Current, Maximum Continuous - I_B

3.1.12.1 *Test Circuit and Condition*



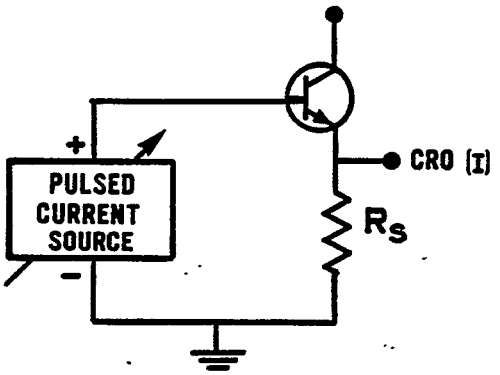
Duration of the test at the rated value for I_B shall be five (5) minutes.

3.1.12.2 *Procedure*

Adjust the current source to obtain the rated I_B.

3.1.13 Base Current, Maximum Pulsed - I_{BM}

3.1.13.1 *Test Circuit and Conditions*



(1) The amplitude, pulse width, and duty cycle shall be specified.

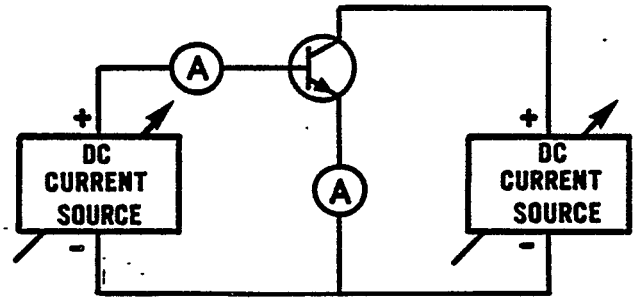
(2) The duration of the test shall be that time adequate to make the reading.

3.1.13.2 *Procedure*

Adjust the pulsed current source to obtain the rated I_{BM}.

3.1.14 Emitter Current, Maximum Continuous - I_E.

3.1.14.1 *Test Circuit and Conditions*



(1) The base current must be specified.

(2) The duration of the test shall be five (5) minutes.

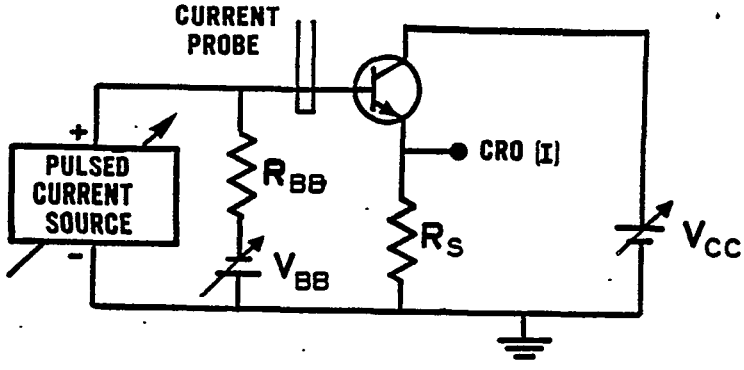
3.1.14.2 *Procedure*

(1) Increase the base drive to obtain the specified I_B.

(2) Increase the collector drive to obtain the rated I_E.

3.1.15 Emitter Current, Maximum Pulsed - I_{EM}

3.1.15.1 *Test Circuit and Conditions*



(1) The amplitude, pulse width, and duty cycle of the base drive pulse shall be specified.

(2) V_{BB} and R_{BB} may be required to insure proper device turn-off.

(3) $R_S = V_{CC}/I_{CM}$

(4) The duration of test shall be that time adequate to make the reading.

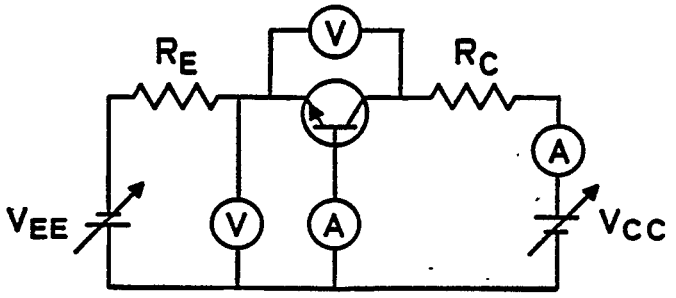
3.1.15.2 *Procedure*

(1) Adjust the pulse generator to obtain the specified drive pulse.

(2) Adjust V_{CC} to obtain the rated I_{EM}.

3.1.16 Power Dissipation, Maximum Continuous - P_T

3.1.16.1 *Test Circuit and Conditions*



(1) V_{CE} must be specified.

(2) The case temperature, T_C, must be 55°C for all devices rated for operating junction temperatures of 125°C or less, and 100°C for all devices rated for operating junction temperatures above 125°C.

(3) The duration of the test shall be five (5) minutes, measured after thermal equilibrium at the required case temperature is reached.

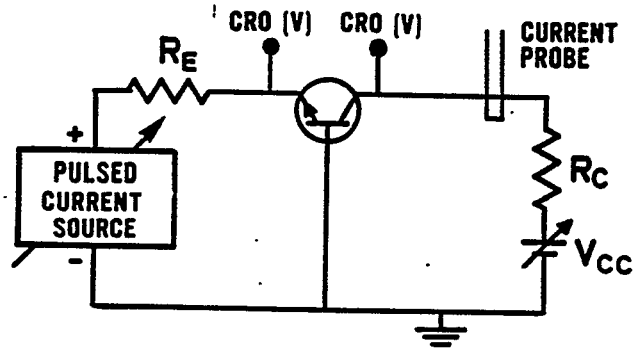
3.1.16.2 *Procedure*

Adjust the bias conditions to achieve the specified V_{CE} and P_T. Do not exceed the maximum I_B or V_{CEO}. The temperature and power dissipation must be such that the junction temperature, T_J, is equal to the maximum operating junction temperature calculated by:

$$T_J = T_C + \frac{P_T}{\text{Derating Factor (W/°C)}}$$

3.1.17 Power Dissipation, Maximum Peak - P_{TM}

3.1.17.1 *Test Circuit and Conditions*



(1) V_{CE} must be specified.

(2) The pulse width and duty cycle of the pulse generator shall be specified.

(3) The duration of test shall be that time adequate to make the reading.

3.1.17.2 *Procedure*

Increase the amplitude of the pulse generator to obtain the rated P_{TM} at the specified V_{CE}.

PART 3

VERIFICATION TESTS

3.2 Safe Operating Conditions

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3.2 SAFE OPERATING CONDITIONS

PART 3.2

3.2 SAFE OPERATING CONDITIONS FOR POWER TRANSISTORS

3.2.1 Introduction

The maximum safe operating condition specifications are developed and guaranteed by the manufacturer. To assist the user in verifying these conditions (not developing them), a verification test circuit, test conditions, and test procedures are provided in the section for four operating modes.

The *verification criterion* for these specifications is that, after successfully completing the test procedures and after cooling to room temperature, the transistor must be capable of meeting the registered characteristics and ratings. However, significant differences between the values obtained for the electrical characteristics before and after the test should be cause for concern.

The maximum safe operating conditions of a transistor depend in a complex way on I_C, V_{CE}, I_B, T_C, and t_p; and on the mode of operation. The majority of transistor applications can be reduced to one or more of the following four modes:

(1) Continuous forward-biased operation and pulsed forward-biased operation

(2) Switching between conduction and cutoff with an unclamped inductive load

(3) Switching between conduction and cutoff with a resistive load

(4) Switching between conduction and cutoff with a clamped inductive load.

The method of specifying these conditions is to define areas within which the transistor may be operated safely. For modes (1), (2), and (3), these conditions are defined in terms of areas on a plane whose coordinates are V_{CE} and I_C. These areas may therefore be considered to be superimposed on the transistor's common emitter output characteristics. For purposes of clarity, a transistor output characteristic is shown in Fig. 1 with the various regions and parts of the characteristic labeled. For operating mode (4), the maximum safe operating conditions are defined in terms of an area on a plane whose coordinates are the peak collector current switched and the load inductance.

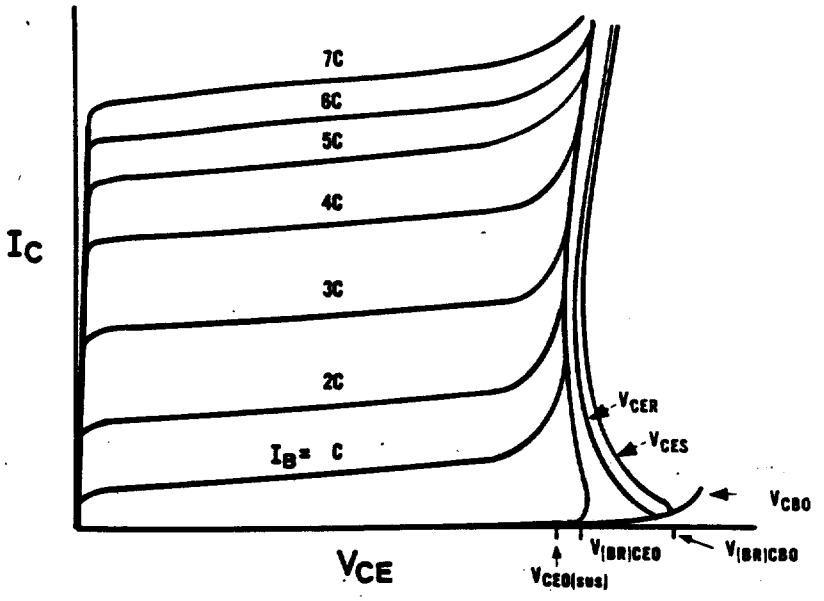


Figure 1 - Schematic drawing of the common-emitter output characteristic family of a transistor for constant forward-base-current drive. Characteristic curves are shown for multiples of constant forward base current, I_B = C, for the base open circuited (V_{CEO}), for the base connected to the emitter terminal via a resistor (V_{CER}), and the base terminal short circuited to the emitter terminal (V_{CES}). The collector-base reverse-bias characteristic V_{CBO}, is also shown. The V_{CEO}, V_{CER}, V_{CES}, and the V_{CBO} versus I_C characteristic curves appear to be superimposed along the voltage axis because of the current range used. The currents to which the negative resistance regions of these curves extend are exaggerated. The level of $V_{CEO(sus)}$ shown, is determined by the region of the V_{CEO} characteristic at relatively high collector current where V_{CEO} is essentially independent of I_C. The levels of $V_{(BR)CEO}$ and $V_{(BR)CBO}$ shown, are determined by the current levels at which these breakdown voltages are to be measured.

3.2.2 Safe Operating Areas for Continuous and Pulsed Forward Biased Operations

3.2.2.1 *Introduction*

Safe operating conditions for forward biased operation may be given as areas such as shown in Fig. 2 where logarithmic coordinate scales are used for the V_{CE} and I_C axes. Representative safe operating areas are shown for continuous operation and pulsed operations for three pulse widths:

t_{p1}, t_{p2}, and t_{p3}; in order of decreasing duration.

For convenience of discussion, the area for continuous operation is divided into three regions. Comments regarding the high power boundaries of these three regions apply also to the equivalent boundaries for the pulsed safe operating areas. Region I is the current-limited region, defined by a maximum collector current line to a specific collector-to-emitter voltage, V_{CE1}. This maximum current corresponds to the maximum collector current rating for the device. See 3.1.9 and 3.1.10 for verification tests of maximum continuous and pulsed current ratings. Region II is the power-limited region. It is bounded by a constant power line (with slope of -1) and is connected at one end to the maximum current line, and at the other end to the lower voltage end of the third region. Region III is a second breakdown or "voltage-limited" region and is bounded by a line with a slope steeper than that of Region II. The slope and extent of this line is determined empirically and is characteristic of a given device design. The usual practice for silicon transistors is to terminate the line at $V_{CE} = V_{CEO(sus)}$.

The safe operating areas shown in Fig. 2 can be transferred to the transistor collector output characteristics of Fig. 1 in order to show their approximate relationship. See Fig. 3 for an example.

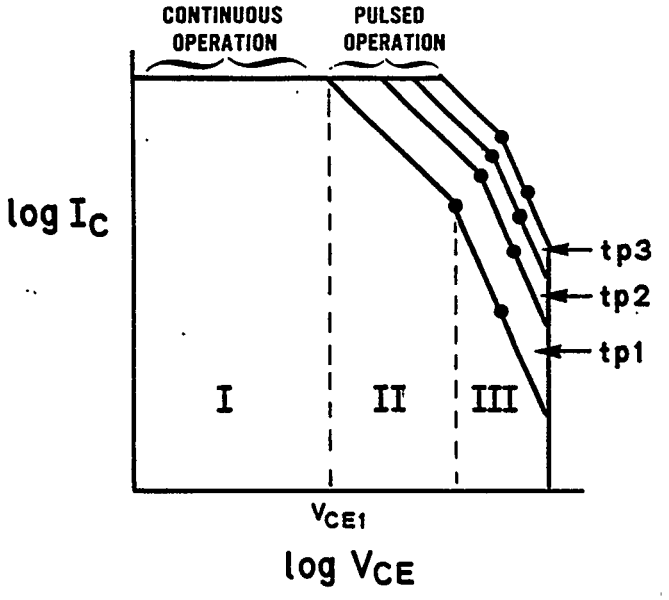


Figure 2 - Typical safe operating areas for continuous and for pulsed forward biased operations. The area for continuous operation is divided into three regions: the current limited (I), the power limited (II), and the second breakdown or voltage limited (III) regions. The pulsed operations are for pulse widths t_{p1}, t_{p2}, and t_{p3}; in order of decreasing duration. The large dots indicate suggested test points for the continuous and pulsed areas in region III.

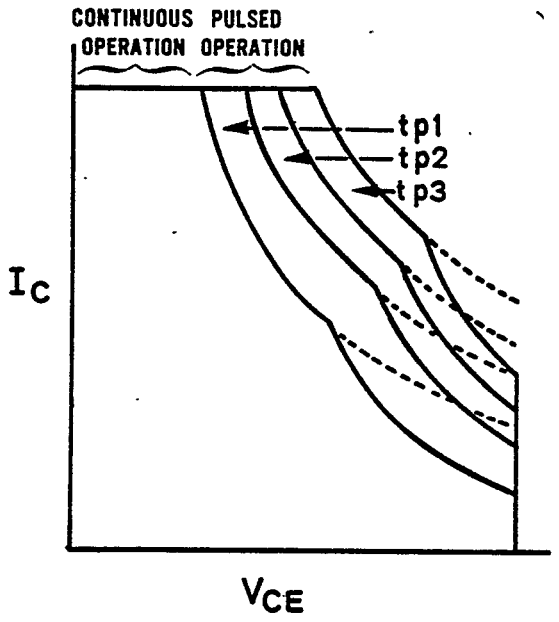


Figure 3. Safe operating area limits from Fig. 2 translated onto common-emitter output characteristic family. Dashed lines indicate extensions of constant power loci.

3.2.2.2 *Verification of Maximum Operating Conditions*

The safe operating areas for continuous and pulsed operation may be verified by tests at two points on the boundary of the second breakdown limited region: at the lowest voltage and at mid-voltage between the lowest and highest voltage of this region (indicated by large dots in Fig. 2), or at the points specified by the registration format.

The temperature-stable, common-base circuit shown in Fig. 4 is recommended for performing the verification tests. However, a common emitter configuration can also be used to verify these safe operating conditions.

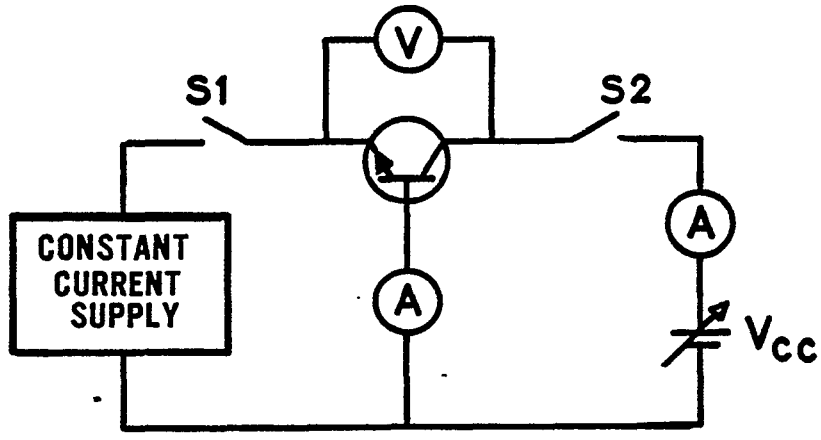


Figure 4 - Test circuit for verifying safe operating areas. Note that switches S1 and S2 are normally closed.

3.2.2.3 *Verification Test Sequence*

(1) With a representative transistor connected in the test circuit of Fig. 4 and fastened to a heat sink sufficient to maintain the case temperatures at the specified level during the test, adjust the circuit parameters as follows:
   (a) With V_{CC} much less than V_{CE} of the test point, adjust the emitter current supply so that I_C is increased to the value of the test-point current. Open switch S1.
   (b) Increase V_{CC} to the V_{CE} of the test point. (Note that $V_{CE} = V_{CB} + V_{BE}$.) Open switch S2.
   (c) Remove representative transistor.

(2) Install the transistor under test in the test circuit and fasten to the heat sink.

(3) Close switch S2.

(4) Close switch S1 for the specified test period. The rise and fall times of the collector current must each be less than one-tenth the test period.

(5) A collapse of V_{CE} is indicative of a failure. In some devices, I_B may also decrease significantly just prior to the collapse of V_{CE}.

(6) Open switch S2.

Note: The time between successive tests of a single transistor must be sufficiently long to allow the junction temperature of the transistor to return to the specified case temperature.

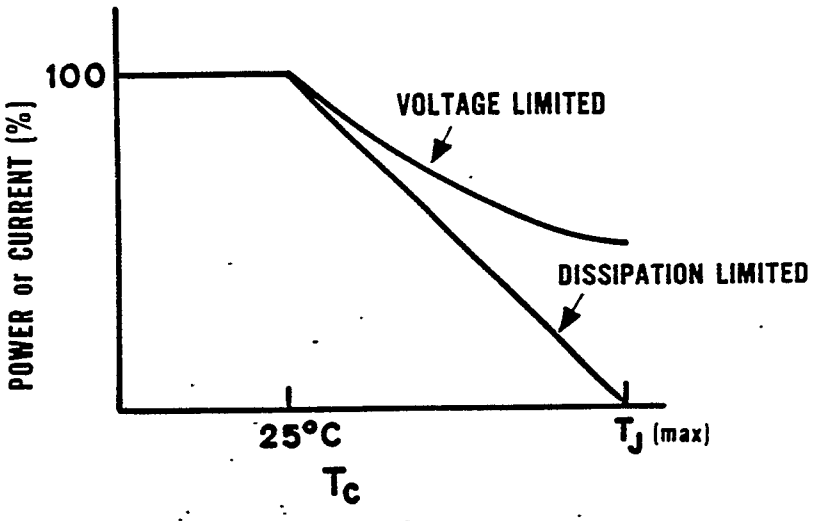


Figure 5 - Curves for temperature derating of collector current for a fixed collector-to-emitter voltage.

3.2.2.4 *Temperature Derating*

The temperature derating should be specified for each region of the rating curve (see Fig. 2). The standard linear derating which applies to Region II will, in most cases, be unduly conservative when applied to Region III. A separate derating curve is developed for Region III by empirical means. One such derating scheme is shown in Fig. 5 and its use is outlined below:

(1) For a given pulse duration and collector-to-emitter voltage, determine from Fig. 2 the maximum collector current allowed at 25°C. Use the constant power lines or their extensions, if necessary.

(2) Having previously calculated the case temperature from known steady-state power and heat sink conditions, refer to the temperature derating curve of Fig. 5. Using the *Dissipation Limited* curve, determine the percent current derating needed from the value of the collector current obtained in step 1.

(3) If the collector-to-emitter voltage condition of step 1 required the use of an extension of the *Dissipation Limited* line, repeat step 1 using the corresponding *Voltage Limited* line of Fig. 2.

(4) Repeat step 2, using now the *Voltage Limited* derating line of Fig. 5.

(5) The maximum allowable current is the smaller of the two values obtained in steps 2 and 4.

For repetitive pulse operation, an "effective" case temperature is used in the temperature derating curves, which is the sum of the maximum ambient temperature, the rise in case temperature, and the rise in junction temperature resulting from the average transistor power dissipation, P_{AVG}. The effective case temperature, $T_{C(EFF)}$ may be calculated by using the following relationships:

$$T_{C(EFF)} = T_A + P_{AVG} R_{\theta CA} + P_{AVG} R_{\theta JC},$$

$$T_{C(EFF)} = T_C + P_{AVG} R_{\theta JC}.$$

3.2.3 Safe Operating Areas for Switching Between Conduction and Cutoff with an Unclamped Inductive Load

3.2.3.1 *Introduction*

Applications exist which necessitate transistor switching between conduction and cutoff with an unclamped inductive load. If the circuit inductance is sufficiently high, the transistor may be driven into the sustaining region where its energy dissipation capability is much lower than in the forward biased region. The specification of safe operating conditions for these applications is different from that for forward base drive operation in that the former is tailored to the character of a specific circuit, of which the test circuit in Fig. 6 is representative.

The maximum safe operating conditions for switching between conduction and cutoff may be shown as areas on a graph of peak collector current versus load inductance as illustrated in Fig. 7. Switching operations are safe if the point determined by the inductance and collector current switched lies in the area bounded by the curve for the specific base drive conditions used. This area is frequently referred to as the reverse-bias safe operating area (RBSOA). If the transistor is to be operated at duty cycles or at case temperatures which are significantly different from those specified, or if the circuit conditions are different, it is advisable to consult the vendor on the possible extrapolation of the specification to particular application needs.

When a forward base drive is applied to the transistor under test (TUT) in the circuit of Fig. 6, by switching on transistor Q, the collector current increases at a rate which is controlled essentially by the inductance and the current-limiting resistance. The critical part of the switching cycle with respect to transistor safety is switching from conduction to cutoff. With the application of a reverse base drive, the collector current will decrease, inducing a back EMF in the inductor and increasing the collector-to-emitter voltage to V_{CEX}. This is indicated by the waveforms in Fig. 6. During the time, (t_2-t_1), in which the collector current decreases linearly with time to its cutoff value, the transistor must dissipate an energy, E, that is equal to the energy stored by the inductor, plus that supplied by the battery during (t_2-t_1), minus the energy dissipated in the current-limiting resistor during (t_2-t_1). Using the notation in Fig. 6 and assuming an immediate rise in V_{CE} to V_{CEX} at I_{CPK}, and a relatively constant value for V_{CEX} with I_C during the discharge time, then

$$E = (1/2)LI_{CPK}^2 + (1/2)V_{CC}\ I_{CPK}(t_2-t_1) - (1/3)R_T\ I_{CPK}^2(t_2-t_1).$$

To eliminate (t_2-t_1) from the above expression the relation $E = (1/2)V_{CEX}\ I_{CPK}(t_2-t_1)$ is used to obtain:

$$E = \frac{3\ LI_{CPK}^2\ V_{CEX}}{6\ (V_{CEX} - V_{CC}) + 4R_T\ I_{CPK}}, \text{ where } R_T = R_L + R_S.$$

In order to make the dependence of E on V_{CEX} negligible, the battery voltage, V_{CC}, and the resistance, R_T, must be reduced sufficiently. In this case, to a good approximation,

$$E = (1/2)LI_{CPK}^2 \qquad (1)$$

It is this value of energy that the maximum safe operating area specification implies the transistor can dissipate in the sustaining region. This energy is determined empirically and is found to be also dependent on the reverse base drive parameters and the junction temperature. This energy is shown in some technical data as $E_{s/b}$ (energy above which second breakdown may occur). When the collector supply voltage cannot be reduced sufficiently, an effective inductance, $L_{(EFF)}$ is used in eq.1 rather than the actual induc-

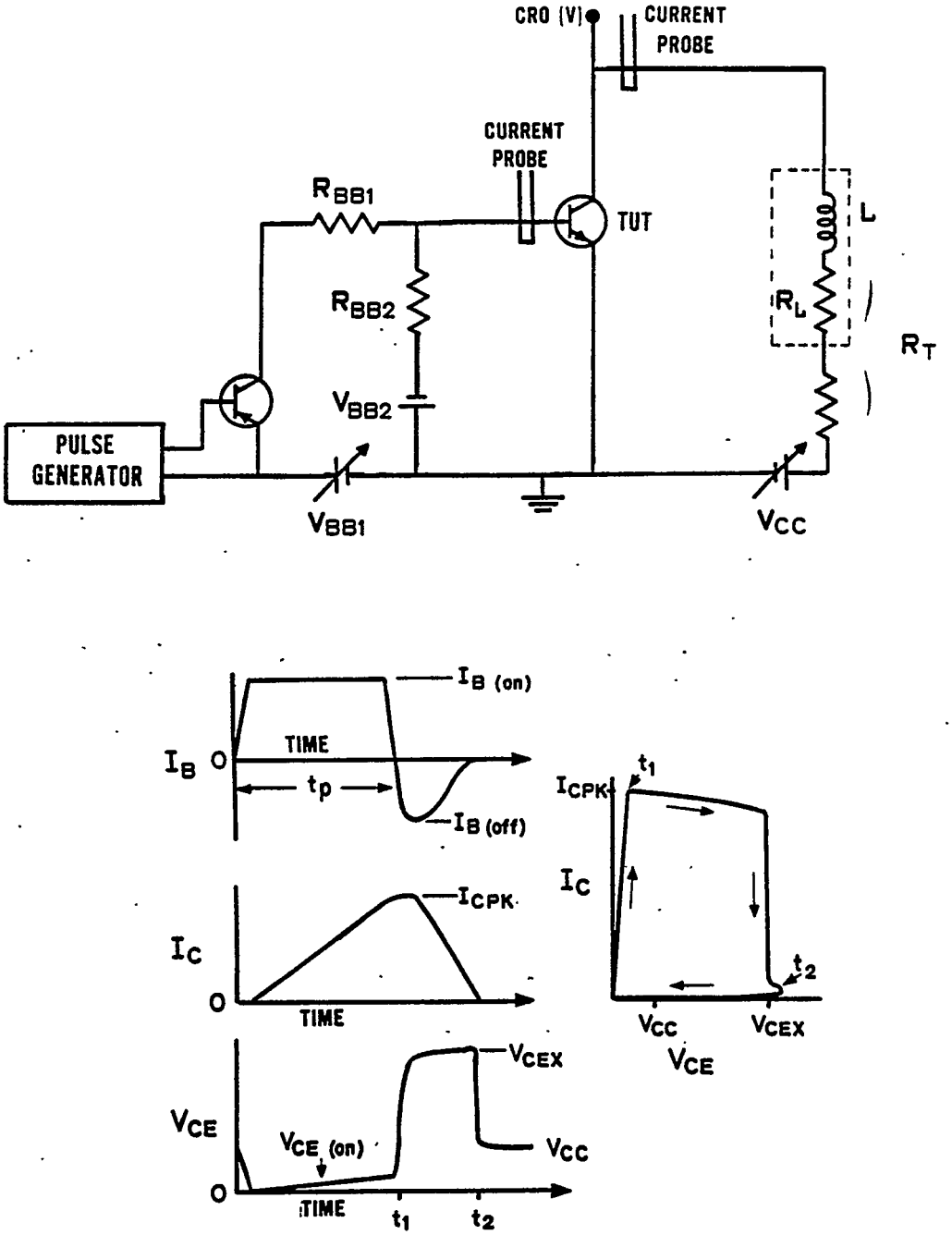


Figure 6. Suggested test circuit for verifying specifications of safe operating areas for switching between conduction and cutoff with an unclamped inductive load, and waveforms while switching.

tance, where

$$L_{(EFF)} = \left(\frac{V_{CEX}}{V_{CEX} - V_{CC}} \right) L$$

The effective inductance takes into account the energy stored in the actual inductor and that which is supplied by the voltage supply used. The effective inductance is used in the safe operating area specification such as illustrated in Fig. 7 to obtain the maximum collector current that can be switched for the cutoff conditions given when V_{CC} is not negligible in comparison with V_{CEX}.

3.2.3.2 *Verification of Maximum Operating Conditions*

The test circuit shown in Fig. 6 may be used to verify the maximum operating conditions. The test point should be selected near the high-inductance, low-collector current end of the curve, or where specified by the manufacturer (see Fig. 7). The following conditions should be specified: case temperature, total circuit resistance and inductance, V_{BB2}, R_{BB2}, I_{CPK}, and $I_{B(on)}$.

When designing and operating the test circuit, the following precautions should be taken:

(1) V_{CC} should be kept as low as possible in order to minimize the uncalculated energy contributed by the supply. To prevent the supply from contributing more than about 10 percent of $(1/2)LI_{CPK}^2$, $V_{CC} \leq 0.1\ V_{CEX}$.

(2) Duty cycle should be kept low and an adequate heat sink should be used to minimize any heating effects and to maintain the specified case temperature of the transistor under test.

(3) Switching time of the base drive waveform should be considerably less than the rise (t_r) or fall time (t_f) of the transistor under test (generally no more than 10 percent). See Fig. 6.

(4) Inductor should be designed so that the inductance is relatively independent of DC load current. Generally, an air coil is used; however, high quality molybdenum permalloy toroids can be used when large inductance is required. The self resonant frequency of the inductor should be equal to or greater than 20 times the f_{hfe} of the transistor under test. The resistive and core losses of the inductor should be small in comparison to the stored energy, generally, $Q \geq 100$ @ 20 kHz. Departure from these criteria will reduce the energy absorbed and should be taken into account.

(5) If the transistor is not to operate in saturation prior to switching, a maximum value of $V_{CE(on)}$ must be specified.

3.2.3.3 *Verification Test Sequence*

(1) Ensure that R_{BB2}, L, and V_{BB2} are at specified values before transistor under test is inserted.

(2) Adjust base drive until specified $I_{B(on)}$ is attained.

(3) Increase V_{CC} and t_p until I_C reaches the test value.
Note: In the event I_{CPK} cannot be obtained when V_{CC} reaches 0.1 V_{CEX}, I_C may be increased by lengthening the pulse width (t_p). The time between the successive pulses must be sufficiently long to allow T_J to return to T_C.

(4) Observe the I_C and V_{CE} waveforms. The transistor should be rejected if the collector-emitter voltage collapses or oscillates during the collector current fall time.

(5) Decrease V_{CC} to zero, before removing transistor under test.

(6) Device failure may be readily detected by a $V_{CEO(SUS)}$ test.

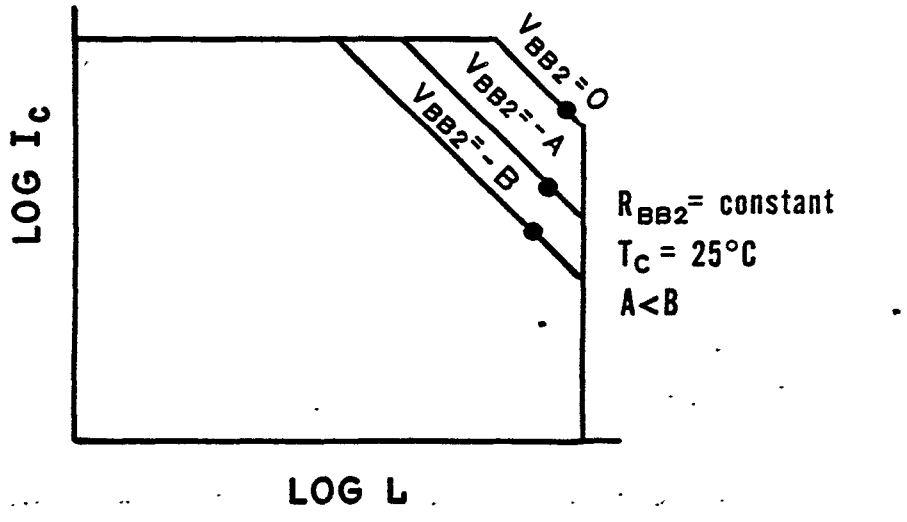


Figure 7. Representative safe operating areas for switching between conduction and cutoff conditions with an unclamped inductive load, L, with circuit shown in Fig. 6 for different reverse base drive conditions. Large dots indicate general region of test points for verifying the safe operating area specifications.

3.2.4 Safe Operating Conditions for Switching from Conduction to Cutoff with a Resistive Load

3.2.4.1 *Introduction*

The maximum safe operating conditions for switching a transistor with a resistive load from conduction to cutoff may be shown by a triangular area on the V_{CE} - I_C plane. Such an area is shown in Fig. 8 where the triangular area is defined by the V_{CE} and I_C axes and the load line for switching from the maximum value for I_C at saturation, I_1, to the maximum value for V_{CE} at cutoff, V_1. Switching operations are safe if the load line lies completely on the triangular area and if switching is performed with the specified reverse base drive at the case temperature and at or below the duty cycle specified.

Instead of providing a drawing of a triangular area, only the maximum value for I_C at saturation and the maximum value for V_{CE} at cutoff may be specified. Safe switching operations are those for which the values of I_C at saturation and V_{CE} at cutoff are less than or equal to the respective maximum values specified.

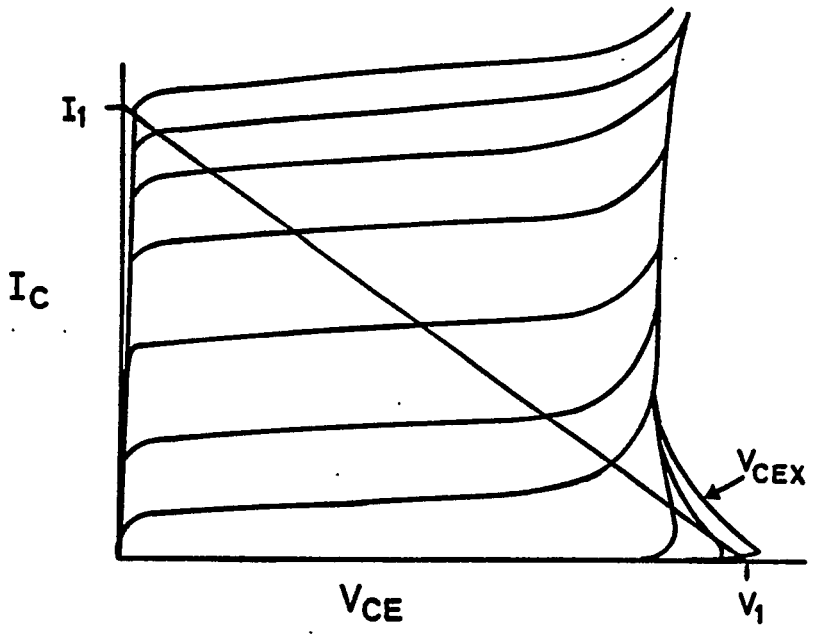


Figure 8. The maximum safe operating conditions for switching from conduction to cutoff with a resistive load, as denoted by a triangular area superimposed on a common-emitter output characteristic family. The output characteristic for the reverse base drive specified for safe operation is indicated by V_{CEX}.

Superimposing the triangular area on the common-emitter output characteristics of the transistor in Fig. 8 is intended to show that the load line, defined by V_1 and I_1, is located under the negative resistance region of the output characteristic for the reverse base drive specified. The load line must not intersect this negative resistive region, otherwise the transistor may not be able to switch from a conducting to a cutoff condition. It should be pointed out that the location and extent of the negative-resistance region may be significant functions of temperature, depending on device design and construction.

If the transistor is to be operated at duty cycles and at case temperatures significantly different from those specified, the operating conditions that are specified may not be safe.

The specification of a maximum safe operating area for switching a transistor with a resistive load from saturation to cutoff is redundant if the maximum safe operating conditions for continuous forward bias or pulsed forward bias operations are specified which enclose the triangular area and if the switching time along the resistive load line is less than the pulse width specified.

3.2.4.2 *Verification of Maximum Operating Conditions*

Verification of the maximum safe switching operation drawn in Fig. 8 is accomplished by switching along the resistive load line with slope V_1/I_1 first from the cutoff condition at $V_{CE} = V_1$ to saturation at $I_C = I_1$ and then back to the cutoff condition at $V_{CE} = V_1$. A suggested test circuit is shown in Fig. 9 and the test procedure using this circuit is dis-

cussed in 3.2.4.3. The maximum base current needed to switch the transistor under test (TUT) into saturation at $I_C = I_1$ as well as the values for R_{BB2} and V_{BB2} must be specified. The rise and fall time of the forward base-drive current pulse shall be less than the specified switching time of the TUT. The duration of this pulse shall be at least ten times the sum of the rise, storage, and fall times of the TUT.

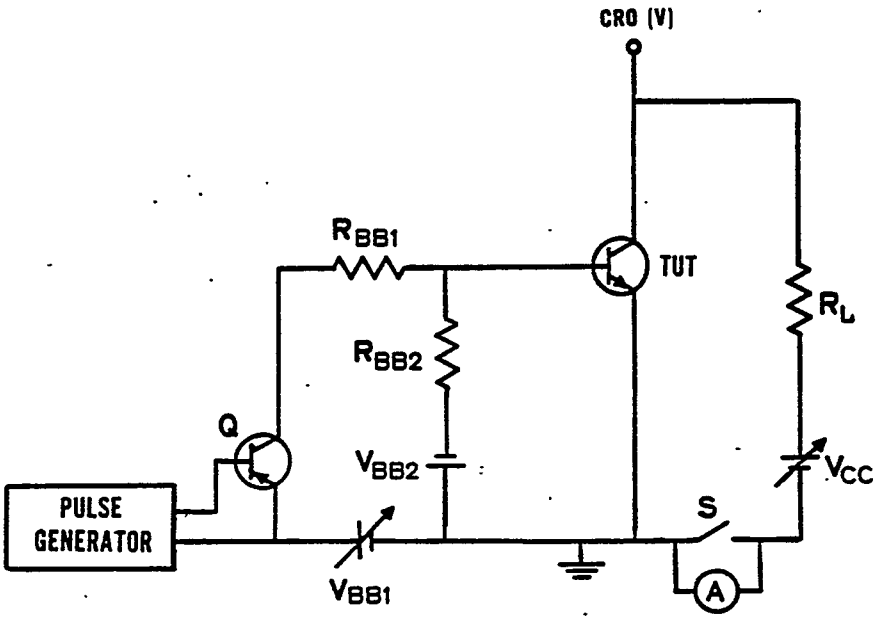


Figure 9. Suggested test circuit for verifying safe operating conditions for switching between conduction and cutoff with a resistive load.

3.2.4.3 *Verification Test Sequence*

(1) Adjust V_{CC} to V_1.

(2) Measure I_C with current meter to determine if transistor under test (TUT) is in the cutoff condition (i.e., $I_C < I_{CEO}$).

(3) Close switch S to shunt the current meter.

(4) Adjust V_{BB1} so that the required forward base current will be applied to the TUT when transistor Q is switched on.

(5) Apply single pulses of increasing duration to transistor Q until $I_C = I_1$ during the pulse. The time between successive pulses shall be such that the average junction temperature will not rise with the application of successive pulses.

(6) V_{CE} must return to V_1 after each pulse as may be determined from an oscilloscopic measurement.

(7) After the last pulse has been applied, open switch S and measure I_C. The TUT must be in a cutoff condition (i.e., $I_C < I_{CEO}$).

3.2.5 Safe Operating Conditions for Switching Between Conduction and Cutoff with a Voltage Clamped Inductive Load

3.2.5.1 *Introduction*

As with switching with an unclamped inductive load, described in 3.2.3.1, the critical part of switching a clamped inductive load with respect to transistor safety is switching from a conduction to a cutoff condition. The same test circuit is used as in 3.2.3 except that a voltage clamping network is added to prevent the induced emf of the inductor from increasing the V_{CE} of the switching transistor above a clamp voltage, V_Z. The clamp voltage must be less than $V_{CEX(sus)}$ of the transistor, for the turnoff base drive condition used, otherwise the circuit will operate as if the inductive load were unclamped.

The switching capability of a transistor is determined empirically by the manufacturer and is found to be dependent not only on the collector current switched, I_{CPK}, and on V_Z, but also on the turnoff base drive conditions, the case temperature, and the duty cycle.

The maximum safe operating conditions for a transistor may be given as an area in a plot of the collector current that may be switched off versus the clamp voltage, or it may be given in terms of the energy that the transistor may dissipate during the turn-off process. The latter specification is generally less practical to verify because of the need to integrate the power during the turn-off time for each transistor tested.

In this section, means for verifying the safe operating conditions for switching from conduction to cutoff are described for three methods of clamping an inductive load.

(1) V_Z Clamp Method

In this method, a clamping network consisting of a clamping diode in series with a power supply is connected in parallel with the emitter and collector terminals of the transistor under test (TUT), as shown in Fig 10. The clamp voltage is equal to the breakdown voltage of the diode minus the voltage of the power supply.

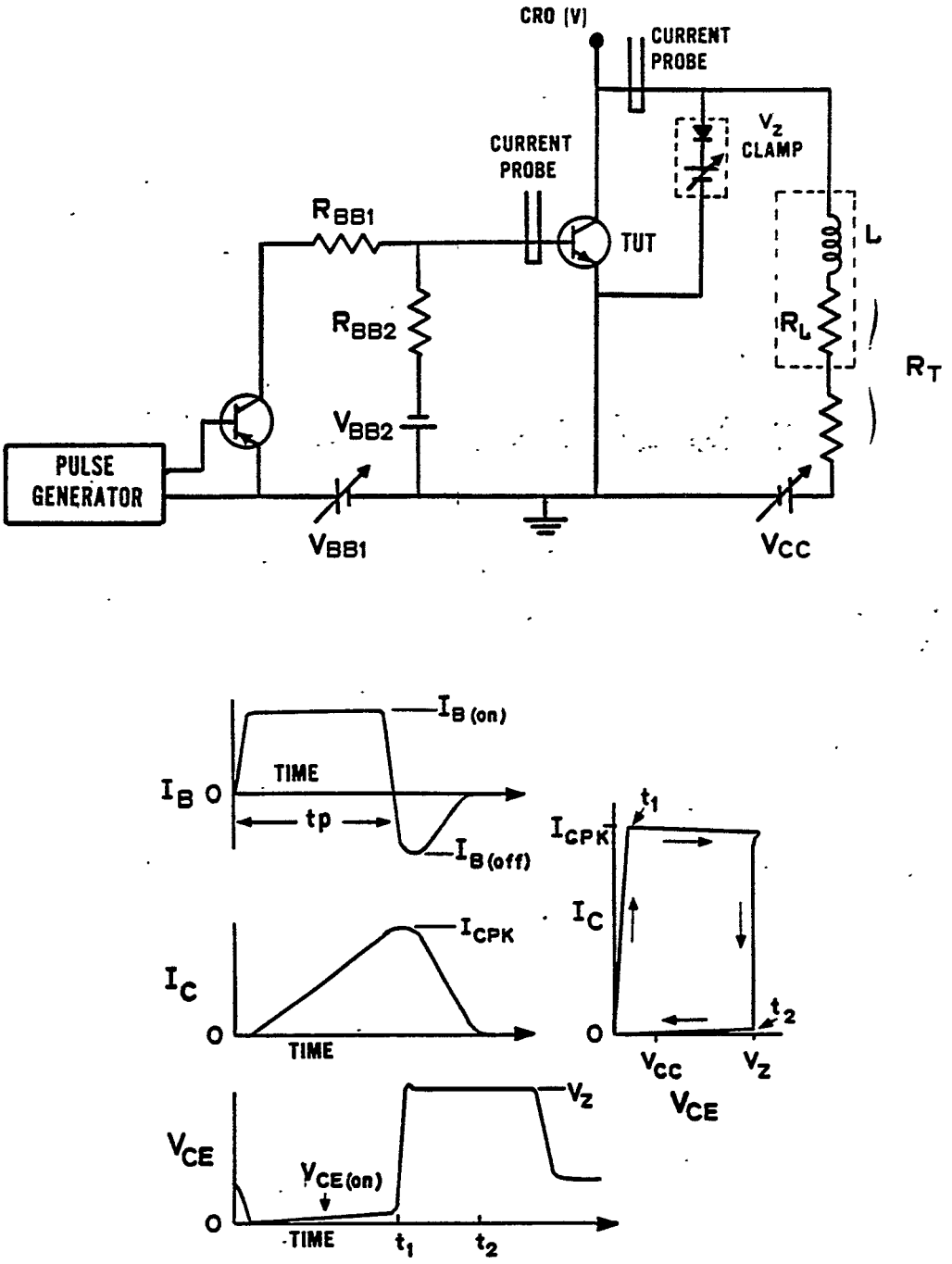


Figure 10. Suggested circuit for verifying safe operating conditions for switching between conduction and cutoff with a V_Z clamped inductive load, and waveforms during switching.

The energy that the TUT must dissipate, E_{TUT}, is dependent on the magnitud of V_{CE} and I_C during the turn-off time (from t_1 to t_2, as shown in Fig 10). This turn-off or collector-current fall time will vary with each transistor and will be dependent on the case temperature and on the values chosen for R_{BB2} and V_{BB2}. The magnitude of E_{TUT} can be determined by evaluating the integral in

$$E_{TUT} = \int_{t_1}^{t_2} I_C V_{CE}\, dt. \qquad (1)$$

The energy that the TUT dissipates will be considerably less than the energy stored by the inductor. The bulk of the energy that must be dissipated while switching from a forward conduction to a cutoff condition is dissipated by the clamping network and any series resistance in the circuit.

(2) V_{CC} Clamp Method

In this method a clamping diode is connected in parallel with the collector terminal of the TUT and the positive terminal of the V_{CC} supply, as shown in Fig 11, so that the diode will conduct and thereby shunt any emf from the inductor. The clamp voltage is essentially equal to the value of V_{CC}.

The magnitude of E_{TUT} can be determined by evaluating the integral in eq. 1. Also, as in the preceding method, the energy that the TUT must dissipate will be considerably less than the energy stored by the inductor during conduction.

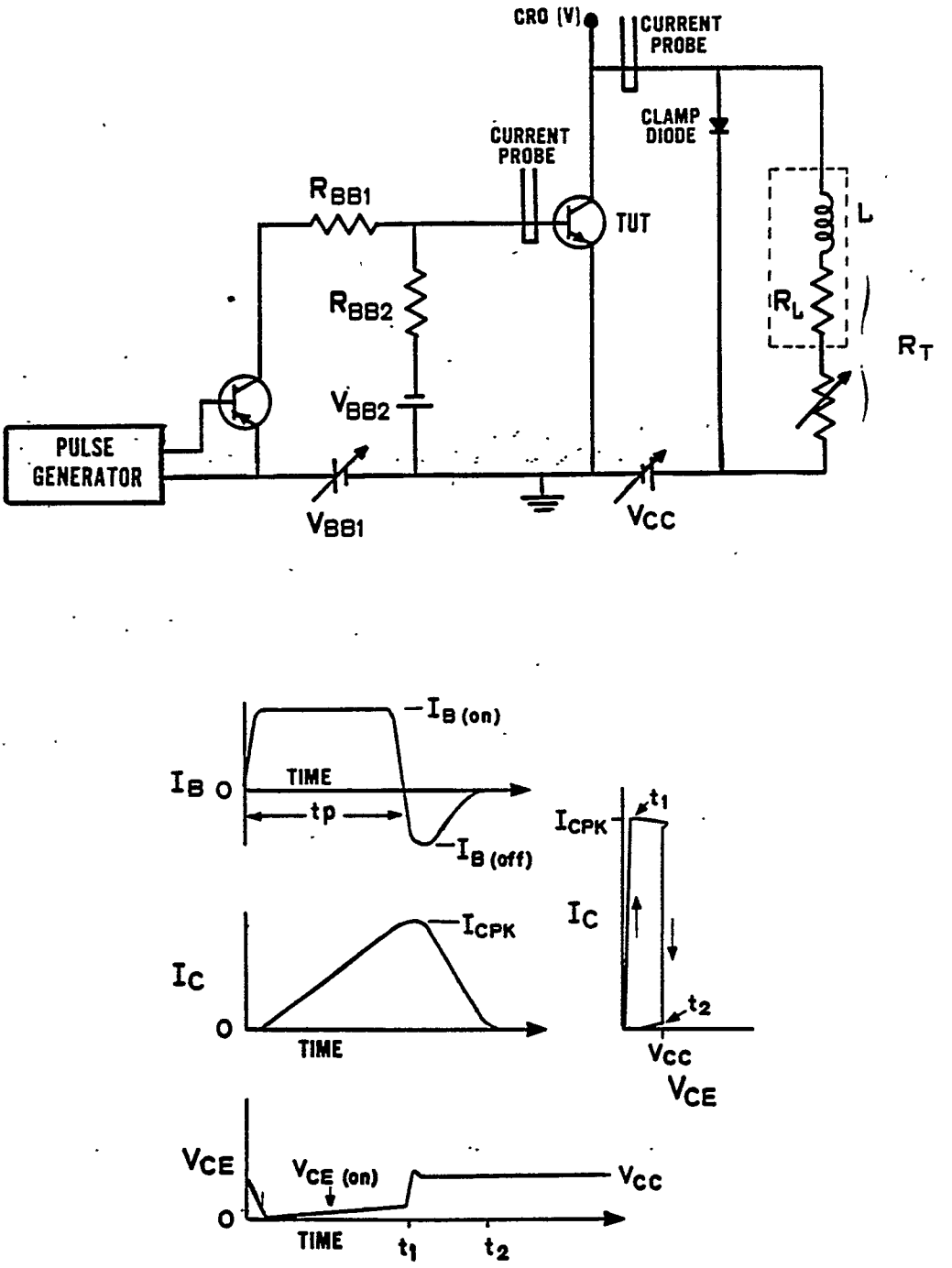


Figure 11. Suggested circuit for verifying safe operating conditions for switching between conduction and cutoff with a V_{CC} clamped inductive load, and waveforms during switching.

(3) V_{CB} Clamp Method

In this method a clamping network consisting of a clamping diode in series with a power supply is connected in parallel with the base and collector terminals of the TUT, as shown in Fig 12. The clamping voltage will be equal to the breakdown voltage of the diode minus the voltage of the power supply. When V_{CE} reaches V_Z, the clamping network will conduct and supply a forward base drive to the TUT so that it operates in a forward bias conduction mode. The TUT *and* the clamping network must dissipate an energy, E, equal to the energy stored by the inductor, plus that supplied by the V_{CC} supply during the turnoff time (from t_1 to t_2), minus the energy dissipated by the current limiting resistor. This energy may be calculated by

$$E = \frac{3\ LI_{CPK}^2\ V_Z}{6(V_Z - V_{CC}) + 4\ R_T\ I_{CPK}}$$

If V_{CC} is small compared to V_Z and the circuit resistance is sufficiently small, then E may be calculated using

$$E = (1/2)\ LI_{CPK}^2.$$

In any of these methods, if the transistor is to be operated at duty cycles, temperatures, and/or conditions of reverse bias significantly different from those specified, it is advisable to consult the transistor manufacturer on possible extrapolation or interpolation of the specification to the application needs of the user.

3.2.5.2 *Verification of Maximum Operating Conditions*

The appropriate test circuit shown in Figs. 10, 11, or 12 may be used to verify the maximum operating conditions, according to which clamping method is used. The following circuit parameters and conditions must be specified for all methods: R_{BB2}, V_{BB2}, $V_{CE(on)}$max, V_Z, I_{CPK}, case temperature, pulse width, and duty cycle. When the V_{CB} clamp method is used the following characteristics of the inductor must be specified: L, Q, and the self resonant frequency.

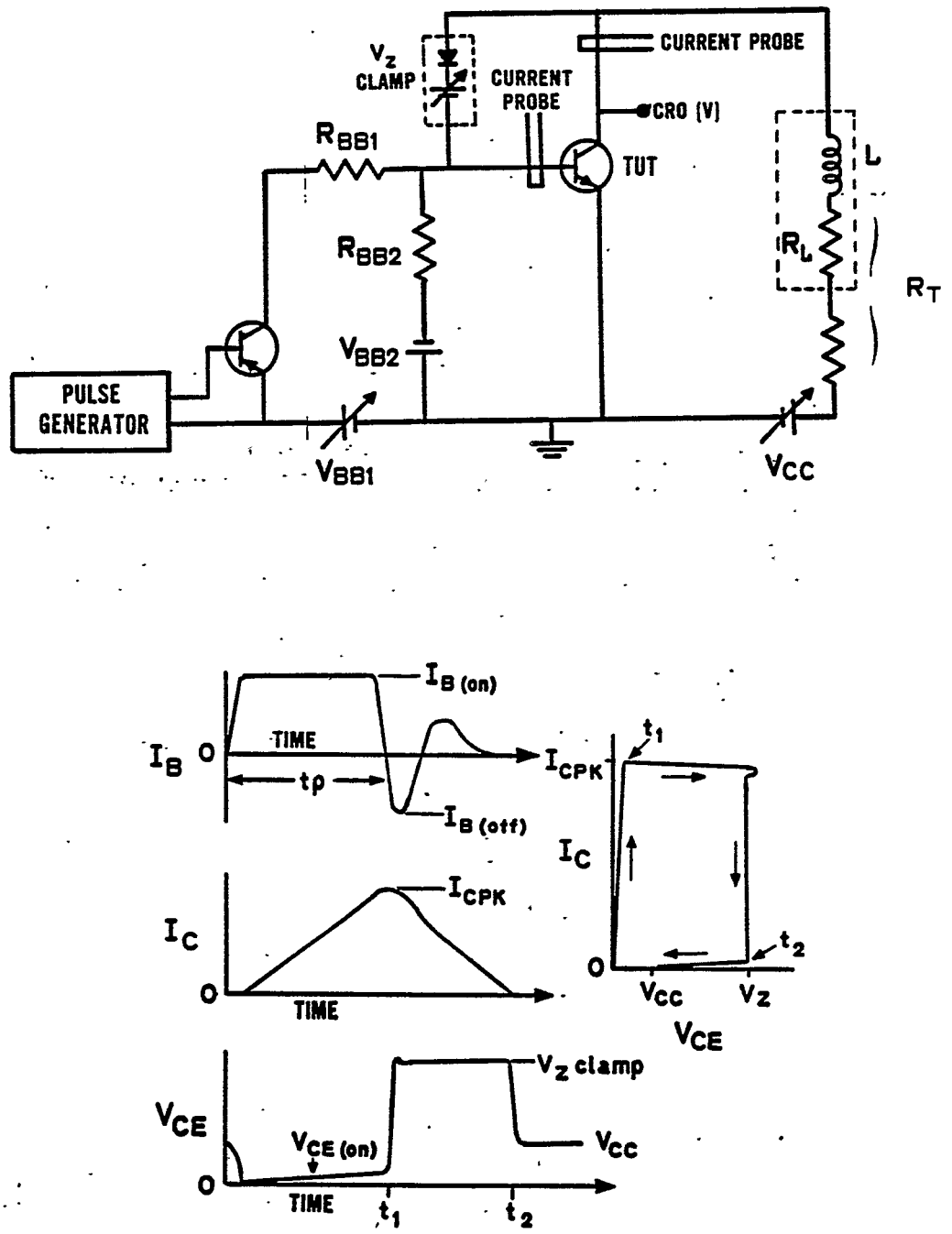


Figure 12. Suggested circuit for verifying safe operating conditions for switching between conduction and cutoff with a V_{CB} clamped inductive load, and waveforms during switching.

When designing and operating the test circuits, the following precautions should be taken:

(1) For the V_{CB} clamp method, V_{CC} should be kept as small as possible in order to minimize the uncalculated energy contributed by the V_{CC} supply. V_{CC} should not exceed 0.1 V_Z to prevent the supply from contributing more than about 10% of $(1/2)LI^2_{CPK}$.

(2) The dynamic impedance of the clamp circuit should be low enough to prevent any significant increase in V_Z during the time it is absorbing energy from the inductive load. The time required for the clamp to become active once V_Z is reached should be such that any voltage overshoot that occurs should not exceed .05 V_Z.

(3) The total circuit resistance, R_T, should be chosen so that the maximum rated collector current (I_{CM}) cannot be exceeded for large-duration forward base drive pulses. Namely,

$$R_T \geq \frac{V_{CC(max)} - V_{CE(on)}}{I_{CM}},$$

Where I_{CM} is the maximum collector current rating of the TUT.

(4) The switching time of the base drive waveform should be considerably less than the rise time (t_r) or fall time (t_f) of the TUT (generally no more than 10%).

(5) The minimum pulse width of the base drive waveform must be at least 10 times the sum of the turn-on and turn-off switching times of the TUT, i.e. t_p min $\geq 10\ (t_{on} + t_{off})$.

(6) The duty cycle should be kept low and an adequate heat sink should be used to minimize any effects due to heating and to maintain the case temperature specified for the TUT.

(7) The V_{CC} clamp circuit requires a constant-voltage, current-limited power supply in order to limit the value of current through the inductor during the ON time of the pulse.

(8) The inductor should be designed so that the inductance is relatively independent of DC load current. Generally, an air coil is used; however, high quality molybdenum permalloy toroids can be used for higher values of inductance.

(a) For V_Z and V_{CC} clamped circuits (Fig. 10 and Fig. 11) the inductance should be sufficiently large to ensure that $I_C \geq 0.9\ I_{CPK}$ when

V_{CE} reaches the clamp voltage. However, for the V_{CB} clamped circuit (Fig. 12) the inductance will be chosen such that the energy stored in the inductor, $1/2\ LI^2$, is approximately equal to the energy rating of the TUT,

(b) The self resonant frequency of the inductor should be equal to or greater than 20 times the f_{hfe} of the TUT.

(c) The resistive and core losses of the inductor should be small in comparison to the stored energy; generally, $Q \geq 100$ @ 20 kHz. Departure from this criterion will reduce the energy absorbed and should be taken into account.

3.2.5.3 *Verification Test Sequence*

(1) Ensure that R_{BB1}, R_{BB2}, R_T, and L are at specified values before TUT is installed in the test circuit.

(2) Adjust the pulse generator for the specified values of pulse width and duty cycle.

(3) Insert the TUT into the test fixture. Note: Heatsinking will be required if the power dissipation and the duty cycle are such that the case temperature will otherwise increase significantly.

(4) For the circuits of Fig. 10 and Fig. 12:

(a) Adjust the clamp voltage to V_Z.

(b) Adjust the output of the pulse generator and the values of V_{BB1} and V_{CC} until the specified I_{CPK} is obtained. V_{CC} should not exceed $0.1\ V_Z$. At I_{CPK}, V_{BB1} must be adjusted to drive the $V_{CE(on)}$ of the TUT to a value equal to or less than the specified maximum $V_{CE(on)}$. In the event that I_{CPK} is not reached when $V_{CC} = 0.1V_Z$ and $V_{CE(on)} = V_{CE(on)max}$, I_C may be increased by lengthening the pulse width (t_p). Adjustment of the off time must then be made to maintain the specified duty cycle.

(5) For the V_{CC} clamp method indicated in Fig. 11:

(a) Adjust V_{CC} to the specified value.

(b) Adjust the output of the pulse generator and the values of V_{BB1} and the current limit on the power supply until the specified I_{CPK} is obtained. V_{BB1} must be adjusted to decrease $V_{CE(on)}$ of the TUT to a value equal to or less than the specified maximum $V_{CE(on)}$.

(6) Observe the I_C and V_{CE} waveform. The transistor should be rejected

if the collector-emitter voltage collapses or oscillates during the collector current fall time.

(7) Decrease first V_{CC} and then V_Z to zero.

(8) Device failure may be readily detected by a V_{CEO} or a $V_{CEO(sus)}$ test.

PART 3

VERIFICATION TESTS

3.3 Electrical Characteristic Tests

Page

3.3 ELECTRICAL CHARACTERISTIC TESTS

3.3 ELECTRICAL CHARACTERISTIC TESTS

3.3.1 Introduction

Accepted test practices are described here as a guide to making power transistor characteristic tests. Only those electrical characteristics included in JC-25 registration formats are included.

All measurements should be made at thermal equilibrium. A condition of thermal equilibrium is achieved if halving the time between application of power and measurement causes no change in the result within the required accuracy.

The inclusion of the following tests does not imply that they all must be performed by either the manufacturer or the user. It is the responsibility of the user and manufacturer to agree to any series of specific tests or test conditions, and the further responsibility of the user to establish meaningful relationship between these tests and the performance of the power transistor in a particular application.

In 3.3.2 and 3.3.3 the device under test and the connections to them are shown separate from the remainder of the test circuit for the following test techniques: for dc operation (D.C.); for curve-tracer operation, using a 60 Hz full-wave rectified sinewave (C.T.); and for pulsed operation using 300-μs duration pulses at a 2% duty cycle (P).

An npn transistor is used as the transistor under test in the test methods below. These test methods will also apply to pnp devices by appropriate polarity changes in the circuit elements.

For small-signal measurements, a signal is used which, when doubled in magnitude, does not produce a change in parameter that is greater than the required accuracy.

In the circuit diagrams shown, certain assumptions are made. Connections between circuit elements have negligible resistance in comparison with their lowest terminating impedance. Resistors, inductors, and capacitors are considered to have an ideal characteristic in the frequency range used. Voltage sources have zero impedance, and current sources have infinite resistance. All voltmeters and oscilloscopes have infinite input resistance and all ammeters have zero resistance, unless otherwise noted.

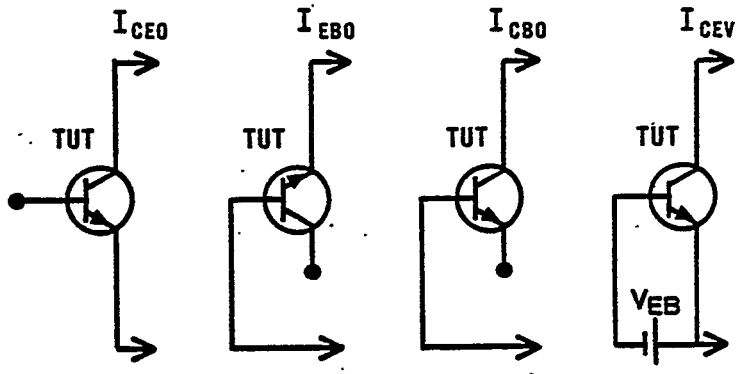
3.3.2 Cutoff Current [I_{CEO}; I_{EBO}; I_{CBO}; I_{CEV}; I_{EB1}]

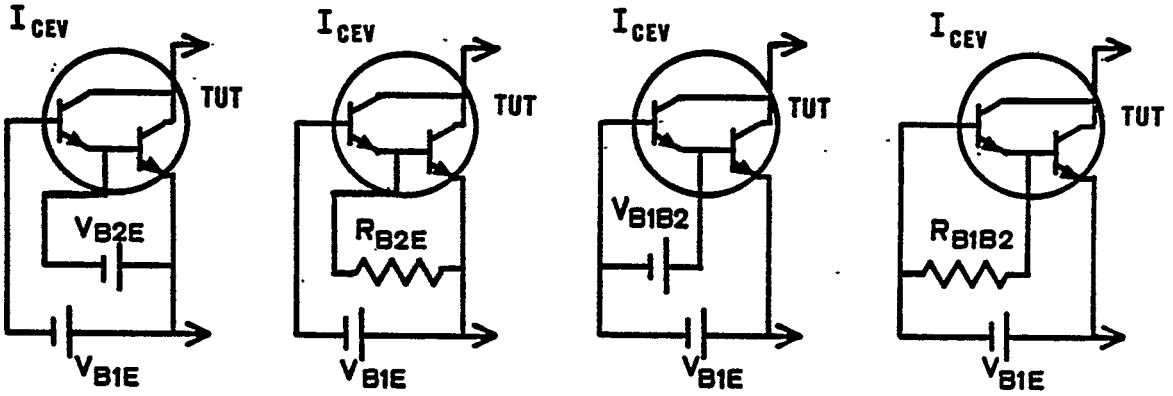
3.3.2.1 *Introduction*

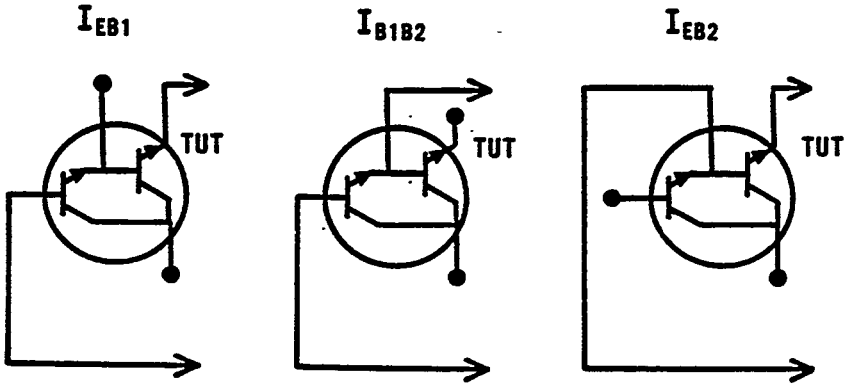
The procedure for testing the cutoff current is to apply the specified reverse voltage and then measure the cutoff current. If testing is done at an elevated temperature, it may be necessary to use a heat sink to prevent thermal runaway that may result because of the temperature dependence of the cutoff current.

3.3.2.2 *Transistor Connections*

Connections for the transistor under test (TUT) are shown here separate from the remainder of the test circuits which are shown in 3.3.2.3.

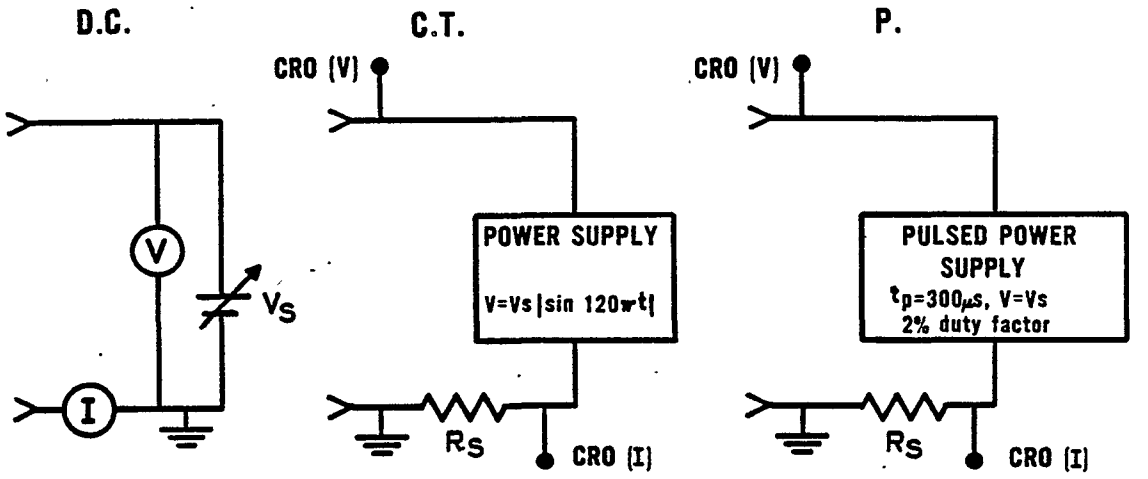






3.3.2.3 *Test Circuits*

The supply voltage, V_s, should be equal to the product of the current sensing resistor, R_s, or the resistance of the ammeter, and the cutoff current (I_{CUTOFF}), plus the specified test voltage. The cutoff current of the transistor in the pulse test circuit must be small compared to the measured cutoff current of the transistor under test. The cutoff current of the transistor under test is measured with an ammeter or with a cathode ray oscilloscope (CRO).



3.3.2.4 *Test Conditions to be Specified*

(1) Case temperature unless T_C = 25°C

(2) Voltages applied to the device: V_{CEO}; V_{EBO}; V_{CBO}; V_{CEV}; V_{EB1}; V_{B1B2}; V_{EB2}

(3) Base termination: V_{EB}; V_{B2E}; R_{B2E}; V_{B1B2}; R_{B1B2}

(4) Technique: D.C.; C.T.; P

3.3.3 Breakdown Voltage [$V_{(BR)CEX}$; $V_{(BR)CEO}$*; $V_{(BR)CES}$; $V_{(BR)EBO}$; $V_{(BR)CER}$]

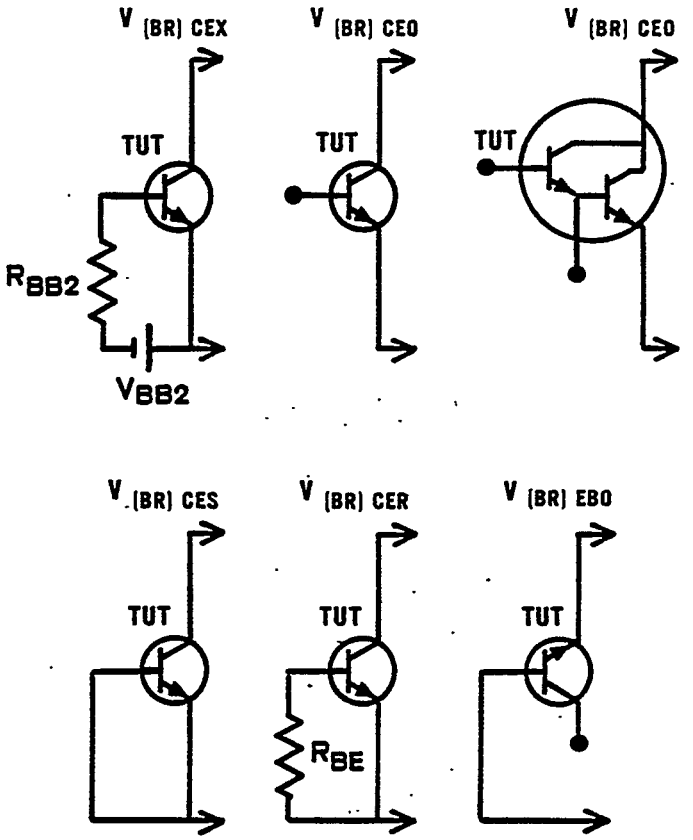
3.3.3.1 *Introduction*

For breakdown voltage measured in the sustaining region, the current should be high enough to insure that the breakdown voltage is relatively insensitive to current.

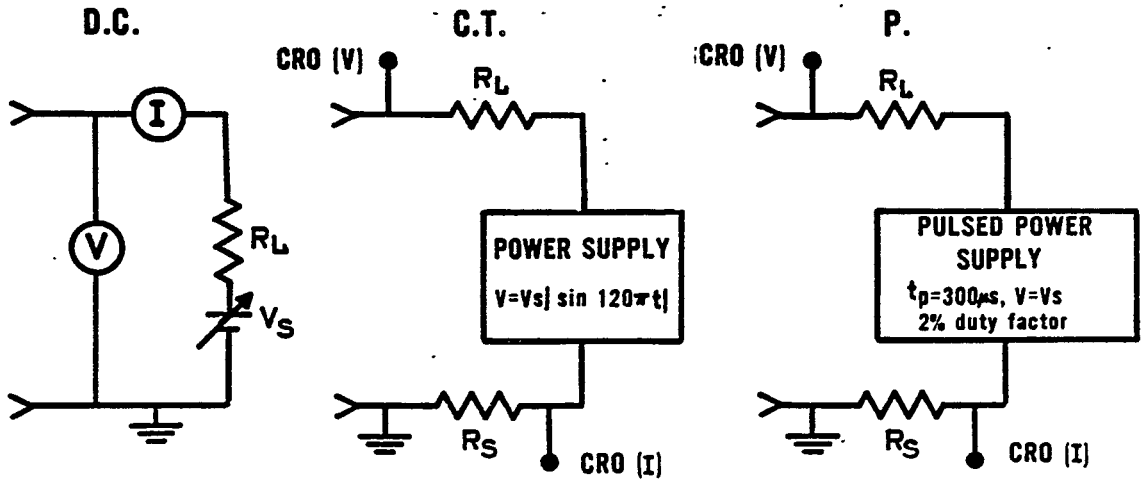
*Commonly referred to as $V_{CEO(SUS)}$

3.3.3.2 *Transistor Connections*

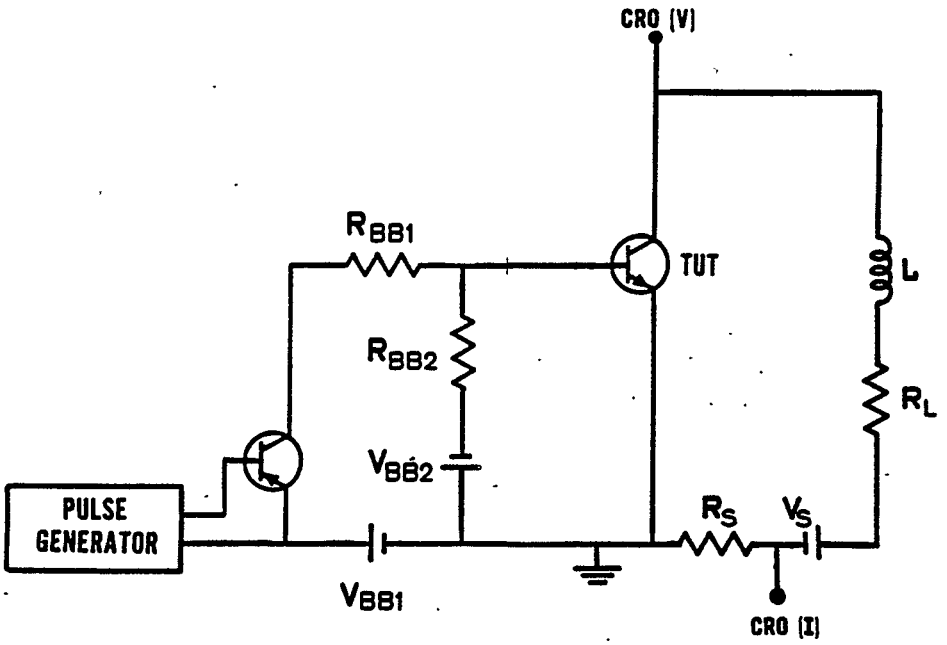
Connections for the transistor under test (TUT) are shown here separate from the remainder of the test circuits which are shown in 3.3.3.3.



3.3.3.3 *Test Circuits*



In addition to the test circuits for D.C., C.T., and P, an inductive sweep circuit is shown. This test circuit is particularly useful for voltage measurements in the sustaining region.



3.3.3.4 *Test Conditions to be Specified*

(1) Case temperature unless T_C = 25°C

(2) Current applied to the device: I_{CEX}, I_{CEO}, I_{CES}, I_{EBO}, I_{CER}.

(3) Base termination and conditions: V_{BB2}; V_{BB1}; R_{BB2}; R_{BB1}; R_{BE}; pulse width; duty cycle

(4) Technique: D.C.; C.T.; P; Inductive Sweep

(5) Load resistance, inductance, and supply voltage where applicable: R_L, L, V_S

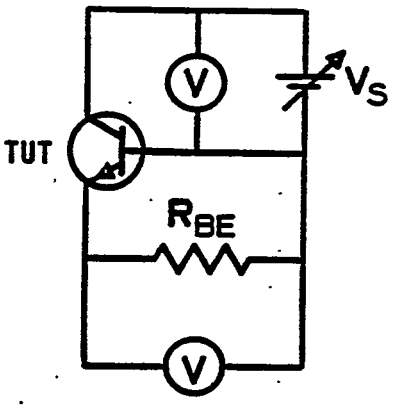
3.3.4.0 Floating Potential [$V_{EB(f1)}$]

3.3.4.1 *Introduction*

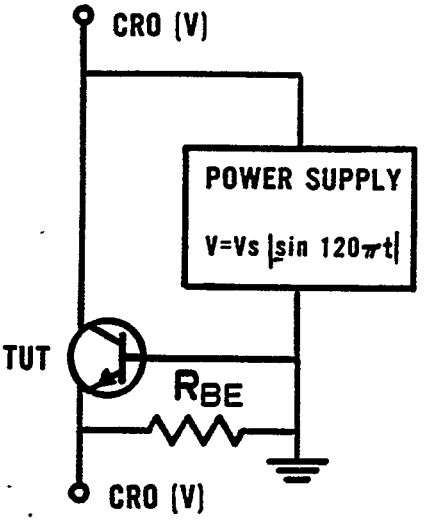
The value of $V_{EB(f1)}$ is related to the thickness of base width.

3.3.4.2 *Test Circuit*

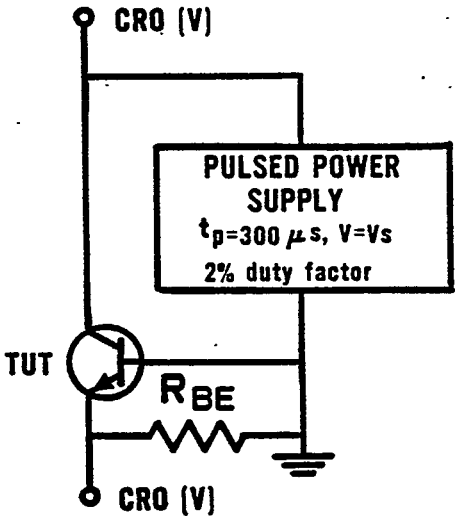
D.C.



C.T.



P.



3.3.4.3 *Test Conditions to be Specified*

(1) Case temperature unless T_C = 25°C

(2) Base-collector voltage: V_{BC}

(3) Base-emitter resistance: R_{BE}

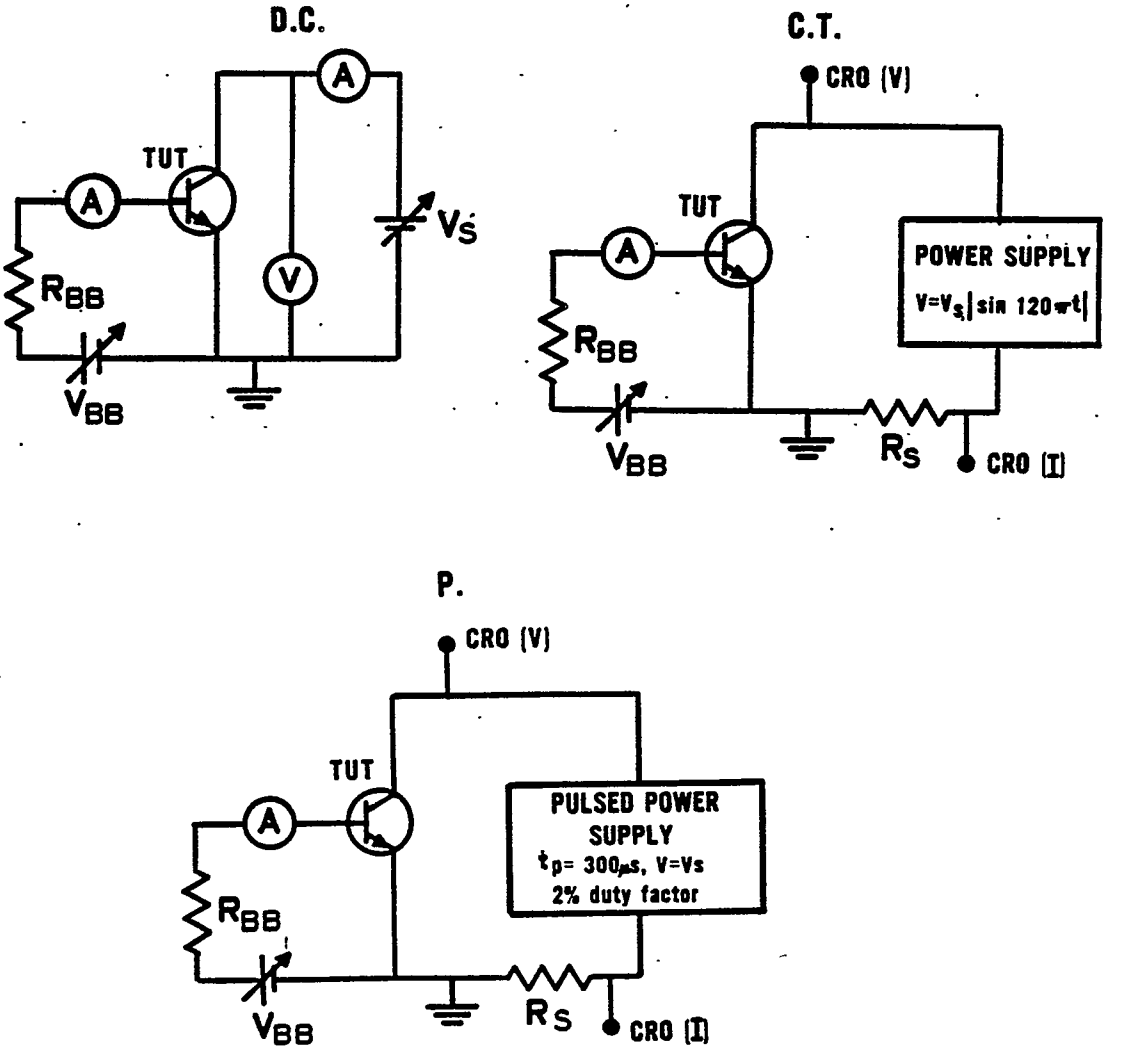
(4) Technique: D.C.; C.T.; P

3.3.5 Current Gain [h_{FE}]

3.3.5.1 *Introduction*

The static forward current transfer ratio in the common-emitter configuration is one of the most important gain characteristics for power transistors. It specifies the relationship of output current to input current.

3.3.5.2 *Test Circuit*



The current gain is given by $h_{FE} = I_C/I_B$. For the C.T. and P tests, $V_{BB} >> \Delta V_{BE}$ so that I_B is constant and relatively independent of V_{BE}.

3.3.5.3 *Test Conditions to be Specified*

(1) Case temperature unless $T_C = 25°C$

(2) Collector emitter voltage: V_{CE}

(3) Collector current: I_C

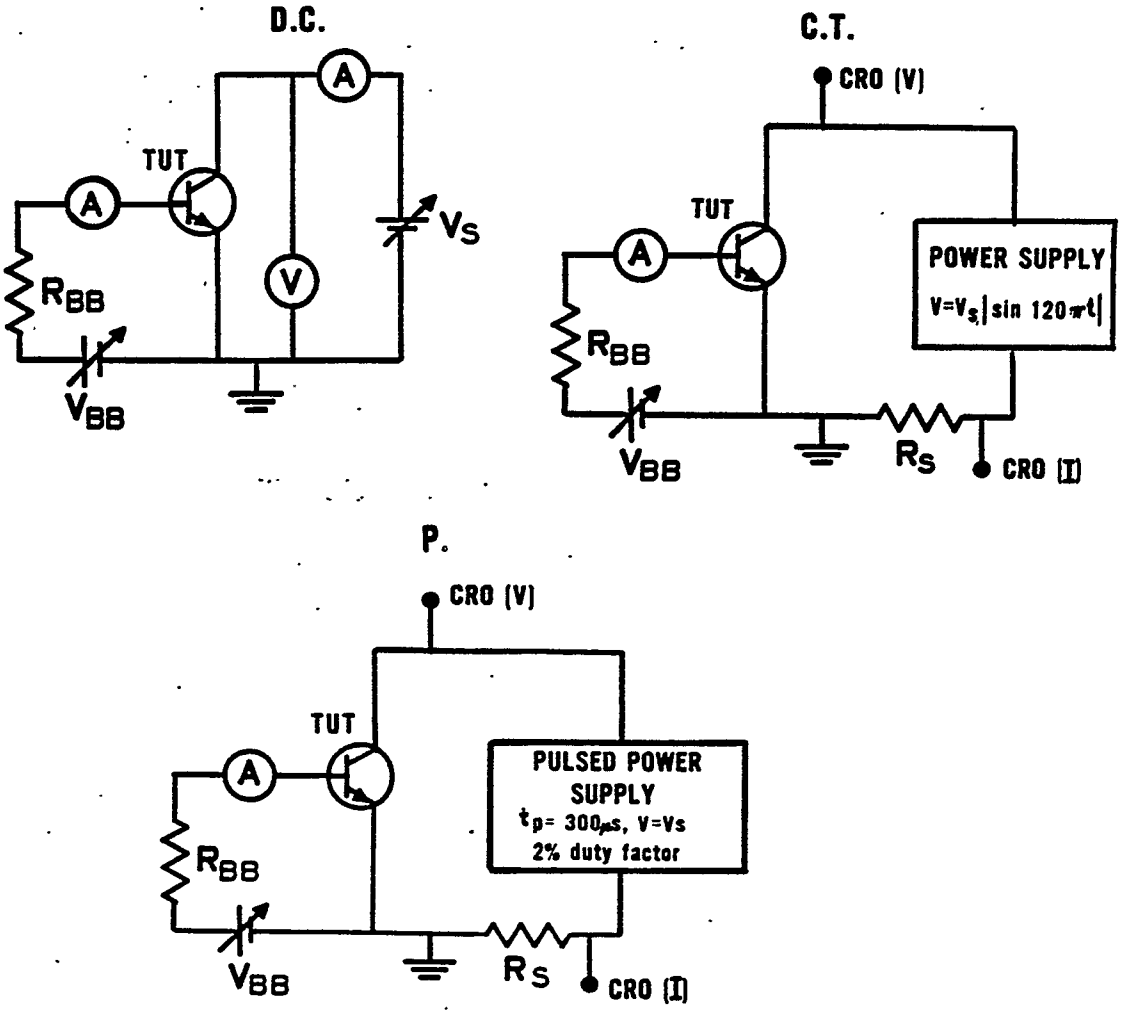
(4) Technique: D.C.; C.T.; P

3.3.6 Saturation Voltage $[V_{CE(sat)}]$

3.3.6.1 *Introduction*

The collector-to-emitter saturation voltage is especially important for switching applications. Together with the collector current, it provides the basis for calculating the power dissipation in the "on" state.

3.3.6.2 *Test Circuit*



For the C.T. and P tests, $V_{BB} >> V_{BE}$ in order to make I_B independent of variations in V_{BE} during the "on" condition for the various devices being tested.

3.3.6.3 *Test Conditions to be Specified*

(1) Case temperature unless T_C = 25°C

(2) Collector current: I_C

(3) Base current: I_B

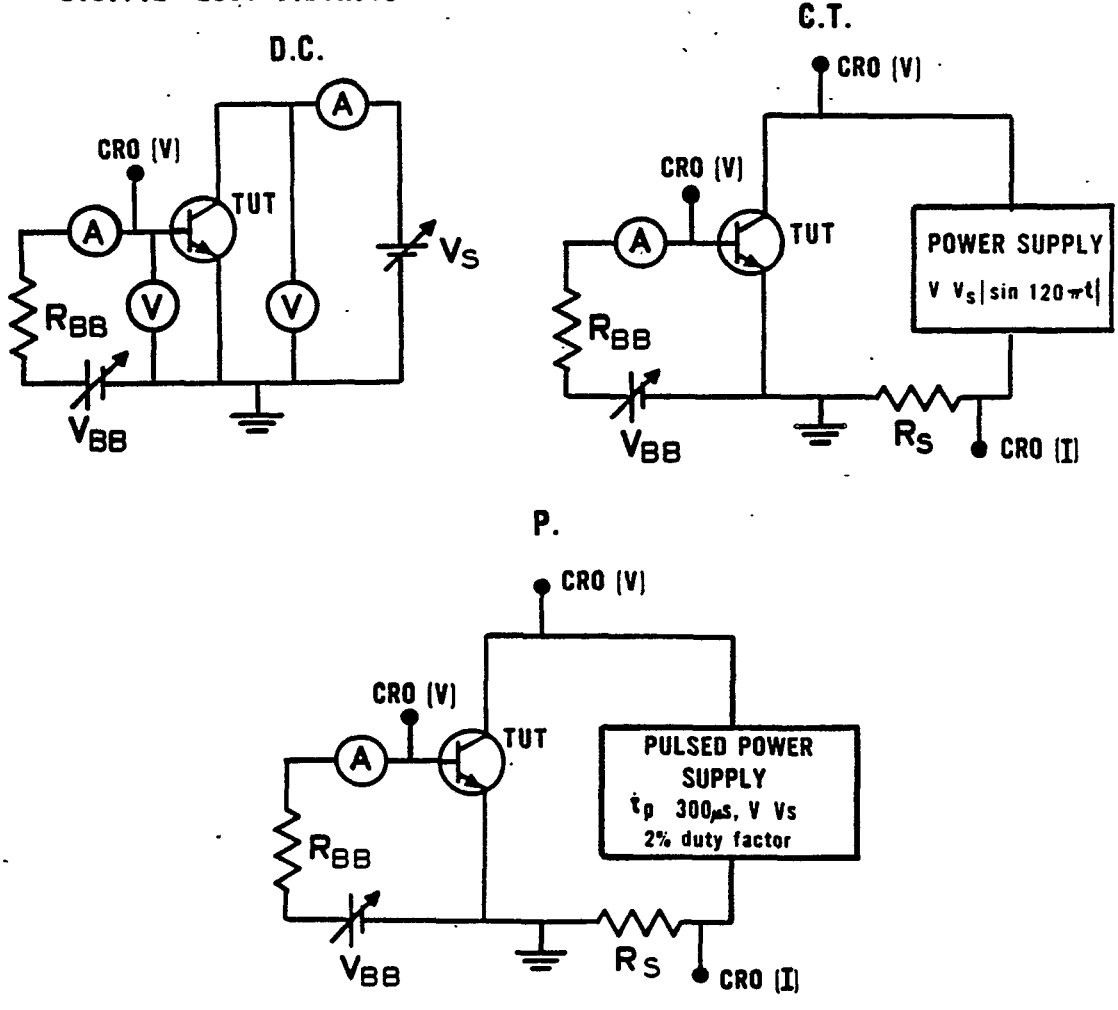
(4) Technique: D.C.; C.T.; P

3.3.7 Base-to-Emitter Voltage [V_{BE}]

3.3.7.1 *Introduction*

There are two conditions of interest for the static base-to-emitter voltage: (1) V_{CE} in saturation (commonly referred to as $V_{BE(sat)}$); and (2) V_{CE} out of saturation (V_{BE}).

3.3.7.2 *Test Circuits*



For the C.T. and P tests, $V_{BB} >> V_{BE}$ in order to make I_B independent of variations in V_{BE} during the "on" condition, for the various devices being tested. The base terminal for Darlington transistors is B1.

3.3.7.3 *Test Conditions to be Specified*

(1) Case temperature unless $T_C = 25°C$

(2) For V_{CE} in saturation ($V_{BE(sat)}$)
   (a) Collector Current: I_C
   (b) Base Current: I_B
   (c) Technique: D.C., C.T., P

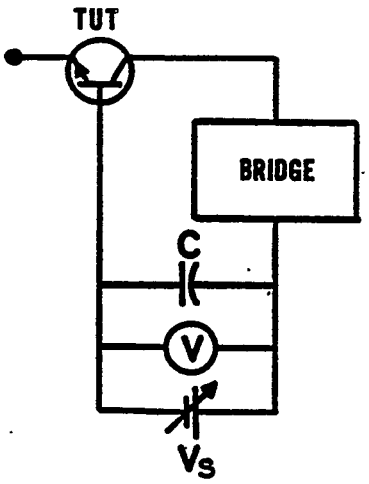
(3) For V_{CE} out of saturation (V_{BE})
   (a) Collector current: I_C
   (b) Collector-to-emitter voltage: V_{CE}
   (c) Technique: D.C.; C.T.; P

3.3.8 Open Circuit Capacitance [C_{obo}]

3.3.8.1 *Description*

The open-circuit output capacitance indicates the frequency limitations of a transistor.

3.3.8.2 *Test Circuit*



The capacitance of C has to be sufficiently large to provide a short-circuit at the test frequency. The bridge has to be nulled with the base-to-collector connection open-circuited. The base terminal for Darlington transistors is B1.

3.3.8.3 *Test Conditions to be Specified*

(1) Case temperature unless T_C = 25°C

(2) Collector-to-base voltage: V_{CB}

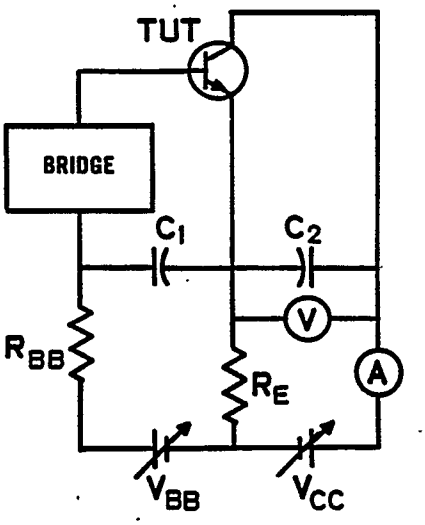
(3) Frequency: f

3.3.9 Small-Signal, Short-Circuit Input Impedance [h_{ie}; $Re(h_{ie})$; $Im(h_{ie})$]

3.3.9.1 *Introduction*

The input impedance is $h_{ie} = v_{be}/i_b$. The real and imaginary parameters are important for designing input matching networks.

3.3.9.2 *Test Circuit*



Capacitors C1 and C2 must represent a short circuit at the measuring frequency. The bridge shall be nulled with a short-circuit across the base-emitter terminals. When h_{ie} is measured at 1 kHz, i_b can be measured with a current probe and v_{be} with an oscilloscope.

3.3.9.3 *Test Conditions to be Specified*

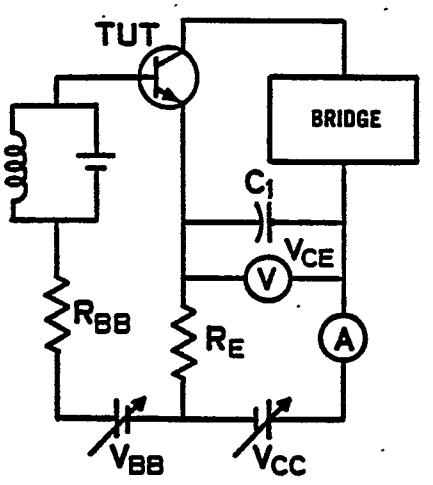
(1) Case temperature unless T_C = 25°C
(2) Collector-to-emitter voltage: V_{CE}
(3) Collector current: I_C
(4) Frequency: f for $Re(h_{ie})$ and $Im(h_{ie})$

3.3.10 Small-Signal, Open-Circuit Output Admittance ($Re(h_{oe})$]

3.3.10.1 *Introduction*

The purpose of this test is to determine the real part of the output admittance.

3.3.10.2 *Test Circuit*



The L-C network in the base circuit shall have a large impedance compared with h_{ie} at the test frequency. Capacitor, C1, shall present a short-circuit at the test frequency.

3.3.10.3 *Test Conditions to be Specified*

(1) Case temperature unless T_C = 25°C
(2) Collector-to-emitter voltage: V_{CE}

(3) Collector current: I_C

(4) Frequency: f

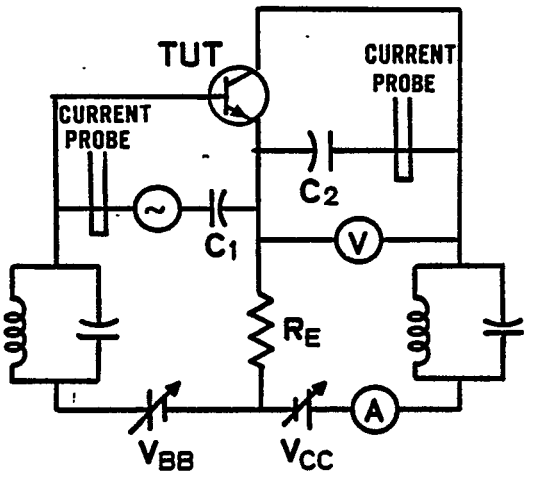
3.3.11 Small-Signal Gain, Cutoff Frequency, and Transition Frequency [h_{fe}, f_{hfe}, f_T, respectively]

3.3.11.1 *Introduction*

These measurements indicate the small-signal gain and the frequency response capabilities of transistors. Both measurements are dependent on the operating point.

The small-signal gain, $h_{fe} = i_c/i_b$, is measured at a frequency of 1 kHz. The cutoff frequency is the frequency at which h_{fe} is 3dB less than its value when measured at a frequency of 1 kHz. The transition frequency, f_T, or the frequency at which $|h_{fe}|$ extrapolates to unity, may be obtained from the relation $f_T = |h_{fe}| \cdot f$ if h_{fe} is measured at a frequency, f, where $|h_{fe}|$ decreases approximately 6dB per octave. The measurement as specified does not assure the 6dB per octave region. The region can be determined by plotting $|h_{fe}|$ versus f.

3.3.11.2 *Test Circuit*



The L-C networks shall have very large impedances compared to those of capacitors C1 and C2. The amplitudes of i_b and i_c are measured with current probes. The ac-impedance represented by C_2, the current probe, and the associated wiring shall be small compared to the output impedance of the transistor under test.

3.3.11.3 *Test Conditions to be Specified*

(1) Case temperature unless T_C = 25°C

(2) Collector-to-emitter voltage: V_{CE}

(3) Collector current: I_C

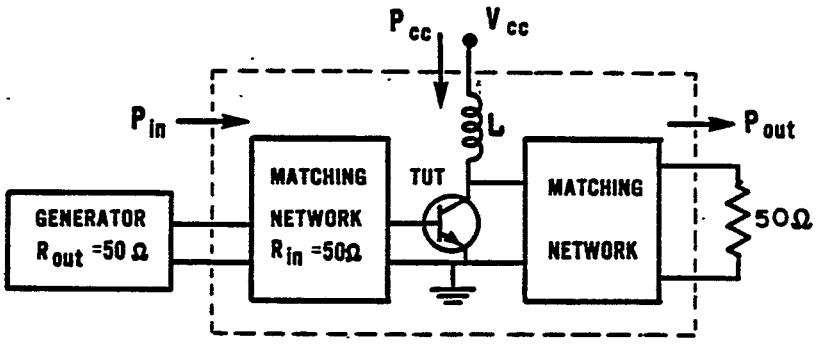
(4) Frequency: f, for f_T only.

3.3.12 Power Gain and Collector Efficiency [G_{PE} and η]

3.3.12.1 *Introduction*

The best way to specify a high frequency transistor is to specify the actual power gain, G_{PE}, and the collector efficiency, η, in an amplifier circuit.

3.3.12.2 *Test Circuit*



Test circuit schematic and component layout-diagram must be supplied by registrant. An effort should be made to keep the test circuit as simple as possible. Physical and electrical characteristics of all critical circuit components must be specified. Total power of harmonic or parasitic frequencies must be 20dB below P_{out} at the specified frequency, $f_{in} = f_{out}$.

The power gain and the collector efficiency are calculated by using the following relations.

$$G_{PE} = 10 \log \frac{P_{out}}{P_{in}} \qquad \eta = \frac{P_{out}}{P_{in} + P_{cc}}$$

3.3.12.3 *Test Condition to be Specified*

(1) Case temperature unless $T_C = 25°C$

(2) Frequency: f_{in}

(3) Supply voltage: V_{CC}

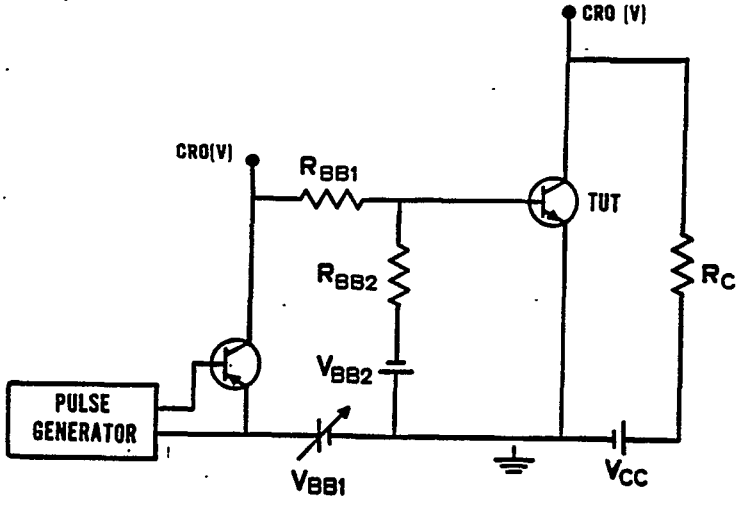
3.3.13 Switching Time $[t_d; t_r; t_s; t_f]$

3.3.13.1 *Introduction*

Switching time may be measured either with a low impedance or a high impedance base drive. For the latter case, charge control theory can be used to predict changes in switching times for different drive and load conditions. For the former measurement approach, it is desirable to minimize the useage of many different variations in the switching circuit used. A circuit similar to that shown in 3.3.13.2 for the limited set of suggested resistor values is recommended for measuring switching times registered on the JC-25, RDF2 format.

3.3.13.2 *Test Circuits*

(1) Low Impedance Base Drive Circuit

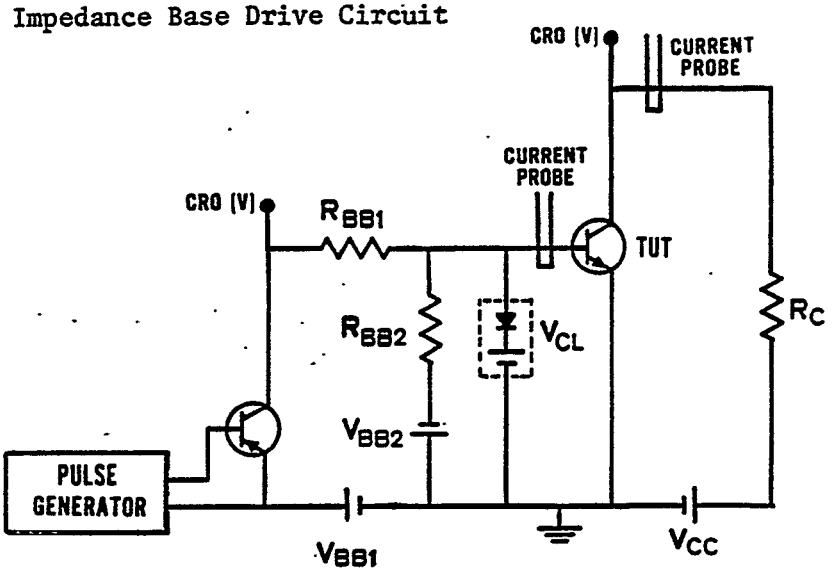


Suggested sets of resistor values:

Circuit	R_{BB1} (Ω)	R_{BB2} (Ω)	R_C (Ω)
1	50	100	20
2	10	10	5
3	1	1	1

The rise and fall time of the input pulse shall be smaller than 10% of the maximum specified rise and fall time of the output pulse. Changing the pulse width, t_p, by a factor of two shall not change the storage time, t_s.

(2) High Impedance Base Drive Circuit



Suggestions:

(a) To maintain test currents constant to ±10% for devices to be tested, the following suggestions are made regarding circuit values:

$$V_{CC} \geq 10\ \Delta V_{CE(sat)},$$
$$V_{BB1} \geq 10\ \Delta V_{BE(on)},$$
$$V_{BB2} \geq 10\ \Delta V_{BE(off)}, \text{ and}$$
$$R_{BB2} \geq 4\ \Omega,$$

where $\Delta V_{CE(sat)}$ and $\Delta V_{BE(on)}$ are the differences between the highest and lowest voltages for the devices to be tested, and where $\Delta V_{BE(off)}$ is the difference between the highest and lowest transient voltage during the current turn-off period, for the devices to be tested. Typical values for V_{BB1} and V_{BB2} are in the range of 5 to 35V.

The diode clamp network should be used if $V_{BB2} > V_{EBO}$. If the delay time is affected by the diode clamp, the clamp should be removed and V_{BB2} reduced to a level that is less than V_{EBO} during this measurement.

(b) To make negligible the effects of variations in the capacitance of devices to be tested, the circuit values should be selected so that $R_C \leq t_f/10C_{obo}$ and $I_C \geq 20\ V_{CC}\ C_{obo}\ f_T$.

(c) To make negligible the effects of temperature and of variations in h_{FE} on the measurement, the duty cycle should be adjusted so that the average junction temperature is less than 5°C above ambient, and the circuit values are selected so that both I_{B1} and $I_{B2} \geq 4I_C/h_{FE(min)}$.

(d) To make measurements essentially independent of input pulse conditions; the pulse shape should be such that pulse rise time is $\leq t_d/4$, the pulse width is $>> t_d + t_r + t_s$, and the pulse fall time is $\leq t_s/4$.

3.3.13.3 *Test Conditions to be Specified*

(1) Low Impedance Base Drive Circuit

(a) Case temperature unless $T_C = 25°C$.

(b) V_{BB1}; V_{BB2}; V_{CC}; R_{BB1}; R_{BB2}; R_C; and t_p and f of the pulse generator.

(2) High Impedance Base Drive Circuit

T_C, V_{CC}, I_C, I_{B1}, I_{B2}, V_{CL}

PART 4

THERMAL CHARACTERISTICS

PART 4

THERMAL CHARACTERISTICS

CONTENTS

PART 4

THERMAL CHARACTERISTICS

4.1 INTRODUCTION

The purpose of this part is to set forth accepted test practices as a guide in making power transistor thermal characteristic tests. Correlation between these tests and specific equipment tests will be the responsibility of the user.

4.2 TEMPERATURE MEASUREMENTS

4.2.1 General

Thermal measurements of transistors involve direct measurements of ambient or surface temperatures, or both, and indirect measurements of internal temperatures. Because the temperature rise of components above ambient temperature depends on parameters such as dissipated power, air velocity, altitude, and ambient temperature, an appropriate choice of these parameters must be made to provide the necessary standardization between the user's and the manufacturer's testing procedures. Temperature measurements by thermocouples, thermometers, pyrometers, temperature-sensitive resistors, and temperature-sensitive paints may be used. When specific temperatures may be measured accurately only with particular methods, these methods will be specified.

4.2.2 Ambient Temperature

Ambient temperature, T_A, as herein used, is the temperature of the medium used for cooling the transistor. For still-air cooling systems (still-air convection cooling), the ambient temperature is the temperature of the air immediately below the transistor when operating under specified conditions. For forced-air cooling systems (forced-air convection cooling), the ambient temperature is the temperature of the air immediately before its entry into the vicinity of the transistor. For cooling mediums other than air, the manufacturer shall be consulted for his recommendation.

4.2.3 Transistor Temperature

4.2.3.1 *General*

Because a transistor is a multi-junction semiconductor structure enclosed in a housing, direct measurement of junction temperature is not possible.

On the other hand, ambient temperature, heat dissipator temperature, mounting surface temperature, and case temperature may be measured directly.

4.2.3.2 *Transistor Junction Temperature*

It is desirable to measure the transistor junction temperature, T_J, at the hottest point on the transistor chip. In general, an indication of the peak junction temperature can only be determined by using an infrared micro-radiometer or similar instrument to monitor the peak temperature on the surface of the transistor chip. Although useful, this type of measurement does not lend itself to the generation of a standardized test-method to measure the thermal characteristics of all types of power transistors. A temperature-sensitive device parameter is therefore used to indirectly measure an average junction temperature of the transistor [see 4.3 for further details].

4.2.3.3 *Case Temperature*

The case temperature, T_C, of a stud-mounted, hexagonal-base transistor is measured at the center of any of the six flats at the base rim. The case temperature of other base-mounted transistors is measured at a point specified by the manufacturer. The recommended case temperature test method employs the use of a thermocouple with characteristics given below. The method and location of attachment to the case is also provided.

An accuracy of ±0.5°C should be expected of the thermocouple and associated measuring system. Under transistor load conditions, slight variations in the temperature of different points on the case may reduce this to ±1.0°C for free air convection cooling, and ±2.0°C for forced-air cooling.

(1) Type of Thermocouple

The thermocouple material shall be copper-constantan (Type T). Its useful temperature range for standard temperature measurements is from -183 to +371°C. The wire size shall be no larger than #30 Awg. The junction of the thermocouple shall be formed by welding together the wires to form a bead rather than having the wires soldered or twisted together. [See 1974 Annual Book of ASTM Standards - Part 30, Method E220 for Calibration of Thermocouples by Comparison Techniques for information on construction and use of thermocouples.]

(2) Mounting Method

A small hole, just large enough to insert the thermocouple, shall be drilled approximately 0.76 mm (0.03 in) deep in the base plate of the

semiconductor device at the point specified by the manufacturer. The edge of the hole should be peened with a small center punch to form a rigid mechanical contact with the welded bead of the thermocouple. In the event that drilling into the base plate of the device case becomes impractical, because of case material or case dimensions, the thermocouple wire may be welded or soldered directly to a specified point on the case. Other methods of mounting thermocouples, with the possible exception of the thermocouple welded or soldered directly to the case, usually result in temperature readings lower than the actual temperature. Such deviations result from inadequate contact with the case when using cemented thermocouples and from the external heat dissipator being in contact with the thermocouple when using pressure contacts.

4.2.4 Mounting Surface Temperature

4.2.4.1 *General*

The mounting surface temperature, T_M, for EIA Registered Power Transistor packages is measured using a thermocouple imbedded in a washer. The use of a washer with an imbedded thermocouple offers the best single method of non-destructive testing that is compatible with most package types. The thermocouple characteristics and details of the washer design are given below. It should be noted that case temperature and mounting surface temperature are sometimes used interchangeably.

The mounting surface technique for measuring the reference point temperature is non-destructive and is generally as repeatable as the case temperature measuring technique. The mounting surface technique is "application oriented" in that it takes into account the mounting surface interface.

4.2.4.2 *Type of Thermocouple* - The thermocouple material shall be copper-constantan (Type T). Its useful temperature range for standard temperature measurements is from -183 to +371°C. The wire size shall be no larger than #30 Awg. The junction of the thermocouple shall be formed by welding the wires together to form a bead rather than having the wires soldered or twisted together. [See 1974 Annual Book of ASTM Standards - Part 30, Method E220 for Calibration of Thermocouples by Comparison Techniques for information on construction and usage of thermocouples].

4.2.4.3 *Mounting Washer Construction* - For all registered TO outlines the following general rules apply:

(1) The base material of the washer shall be copper (half hard or softer is preferred).

(2) The thickness of the washer shall be 3.18 ± 0.13 mm (0.125 ± 0.005 in)

(3) The outline of the washer shall be larger by 0.76 to 1.52 mm (0.03 to 0.06 in) than the outline of the seating surface of the package for which the washer is intended.

(4) Clearance holes shall be 0.41 to 0.79 mm (0.016 to 0.031 in) larger than the maximum outside diameter of the studs or screws intended to pass through the holes.

(5) The surface of the washer shall be flat within 25 μm per 25 mm (0.001 in per in) and parallel within 75 μm per 25 mm (.003 in per in) and shall be nickel plated to a thickness of 1.27 to 2.54 μm (50 to 100 μin). [See ANSI B46.1 - 1962, Surface Texture for further details].

(6) The surface of the washer shall be free from burrs, but the maximum chamfering of edges or holes shall not exceed 0.41 mm (0.016 in) by 45 degrees so as not to effectively reduce the contact area of the washer.

(7) Both surfaces of the washer shall have a 1.60 μm (63 μin) finish or better and be free of oxides. [See ANSI B46.1 - 1962, Surface Texture for further details].

(8) The thermocouple hole shall be drilled into the washer midway between and parallel to the top and bottom surfaces. The size of the thermocouple hole shall be no greater than 1.52 mm (0.06 in) in diameter but it is recommended that it be no larger than necessary to accept the thermocouple.

(9) For flat-type packages (such as the TO-3), the bottom of the thermocouple hole shall extend approximately 0.8 mm (0.03 in) beyond the geometric center of the washer. Radial orientation of thermocouple hole is arbitrary.

(10) For stud-type packages (such as the TO-61), the bottom of the thermocouple hole shall be approximately 0.8 mm (0.03 in) from the inside hole of the washer.

(11) For tab-type packages, the bottom of the thermocouple hole shall extend approximately 0.8 mm (0.03 in) beyond the geometric center of the seating surface.

(12) It is recommended that the thermocouple be secured into the washer with a thermal conducting adhesive and that particular attention be paid to minimizing air voids around the ball of the thermocouple.

(The thermocouple bead should be in direct contact with the copper washer).

(13) Clearance holes for device leads should allow suitable clearance to prevent electrical shorting to the washer. It is recommended that this clearance hole be approximately 1.5 mm (0.06 in) larger in diameter than the lead to allow clearance for insulating sleeving to be used on the leads.

(14) Device mounting torque should comply with the manufacturer's recommendations.

(15) A thermal conducting compound should be used on both sides of the washer to interface with the device and the heat sink.

(16) Special care must be taken so that only the bead of the thermocouple is allowed to come into mechanical contact with the washer.

4.2.5 Still-Air Convection Measurements

Still-air measurements shall be based on the following conditions:

(1) The transistor shall be mounted vertically (with the leads down) in a cubic enclosure of not less than 30 cm (1 ft) on a side. If the transistor is mounted on a heat dissipator, e.g., a square metal plate, each internal dimension of the enclosure should be a minimum of four times the dissipator height. The heat dissipator should be suspended vertically in the cubic enclosure.

(2) There shall be no radiation sources other than the transistor under test in the enclosure.

(3) The interior enclosure wall shall have a low-reflectance finish (emissivity ≈ 1.0).

(4) The transistor shall be mounted in a socket in such a manner that conduction cooling through the leads or the socket or both shall be small compared to the other cooling mechanisms. The transistor leads shall be cut to the standard length designated for socket insertion for the base being used and should be inserted in the socket to a standard insertion depth. No part of the socket shall extend above the seating plane of the transistor.

(5) More than one transistor may be put in the enclosure but all must be mounted on the same horizontal plane and shall be at least five case-dimensions away from each other and from the walls. Only one transistor may be energized at a time.

The ambient temperature should be measured by means of a thermocouple mounted at a distance of one-fourth the dissipator height, directly below the center of the bottom of the heat dissipator; or in the case of lead mounted devices, approximately 1.3 mm (0.5 in) directly beneath the device under test.

4.2.6 Forced-Air Convection Measurements

The device manufacturer should be consulted for details.

4.3 THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS

4.3.1 Introduction

The thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure to provide for heat removal from the active semiconductor element; it is an indication of the power handling ability of a semiconductor device.

Thermal resistance is measured in terms of the temperature rise of the transistor junction, in degrees Celsius, above a reference point, such as case, mounting surface, or ambient, per watt of continuous dissipation. Thermal resistance specifications must always include the two points between which the thermal resistance value applies. The most common specifications are:

(1) $R_{\theta JC}$ - thermal resistance, from junction to case.
(2) $R_{\theta JM}$ - thermal resistance, from junction to mounting surface.
(3) $R_{\theta JA}$ - thermal resistance, from junction to ambient with the device unattached to a heat dissipator or attached to a specified heat dissipator.

The term virual junction temperature is here applied to multi-junction devices to indicate the temperature of the active semiconductor element for use in device test methods and specifications and is used interchangeably with the term junction temperature in this document.

4.3.2 General Considerations

In most devices, the maximum junction temperature cannot be measured directly since the area of interest is not accessible due to packaging considerations. Thus, indirect means are used to infer the temperature of a specific area on the chip. The thermal resistance of a semiconductor device is therefore determined

by the measurement of a temperature-sensitive electrical parameter of a semiconductor junction within the device.

The measured thermal resistance of transistors is not constant as frequently assumed, but depends on the device operating conditions, the junction and reference point temperatures, and the temperature sensitive parameter chosen. When specifying thermal resistance, it is therefore important to indicate clearly the measurement method and conditions used.

In measuring the thermal resistance of a power transistor, either of two methods may be used; one uses the emitter-base and the other uses the collector-base forward voltage as the temperature sensitive electrical parameter to measure junction temperature.

While both methods are equally precise, the emitter-base forward voltage method is the more accurate; i.e., its use results in a measured junction temperature more nearly equal to the actual peak temperature in the chip. Greater accuracy accrues when using the emitter-base junction because the distribution of the forward measuring current during the power test deviates less from its distribution during calibration than when using the collector-base junction.

4.3.3 Emitter-Base Forward Voltage Method

4.3.3.1 *Introduction*

The purpose of the test method is to measure the junction-to-specified-reference-point thermal resistance, $R_{\theta JR}$, of single-element transistors. The method uses the emitter-base forward voltage as the temperature sensitive parameter, TSP. The method also uses an emitter-only switching mode in which the heating current is interrupted at the emitter during the measurement of the TSP in the power application step. The collector-emitter voltage remains unchanged by the interruption and equal to that used during calibration.

4.3.3.2 *Procedure*

The test method involves the measurement of the TSP as part of two steps in the procedure, the calibration and the power application steps. In the calibration step, the TSP is measured to determine the TSP temperature coefficient of the transistor-under-test. In the power application step, the TSP is measured to determine the increase in the junction temperature

due to power dissipation in the transistor-under-test.

The temperature coefficient of the TSP is obtained by measuring the TSP as a function of the reference-point temperature which may be varied by externally heating the transistor-under-test in an oven or on a temperature-controlled heat sink. The TSP is measured at a specified collector-emitter voltage and constant forward measuring current, I_M. The magnitude of I_M selected is small enough so that the TSP decreases linearly with increasing temperature over the temperature range of interest. A measuring current ranging from 1.0 to 50 mA is generally used, depending on the rating and operating conditions of the transistor-under-test. Typically, there is negligible internal heating during the measuring interval. In this case, the reference-point temperature is approximately equal to the junction temperature during calibration.

The power application step of the procedure is divided into two parts. For both parts, the temperature of the reference point is held at a preselected, constant value. In the first part, the value of the TSP, V_{M1}, is measured with the same measuring current, I_M, and at the same collector-emitter voltage used during the calibration procedure. The power dissipation during this part of the test, $P_1 = I_M V_{BE} + I_C V_{CB}$, is generally negligible in comparison to the power dissipation, $P_2 = I_E V_{BE} + I_C V_{CB}$, used in the second part of the power application step.

In the second part, the transistor-under-test is operated at higher power, P_2, which is intermittently applied at a very high duty factor (greater than 99 percent). The collector-emitter voltage is equal to that used in the first part. In order to reach the higher power level, the emitter current is increased. The value of the TSP, V_{M2}, is measured during the interval between heating pulses (generally $\leq$ 250 µs) using the same constant measuring current as is used in the calibration step. Only the emitter-base junction is switched to interrupt heating power.

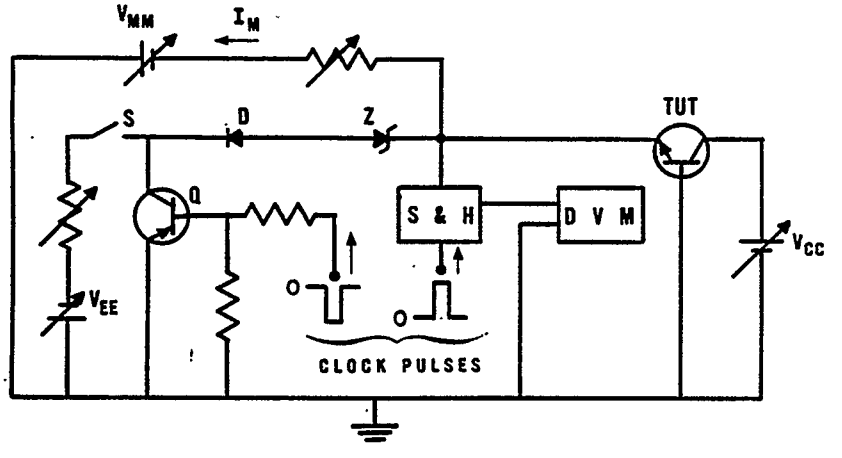
To obtain the most accurate measure of the virtual junction temperature, the TSP should be measured at the instant that the heating power is discontinued. However, it is not possible to do this because a finite time is required for the transistor current to decay from the heating value to the measuring value. In addition, transients in the measuring-voltage waveform are present for some time after the measuring current value has been reached which delays

further the time when a measurement of the TSP can be made. The transients are primarily due to charge storage effects in the transistor-under-test. The time before the TSP can be measured in most transistors is in the range from 5 to 100 μs.

Because some cooling occurs between the time that the heating power is removed and the time that the TSP is measured, the junction temperature value determined from the TSP will be in error, leading to the calculation of a deceptively low thermal resistance. It may therefore be necessary to extrapolate the measured junction temperature back to the time when the heating power was terminated, based on the shape of the cooling waveform beyond the measuring point. The extrapolated value should then be used in the calculation of thermal resistance. The procedure for performing this extrapolation is described in 4.3.6.

It is recommended that in the power application step, conditions are used so that the junction temperature of the test device is representative of worse-case usage. Consistent with this, the reference point temperature should be chosen so that it is at least 30°C less than the measured junction temperature. The heat dissipator used must allow that such a temperature difference be achieved.

4.3.3.3 *Test Circuit*



Note: To prevent oscillations in the transistor-under-test, it may be necessary to use lossy ferrite beads on the emitter and base leads, and to connect a capacitor between the collector and ground.

The circuit is controlled by two coincident clock pulses with equal widths of approximately 250 μs* and a repetition rate of approximately 4 Hz*. During the heating interval of the test cycle (between clock pulses), transistor Q is off and the current through the transistor-under-test, TUT is the sum of the heating current (switch S closed) and the measuring current. The heating current is furnished by the V_{EE} supply, and the measuring current by the V_{MM} supply. A negative-voltage clock pulse is used to end the heating part of the test cycle by biasing transistor Q on, which reverse biases diode D so that the heating current no longer passes through the transistor-under-test. The function of the regulator (Zener) diode Z is to decrease the switching time of the transistor-under-test. The use of such a diode is optional. If used, however, the regulator voltage of diode Z should be equal to or less than the maximum rated V_{EBO} of the transistor-under-test. A clock pulse is also delivered to the sample-and-hold unit, S & H. After a delay, usually 5 to 100 μs, the sample-and-hold unit senses the TSP, i.e., V_{M2}, for a 1.5-μs* period and displays its value on the digital voltmeter, DVM. The temperature coefficient of the TSP and the required voltage, V_{MC}, (for $T_{MC} = T_R$) are obtained by making the required measurements with the heating current supply disconnected (switch S open). A digital voltmeter should be used to measure the power dissipation of the transistor-under-test ($P = I_E V_{BE} + I_C V_{CB}$) by connecting it across the junction(s) to measure the voltage(s), and across a suitable non-inductive current sensing resistor(s) to measure the current (s).

4.3.4 Test Conditions to be Specified

(1) Temperature sensitive parameter
(2) Junction(s) switched to interrupt heating power
(3) Case temperature range during calibration
(4) Forward measuring current
(5) Heating current
(6) Collector-emitter voltage
(7) Heating power duty factor
(8) Heating power repetition rate

* Typcial value

(9) Delay time before measurement of TSP

(10) Total heating time duration

(11) Reference-temperature measuring point

(12) Reference point temperature for heating power measurements

(13) Mounting torque

(14) Mounting arrangement

(15) Extrapolation procedure

4.3.5 Calculation of Thermal Resistance

To calculate the junction-to-reference point thermal resistance the following equation is used,

$$R_{\Theta JR} = \frac{T_J - T_R}{P(AVG)} = \frac{V_{M2} - V_{M1}}{(P_2 - P_1)\cdot D} \cdot \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{calibration}}$$

where:

$R_{\Theta JR}$ = thermal resistance, junction-to-reference-point (°C/W),

T_J = virtual junction temperature (°C),

T_R = reference-point temperature (°C),

$P(AVG)$ = average heating power applied to transistor causing temperature difference $T_J - T_R$ (W),

P_2 = magnitude of higher heating power applied to transistor (W),

P_1 = magnitude of lower heating power applied to transistor (W),

V_{M2} = value of TSP corresponding to the temperature of the junction heated by P_2 (mV),

V_{M1} = value of TSP corresponding to the temperature of the junction heated by P_1 (mV),

D = heating power duty factor,

$\frac{\Delta V_{MC}}{\Delta T_{MC}}$ = temperature sensitive parameter temperature coefficient measured at I_M (mV/°C),

T_{MC} = calibration temperature measured at reference point (°C), and

V_{MC} = value of TSP during calibration at I_M and specific value of T_{MC} (mV).

The equation to calculate $R_{\theta JR}$ can be simplified if (1) the lower heating power, P_1, is equal to the power dissipation during calibration, so that $V_{M1} = V_{MC}$ (for $T_{MC} = T_R$), and if (2) the power dissipation during calibration is negligible so that $P_1 \simeq 0$. The simplified equation is,

$$R_{\theta JR} = \frac{V_{M2} - V_{MC}}{P_2 D} \cdot \left[\frac{\Delta V_{MC}}{\Delta T_{MC}}\right]^{-1}_{\text{calibration}}$$

Measurements of T_R and T_{MC}, are made by means of a thermocouple attached to the reference point. See 4.2 for information on reference-point temperature measurements of conduction-cooled power transistors.

4.3.6 Extrapolation Procedure

The extrapolation procedure is based on the assumption that the thickness of the heat source is small compared to that of the chip, and that for approximately the first 200 or 250 μs of cooling, the heat flow is essentially one dimensional. Therefore, the junction temperature, $T_{J(Cooling)}$, during the first 200 or 250 μs of cooling can be represented by:

$$T_{J(Cooling)}(t) = T_{J(S.S.)} - Kt^{1/2} \qquad (1)$$

where K is approximately constant and $T_{J(S.S.)}$ is the steady state junction temperature.

If $T_{J(Cooling)}(t)$ versus $t^{1/2}$ is plotted on linear graph paper, the generated curve will be a straight line with $T_{J(S.S.)}$ as the temperature axis intercept. Plotting this curve for an actual device also provides a means for determining when non-thermal switching transients are significant because the curve, as plotted, will be non-linear under this condition.

To calculate the extrapolated value $T_{J(S.S.)}(t = 0)$, the following expression (developed from e.g. (1)) can be used with two measurements of T_J during junction cooling,

$$T_{J(S.S.)}(t = 0) = T_{JI} + \frac{T_{J2} - T_{JI}}{t_1^{1/2} - t_2^{1/2}} \cdot t_1^{1/2}$$

where:

$T_{J(S.S.)}(t = 0)$ = junction temperature, extrapolated to the time at which the heating power is terminated (°C),

t = delay time after heating power is terminated (μs),

T_{J1} = junction temperature at time $t = t_1$ (°C),

T_{J2} = junction temperature at time $t = t_2 < t_1$ (°C).

PART 5

A USERS GUIDE

PART 5

A USERS GUIDE

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PART 5

A USERS GUIDE

5.1 INTRODUCTION

The purpose of this part is to offer to the user some general information about different failure modes, temperature effects on transistor parameters, and trouble-shooting. This information is not meant to be complete or exhaustive, and it does not include detailed application information.

5.2 PRODUCT SAFETY

It is the responsibility of the power transistor user to anticipate the possibility of transistor failure.

A transistor failure should not render the equipment unsafe for any reason in terms of electrical shock, explosion, etc.

5.3 TRANSISTOR FAILURE MODES

5.3.1 Introduction

Transistor failure occurs when the transistor can no longer meet all the electrical characteristics specified in the registration. There are two general classes of failure modes: catastrophic failure and degradation. Catastrophic failure occurs when at least one of the electrical parameters undergoes a sudden change which renders the transistor inoperable. Degradation occurs when at least one of the electrical parameters has changed so that it no longer meets the characteristic specified in the registration or those limits agreed upon by the buyer and seller.

5.3.2 Catastrophic Failure

Catastrophic failure can occur whenever the transistor is operated beyond the registered maximum ratings. This failure is usually manifested either by a short circuit or an open circuit.

An open circuit is usually due to the vaporization of a part of a lead wire electrically connecting the terminal lead to the semiconductor die and is caused by excessive current through the wire.

A short circuit may be due to any one of a number of effects, for example, fusing of the collector and emitter, surface arcing across p-n junctions or adjacent evaporated leads, or "solder balls" touching adjacent metal areas.

Fusing of the collector and emitter can occur when the temperature in the bulk becomes high enough to melt the semiconductor material. It can also occur if the temperature at the surface is high enough to have the emitter metal-contact alloy through the base region. In planar devices with aluminum metallization, the location and lateral extent of the short circuit site usually may

be determined by viewing the emitter metallization. The high surface temperature can result in the formation of a silicon-aluminum eutectic over the site. This is seem as an apparent discoloration of the metallization when viewed under a microscope.

The high temperature to produce fusing or other thermal damage may be caused by exceeding the ambient temperature rating or the power dissipation rating of the transistor. The area over which the fusing occurs depends on the distribution of power dissipation within the transistor at the time the intrinsic temperature of the semiconductor material is reached. The failure can be the result of using an inadequate heat sink or poor circuit design which allows a cumulative increase in power dissipation with increasing junction temperature. This thermal runaway condition can occur because of the positive temperature coefficient of the collector current. The primary causes for this dependence are the exponential increase with temperature of the collector junction leakage current, the exponential increase with temperature of the emitter current for a constant emitter junction voltage, and the increase with temperature of the dc common-emitter current gain. When thermal runaway occurs in germanium power transistors, it is usually due to the temperature dependence of the collector junction leakage current. In silicon power transistors, the temperature dependences of the emitter current and gain are more important. Thermal runaway is most apt to be a problem when the transistor is operated in a circuit which attempts to maintain a constant emitter junction voltage or a constant base current.

High temperatures within a small volume of the transistor may result when the maximum operating conditions of the transistor are exceeded. Exceeding these conditions may allow the development of a lateral current-instability leading to second breakdown. The current constriction of second breakdown resulting from this instability can create localized junction temperatures high enough to produce a collector-to-emitter short circuit. This can occur even though the collector current is kept below the rated value.

The problem of inadvertant excursions beyond the limits of the registered maximum operating conditions is generally more serious for high-frequency transistors. Such transistors require greater care in their use. Greater awareness of the effects of reactive loads, even of leakage inductance, is required. A transistor operating as a vhf or uhf power amplifier may be made to fail by detuning the associated circuitry or by abruptly changing the load impedance. Caution should therefore be observed when selecting a transistor with a frequency capability greater than needed for the circuit function in attempting to achieve greater reliability. For example, this might be done to achieve greater radiation resistance. Then it is important to recognize the compromise that may be made in the second breakdown resistance of the transistor.

Surface arcing may be produced, especially by short rise-time voltage transients, when the peak voltage across reverse-biased junctions exceeds the rated voltage of the junctions involved. The arc may form a conducting path along the surface and thereby produce a short circuit. This may occur across the collector-base junction in high voltage mesa transistors. It may also occur along the silicon-to-oxide-passivation interface between two evaporated leads which connect at least one p-n junction.

High-temperature stresses may result in the formation of tin "solder-balls" in transistors using a tin-based alloy. After being formed, they may be jolted loose and relocated at a site which will produce a short circuit. Temperatures in excess of the melting temperature of tin (231°C) are believed to be required for their formation. Among the overstresses that may produce such temperatures is a momentary excursion into second breakdown.

While electrical or thermal overstress is usually the cause for failure, it is important to recognize that physical overstress to the package can also lead to device failure. For example, with stud-mounted packages, it is important to use the recommended mounting torque, which is given for clean, dry threads. Excessive torque can deform the semiconductor die mounting surface and produce failure especially under temperature- or power-cycling conditions.

5.3.3 Degradation

Some change in the transistor's electrical parameters with time is considered normal. Such changes can take place during storage or operation. Degradation is defined to occur when such changes are so large that one or more of these parameters no longer meets the limits of the registration or those limits agreed upon by the buyer and seller. Those parameters which are most often found to vary are the junction leakage currents and the transistor gain. The user may reduce such changes and hence also the possibility of degradation by operating within the conditions specified by the maximum ratings, especially for temperature and maximum operating conditions.

5.4 EFFECT OF TEMPERATURE VARIATIONS ON ELECTRICAL PARAMETERS

The electrical parameters of semiconductor devices are temperature sensitive. This face should be taken into consideration whenever a parameter of a semiconductor is being measured or is being relied upon. In an effort to eliminate a device temperature variation during measurements, the industry has adopted short pulse, low duty cycle tests (usually 300 μs at 1 or 2% duty cycle). This is particularly necessary for measurements of power semiconductors because of the high power levels involved during some of the measurements.

Some general rules of how different parameters behave with temperature are as follows:

(1) I_{CBO}, I_{EBO}. Each of these parameters may be divided into two components; the bulk and the surface leakage. In general, the bulk leakage will double for every 10°C rise for germanium devices and will double for every 8°C rise for silicon devices. The surface component is rather unpredictable but, in general, it will increase with temperature. Since the surface leakage is the predominant component, it is almost impossible to extrapolate the actual leakage of a typical power transistor at high temperature.

(2) V_{EB}, V_{CB}. The temperature coefficient of the forward voltage for both transistor junctions depends on the forward voltage itself and the temperature. Only at the highest currents may the temperature coefficient be positive, otherwise, it is negative. For small currents, the rule of thumb is that the coefficient is -2.0 mV/°C.

(3) h_{FE}. The temperature coefficient of the transistor gain depends on the device structure as well as on the current and temperature. Generally, the temperature coefficient of gain is positive for all but the extreme conditions of current and temperature where it then may be negative.

(4) $V_{(BR)CBO}$, $V_{(BR)EBO}$, $V_{(BR)CEO}$. In general, the temperature coefficients of $V_{(BR)CBO}$ and $V_{(BR)EBO}$ are positive for silicon, and negative for germanium transistors. The temperature coefficient of $V_{(BR)CEO}$ at low currents of both silicon and germanium transistors is negative. At large currents, it may be positive or negative.

(5) t_d, t_r, t_s, t_f. The effect of temperature on t_r and t_f varies for different transistor types and cannot be defined. The temperature coefficients of t_d and t_s are more consistent. Except for extreme operating conditions, the temperature coefficient of t_d is negative and t_s is positive. It should be noted that the temperature coefficient of t_s is larger than those of all the other switching parameters, which together comprise the total switching time of the transistor.

5.5 SIMPLE MEASUREMENTS IN TROUBLE SHOOTING TRANSISTOR CIRCUITS

5.5.1 Introduction

For most people, trouble shooting is as much a part of the equipment design process as breadboarding and worst case analyses. This section will discuss briefly some of the basic tools and techniques of trouble shooting. For the purposes of this discussion, it will be assumed the circuit is one that has been designed by or is of a type with which the engineer is familiar.

5.5.2 Tools

(1) The Circuit Diagram - Though one feels one knows the circuit totally, a circuit diagram is a necessity.

(2) Soldering Iron - Ideally, the iron should be transformer isolated from the power line or it should have a 3-wire cord so the body of the iron can be grounded to eliminate leakage currents to the tip. If this is not possible, the iron tip should be periodically checked with a neon bulb for leakage.

(3) Clip Leads of Various Lengths - The more the better.

(4) A 20,000 Ω/V Volt-Ohm Meter (VOM) - Extremely useful. Make a record of the voltage, polarity, and short circuit current for each Ohms range position of the VOM.

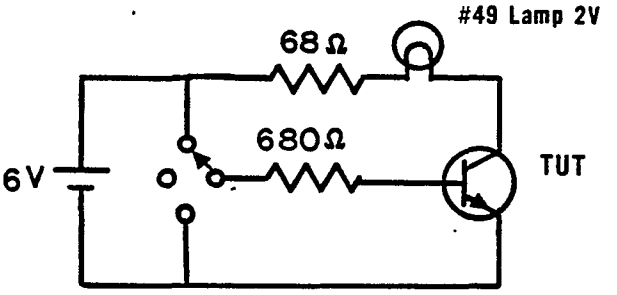
(5) An Electronic Voltmeter - It should have a position for 0.5 volt full scale deflection. Also, it is most desirable that it have a floating common which will permit the unit to measure potential drops where both points are above ground.

(6) An Electric Hairdryer and Cold Spray - Indispensable when searching for temperature sensitive defects.

(7) A Small Portable Radio - A good indicator of oscillations.

5.3.3 Basic Transistor Tests

(1) Go-No-Go Test - The circuit below shows a go-no-go tester for bipolar transistors. The connections are shown for a NPN transistor. When the base resistor is connected to the plus side of the battery, the lamp will light if the transistor is operative; likewise, the lamp will go out if the resistor is in the open position or connected to the emitter side of the battery.



(2) Ohmmeter Test - A rough but useful check of the condition of the junctions may be made with an ohmmeter. First, however, the polarity of the ohmmeter leads should be determined.

The forward resistance of both junctions may be measured first. A normal unit will have less than 500 ohm resistance. Reversing the leads, the reverse resistance of the junctions may then be measured. Here, one needs to know the battery voltages of the ohmmeter. Do not use an ohms position which entails a battery voltage greater than 4.5 volts. A higher voltage could endanger mesa and planar emitter junctions. The reverse leakage resistance of a normal unit will be 500,000 ohms or greater.

Repeat - do not use an ohm scale that requires battery voltages greater than 4.5 volts when measuring the reverse resistance of a junction.

5.5.4 Circuit Tests

(1) Quiescent (Q) Point Tests - This is basically the same routine used in radio and TV servicing, with some refinements:

(a) Refer to the existing circuit diagram or draw one of the circuit under consideration. Use Thevenin and Norton equivalents and write Kirchoff loop equations passing through only base-emitter junctions to determine the quiescent voltage (Q point) condition at each base, emitter, and collector.

(b) Check all electrolytics and diodes to ascertain that they have been inserted with the correct polarity and are operable.

(c) Apply power to the circuit. Measure the Q point voltages. Compare each reading with the circuit calculations. Use an electronic voltmeter if possible. If the measured voltages differ vastly from the calculated voltages and yet ohmic tests are satisfactory, an oscillation condition is often present.

(2) Click Test - Should the Q point measurements not show up the difficulty, another technique is "click testing". This may be done by momentarily forcing one device or another into the cut-off condition and observing the voltage change at the collectors of the devices in question. This is especially useful when checking out logic chains and flop-flops.

The device may be forced either by shorting the base to emitter or by using a 1 kΩ to 10 kΩ resistor (depending on the circuit) and a battery of appropriate value and polarity. The latter method is preferred.

When dealing with power devices, it is well to remember that transistors seldom fail by themselves. If a defective device is found, the trouble search should continue until one is satisfied that all the defective elements have been located.

(3) Temperature Tests - When the circuit problem is one of intermittents, drifting, or wandering, a Q point test or a test for oscillations, while the circuit is temperature stressed, is worthwhile. A gun-type hairdryer and a bottle of a compressed flurocarbon will quickly heat or cool the troublesome circuit while voltages are monitored or signal trace procedures are followed. This hot-cold technique is good for quickly testing the circuit under worst conditions as well as for locating cold solder joints, poor socket contacts, defective electrolytics, intermittent resistors, solder balls, wire scraps, etc.

(4) Portable Radio Test and Reduced-Voltage Testing - In item (1), the matter of oscillations was mentioned. If when making Q-point readings and the voltages measured appear to be wildly askew and bear little apparent relation to circuit values, parasitic oscillations should be suspected. Of course, the test leads of the VOM could themselves be responsible; however, with solid-state circuits, this is much less likely than with vacuum tubes.

One way of checking for oscillations is to vary the supply voltage and monitor the devices for sudden voltage changes. Quite often, since the oscillations have such a large harmonic content, they may often be heard on a small portable radio placed near the offending chassis. Used with a little ingenuity, a radio can be a great help in fixing this sort of trouble. If the parasitic oscillations can be heard on the portalbe radio, it may be possible to reduce the supply voltage to the troublesome circuit until it just starts to oscillate and then proceed with the trouble shooting routine. As the cures are effected, the voltage can be increased until it is back to the design value. If the oscillation worsens as the voltage is reduced, it is often a symptom of deficient power supply filtering.

When dealing with parasitic problems, one must remember that transistors do not oscillate by themselves. They need power and reactive components to make them oscillate. Search for defective or deficient filtering or bypassing. Do not rely on the "500 μF ought to be enough" attitude. Calculate the reactance of the capacitor at the frequencies of concern and relate the values to the circuit loads and currents. Most modern transistors have cut-off frequencies that were unheard of a few years ago. Many electrolytics do not work very well at high frequencies and may require additional bypassing with ceramic or paper capacitors.

Long emitter leads and low-value, high-wattage wire wound emitter resistors frequently cause trouble. Every reactance in the emitter circuit is multiplied by h_{fe} at the base and can appear as a reactive load to the preceeding stage.

PART 6

MILITARY SPECIFICATIONS

PART 6

MILITARY SPECIFICATIONS

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PART 6

MILITARY SPECIFICATIONS

6.1 PURPOSE AND STRUCTURE

Military specifications are prepared as procurement documents to describe various items purchased by the United States Government. Semiconductor devices are covered under Military Specification MIL-S-19500, "Semiconductor Devices, General Specification for". This document contains the general requirements and provisions for such things as materials, marking, formation of lots, qualification provisions, quality conformance inspection requirements, preparation for delivery, etc., which are applicable to all types of semiconductor devices. It also references other specifications and standards which are applicable such as MIL-STD-750, MIL-S-19491, MIL-STD-105, etc. These are considered to be a part of the specification to the extent specified, which may be the entire document or a single provision such as a particular test method taken from MIL-STD-202.

Particular semiconductor device types are covered by detail specifications prepared under and referencing MIL-S-19500. These detail specifications bear a MIL-S-19500/XXX number and the device types covered are shown in the title. The body of these specifications completely describes the device in terms of its mechanical and electrical characteristics and ratings, and its quality and reliability test requirements. Also, any necessary exceptions to the general specification are taken in the detail specification. A periodic supplement to MIL-S-19500 is available which lists the detail device specifications which have been issued and have remained in active status.

6.2 OTHER SPECIFICATIONS

In addition to those mentioned above which apply only to products, a particular procurement contract or customer order may invoke the requirements of any of several other general Government specifications issued by the DoD agencies.

One of particular importance is MIL-Q-9858A, "Quality Program Requirements". This requires that the contractor establish and maintain a completely documented Quality Control System including control of design, changes, manufacturing processes, product test, and shipping. Another is MIL-I-45208, "Inspection System Requirements". A Government Representative will usually conduct a survey before permitting shipment against a contract which requires compliance to MIL-Q-9858 or MIL-I-45208.

6.3 MILITARY STANDARDS

A number of standards may be referred to in military specifications. These are general purpose descriptions of requirements or testing procedures which are applicable to many classes or types of items; as such, they refer the detailed requirements to the detailed specifications for the particular item. These standards serve these dual purposes:

(1) Reduce the amount of repetitious printing which would be required if all of the procurement information about an item were included in each detail specification.

(2) Standardize test methods and equipment, material requirements, etc. in the interests of economy and of interchangeability of items supplied by different manufacturers.

6.4 PREPARATION, REVISION, AND COORDINATION

MIL-S-19500 and referenced documents are revised or amended as required to incorporate new concepts and to accomplish necessary changes. The formal revision is handled at a joint meeting of the Military Services with invited members of the supplier and user industry present. Suggestions and comments from industry associations such as EIA are given due consideration during these meetings; however, the Services reserve the authority to make all final decisions. Revisions of specifications is indicated by a suffix letter, e.g., MIL-S-19500E, where E is the revision letter. Unless called out otherwise, it is understood that reference to MIL-S-19500 or referenced document, means the latest revision.

6.5 MILITARY PREPARING ACTIVITIES

Naval Electronics System Command
Washington, D. C. 20360
Attn: Code 05143, Me. C. E. Suman

U. S. Army Electronics Command
Fort Monmouth, New Jersey 07703
Attn: AMSEL-PP-EM-2, Mr. J. Deisler

Rome Air Development Center
Griffiss Air Force Base
Rome, New York 13442
Attn: EMNRB, Mr. E. J. Wojnas

Defense Electronics Supply Center
Dayton, Ohio 45401
Attn: DESC-ECS, Mr. N. A. Hauck

Note: DESC acts as agent for the preparing activity, when requested.

Each of the above agencies issues specifications for the use of its Service. When they are issued without formal review and concurrence by the other Services, they are referred to as "single service" or limited coordination (LC) specifications, and may be recognized as such by a parenthetical designation following the slash number such as (NAVY), (EL) or (USAF) to indicate Navy, Army, or Air Force, respectively.

When devices specified in LC specifications are found to be of interest to the other Services, the specification is formally reviewed and concurrence

for use by all Services is reached. The document is then revised and considered to be coordinated and the parenthetical service designator is dropped.

6.6 QUALIFIED PRODUCTS

The "JAN" brand is registered as a U. S. Government certification mark as number 504860 by the U. S. Patent Office.

Before a manufacturer may sell products which bear the military JAN brand, he must meet the qualification requirements of the general specification and applicable detail specification and be approved for listing on the QPL (see section 6.9). Qualification approval is granted by the Qualifying Activity mentioned in the specification after the necessary tests have been successfully conducted and reported.

6.7 QUALIFICATION APPROVAL

The procedure for obtaining qualification approval is detailed in "Provisions Governing Qualification" and in the DESC publication "Qualification Information for Manufacturers". It is essential that any manufacturer who expects to offer qualified products for sale be familiar with these qualification procedures, and that he obtain copies of all pertinent specifications including amendments and referenced documents before initiating testing. The test facilities that the manufacturer desires to use for qualification testing must be approved by the Qualifying Activity. These facilities may be either in the manufacturer's plant or in a commercial laboratory. If the facilities have not been previously found suitable for qualification testing, a list of test facilities and other information about the laboratory must be sent to the Qualifying Activity prior to a survey of the facilities. The time involved may vary considerably depending on the completeness of the information furnished, availability of qualifying activity personnel to conduct a facilities survey, etc.

A manufacturer who desired to qualify a product requests authorization to conduct qualifying tests by submitting the appropriate forms. He receives authorization to conduct the test a short time later. Qualification inspection involves testing specific samples of units in accordance with procedures of the agency involved and under cognizance of a government inspector. A maximum number of allowed defectives is prescribed; excessive failures at this point are a serious setback. Under best possible conditions, testing requires at least six weeks because of 1000-hour life tests. When the testing has been completed, the manufacturer makes a detailed report of test results to the cognizant agency. If he has experienced trouble, he must explain the reasons and outline the corrective action taken. Depending upon the nature of the trouble, he may be required to do only a retest of the sample on the test failed, or a complete qualification test on a new sample.

Qualification is granted two to three weeks after the manufacturer submits a satisfactory report. The total time for this process is usually four to five months if all goes well.

6.8 RESPONSIBILITY FOR TESTING

The current military specification practice places the responsibility on the supplier for the conduct of the required qualification and quality conformance inspection testing. The supplier is also placed under the surveillance of a Government Quality and Assurance Representative (QAR) who is assigned to cover a particular order. Equipment contractors are permitted to request Government Procurement Quality Assurance (PQA) action at subcontract level on items which they purchase for use in military equipment. Government inspection at subcontract level can only be contractually required when authorized by the equipment contractor's QAR.

6.9 QPL LISTING

A "qualified" item of a supplier is placed on a continually updated "Qualified Products List" (QPL) which is used by the Government and by its contractors to determine the eligible suppliers of a particular item covered by a military specification. If a supplier is not listed on the QPL for the desired item, he will ordinarily not be solicited for bids to supply the item. An exception to this status occurs when the Military Qualifying Activity has advised a supplier that his product has passed the qualification testing procedure, but he is not yet listed for the item because of QPL revision and printing time. In this case, he may publicize his qualifications, accept orders for the item, and proceed with acceptance testing using his authorization from the qualifying activity as evidence of his qualification status.

6.10 APPLICABLE REVISION AND ORDER OF PRECEDENCE

In Government procurement practice, the issue of a military specification or standard which is in effect on the date of invitation for bids for an item is considered to apply to the resulting contractor order for the item.

It should be noted that this practice applies to all referenced documents as well as to the detail specification. Because the different documents are revised independently, it is occasionally found that conflicting requirements exist in the detail specification and reference documents. These cases are ultimately resolved by revision of the detail specification but, in the interim, relief is usually afforded by means of suitable interpretation by the preparing activity for the detail specification (listed in 6.5 above). Such interpretation may be requested when the question cannot be resolved by considering the order of precedence of the documents involved, which is:

(1) The contract or purchase order. Its requirements take precedence over all others except as limited by the JAN branding provisions of MIL-S-19500.

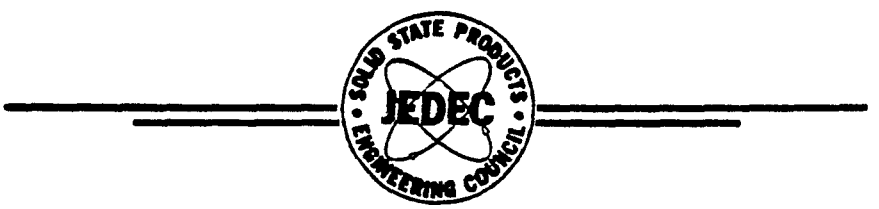
(2) The detail specification for the item.

(3) The general specification for the item.

(4) The referenced documents.

6.11 MILITARY SPECIFICATION FORMAT

Though each component category will have its unique requirements, most specifications follow similar patterns whether they are prepared as a "general" or as a "detailed" specification. Format guidelines, policies, and procedures are strictly governed by Defense Standardization Manual 4120.3-M (formerly M200). Because some "detailed" specifications can become rather lengthy, the front page is devoted to giving a summary of the device's maximum ratings and primary characteristics. This provides the potential user with a quick check list to determine if the devices covered therein can be applied to his circuit design. DESC-ECS (see address in 6.5) has available, upon request, limited quantities of "detail" specification formats covering the more common semiconductor devices such as low power transistors.


SOLID STATE PRODUCTS
JEDEC
ENGINEERING COUNCIL