EIA-397

EIA STANDARD

Recommended Standard for Thyristors

EIA-397

JUNE 1972
(Reaffirmed November, 1979)

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT

NOTICE

EIA Engineering Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or non-member of EIA from manufacturing or selling products not conforming to such Standards and Publications, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than EIA members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by EIA without regard to whether or not their adoption may involve patents on articles, materials, or processes. By such action, EIA does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the Recommended Standard or Publication.

This EIA Standard is considered to have International Standardization implication, but the International Electrotechnical Commission activity has not progressed to the point where a valid comparison between the EIA Standard and the IEC document can be made.

This Standard does not purport to address all safety problems associated with its use or all applicable regulatory requirements. It is the responsibility of the user of this Standard to establish appropriate safety and health practices and to determine the applicability of regulatory limitations before its use.

Published by

Copyright 1972

ELECTRONIC INDUSTRIES ASSOCIATION
Engineering Department
1722 Eye Street
Washington, D.C. 20006

PRICE: $36.00

Printed in U.S.A.

RECOMMENDED STANDARDS FOR THYRISTORS

(From JEDEC Suggested Standard No. 7 and Standards Proposal No. 1101, formulated under the cognizance of JEDEC Committee JC-22 on Rectifier Diodes and Thyristors.)

INDEX

PART 1

THYRISTOR DEFINITIONS

INDEX

1.2.8 Main Terminals

1.2.9 Main Terminal 1 (of a Bidirectional Thyristor)

1.2.10 Main Terminal 2 (of a Bidirectional Thyristor)

1.2.11 Anode Terminal

1.2.12 Cathode Terminal

1.2.13 Gate Terminal

1.3 Electrical Characteristic and Rating Terms

1.3.1 Principal Voltage-Current Characteristic (Principal Characteristic)

1.3.2 Anode-to-Cathode Voltage-Current Characteristic (Anode Characteristic)

1.3.3 On-State

1.3.4 Off-State

1.3.5 Breakover Point

1.3.6 Negative Differential Resistance Region

1.3.7 Reverse Blocking State (of a Reverse Blocking Thyristor)

1.3.8 Off-Impedance

1.3.9 On-Impedance

1.3.10 Reverse Blocking Impedance (of a Reverse Blocking Thyristor)

1.3.11 Principal Voltage

1.3.12 Anode-to-Cathode Voltage (Anode Voltage)

1.3.13 Forward Voltage (of a Reverse Blocking or Reverse Conducting Thyristor)

1.3.14 Off-State Voltage

1.3.15 Working Peak Off-State Voltage

1.3.16 Repetitive Peak Off-State Voltage

1.3.17 Non-Repetitive Peak Off-State Voltage

1.3.18 Critical Rate of Rise of Off-State Voltage

1.3.19 Breakover Voltage

1.3.20 On-State Voltage

1.3.21 Minimum On-State Voltage

1.3.22 Principal Current

1.3.23 On-State Current

1.3.24 Forward Current (of a Reverse Blocking or Reverse Conducting Thyristor)

1.3.25 Repetitive Peak On-State Current

1.3.26 Overload On-State Current

1.3.27 Surge (Non-Repetitive) On-State Current

1.3.28 Critical Rate of Rise of On-State Current

1.3.29 Off-State Current

1.3.30 Repetitive Peak Off-State Current

1.3.31 Breakover Current

1.3.32 Holding Current

1.3.33 Latching Current

1.3.34 Reverse Voltage (of a Reverse Blocking or Reverse Conducting Thyristor)

1.3.35 Working Peak Reverse Voltage (of a Reverse Blocking Thyristor)

1.3.36 Repetitive Peak Reverse Voltage (of a Reverse Blocking Thyristor)

1.3.37 Non-Repetitive Peak Reverse Voltage (of a Reverse Blocking Thyristor)

1.3.38 Reverse Breakdown Voltage (of a Reverse Blocking Thyristor)

1.3.39 Reverse Current (of a Reverse Blocking or Reverse Conducting Thyristor)

1.3.40 Reverse Blocking Current (of a Reverse Blocking Thyristor)

1.3.41 Repetitive Peak Reverse Current (of a Reverse Blocking Thyristor)

1.3.42 Reverse Breakdown Current (of a Reverse Blocking Thyristor)

1.3.43 Gate Voltage

1.3.44 Gate Current

1.3.45 Gate Trigger Voltage

1.3.46 Gate Non-Trigger Voltage

1.3.47 Gate Turn-Off Voltage (of a Turn-Off Thyristor)

1.3.48 Gate Trigger Current

1.3.49 Gate Non-Trigger Current

1.3.50 Gate Turn-Off Current (of a Turn-Off Thyristor)

1.3.51 Thermal Resistance (of a Semiconductor Device)

1.3.52 Transient Thermal Impedance (of a Semiconductor Device)

1.3.53 Gate-Controlled Turn-On Time

1.3.54 Gate-Controlled Delay Time

1.3.55 Gate-Controlled Rise Time

1.3.56 Gate-Controlled Turn-Off Time (of a Turn-Off Thyristor)

1.3.57 Circuit-Commutated Turn-Off Time

1.3.58 Reverse Recovery Time (of a Reverse Blocking Thyristor)

1.3.59 Critical Rate of Rise of Commutation Voltage for Bidirectional Thyristors

1.3.60 Virtual Junction Temperature

PART 1

THYRISTOR DEFINITIONS

1.1 CLASSES OF THYRISTORS

1.1.1 Thyristor

A bistable semiconductor device comprising three or more junctions, which can be switched from the off-state to the on-state or vice versa, such switching occurring within at least one quadrant of the principle voltage-current characteristic. (See Figures 1-5.)

1.1.2 Reverse Blocking Diode Thyristor

A two-terminal thyristor which switches only for positive anode-to-cathode voltages and exhibits a reverse blocking state for negative anode-to-cathode voltages.

1.1.3 Reverse Blocking Triode Thyristor

A three-terminal thyristor which switches only for positive anode-to-cathode voltages and exhibits a reverse blocking state for negative anode-to-cathode voltages.

1.1.4 Reverse Conducting Diode Thyristor

A two-terminal thyristor which switches only for positive anode-to-cathode voltages and conducts large currents at negative anode-to-cathode voltages comparable in magnitude to the on-state voltage.

1.1.5 Reverse Conducting Triode Thyristor

A three-terminal thyristor which switches only for positive anode-to-cathode voltages and conducts large currents at negative anode-to-cathode voltages comparable in magnitude to the on-state voltage.

1.1.6 Bidirectional Diode Thyristor

A two-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

1.1.7 Bidirectional Triode Thyristor

A three-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

1.1.8 Turn-Off Thyristor

A thyristor which can be switched from the on-state to the off-state and vice versa by applying control signals of appropriate polarities to the gate terminal, with the ratio of triggering power to triggered power appreciably less than one.

1.1.9 P-Gate Thyristor

A thyristor in which the gate terminal is connected to the P-region adjacent to the region to which the cathode terminal is connected and which is normally switched to the on-state by applying a positive signal between gate and cathode terminals.

1.1.10 N-Gate Thyristor

A thyristor in which the gate terminal is connected to the N-region adjacent to the region to which the anode terminal is connected and which is normally switched to the on-state by applying a negative signal between gate and anode terminals.

1.1.11 Semiconductor Controlled Rectifier (SCR)

An alternative name used for the reverse blocking triode thyristor.

NOTE: Although not an official definition, the term unidirectional is sometimes used to describe the single switching class of thyristors consisting of reverse blocking and reverse conducting thyristors. This term is useful for comparing or contrasting this class of thyristor with bidirectional thyristors.

1.1 PHYSICAL STRUCTURE NOMENCLATURE

1.2.1 Electrode (of a Semiconductor Device)

An electrical and mechanical contact to a region of a semiconductor device.

1.2.2 Anode

The electrode by which current enters the thyristor, when the thyristor is in the on-state with the gate open-circuited.

NOTE: This term does not apply to bidirectional thyristors.

1.2.3 Cathode

The electrode by which current leaves the thyristor, when the thyristor is in the on-state with the gate open-circuited.

NOTE: This term does not apply to bidirectional thyristors.

1.2.4 Gate

An electrode connected to one of the semiconductor regions for introducing control current.

1.2.5 Collector Junction

The junction across which the polarity of the voltage reverses when switching occurs. See Figure 1.

1.2.6 Junction (of a Semiconductor Device)

A region of transition between semiconductor regions of different electrical properties (e.g., n-n+, p-n, p-p+ semiconductors), or between a metal and a semiconductor.

1.2.7 Terminal (of a Semiconductor Device)

The externally available point of connection to one or more electrodes.

1.2.8 Main Terminals

The terminals through which the principal current flows.

1.2.9 Main Terminal 1 (of a Bidirectional Thyristor)

The main terminal which is named "1" by the device manufacturer.

1.2.10 Main Terminal 2 (of a Bidirectional Thyristor)

The main terminal which is named "2" by the device manufacturer.

1.2.11 Anode Terminal

The terminal which is connected to the anode.

NOTE: This term does not apply to bidirectional thyristors.

1.2.12 Cathode Terminal

The terminal which is connected to the cathode.

NOTE: This term does not apply to bidirectional thyristors.

1.2.13 Gate Terminal

A terminal which is connected to a gate.

1.3 ELECTRICAL CHARACTERISTIC AND RATING TERMS (See note at end of section.)

1.3.1 Principal Voltage-Current Characteristic (Principal Characteristic)

The function, usually represented graphically, relating the principal voltage to the principal current with gate current, where applicable, as a parameter.

1.3.2 Anode-to-Cathode Voltage-Current Characteristic (Anode Characteristic)

A function, usually represented graphically, relating the anode-to-cathode voltage to the principal current with gate current, where applicable, as a parameter.

NOTE: This term does not apply to bidirectional thyristors.

1.3.3 On-State

The condition of the thyristor corresponding to the low-resistance low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).

NOTE: In the case of reverse conducting thyristors, this definition is applicable only for a positive anode-to-cathode voltage.

1.3.4 Off-State

The condition of the thyristor corresponding to the high-resistance low-current portion of the principal voltage-current characteristic between the origin and the break-over point(s) in the switching quadrant(s).

1.3.5 Breakover Point

Any point on the principal voltage-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value. See Figures 2 and 4.

1.3.6 Negative Differential Resistance Region

Any portion of the principal voltage-current characteristic in the switching quadrant(s) within which the differential resistance is negative. See Figures 2 and 4.

1.3.7 Reverse Blocking State (of a Reverse Blocking Thyristor)

The condition of a reverse blocking thyristor corresponding to the portion of the anode-to-cathode voltage-current characteristic for reverse currents of lower magnitude than the reverse breakdown current. See Figure 2.

1.3.8 Off-Impedance

The differential impedance between the terminals through which the principal current flows, when the thyristor is in the off-state at a stated operating point.

1.3.9 On-Impedance

The differential impedance between the terminals through which the principal current flows, when the thyristor is in the on-state at a stated operating point.

1.3.10 Reverse Blocking Impedance (of a Reverse Blocking Thyristor)

The differential impedance between the two terminals through which the principal current flows, when the thyristor is in the reverse blocking state at a stated operating point.

1.3.11 Principal Voltage

The voltage between the main terminals.

NOTE: 1. In the case of reverse blocking and reverse conducting thyristors, the principal voltage is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential.

2. For bidirectional thyristors, the principal voltage is called positive when the potential of main terminal 2 is higher than the potential of main terminal 1.

1.3.12 Anode-to-Cathode Voltage (Anode Voltage)

The voltage between the anode terminal and the cathode terminal.

NOTE: 1. It is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential.

2. This term does not apply to bidirectional thyristors.

1.3.13 Forward Voltage (of a Reverse Blocking or Reverse Conducting Thyristor)

A positive anode-to-cathode voltage.

1.3.14 Off-State Voltage

The principal voltage when the thyristor is in the off-state.

1.3.15 Working Peak Off-State Voltage

The maximum instantaneous value of the off-state voltage which occurs across a thyristor, excluding all repetitive and non-repetitive transient voltages.

1.3.16 Repetitive Peak Off-State Voltage

The maximum instantaneous value of the off-state voltage which occurs across a thyristor, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.

1.3.17 Non-Repetitive Peak Off-State Voltage

The maximum instantaneous values of any non-repetitive transient off-state voltage which occurs across the thyristor.

1.3.18 Critical Rate of Rise of Off-State Voltage

The minimum value of the rate of rise of principal voltage which will cause switching from the off-state to the on-state.

1.3.19 Breakover Voltage

The principal voltage at the breakover point.

1.3.20 On-State Voltage

The principal voltage when the thyristor is in the on-state.

1.3.21 Minimum On-State Voltage

The minimum positive principal voltage for which the differential resistance is zero with the gate open-circuited.

1.3.22 Principal Current

A generic term for the current through the collector junction.

NOTE: It is the current through both main terminals.

1.3.23 On-State Current

The principal current when the thyristor is in the on-state.

1.3.24 Forward Current (of a Reverse Blocking or Reverse Conducting Thyristor)

The principal current for a positive anode-to-cathode voltage.

1.3.25 Repetitive Peak On-State Current

The peak value of the on-state current including all repetitive transient currents.

1.3.26 Overload On-State Current

An on-state current of substantially the same waveshape as the normal on-state current and having a greater value than the normal on-state current.

1.3.27 Surge (Non-Repetitive) On-State Current

An on-state current of short-time duration and specified waveshape.

1.3.28 Critical Rate of Rise Of On-State Current

The maximum value of the rate of rise of on-state current which a thyristor can withstand without deleterious effect.

1.3.29 Off-State Current

The principal current when the thyristor is in the off-state.

1.3.30 Repetitive Peak Off-State Current

The maximum instantaneous value of the off-state current that results from the application of repetitive peak off-state voltage.

1.3.31 Breakover Current

The principal current at the breakover point.

1.3.32 Holding Current

The minimum principal current required to maintain the thyristor in the on-state.

1.3.33 Latching Current

The minimum principal current required to maintain the thyristor in the on-state immediately after switching from the off-state to the on-state has occurred and the triggering signal has been removed.

1.3.34 Reverse Voltage (of a Reverse Blocking or Reverse Conducting Thyristor)

A negative anode-to-cathode voltage.

1.3.35 Working Peak Reverse Voltage (of a Reverse Blocking Thyristor)

The maximum instantaneous value of the reverse voltage which occurs across the thyristor, excluding all repetitive and non-repetitive transient voltages.

1.3.36 Repetitive Peak Reverse Voltage (of a Reverse Blocking Thyristor)

The maximum instantaneous value of the reverse voltage which occurs across the thyristor, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.

1.3.37 Non-Repetitive Peak Reverse Voltage (of a Reverse Blocking Thyristor)

The maximum instantaneous value of any non-repetitive transient reverse voltage which occurs across a thyristor.

1.3.38 Reverse Breakdown Voltage (of a Reverse Blocking Thyristor)

The value of negative anode-to-cathode voltage at which the differential resistance between the anode and cathode terminals changes from a high value to a substantially lower value.

1.3.39 Reverse Current (of a Reverse Blocking or Reverse Conducting Thyristor)

The current for negative anode-to-cathode voltage.

1.3.40 Reverse Blocking Current (of a Reverse Blocking Thyristor)

The reverse current when the thyristor is in the reverse blocking state.

1.3.41 Repetitive Peak Reverse Current (of a Reverse Blocking Thyristor)

The maximum instantaneous value of the reverse current that results from the application of repetitive peak reverse voltage.

1.3.42 Reverse Breakdown Current (of a Reverse Blocking Thyristor)

The principal current at the reverse breakdown voltage.

1.3.43 Gate Voltage

The voltage between a gate terminal and a specified main terminal.

NOTE: Gate voltage polarity is referenced to the specified main terminal.

1.3.44 Gate Current

The current that results from the gate voltage.

NOTE: 1. Positive gate current refers to conventional current entering the gate terminal.

2. Negative gate current refers to conventional current leaving the gate terminal.

1.3.45 Gate Trigger Voltage

The gate voltage required to produce the gate trigger current.

1.3.46 Gate Non-Trigger Voltage

The maximum gate voltage which will not cause the thyristor to switch from the off-state to the on-state.

1.3.47 Gate Turn-Off Voltage (of a Turn-Off Thyristor)

The gate voltage required to produce the gate turn-off current.

1.3.48 Gate Trigger Current

The minimum gate current required to switch a thyristor from the off-state to the on-state.

1.3.49 Gate Non-Trigger Current

The maximum gate current which will not cause the thyristor to switch from the off-state to the on-state.

1.3.50 Gate Turn-Off Current (of a Turn-Off Thyristor)

The minimum gate current required to switch a thyristor from the on-state to the off-state.

1.3.51 Thermal Resistance (of a Semiconductor Device)

The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium.

1.3.52 Transient Thermal Impedance (of a Semiconductor Device)

The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval causing the change of temperature difference.

1.3.53 Gate-Controlled Turn-On Time

The time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified low (high) value during switching of a thyristor from off-state to the on-state by a gate pulse.

1.3.54 Gate-Controlled Delay Time

The time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified value near its initial value during switching of a thyristor from the off-state to the on-state by a gate pulse.

1.3.55 Gate-Controlled Rise Time

The time interval between the instants at which the principal voltage (current) has dropped (risen) from a specified value near its initial value to a specified low (high) value during switching of a thyristor from the off-state to the on-state by a gate pulse.

NOTE: This time interval will be equal to the rise time of the on-state current only for pure resistive loads.

1.3.56 Gate-Controlled Turn-Off Time (of a Turn-Off Thyristor)

The time interval between a specified point at the beginning of the gate pulse and the instant when the principal current has decreased to a specified value during switching from the on-state to the off-state by a gate pulse.

1.3.57 Circuit-Commutated Turn-Off Time

The time interval between the instant when the principal current has decreased to zero after external switching of the principal voltage circuit, and the instant when the thyristor is capable of supporting a specified principal voltage without turning on.

1.3.58 Reverse Recovery Time (of a Reverse Blocking Thyristor)

The time required for the principal current or voltage to recover to a specified value after instantaneous switching from an on-state to a reverse voltage or current.

1.3.59 Critical Rate of Rise of Commutation Voltage (of a Bidirectional Thyristor)

The minimum value of the rate of rise of principal voltage which will cause switching from the off-state to the on-state immediately following on-state current conduction in the opposite quadrant.

1.3.60 Virtual Junction Temperature

A theoretical temperature based on a simplified representation of the thermal and electrical behavior of the semiconductor device.

NOTE: This term (and its definition) is taken from IEC standards. It is particularly applicable to multi-junction semiconductors and is used in this publication to denote the temperature of the active semiconductor element when required in specifications and test methods. The term

"virtual junction temperature" is used interchangeably with the term "junction temperature" in this standard.

NOTE: To aid the reader in understanding the terms "characteristic" and "rating" as applied to electrical devices, the following definitions from IEC Publication No. 134 are offered:

Characteristic

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Rating

A value which established either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

NOTE: Limiting conditions may either be maxima or minima.

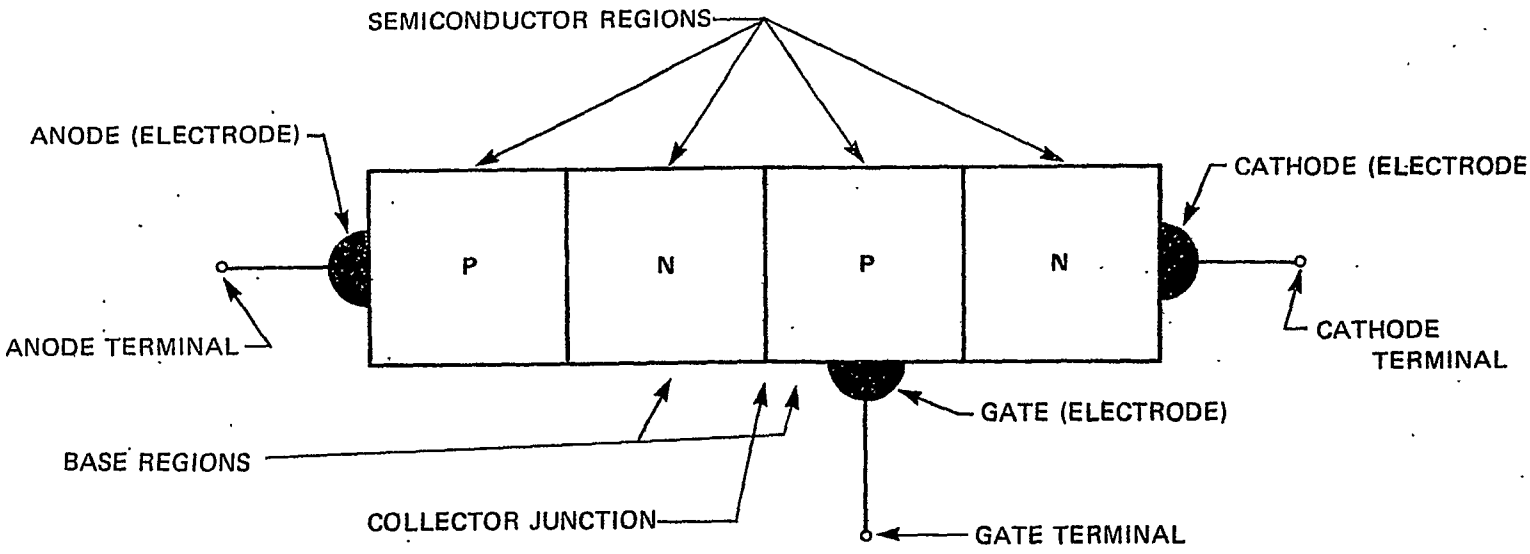


Fig. 1 – Schematic representation of a reverse blocking triode thyristor. (Note: The gate electrode is connected to the N type base region in some structures or omitted in the case of a diode thyristor.)

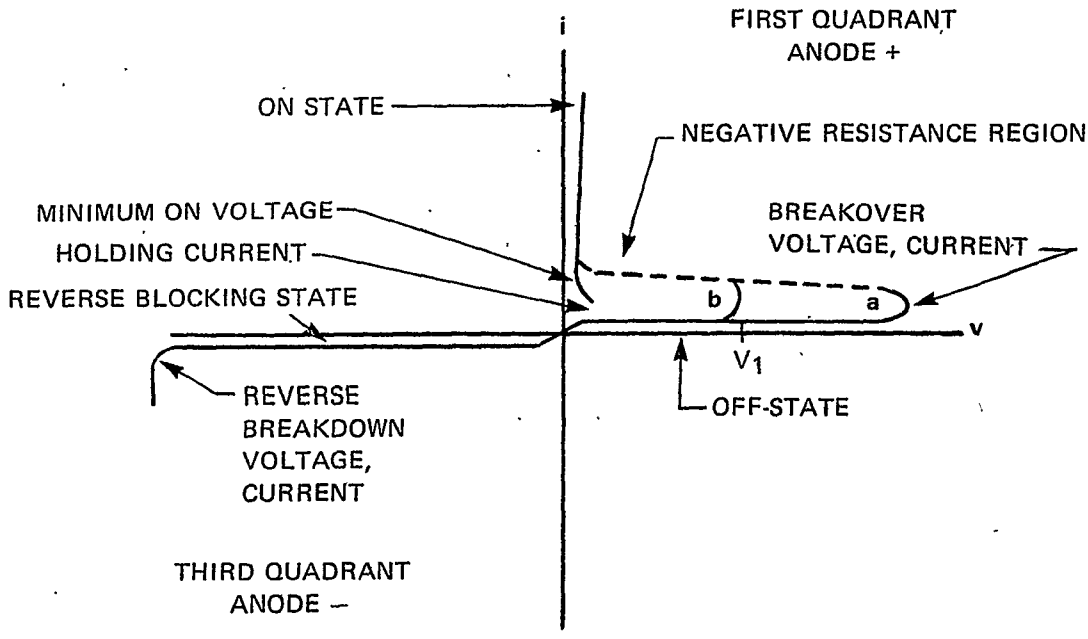


Fig. 2 – Principal voltage-current characteristics (Anode-to-cathode voltage – current characteristic) of a typical reverse blocking thyristor. (Note: Curve "a" applies for zero gate current or a diode thyristor. Curve "b" is with gate trigger present when off-state voltage is V_1).

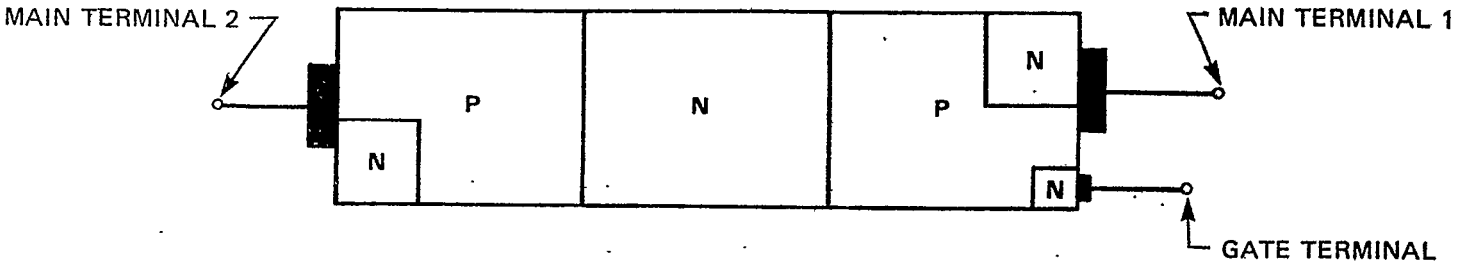


Fig. 3 — Schematic representation of typical bidirectional triode thyristor. (Note: Gate is omitted in a diode bidirectional thyristor.)

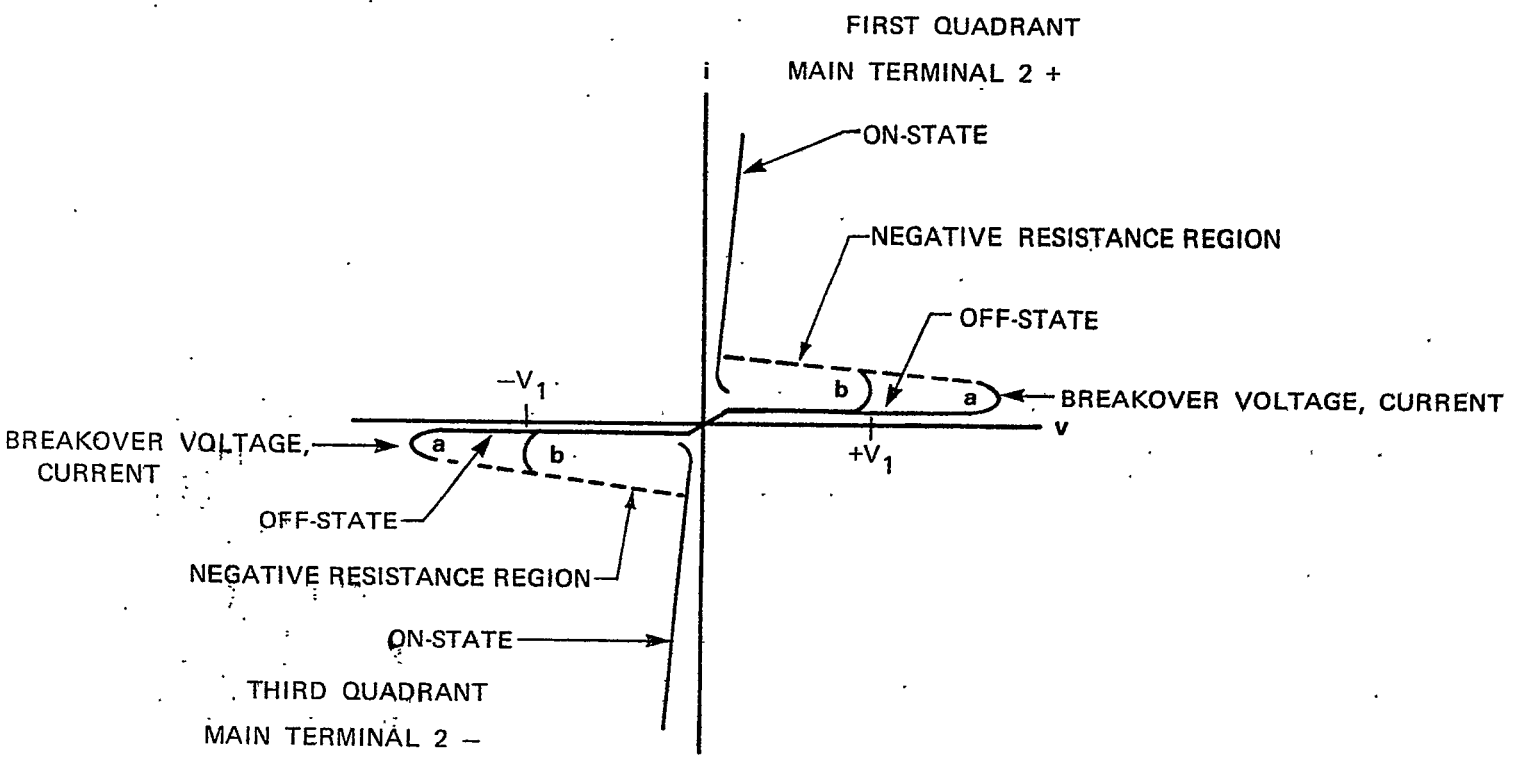


Fig. 4 — Principal voltage-current characteristic of a typical bidirectional thyristor. (Note: Curve "a" applies for zero gate current or a diode bidirectional thyristor. Curve "b" applies for the case of gate trigger current applied when the off-state voltage is $\pm V_1$.)

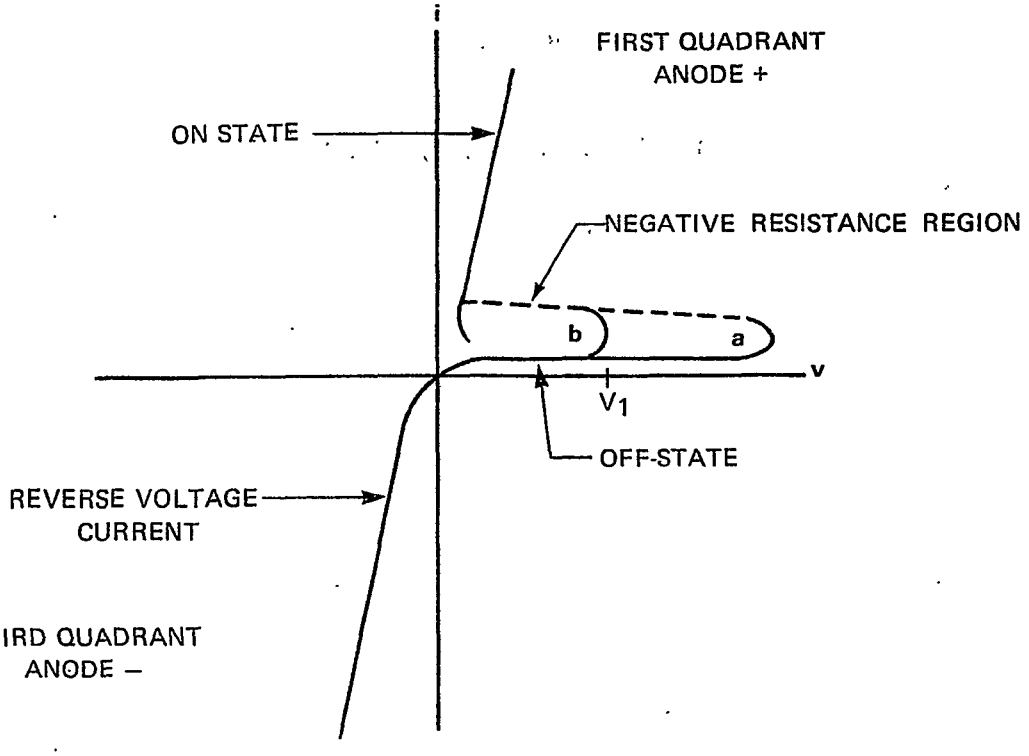


Fig. 5 – Principal voltage-current characteristic (Anode-to-cathode voltage – current characteristics) of a typical reverse conducting thyristor. (Note: Curve 'a' applies for zero gate current or a diode thyristor. Curve 'b' applies with gate trigger current present when off-state voltage is V_1).

THYRISTORS			
Behavior in the Third Quadrant / Number of Terminals	Blocking	Conducting	Switching
2	Reverse Blocking Diode Thyristor	Reverse Conducting Diode Thyristor	Bidirectional Diode Thyristor
3	Reverse Blocking Triode Thyristor	Reverse Conducting Triode Thyristor	Bidirectional Triode Thyristor

TABLE 1 – THYRISTOR IDENTIFICATION TABLE

PART 2

THYRISTOR LETTER SYMBOLS

INDEX

PART 2

THYRISTORS LETTER SYMBOLS*

2.1 GENERAL LETTER SYMBOLS

Ambient Temperature	T_A
Case Temperature	T_C
Virtual Junction Temperature	T_J
Storage Temperature	T_{stg}
Thermal Resistance	R_θ
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$
Thermal Resistance, Case-to-Ambient	$R_{\theta CA}$
Transient Thermal Impedance	$Z_{\theta(t)}$
Transient Thermal Impedance, Junction-to-Ambient	$Z_{\theta JA(t)}$
Transient Thermal Impedance, Junction-to-Case	$Z_{\theta JC(t)}$
Delay Time	t_d
Rise Time	t_r
Fall Time	t_f
Reverse Recovery Time	t_{rr}
Gate-Controlled Turn-On Time	t_{gt}
Gate-Controlled Turn-Off Time	t_{gq}
Circuit-Commutated Turn-Off Time	t_q

*For data sheets, specifications and technical reports prepared on a typewriter and intended for reproduction by a photo-offset process, the use of conventional typewriter type faces is recommended for letter symbols including letter or numerical subscripts and parenthetical descriptive information – Section A, JEDEC Publication No. 77

2.2 DEVICE LETTER SYMBOLS

2.2.1 Letter Symbol Subscripts

The following letters are used as qualifying subscripts for Thyristor Letter Symbols.

A-a	Anode	W	Working
K-k	Cathode	O-o	Open Circuit
G-g	Gate	S-s	Short Circuit, or as a Second Subscript, Non-Repetitive
R-r	Reverse or, as a Second Subscript, Repetitive	X-x	Specified Circuit
D-d	Off-State, Non-Trigger	H-h	Holding
T-t	On-State, Trigger	(BR)	Breakdown
M-m	Maximum Value	(BO)	Breakover
MIN-min	Minimum Value	Q-q	Turn-Off, Recovery
AV-av	Average Value	(TO)	Threshold
RMS	Total RMS Value	(OV)	Overload

2.2.2 Letter Symbol Table

Quantity	Total RMS Value	DC Value, No Alternating Component	DC Value, With Alternating Component	Instantaneous Total Value	Maximum (Peak) Total Value
On-State Current	$I_{T(RMS)}$	I_T	$I_{T(AV)}$	i_T	I_{TM}
Repetitive Peak On-State Current	–	–	–	–	I_{TRM}
Surge (Non-Repetitive) On-State Current	–	–	–	–	I_{TSM}
Overload On-State Current	–	–	–	–	$I_{T(OV)}$
Breakover Current	–	$I_{(BO)}$	–	$i_{(BO)}$	
Off-State Current	$I_{D(RMS)}$	I_D	$I_{D(AV)}$	i_D	I_{DM}
Repetitive Peak Off-State Current	–	–	–	–	I_{DRM}
Reverse Current	$I_{R(RMS)}$	I_R	$I_{R(AV)}$	i_R	I_{RM}

2.2.2 Letter Symbol Table (continued)

Quantity	Total RMS Value	DC Value, No Alternating Component	DC Value With Alternating Component	Instantaneous Total Value	Maximum (Peak) Total Value
Repetitive Peak Reverse Current	–	–	–	–	I_{RRM}
Reverse Breakdown Current	–	$I_{(BR)R}$	–	$i_{(BR)R}$	–
On-State Voltage	$V_{T(RMS)}$	V_T	$V_{T(AV)}$	v_T	V_{TM}
Breakover Voltage	–	$V_{(BO)}$	–	$v_{(BO)}$	–
Off-State Voltage	$V_{D(RMS)}$	V_D	$V_{D(AV)}$	v_D	V_{DM}
Minimum On-State Voltage	–	$V_{T(MIN)}$	–	–	–
Working Peak Off-State Voltage	–	–	–	–	V_{DWM}
Repetitive Peak Off-State Voltage	–	–	–	–	V_{DRM}
Non-Repetitive Peak Off-State Voltage	–	–	–	–	V_{DSM}
Reverse Voltage	$V_{R(RMS)}$	V_R	$V_{R(AV)}$	v_R	V_{RM}
Working Peak Reverse Voltage	–	–	–	–	V_{RWM}
Repetitive Peak Reverse Voltage	–	–	–	–	V_{RRM}
Non-Repetitive Peak Reverse Voltage	–	–	–	–	V_{RSM}
Reverse Breakdown Voltage	–	$V_{(BR)R}$	–	$v_{(BR)R}$	–
Holding Current	–	I_H	–	i_H	–
Latching Current	–	I_L	–	i_L	–
Gate Current	–	I_G	$I_{G(AV)}$	i_G	I_{GM}
Gate Trigger Current	–	I_{GT}	–	i_{GT}	I_{GTM}
Gate Non-Trigger Current	–	I_{GD}	–	i_{GD}	I_{GDM}
Gate Turn-Off Current	–	I_{GQ}	–	i_{GQ}	I_{GQM}
Gate Voltage	–	V_G	$V_{G(AV)}$	v_G	V_{GM}
Gate Trigger Voltage	–	V_{GT}	–	v_{GT}	V_{GTM}
Gate Non-Trigger Voltage	–	V_{GD}	–	v_{GD}	V_{GDM}
Gate Turn-Off Voltage	–	V_{GQ}	–	v_{GQ}	V_{GQM}
Gate Power Dissipation	–	P_G	$P_{G(AV)}$	P_G	P_{GM}

PART 3

THYRISTOR REGISTRATION FORMATS

INDEX

NOTE: The formats in this part are included for the purpose of illustration. For device registration purposes, contact the EIA Type Administration Office, at 2001 Eye Street, N.W., Washington, D.C., 20006 for the latest revisions. Notation at the bottom of the first page of each registration data format indicates the issue number and date.

PART 3

THYRISTOR REGISTRATION FORMATS

3.1 GENERAL DESCRIPTION AND PURPOSE OF REGISTRATION

Semiconductor manufacturers may register with JEDEC the devices they manufacture for sale. The actual registration procedure and type number assignment system are administered by the Electronic Industries Association.

The purpose of the type designation and registration system is to facilitate the purchase and distribution of solid state devices by non-technical individuals. The registration procedures are designed to ensure that devices registered with the JEDEC Solid State Products Council differ from each other in performance characteristics or physical dimensions.

The following are some of the many ways in which the JEDEC registration system is useful to many segments of the electronics industry: (1) A single number replaces the multiple house numbers of various manufacturers that would be used where there are two or more manufacturers of a particular device. (2) Publication of the registration information encourages multiple sources of supply. (3) The specifications of registered devices carrying the authorized designations cannot be changed at will by the first or any subsequent manufacturer, thus promoting standardization and interchangeability. (4) Types registered under the JEDEC system can be more easily compared because defining characteristics of the specification must be based upon standard test conditions and registered according to standard formats. (5) JEDEC registration provides a permanent record for future procurement in those cases where the original manufacturers no longer exist or make the type.

Registration consists of the assignment of type designations to solid state devices in accordance with established rules, recording of the assignment and defining data, and the full dissemination of the information to the electronics industry.

Registration procedures and rules are established by the Joint Electron Device Engineering Council, which is sponsored jointly by the Electronic Industries Association and the National Electrical Manufacturers Association. In any event, JEDEC neither assumes liability for nor endorses the use of, any products which bear its authorized registration number. The Council has as its primary objective the development of recommended standards in the field of solid state devices. An effective registration procedure is considered basic to the achievement of that end.

3.2 BRIEF OUTLINE OF REGISTRATION PROCEDURES

3.2.1 Request

The manufacturer furnishes to the Type Administrator defining data for a device in accordance with the applicable registration format and requests assignment of a type designation.

3.2.2 Assignment

The Type Administrator assigns a type designation and notifies the manufacturer of the assignment.

3.2.3 Release (Public Announcement)

Within one hundred and twenty (120) days after date of assignment, the Type Administrator announces the registration of the type by distributing the data to the manufacturers of solid state devices and to users.

3.2.4 Reregistration and Correction Notice

Once data on a type has been released, it is possible to change the defining data for that type only by either of two methods:

1) Correction Notice

   In those cases where an error has been discovered in the data submitted, a correction notice may be filed only by the original sponsor or the Type Administrator within sixty (60) days after registration.

2) Reregistration

   Any device manufacturer may, at any time, propose a reregistration to change the registered values for a device. In order for the change to be adopted, however, there must be no opposition to the proposal from any other manufacturer of the device.

3.2.5 Suffix Letter Registration Numbers

It is possible for a manufacturer to register a device that is very similar to an existing type by obtaining a new type number that is identical to the existing one except a suffix letter is added. In this case the new device must be mechanically interchangeable, must possess the same ratings, but must possess some superior characteristics when compared to the existing device. The new device with the suffix letter must be unilaterally interchangeable with the existing type.

NOTE: For a detailed explanation of the procedures and rules governing semiconductor device type registration, refer to latest issue of JEDEC Publication No. 15, "Semiconductor Device Type Assignment Procedures."

3.3 THYRISTOR REGISTRATION FORMATS

The formats that follow are included for the purpose of illustration. For device registration purposes, the reader is advised to contact the EIA Type Administration Office, at 2001 Eye Street, N.W., Washington, D.C. 20006, for the latest revisions. Notation at the bottom of the first page of each registration data format indicates the issue number and date.

3.3.1 Thyristor, Triode RDF-1

JOINT ELECTRON DEVICE ENGINEERING COUNCIL

REGISTRATION DATA

THYRISTOR, TRIODE

M I. GENERAL DESCRIPTION

This device is a *germanium, silicon, etc.,* *III.C.1.a or III.C.2.a AVG, dc* ampere rated reverse *blocking or conducting,* triode thyristor designed primarily for *general switching, phase control, etc.,* in *consumer, industrial, military, etc.* service. The gate signal is referenced to the cathode. *The device also has gate turn-off characterization upto* _____ *A dc.*

Refer to Note 7 when registering a thyristor with an integral heat dissipator.

M II. MECHANICAL DATA

A. OUTLINE: TO-_____

If no applicable registered outline exists, an outline drawing must be furnished in conformance with "JEDEC Type Registration for Semiconductor Devices, Preparation of Outline Drawings," EIA Standard RS-308.

B. TERMINAL DESIGNATIONS

TERMINAL	ELEMENT
1	_____
2	_____
3	_____
Case	_____

Indicate all unconnected terminals as "NC". If the case is metallic and if the case is unconnected, state "all leads insulated from case."

C. HANDLING PRECAUTIONS *Include all necessary handling precautions.*

D. MOUNTING POSITIONS *Include any restrictions on mounting positions.*

III. MAXIMUM RATINGS

A. Temperature

M 1. Operating temperature *See Note 1.*

Temperature reference point: _____

Temperature reference point must be on the case or on a lead adjacent to the case. State exact point of temperature measurement.

a. Minimum operating temperature (T_1) _____ °C

b. Normal range (no derating) (T_2) _____ °C to (T_3) _____ °C

c. Temperature for current given in III.C.1.b or III.C.2.b (T_4) _____ °C

If T_4 is specified for Item III.C.2.b, then this reference must be verified on the completed data sheet, as it may be affected by the renumbering of the items in accordance with Instruction 3 at end of this format.

d. Maximum operating temperature (T_5) _____ °C

The values supplied for T_1 through T_5 above are the values which should be used throughout the format.

M 2. Storage temperature range (T_{stg}) (T_6) _____ °C to (T_7) _____ °C

3. Lead or terminal temperature for soldering purposes at a distance ≥ 1/16" from the seated surface (or case) for _____ seconds _____ °C

4. Maximum operating junction temperature _____ °C

B. Voltage at T_2 to T_5 *See Note 2.*

M *Specify either Item 1 or 2 below.*

1. Alternating principal voltage, 50-400 Hz

Gate bias conditions:

Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

a. Repetitive peak off-state voltage, half sine wave (V_{DRM}) _____ V

b. Repetitive peak reverse voltage, half sine wave (V_{RRM}) _____ V

c. Non-repetitive peak reverse voltage, half sine wave (V_{RSM}) _____ V

2. Direct principal voltage

   Gate bias conditions:

   Source voltage = _____ V and
   Source resistance = _____ Ω or
   Gate bias resistance = _____ Ω

   a. Off-state voltage (V_D) _____ V

   b. Reverse voltage (V_R) _____ V

3. Peak positive anode voltage _____ V

   Gate bias conditions:

   Source voltage = _____ V and
   Source resistance = _____ Ω or
   Gate bias resistance = _____ Ω

4. Peak negative gate voltage (V_{GM}) _____ V

C. Current

M *Specify Items III.C.1 and III.C.5.a and b if Item III.B.1 was chosen; specify Items III.C.2 and III.C.5.d if Item III.B.2 was chosen.*

1. Full cycle average on-state current, half sine wave [$I_{T(AV)}$]

   a. At T_2 to T_3 _____ A, avg

   b. At T_4 *This current must be 1/3, 1/2, or 2/3 of III.C.1.a.* _____ A, avg

2. Direct on-state current (I_T)

   a. At T_2 to T_3 _____ A, avg

   b. At T_4 *This current must be 1/3, 1/2, or 2/3 of III.C.2.a.* _____ A, avg

3. Peak positive gate current (I_{GM}) _____ A

4. Peak repetitive on-state current (I_{TRM}) at T_2 to T_3 _____ A

   Specify pulse width, rise time, duty cycle and gate drive.

5. Surge (non-repetitive) on-state current (I_{TSM})
See Note 3.

a. Peak 1/2 cycle sine wave, 60 Hz at T_3 _____ A

This is preceded and followed by III.C.1.a ampere average current and is preceded by III.B.1.b peak volts and followed by 1/2 cycle of III.B.1.c volts and then III.B.1.b volts.

b. Peak 1/2 cycle sine wave, 1.5 ms pulse width at T_5 _____ A

This is preceded and followed by no current or voltage.

c. Peak 1/2 cycle sine wave, 0.5 ms pulse width at T_5 _____ A

This is preceded by III.B.1.a peak volts and followed by no current or voltage.

Gate trigger pulse conditions:

Source voltage = _____ V
Source resistance = _____ Ω
Rise time = _____ μs
Width = _____ μs

d. Peak rectangular pulse at T_3 _____ A

Specify pulse width, rise time, duty cycle and gate drive.

This is preceded and followed by III.C.2.a ampere dc.

6. Critical rate of rise of on-state current (di/dt)

a. Repetitive rating at T_5, gate-triggered _____ A/μs

With resistor-capacitor series combination connected across device

R = _____ Ω C = _____ μF

b. Non-repetitive rating at T_5, gate-triggered _____ A/μs

With resistor-capacitor series combination connected across device

R = _____ Ω C = _____ μF

See Note 3.

c. Non-repetitive rating at T_5, breakover-voltage-triggered _____ A/μs

With resistor-capacitor series combination connected across device

R = _____ Ω C = _____ μF

See Note 3.

Test Conditions:

1. Time t_1 = ≥1 μs
2. Peak on-state current = ≥ *2 X(III.C.1.a or III.C.2.a)* _____ A
3. Off-state voltage = *III.B.1.a or III.B.2.a* V
4. Pulse repetition rate for repetitive ratings = 400 pps
5. Gate trigger pulse conditions for gate-triggered cases:

   Source voltage = _____ V
   Source resistance = _____ Ω
   Rise time = _____ μs
   Width = _____ μs

6. Rate of rise of test voltage for the breakover-voltage-triggered case ≤ 1.0 V/μs

7. Repetitive pulse current rating under specified turn-off conditions _____ A, pk

M *Item III.C.7 is required only when Item IV.O is given. This current rating and its conditions are exactly as specified in Item IV.O.*

M D. Gate Power Dissipation at T_3 *See Note 4.*

1. Peak gate power dissipation (P_{GM}) for max pulse width = _____ μs _____ W
2. Average gate power dissipation [$P_{G(AV)}$] for max averaging time = _____ ms _____ W

IV. ELECTRICAL CHARACTERISTICS

M *Specify Items IV.A.1, IV.B.1, and IV.D.1 if Item III.B.1 was chosen; specify Items IV.A.2, IV.B.2, and IV.D.2 if Item III.B.2 was chosen.*

	MIN	MAX
A. Off-State Current		
Gate bias conditions:		
Source voltage = _____V and Source resistance = _____Ω or Gate bias resistance = _____Ω		
1. Repetitive peak off-state current at rated peak V_{DRM} volts at T_S (I_{DRM})		_____ mA
2. Direct off-state current at rated V_D volts dc at T_S (I_D)		_____ mA
B. Reverse Current		
Gate bias conditions:		
Source voltage = _____V and Source resistance = _____Ω or Gate bias resistance = _____Ω		
1. Repetitive peak reverse current at rated peak V_{RRM} volts at T_S (I_{RRM})		_____ mA
2. Direct reverse current at rated V_R volts at T_S (I_R)		_____ mA
C. Peak Negative Gate Current		
At *III.B.4* peak volts with anode open-circuited at T_S (I_{GM})		_____ mA
D. On-State Voltage at 25°C *Case or Ambient* Temperature		
1. Peak voltage at *π times (III.C.1.a)* peak amperes (V_{TM}) (Pulse width 1 to 2 ms, duty cycle ≤ 2%)		_____ V

		MIN	MAX
	2. Direct voltage at *III.C.2.a* amperes (V_D) (Pulse width 1 to 2 ms, duty cycle ⩽ 2%)		_____ V

E. DC Gate Trigger Voltage

Gate bias conditions:

Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

M	1. At anode source voltage = 12V pk *(6V is a permissible option)*, R_L = _____ Ω at T_2 (V_{GT})		_____ V
	2. At anode source voltage = *III.B.1.a or III.B.2.a* volts, R_L = _____ Ω at T_5 (V_{GT})	_____	V

F. DC Gate Trigger Current

Gate bias conditions:

Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

Specify whether trigger current is measured into network plus device or only measured into device.

M	1. At anode source voltage = 12V pk *(6V is a permissible option)*, R_L = _____ Ω at T_2 (I_{GT})		_____ mA
	2. At anode source voltage = *III.B.1.a or III.B.2.a* volts, R_L = _____ Ω at T_5 (I_{GT})	_____	mA

G. Holding Current (I_H)

M	1. At T_2		_____ mA
	2. At T_5	_____	mA

	MIN	MAX	

Test Conditions:

1. Gate bias conditions
   Source voltage = _____ V and
   Source resistance = _____ Ω or
   Gate bias resistance = _____ Ω

2. Anode source voltage = 12V pk
   (6V and 24V are permissible options)

3. Peak initiating on-state current = ____mA

   Current must be high enough to assure device is fully turned on and of short duration to limit junction heating.

H. Latching Current (I_L)

1. At T_2 _____ mA
2. At T_5 _____ mA

Test Conditions:

1. Gate bias conditions
   Source voltage = _____V and
   Source resistance = _____ Ω or
   Gate bias resistance = _____ Ω

2. Anode source voltage = 12V pk
   (6V and 24V are permissible options)

3. Gate trigger pulse conditions
   Source voltage = _____ V and
   Source resistance = _____ Ω
   Pulse width = _____ μs
   Rise time = _____ μs
   Fall time = _____ μs
   Repetition rate = 60 pps

M *For gate turn-off devices complete I and J.*

I. Peak Gate Turn-Off Voltage at T_3 (V_{GQM}) _____ V

Test Conditions:

1. Anode source voltage = _____V
   Max rated V_{DRM} or V_D preferred.

MIN MAX

2. Load current from _____ A dc min
to _____ A dc max

3. Minimum gate pulse width = _____ μs

4. Load inductance = _____mH

5. Gate bias conditions

Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

J. Peak Gate Turn-Off Current at T_3 (I_{GQM}) _____ mA

Test conditions: Same as in Item _____.

Same as in IV.I but fill in appropriate reference when numbering on data sheet.

K. Gate-Controlled Turn-On Time (t_{gt})

M *Specify 1 and 2, or 3 below.*

1. Delay time (t_d) _____ μs
2. Rise time (t_r) _____ μs
3. Total turn-on time _____ μs

Test conditions:

1. Gate bias conditions:

Source voltage = _____V and
Source resistance = _____Ω or
Gate bias resistance = _____Ω

2. Gate trigger pulse conditions:

Source voltage = _____ V and
Source resistance = _____ Ω
Pulse width = _____ μs
Rise time = _____ μs

3. Temperature = _____°C

4. Off-State voltage = _____V *III.B.1.a or III.B.2.a value preferred*

	MIN	MAX

5. On-stage current = _____ A π *X (III.C.1.a or III.C.2.a) value preferred*

L. Gate-Controlled Turn-Off Time (t_{gq})

1.	Gate storage time		_____ µs
2.	Gate fall time		_____ µs
3.	Gate pulse width *See Note 5*	_____	µs

Test Conditions:

1. Off-state voltage = *III.B.1.a or III.B.2.a V*
2. On-stage current = _____ A
3. Switching repetition rate = _____ pps
4. Duty cycle = _____ %
5. Temperature = _____ °C
6. Bias network *show circuit*
7. Gate turn-off current peak = _____ mA
   or Gate turn-off pulse _____ V,
   _____ Ω

M. Circuit-Commutated Turn-Off Time

1.	Total turn-off time (t_q)		_____ µs
2.	Reverse recovery time (i_{RX}= _____ mA) (t_{rr})		_____ µs

Test Conditions:

1. On-state current amplitude = _____ A
2. On-state current duration = _____ µs

	MIN	MAX

3. Commutation rate (di/dt) = _____ A/μs
   (the slope of the line connecting 50% points of peak on-state and reverse currents)

4. Peak reverse voltage (max) = _____ V

5. Reverse voltage at t_1 (max) = _____ V

6. Operating temperature = _____ °C

7. Test repetition rate = _____ pps

8. Rate of rise of re-applied off-state voltage (dv/dt) = _____ V/μs

9. Off-state voltage = _____ V

10. Gate bias conditions

    Source voltage = _____ V and
    Source resistance = _____ Ω or
    Gate bias resistance = _____ Ω

N. Critical Rate of Rise of Off-State Voltage (dv/dt)

At T_5, exponential waveform _____ V/μs

Test conditions:

1. Off-state voltage at *rated V_{DRM} volts or rated V_D volts dc*

2. Gate bias conditions:

    Source voltage = _____ V and
    Source resistance = _____ Ω or
    Gate bias resistance = _____ Ω

O. Pulse-Circuit-Commutated Turn-Off Time (t_q)

Turn-off time (t_q) _____ μs

Average power dissipation _____ W

TEST CONDITIONS

1. On-state current pulse time to peak ($t_2 - t_1$) _____ μs
2. On-state current pulse base width ($t_3 - t_1$) _____ μs
3. Peak on-state current (t_2) _____ A
4. On-state current pulse repetition rate _____ pps
5. Peak reverse voltage (t_5) _____ V Max
6. Reverse voltage (t_6) _____ V
7. Peak off-state voltage (t_0, t_8) _____ V
8. Peak reverse current (t_4) _____ A Min
   _____ A Max
9. Rate of rise of off-state voltage (linear ramp) (t_6 to t_8) _____ V/μs
10. Case temperature _____ °C
11. Gate trigger pulse
    Source Voltage _____ V
    Source Resistance _____ Ω
12. Gate trigger pulse width (90% points) _____ μs
    (base width must be less than $t_3 - t_0$ but greater than $t_1 - t_0$)
13. Gate trigger pulse rise time (10% to 90%) _____ μs
14. Gate bias conditions
    Source Voltage and _____ V
    Source Resistance or _____ Ω
    Gate Bias Resistance _____ Ω
15. Reapplied voltage duration ($t_9 - t_8$) _____ μs Min
16. Off-state voltage supply decay (t_8 to t_9) *5% of Test Condition 7 Max*

V. THERMAL CHARACTERISTICS

		MIN	MAX	
M	A. Maximum Steady State Thermal Resistance Between Virtual Junction and Specified Temperature Reference Point *Registration is optional when III.C.1.a or III.C.2.a ≤ 10A.*		_____	°C/W
	B. Transient Thermal Impedance *Register in tabular form or as a curve.*			

		MIN	MAX
M C.	Maximum Thermal Resistance Between Case and Ambient Which Assures Device Blocking Stability Over the Registered Voltage and Temperature Range. *See Note 6.*		
	1. For voltage ratings given in III.B.1.a and III.B.1.b		_____ °C/W
	2. For voltage ratings given in III.B.2.a and III.B.2.b		_____ °C/W

INSTRUCTIONS FOR THE USE OF THE DATA FORMAT

1. *For those items indicated by an "M", all existing blanks must be filled in.*

2. *The data supplied should adequately define the device in terms of interchangeability in the intended application and should distinguish it from existing registered devices. If it is felt that additional data are absolutely necessary to insure interchangeability, the data may be submitted for consideration as part of the registration.*

3. *When preparing a registration data sheet for release, delete all italicized notes, all unused items, and all "M's". Where necessary, renumber items in proper sequence.*

4. *Existing JEDEC standards for measurement methods, preferred values, definitions, and letter symbols shall be used as applicable.*

N.B. All data submitted for registration, whether designated mandatory or not, becomes part of the formal registration. Upon publication of the release, commercial data sheets must include all data exactly as registered, with all registered data identified by asterisks.

NOTES

1. The temperatures T_1 through T_7 are to be selected in accordance with the instructions listed below. T_1, T_2, and T_6 may be decreased in increments of 5°C. T_3, T_4, T_5, and T_7 may be increased in increments of 5°C. No intermediate temperatures are to be used.

   T_1 and T_6 must be specified at 0°C or lower.

   T_2 must be specified at 25°C or lower.

   T_3 must be specified to meet the requirements of the table below, depending upon the value of maximum operating temperature (T_5) specified.

Maximum Operating Temperature (T_5)	Permissible Range of Max Case Temperatures at Full Load (T_3)	Preferred Max Case Temperature at Full Load (T_3)
Case 100°C	40-65	55
Case 125°C	60-85	70
Case 150°C	85-110	100
Case 175°C	to be established	to be established

It is desirable that all thyristors of a given general configuration be registered to have identical temperatures for T_3. It is suggested that the registrant attempt to use a value which is the same as for a similar device which has already been registered.

T_4 must be specified at least 5°C higher than T_3.

T_5 must be specified at least 5°C higher than T_4.

T_7 must be specified equal to T_5 or higher.

2. The electrical ratings of a triode thyristor as used herein are the maximum input voltage rating and maximum on-state current rating that can be continuously obtained over the normal operating temperature range. Provisions are made for registration for two types of usage, ac and dc.

   In the ac case, the device is assumed to operate in a single phase, half wave circuit with 50 to 400 Hz sinusoidal voltage source, resistive load, and a 180° ± 5% conduction angle.

   For the dc case, the device is assumed to operate as a switch in a circuit with a dc source. It is intended that the rating be established on the basis of blocking full rated voltage in either the off-stage or reverse direction immediately (excepting turn-off interval) following conduction of rated on-state current for a period long enough to establish the pulse conditions.

   It is not required to register values for both types of operation, but if this is not done, one type of operation must be consistently followed, i.e., Items III.B.1, III.C.1, III.C.5.a, IV.A.1, IV.B.1 and IV.D.1 represent ac operation and Items III.B.2, III.C.2, III.C.5.d, IV.A.2, IV.B.2, and IV.D.2 represent dc operation. If certain ratings and characteristics are registered at specified gate bias conditions, it is recommended that where practical the same gate bias conditions be used throughout. In all cases, the gate source voltage polarity must be specified.

3. These surges may be repeated after the device has returned to the original thermal equilibrium conditions. The rating is non-repetitive, and the device should be capable of withstanding a minimum of 100 such surges during its life. The device

is not required to retain gate control until the original (thermal equilibrium) conditions are re-established.

4. Gate power dissipation ratings apply simultaneously with other ratings in Section III.

5. Turn-off gate pulse width is defined as the minimum width pulse which will turn the device off under the conditions specified.

6. During block voltage measurements, the test device must be attached to a heat sink of sufficient size to insure that the specified case temperature is not exceeded.

7. When registering a thyristor with an integral heat dissipator, add a statement such as "supplied with an integral heat dissipator" to the descriptive paragraph in Item I, and observe the following:

   a) In Item III.A.1 use ambient temperature as the temperature reference point. The ambient temperature specified shall be that of the incoming fluid and its preferred value, corresponding to rated current (T_3), shall be 40°C. Also to be specified are the cooling conditions; such as type of fluid (air, water, oil, etc.), forced or free convection, velocity or flow of fluid when forced convection is used, and pressure drop across the dissipator under forced-convection flow conditions.

   b) For Items V.A. and V.B, cooling conditions are as specified in Item III.A.1. Delete V.C.

3.3.2 Thyristor, Bidirectional Triode RDF-2

JOINT ELECTRON DEVICE ENGINEERING COUNCIL

REGISTRATION DATA

THYRISTOR, BIDIRECTIONAL TRIODE

M I. GENERAL DESCRIPTION

This device is a *germanium, silicon, etc., III.C.1.a* ampere rms, bidirectional triode thyristor designed primarily for application in *industrial, military, etc.* service. The device may be triggered by a *plus (+) and/or minus (–)* gate signal with Main Terminal 2 positive and by a *plus (+) and/or minus (–)* gate signal with Main Terminal 2 negative.

See Note 1

M II. MECHANICAL DATA

A. OUTLINE: TO- _____

If no applicable registered outline exists, an outline drawing must be furnished in conformance with "JEDEC Type Registration for Semiconductor Devices, Preparation of Outline Drawings," EIA Standard RS-308.

B. TERMINAL DESIGNATIONS

TERMINAL	ELEMENT
1	_____
2	_____
3	_____
Case	_____

Indicate all unconnected terminals as "NC." If the case is metallic and if the case is unconnected, state "all leads insulated from case."

C. HANDLING PRECAUTIONS *Include all necessary handling precautions.*

D. MOUNTING POSITIONS *Include any restrictions on mounting positions.*

III. MAXIMUM RATINGS

A. Temperature

M 1. Operating temperatures *See Note 2*

Temperature reference point:

Temperature reference point must be on the case or on a lead adjacent to the case. State exact point of temperature measurement.

a. Minimum operating temperature (T_1) _____ °C

b. Normal range (no derating) (T_2) _____ °C to (T_3) _____ °C

c. Temperature for current given in III.C.1.b. (T_4) _____ °C

d. Maximum operating temperature (T_5) _____ °C

The values supplied for T_1 through T_5 above are the values which should be used throughout the format.

M 2. Storage temperature range, T_{stg} (T_6) _____ °C to (T_7) _____ °C

3. Lead or terminal temperature for soldering purposes at a distance ≥ 1/16" from the seated surface (or case) for _____ seconds _____ °C

M B. Voltage at T_2 to T_5 *See Note 3*

1. Repetitive peak off-state voltage, half sine wave 50 to *60 or 400 (specify one)* Hz (V_{DRM}) _____ V

Gate bias conditions:
Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

2. Peak principal voltage _____ V

Gate bias conditions
Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

3. Peak positive gate voltage (V_{GM}) _____ V

4. Peak negative gate voltage (V_{GM}) _____ V

C. Current

M 1. On-state rms current, full cycle sine wave, 50 to *60 or 400 (specify one)* Hz ($I_{T(RMS)}$)

a. At T_2 to T_3 _____ A, rms

b. At T_4 *This current must be 1/3, 1/2, or 2/3 of Item III.C.1.a.* _____ A, rms

2. Peak positive gate current (I_{GM}) _____ A

3. Peak negative gate current (I_{GM}) _____ A

M 4. Surge (non-repetitive) on-state current (I_{TSM}) at T_3 *See Note 4* _____ A, peak

One full cycle 60 Hz sine wave surge preceded and followed by *III.C.1.a* current

5. Critical rate of rise of on-state current (di/dt) *See Note 3*

a. Repetitive rating at T_S, gate-triggered With resistor-capacitor series combination connected across device. _____ A/μs

R = _____ Ω C = _____ μF

b. Non-repetitive rating at T_S, gate-triggered With resistor-capacitor series combination connected across device _____ A/μs

R = _____ Ω C = _____ μF

See Note 4

c. Non-repetitive rating at T_S, breakover-voltage-triggered With resistor-capacitor series combination connected across device _____ A/μs

R = _____ Ω C = _____ μF

See Note 4

Test conditions:

1. Time t_1 = ⩾ 1 μs
2. Peak on-state current = ⩾ 2 x *(III.C.1.a)* A
3. Off-state voltage = *III.B.1* V
4. Pulse repetition rate for repetitive ratings = 60 pps
5. Gate trigger pulse conditions for gate-triggered cases

Source voltage = _____ V

Source resistance = _____ Ω

Rise time = _____ μs

Width = _____ μs

6. Rate of rise of test voltage for the breakover-voltage-triggered case ⩽ 1.0 V/μs

M D. Gate Power Dissipation at T_3 *See Note 5*

1. Peak gate power dissipation (P_{GM}) for max pulse width = ____ μs _____ W

2. Average gate power dissipation [$P_{G(AV)}$] for max averaging time = _____ ms _____ W

IV. ELECTRICAL CHARACTERISTICS *See Note 3*

		MIN	MAX	
M	A. Repetitive Peak Off-State Current (I_{DRM}) At T_5 and Rated Peak V_{DRM} Volts		_____	mA

Gate bias conditions:
Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

M	B. Peak On-State Voltage at 25°C *Case or Ambient* Temperature (V_{TM})		_____	V

At $\sqrt{2}$ *X (III.C.1.a)* peak amperes
(Pulse width 1 to 2 ms, duty cycle ≤ 2%)

C. Peak Gate Trigger Voltage, Main Terminal 2 Positive

Minimum gate pulse width _____ μs

1. At source voltage = 12V pk *(6V is a permissible option)*

R_L = ___ Ω, at T_2

M *Specify Item a. and/or b. below.*

a.	Positive gate trigger voltage (V_{GTM})		_____	V
b.	Negative gate trigger voltage (V_{GTM})		_____	V

2. At source voltage = *III.B.1* V:

R_L = ___ Ω, at T_5

a.	Positive gate trigger voltage (V_{GTM})	_____		V
b.	Negative gate trigger voltage (V_{GTM})	_____		V

D. Peak Gate Trigger Voltage, Main Terminal 2 Negative

Minimum gate pulse width = _____ μs

1. At source voltage = 12V pk *(6V is a permissible option)*

R_L = ___ Ω, at T_2

		MIN	MAX	
M	*Specify Item a. and/or Item b. below.*			
	a. Positive gate trigger voltage (V_{GTM})		_____	V
	b. Negative gate trigger voltage (V_{GTM})		_____	V
	2. At source voltage = *III.B.1* V.			
	R_L = ___ Ω, at T_5			
	a. Positive gate trigger voltage (V_{GTM})	_____		V
	b. Negative gate trigger voltage (V_{GTM})	_____		V

E. Peak Gate Trigger Current, Main Terminal 2 Positive

Minimum gate pulse width = _____ μs

1. At source voltage = 12V pk *(6V is a permissible option)*

R_L = ___ Ω, at T_2

M *Specify Item a. and/or b. below.*

a. Positive gate trigger current (I_{GTM}) _____ mA

b. Negative gate trigger current (I_{GTM}) _____ mA

F. Peak Gate Trigger Current, Main Terminal 2 Negative

Minimum gate pulse width = _____ μs

1. At source voltage = 12V pk *(6V is a permissible option)*

R_L = ___ Ω, at T_2

M *Specify Item a. and/or b. below.*

a. Positive gate trigger current (I_{GTM}) _____ mA

b. Negative gate trigger current (I_{GTM}) _____ mA

G. Holding Current (I_H)

M	1. At T_2		_____	mA
	2. At T_5	_____		mA

Test conditions:

1. Gate bias conditions:
   - Source voltage = _____ V and
   - Source resistance = _____ Ω or
   - Gate bias resistance = _____ Ω

MIN MAX

2. Anode source voltage = 12V *(6V and 24V are permissible options)*

3. Peak initiating on-state current = _____ mA

Current must be high enough to assure device is fully turned on and of short duration to limit junction heating.

H. Latching Current (I_L)

1. At T_2 _____ mA

2. At T_5 _____ mA

Test conditions:

1. Gate bias conditions:

Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

2. Anode source voltage = 12V *(6V and 24V are permissible options)*

3. Gate trigger pulse conditions:

Source voltage = _____ V and
Source resistance = _____ Ω
Pulse width = _____ μs
Rise time = _____ μs
Fall time = _____ μs
Repetition = 60 pps

I. Gate-Controlled Turn-On Time (t_{gt})

M *Specify 1 and 2, or 3.*

1. Delay time (t_d) _____ μs

2. Rise time (t_r) _____ μs

3. Total turn-on time _____ μs

Test conditions:

1. Gate bias conditions:

Source voltage = _____ V and
Source resistance = _____ Ω or
Gate bias resistance = _____ Ω

MIN MAX

2. Gate trigger pulse conditions:

Source voltage = _____ V and
Source resistance = _____ Ω
Pulse width = _____ μs
Rise time = _____ μs

3. Temperature = _____°C

4. Off-state voltage _____V *III.B.1 value preferred*

5. On-state current _____A$\sqrt{2}$ *X (III.C.1.a) value preferred*

J. Critical Rate of Rise of Off-State Voltage (dv/dt)

At T_5, Exponential Waveform _____ V/μs

Test conditions:

1. Off-state voltage at *rated V_{DRM} volts*

2. Gate bias conditions:

Source voltage = _____V and
Source resistance = _____Ω or
Gate bias resistance = _____ Ω

K. Critical Rate of Rise of Commutation Voltage _____ V/μs

(The numerical value of the rate of rise of voltage is the slope of the straight line connecting the 10% and 63% test voltage points.)

Test conditions applying for each half cycle of the test voltage and current:

1. Frequency of single phase sinusoidal ac supply = _____Hz
   50, 60 or 400 Hz recommended
2. Peak on-state current ($I_{TM} \simeq \frac{EM}{Z_L}$) = _____A
3. On-state current duration = _____ms
   90% of half cycle recommended
4. Rate of reversal of on-state current (di/dt) = _____A/ms
   The slope of the line connecting the 50% and 0% I_{TM} points; $di/dt \cong 2\pi f I_{TM}$
5. Peak off-state voltage ($V_{DM} \simeq E_M$) = _____V

6. Off-state voltage duration = _____ μs
200 μs min recommended

7. Gate bias conditions (between current pulses)

Gate source voltage = _____ V, and
Gate source resistance = _____ Ω or
Gate bias resistance = _____ Ω

8. Case temperature = _____ °C

V. THERMAL CHARACTERISTICS *See Note 6*

M A. Maximum Steady State Thermal Resistance Between Virtual Junction and Specified Temperature Reference Point _____ °C/W

Registration is optional when III.C.1.a ⩽ 10 amp.

B. Transient Thermal Impedance

Register in tabular form or as a curve.

M C. Maximum Thermal Resistance Between Case and Ambient Which Assures Device Blocking Stability Over the Registered Voltage and Temperature Range. *See Note 7*

1. For voltage ratings given in III.B.1 _____ °C/W

INSTRUCTIONS FOR THE USE OF THE DATA FORMAT

1. *For those items indicated by an "M", all existing blanks must be filled in.*

2. *The data supplied should adequately define the device in terms of interchangeability in the intended application and should distinguish it from existing registered devices. If it is felt that additional data are absolutely necessary to insure interchangeability, the data may be submitted for consideration as part of the registration.*

3. *When preparing a registration data sheet for release, delete all italicized notes, all unused items, and all "M's". Where necessary, renumber items in proper sequence.*

4. *Existing JEDEC standards for measurement methods, preferred values, definitions, and letter symbols shall be used as applicable.*

N.B. All data submitted for registration, whether designated mandatory or not, becomes part of the formal registration. Upon publication of the release, commercial data sheets must include all data exactly as registered, with all registered data identified by asterisks.

NOTES

1. The two principal terminals are designated as Main Terminal 1 (MT1) and Main Terminal 2 (MT2). Main Terminal 1 is defined as the terminal to which the gate signal and MT2 voltage is referenced. Positive gate voltage and current are defined as the gate terminal positive with respect to Main Terminal 1.

2. The temperatures T_1 through T_7 are to be selected in accordance with the instructions listed below. T_1, T_2, and T_6 may be decreased in increments of 5°C. T_3, T_4, T_5, and T_7 may be increased in increments of 5°C. No intermediate temperatures are to be used.

   T_1 and T_6 must be specified at 0°C or lower.

   T_2 must be specified at 25°C or lower.

   T_3 must be specified to meet the requirements of the table below, depending upon the value of maximum operating temperature (T_5) specified.

Maximum Operating Temperature (T_5)	Permissible Range Of Max Case Temperatures at Full Load (T_3)	Preferred Max Case Temperature at Full Load (T_3)
Case 100°C	40-65	55
Case 125°C	60-85	70
Case 150°C	85-110	100
Case 175°C (for future use)	to be established	to be established

   It is desirable that all thyristors of a given general configuration be registered to have identical temperatures for T_3. It is suggested that the registrant attempt to use a value which is the same as for a similar device which has already been registered.

   T_4 must be specified at least 5°C higher than T_3.

   T_5 must be specified at least 5°C higher than T_4.

   T_7 must be specified equal to T_5 or higher.

3. The ratings and characteristics are to be registered on the basis of a symmetrical operation of the device and should be the limiting value for either direction of operation. If a characteristic is sensitive to the gate triggering mode, the mode (or modes) applicable to the registered values should be specified. When specifying gate bias conditions, the polarity of the gate source voltage must be given.

4. These surges may be repeated after the device has returned to the original thermal equilibrium conditions. The rating is non-repetitive, and the device should be capable of withstanding a minimum of 100 such surges during its life. The device is not required to retain gate control until the original thermal equilibrium conditions are re-established.

5. Gate power dissipation ratings apply simultaneously with other ratings in Section III.

6. Thermal characteristics are to be measured with the device operating in only one direction. The values registered are to be the limiting value for either direction. Transient thermal characteristics may be supplied in tabular form or as a curve.

7. During blocking voltage measurements, the test device must be attached to a heat sink of sufficient size to insure that the specified case temperature is not exceeded.

3.3.3 Thyristor, Diode, Power RDF-3

JOINT ELECTRON DEVICE ENGINEERING COUNCIL

REGISTRATION DATA

THYRISTOR, DIODE, POWER

This format applies to devices intended for power control applications. For thyristors intended for signal level applications, refer to formats in the JC-20 series.

M I. GENERAL DESCRIPTION

This device is a *germanium, silicon, etc., III.C.1.a* avg, rms, ampere, *reverse blocking or bidirectional,* diode thyristor designed primarily for application in *industrial, military, etc.* service. The switching of the device is initiated by *voltage breakover, rate of applied voltage, etc.*

M II. MECHANICAL DATA

A. OUTLINE: DO-_____

If no applicable registered outline exists, an outline drawing must be furnished in conformance with "JEDEC Type Registration for Semiconductor Devices, Preparation of Outline Drawings," EIA Standard RS-308.

B. TERMINAL DESIGNATIONS *See Note 1*

TERMINAL	ELEMENT
1	_____
2	_____
Case	_____

Indicate all unconnected terminals as "NC"
If the case is metallic and if the case is unconnected, state "all leads insulated from case."

C. HANDLING PRECAUTIONS *Include all necessary handling precautions.*

D. MOUNTING PRECAUTIONS *Include any restrictions on mounting positions.*

III. MAXIMUM RATINGS

A. Temperature

M 1. Operating temperatures *See Note 2*

Temperature reference point: _____

Temperature reference point must be on the case or on a lead adjacent to the case. State exact point of temperature measurement.

a. Minimum operating temperature (T_1) _____ °C

b. Normal range (no derating) (T_2) _____ °C to (T_3) _____ °C

c. Temperature for current given in III.C.1.b (T_4) _____ °C

d. Maximum operating temperature (T_5) _____ °C

The values supplied for T_1 through T_5 above are the values which should be used throughout the format.

M 2. Storage temperature range (T_{stg}) (T_6) _____ °C to (T_7) _____ °C

3. Lead or terminal temperature for soldering purposes at a distance ≥ 1/16" from seated surface (or case) for _____ seconds _____ °C

B. Voltage at T_2 to T_3 *See Note 3*

M *For reverse blocking devices, specify Items 1 and 2, 50-400 Hz. For bidirectional devices, specify only Item 1, 50-60 Hz or 50-400 Hz.*

1. Repetitive peak off-state voltage, half sine wave *50 to 400 Hz (for reverse blocking devices), 50 to 60 or 400 Hz (for bidirectional devices; specify one)* (V_{DRM}) _____ V

2. Repetitive peak reverse voltage, half sine wave 50-400 Hz (V_{RRM}) _____ V

M C. Current

1. On-state current, *half sine wave, average 50 to 400 Hz ($I_{T(AV)}$) (for reverse blocking devices); full sine wave, rms 50 to 60 or 400 Hz ($I_{T(RMS)}$) (for bidirectional devices; specify one)*

   a. At T_2 to T_3 _____ A, *avg, rms*

   b. At T_4 _____ A, *avg, rms*

2. Surge (non-repetitive) on-state current at T_3 (I_{TSM})

   See Note 4

   For reverse blocking devices, peak 1/2 cycle 60 Hz sine wave surge preceded and followed by *III.C.1.a* current and *III.B.2* reverse voltage. For bidirectional devices, full cycle sine wave 60 Hz surge preceded and followed by *III.C.1.a* current.

IV. ELECTRICAL CHARACTERISTICS *See Note 3*

	MIN	MAX	
M A. Breakover Voltage and Current for Bidirectional Devices			
1. Breakover voltage at T_2 to T_5 (v_{BO}) *For sinusoidal waveforms that do not exceed 60 or 400 Hz.*	_____	_____	V
2. Peak breakover current at T_2 (i_{BO})		_____	mA
M B. *For reverse blocking devices specify Items 1 and 2. For bidirectional devices specify only Item 1.*			
1. Repetitive peak off-state current at rated peak V_{DRM} volts at T_5 (I_{DRM})		_____	mA
2. Repetitive peak reverse current at rated peak V_{RRM} volts at T_5 (I_{RRM})		_____	mA

		MIN	MAX	
M	C. *For reverse blocking devices specify Item 1. For bidirectional devices specify Item 2.*			
	1. Peak on-state voltage at 25°C ambient and π X *(III.C.1.a)* amperes peak, (V_{TM}) (Pulse width 1 to 2 ms, duty cycle ≤ 2%)			_____ V
	2. Peak on-state voltage at 25°C ambient and $\sqrt{2}$ X *(III.C.1.a)* amperes peak, (V_{TM}) (Pulse width 1 to 2 ms, duty cycle ≤ 2%)			_____ V
M	D. Holding Current at T_2 (I_H)			_____ mA
	Test Conditions:			
	1. Anode source = 12V (6V and 24V are permissible options)			
	2. Peaking initiating on-state current = _____ mA			
	Current must be high enough to assure device is fully turned on and of short duration to limit self heating.			
	E. Latching Current T_2 (I_L)			_____ mA
	Test Conditions:			
	1. Voltage trigger pulse			
	a. rise time (10% to 90%) = _____ μs			
	b. peak magnitude = _____ V			
	c. pulse width between 50% points = _____ μs			
	2. Anode source voltage = 12V (6V and 24V are permissible options)			
	3. Test repetition rate = 60 pps			
	F. Turn-On Time at T_2			
	a. delay time (t_d)			_____ μs
	b. rise time (t_r)			_____ μs
	Test conditions:			
	1. Voltage trigger pulse			
	a. rise time (10% to 90%) = _____ μs min			
	b. peak magnitude = _____ V min			
	c. pulse width (between 50% points) = _____ μs			

	MIN	MAX

2. Initital off-state voltage = _____V
III.B.1 value preferred

3. Final on-state current = _____A
π X (III.C.1.a) or $\sqrt{2}$ X (III.C.1.a) value preferred

G. Circuit-Commutated Turn-Off Time

For reverse blocking thyristors only.

1. Total turn-off time (t_q) _____ μs

2. Reverse recovery time (i_{RX} = _____ mA) (t_{rr}) _____ μs

Test conditions:

1. On-state current amplitude = _____ A
2. On-state current duration = _____ μs
3. Test repetition rate = _____ pps
4. Commutation rate (di/dt) _____ A/μs
   Measured as the slope of the straight line connecting the 50% peak on-state and peak reverse current points.
5. Peak reverse voltage (max) = _____ V
6. Reverse voltage at time t_1 (max) = _____ V
7. Operating temperature = _____ °C
8. Rate of rise of reapplied off-state voltage (dv/dt) = _____ V/μs
9. Off-state voltage = _____V

H. Critical Rate of Rise of Off-State Voltage (dv/dt) _____ V/μs

At T_5, exponential waveform

Test conditions:

1. Exponential test voltage waveform
2. Off-state voltage = *III.B.1 V*

V. THERMAL CHARACTERISTICS *See Note 5*

M A. Maximum Steady State Thermal Resistance Between Virtual Junction and Specified Temperature Reference Point _____ °C/W

(Registration is optional for devices with III.C.1.a current ratings ≤ 10 amperes.)

B. Transient Thermal Impedance

Register in tabular form or as a curve.

	MIN	MAX	
C. Maximum Thermal Resistance Between Case and Ambient Which Assures Device Blocking Stability Over The Registered Voltage and Temperature Range. *See Note 6.*			
1. For voltage ratings given in *III.B.1 or III.B.2*			_____ °C/W

INSTRUCTIONS FOR USE OF THE DATA FORMAT

1. *For those items indicated by an "M", all existing blanks must be filled in.*

2. *The data supplied should adequately define the device in terms of interchangeability in the intended application and should distinguish it from existing registered devices. If it is felt that additional data are absolutely necessary to ensure interchangeability, the data may be submitted for consideration as part of the registration.*

3. *When preparing a registration data sheet for release, delete all italicized notes, all unused items, and all "M's". Where necessary, renumber items in proper sequence.*

4. *Existing JEDEC standards for measurement methods, preferred values, definitions, and letter symbols shall be used as applicable.*

N.B. All data submitted for registration, whether designated mandatory or not, becomes part of the formal registration. Upon publication of the release, commercial data sheets must include all data exactly as registered, with all registered data identified by asterisks.

NOTES

1. For bidirectional devices the terminals are designated as Main Terminal 1 (MT1) and Main Terminal 2 (MT-2).

2. The temperatures T_1 through T_7 are to be selected in accordance with the instructions listed below. T_1, T_2 and T_6 may be decreased in increments of 5°C. No intermediate temperatures are to be used.

   T_1 and T_6 must be specified at 0°C or lower.

   T_2 must be specified at 25°C or lower.

   T_3 must be specified to meet the requirements of the table below, depending upon the value of maximum operating temperature (T_5) specified.

Maximum Operating Temperature (T_5)	Permissible Range of Max Case Temperatures at Full Load (T_3)	Preferred Max Case Temperature Full Load (T_3)
Case 100°C	40-65	55
Case 125°C	60-85	70
Case 150°C	85-100	100
Case 175°C (for future use)	to be established	to be established

It is desirable that all thyristors of a given general configuration be registered to have identical temperatures for T_3. It is suggested that the registrant attempt to use a value which is the same as for a similar device which has already been registered.

T_4 must be specified at least 5°C higher than T_3.

T_5 must be specified at least 5°C higher than T_4.

T_7 must be specified equal to T_5 or higher.

3. For bidirectional devices the ratings and characteristics are to be registered on the basis of symmetrical operation of the device, and should be the limiting value for either direction of operation.

4. These surges may be repeated after the device has returned to the original thermal equilibrium conditions. The rating is non-repetitive, and the device should be capable of withstanding a minimum of 100 such surges during its life.

5. For bidirectional devices thermal characteristics are to be measured with the device operating in only one direction. The values registered are to be the limiting values for either direction. Transient thermal characteristics may be supplied in tabular form or as a curve.

6. During blocking voltage measurements, the test device must be attached to a heat sink of sufficient size to insure that the specified case temperature is not exceeded.

PART 4

USE OF REGISTRATION FORMATS

INDEX

4.2 Use of Registration Format for Triode Thyristor, JC-22 RDF-1

4.2.1 General Description

4.2.2 Mechanical Data

4.2.3 Maximum Ratings

4.2.3.1 Temperature

4.2.3.2 Voltage at T_2 to T_5

4.2.3.3 Current

4.2.3.4 Gate Power Dissipation at T_3

4.2.4 Electrical Characteristics

4.2.4.1 Off-State Current

4.2.4.2 Reverse Current

4.2.4.3 Peak Negative Gate Current

4.2.4.4 On-State Voltage at 25°C Ambient or Case Temperature

4.2.4.5 DC Gate Trigger Voltage

4.2.4.6 DC Gate Trigger Current

4.2.4.7 Holding Current

4.2.4.8 Latching Current

4.2.4.9 Peak Gate Turn-Off Voltage at T_3

4.2.4.10 Peak Gate Turn-Off Current at T_3

4.2.4.11 Gate-Controlled Turn-On Time

4.2.4.12 Gate-Controlled Turn-Off Time

4.2.4.13 Circuit-Commutated Turn-Off Time

4.2.4.14 Critical Rate of Rise of Off-State Voltage

4.2.4.15 Pulse-Circuit-Commutated Turn-Off Time

4.2.5 Thermal Characteristics

4.3 Use of Registration Format for Bidirectional Triode Thyristor, JC-22 RDF-2

4.3.1 General Description

4.3.2 Mechanical Data

4.3.3 Maximum Ratings

4.3.3.1 Temperature

4.3.3.2 Voltage at T_2 to T_5 and Current

4.3.3.3 Gate Power Dissipation at T_3

4.3.4 Electrical Characteristics

4.3.4.1 Repetitive Peak Off-State Current

4.3.4.2 Peak On-State Voltage at 25°C Ambient or Case Temperature

4.3.4.3 Peak Gate Trigger Voltage, Main Terminal 2 Positive

4.3.4.4 Peak Gate Trigger Voltage, Main Terminal 2 Negative

4.3.4.5 Peak Gate Trigger Current, Main Terminal 2 Positive

4.3.4.6 Peak Gate Trigger Current, Main Terminal 2 Negative

4.3.4.7 Holding Current

4.3.4.8 Latching Current

4.3.4.9 Gate-Controlled Turn-On Time

4.3.4.10 Critical Rate of Rise of Off-State Voltage

4.3.4.11 Critical Rate of Rise of Commutation Voltage

4.3.5 Thermal Characteristics

4.4 Use of Registration Format for Power Diode Thyristors, JC-22 RDF-3

4.4.1 General Description

4.4.2 Mechanical Data

4.4.3 Maximum Ratings

4.4.3.1 Temperature

4.4.3.2 Voltage at T_2 to T_5

4.4.3.3 Current

4.4.4 Electrical Characteristics

4.4.4.1 Breakover Voltage and Current for Bidirectional Devices

4.4.4.2 Repetitive Peak Off-State and Reverse Currents at T_5

4.4.4.3 Peak On-State Voltage

4.4.4.4 Holding Current

4.4.4.5 Latching Current

4.4.4.6 Turn-On Time at T_5

4.4.4.7 Circuit-Commutated Turn-Off Time

4.4.4.8 Critical Rate of Rise of Off-State Voltage

4.4.5 Thermal Characteristics

PART 4

USE OF REGISTRATION FORMATS

4.1 GENERAL

Information given in this section provides the guidelines for filling in the thyristor registration information required in all the registration formats contained in Part 3. In subsequent sections, instructions specifically pertaining to the individual formats will be given.

Every item on a given format preceded by an "M" must be completely filled in, since it represents the essential ratings and characteristics required to insure device interchangeability in the broad general thyristor applications. The data requested in other items are optional and should be filled in as appropriate to insure interchangeability in those special applications in which the device is intended to serve. In any event, the data supplied should adequately define the device in terms of interchangeability in the intended application and should distinguish it from existing registered devices. If it is felt that additional data are absolutely necessary to assure interchangeability, the data may be submitted for consideration as part of the registration. When data are submitted for which no blanks appear in the registration, care must be taken to completely describe the conditions under which the specified performance characteristics are to be met.

When preparing a registration data sheet for release, delete all italicized notes, all unused items, and all "M's". Renumber the items in proper sequence wherever necessary to avoid gaps in the item numbers used.

Existing JEDEC standards for measurement methods (refer to Parts 5 and 6), preferred voltage, current and temperature values (given in paragraphs 4.1.1 and 4.1.2), and definitions and letter symbols (refer to Parts 1 and 2) are to be used, as applicable.

JEDEC registered data must appear on the device manufacturers commercial data sheets and be identified as JEDEC registration data by means of asterisks. No data can appear in commercial data sheets for which provisions are made in the registration format for registration, but the device manufacturer has not registered the data.

For additional information on the industry registration of semiconductor devices, see (1) latest issue of JEDEC Publication No. 15, "Semiconductor Device Type Assignment Procedures," and (2) EIA Standard RS-370, "Designation System for Discrete Solid State Devices."

4.1.1 Preferred Voltage and Current Ratings

In the interest of standardization, it is recommended that only thyristors possessing the following voltage and current ratings be registered.

Preferred Voltage Ratings-Volts		
25	100	1000
50	200	1200
	400	1500
	600	2000
	800	

Preferred Current Ratings at T_3 DC, Average or RMS Amperes*			
0.10	1.0	10	100
0.25	2.5	15	150
0.60	6.0	25	250
		40	400
		60	600

*a. Amperes dc for dc-rated and average amperes, 50 to 400 Hz, for ac-rated reverse blocking thyristors.

b. RMS amperes, 50 to 60 or 400 Hz, for bidirectional thyristors.

NOTE: If it is absolutely necessary to register values other than those given above, use values from the list of ASA series (rounded) 10 numbers which are: 1.0, 1.2, 1.5, 2.0, 2.5, 3.0, 4.0, 5.0, 6.0, 8.0 times any power of 10.

4.1.2 Preferred Temperature Values

In the interest of standardization, the following temperatures are recommended for use in the registration of thyristors:

Preferred Temperature Values – Degrees Celsius

–273*	–65*	40	175*
–250*	–55*	55*	200*
–200*	–40	70*	230
–175*	–25*	85*	250*
–150*	–10	100*	300*
–125*	0*	125*	350*
–100*	25*	150*	400*

*Recommended for use in new documents.

If it is absolutely necessary to register values other than those given above, they should be in multiples of five degrees Celsius.

4.1.3 Terminal Color Coding

When it is required to color code thyristor terminals or leads, the following is recommended in the interest of standardization:

1. For reverse blocking or conducting triode or diode thyristors:

Anode – Black
Cathode – Red
Gate – White

2. For bidirectional thyristors:

Main Terminal 2 – Black
Main Terminal 1 – Red
Gate – Yellow

NOTE: Auxiliary terminals or leads should be color coded the same as their corresponding principal terminal or lead. For example, the auxiliary cathode lead that is often provided for the gate trigger signal return should be color coded red.

4.1.4 Conditions To Be Met for New Registrations or Modifications of Existing Types

When considering the registration of a new thyristor, it must be decided whether a new type number should be issued, or whether the addition of a suffix letter to an existing type number is better, or whether the new type is so similar to existing types that it is preferable not to register it at all. The guidelines given below are used by the Type Administrator in reaching the best decision in each case.

If the device outline is identical to that of an existing type, a letter suffix can be considered. If the outline differs in some minor respect, and if the new type may be physically substituted for the existing type, a suffix may be considered. If the new outline differs significantly, such as would be the case if it had a different registration (DO or TO) number, a new type number is required, even if electrical ratings and characteristics are the same.

One or more of the following differences between a new device and an older registered device require that the new device be given a new type number:

1. Any change in on-state current rating (must conform to table in paragraph 4.1.1).

2. Any change in off-state or reverse voltage rating (must conform to table in paragraph 4.1.1).

3. Any change in storage or operating temperature rating (must conform to table in paragraph 4.1.2).

4. A rating or characteristic is to be registered which is not required in the older device. Note: If the older device were to be reregistered (this doesn't add a suffix; only industry agreement required) to specify the additional rating or characteristic, a suffix may be assigned the old device if it is again registered to meet tighter limits for this same rating or characteristic.

5. A very great change in one or more characteristics (see table on next page).

6. New outline dimensions (as mentioned above).

Suffixes are to be issued only when there is a change in characteristics or a rating not specified above. The change in characteristics or rating must be such that the new device is unilaterally interchangeable with the older one having the same basic number, so that the new type, which has been given the letter suffix, may be used to replace the original type device.

To warrant being assigned a suffix letter, the new device should have one or more characteristics or ratings significantly different from those in the original device. The characteristic(s) or rating(s) which are changed should differ from the original value(s) at least by the amount(s) given in the table below. On the other hand, if the change in any one characteristic or rating exceeds the maximum value given in the table, a new type number is required.

PER CENT CHANGE* OF CHARACTERISTIC OR RATING REQUIRED FOR LETTER SUFFIX

Parameter	Min. Change Required	Max. Change Permitted	Direction Of Change
Off-State Current	50%	500%	Reduction
Reverse Current	50%	500%	Reduction
Peak Negative Gate Current	50%	500%	Reduction
On-state Voltage	20%	40%	Reduction
DC Gate Trigger Voltage	20%	50%	Reduction
DC Gate Trigger Current	50%	500%	Reduction
Holding Current	50%	500%	Reduction
Latching Current	50%	500%	Reduction
Peak Gate Turn-Off Voltage	25%	250%	Reduction
Peak Gate Turn-Off Current	50%	500%	Reduction
Gate-Controlled Turn-On Time	50%	500%	Reduction
Gate-Controlled Turn-Off Time	25%	250%	Reduction
Circuit-Commutated Turn-Off Time	25%	250%	Reduction
Critical Rate of Rise of Off-State Voltage	50%	500%	Increase
Peak Negative Gate Voltage	50%	500%	Increase
Peak Positive Gate Current	50%	500%	Increase
Surge (Non-Repetitive) On-State Current	50%	250%	Increase
Critical Rate of Rise of On-state Current	50%	500%	Increase
Gate Power Dissipation	50%	500%	Increase

$$\text{Per Cent Change} = \frac{\text{Existing Parameter Limit} - \text{New Limit (if less)}}{\text{Existing Parameter Limit}} \times 100$$

or

$$= \frac{\text{New Limit (if more)} - \text{Existing Parameter Limit}}{\text{Existing Parameter Limit}} \times 100$$

*These changes should always be in the direction to result in device improvement.

4.1.5 I. GENERAL DESCRIPTION

Information given in this section of the format establishes the broad descriptive classifications pertaining to the device to be registered. For instance, the semiconductor material used, the nominal current rating of the device, and its basic electrical configuration (diode, triode, reverse blocking, bidirectional, etc.) are to be given here; also, the major areas of usage and similar facts.

4.1.6 II. MECHANICAL DATA

The outline dimensions of the device are to be given in this section. If possible, an outline drawing registered with JEDEC should be used. Registered outlines are found in JEDEC Publication Number 12. They are assigned numbers beginning with "DO" (for two-terminal housings) and "TO" (for three or more terminal housings). If such a registered outline is not applicable, an outline drawing must be furnished on a separate page attached to the format. This drawing must be prepared so as to conform with EIA Standard RS-308, "JEDEC Type Registration for Semiconductor Devices, Preparation of Outline Drawings."

The electrical function of each terminal of the device is also to be given in this section. Terminal functions for existing registered outlines are shown in the table below. When a non-registered package is used the terminal functions should follow as closely as possible the pattern of the closest standard package.

ELECTRICAL FUNCTION OF DEVICE TERMINALS

Type of Package	Terminal Description	Reverse Blocking or Conducting Triode Thyristors	Bidirectional Triode Thyristors
Three Lead mounted (incl. TO-5, -8, -18, -46, and -52)	1* 2* 3* Case	Cathode Gate Anode Common with #3 unless electrically isolated	Main Terminal 1 Gate Main Terminal 2
Two-terminal, bolt down case (incl. TO-3, -41, and -66)	1* 2* Case	Gate Cathode Anode	Gate Main Terminal 1 Main Terminal 2
Two-terminal, stud, clamp-down or integral heat sink case (incl. TO-48, 49, 64, and 83)	Small insul. terminal (#1*) Large insul. terminal (#2*) Case (#3*)	Gate Cathode Anode	Gate Main Terminal 1 Main Terminal 2

ELECTRICAL FUNCTION OF DEVICE TERMINALS (Continued)

Type of Package	Terminal Description	Reverse Blocking or Conducting Triode Thyristors	Bidirectional Triode Thyristors
Three-terminal, stud, clamp-down or integral heat sink case (inc. TO-93 and -94)	1*	Gate	Gate
	2*	Gate Return to Cathode	Gate Return to Main Terminal 1
	3*	Cathode	Main Terminal 1
	4*	Anode	Main Terminal 2

Type of Package	Terminal Description	Reverse Blocking or Conducting Diode Thyristors	Bidirectional Diode Thyristors
Two Lead mounted	1*	Cathode	Main Terminal 1
	2*	Anode	Main Terminal 2
Single terminal stud, clamp down or bolt down case	1	Cathode	Main Terminal 1
	Case	Anode	Main Terminal 2
Two terminal bolt down case (inc. TO-3, 41 & 66)	1*	Anode	Main Terminal 2
	2*	Cathode	Main Terminal 1
	Case	Anode	Main Terminal 2

*As numbered on registered outline.

If the case is also an electrical terminal, its electrical function should be given. Otherwise, a note is to be included stating "all leads insulated from case". Any terminal not performing an electrical function is to be designated "NC".

If any special precautions are necessary for the proper handling of the device, these are to be given in this section. Likewise, any restrictions as to mounting positions which may be required in order to insure proper operation of the device should be given here.

4.1.7 III. MAXIMUM RATINGS

Maximum thermal and electrical ratings assigned to the device are to be given in this section.

4.1.7.1 Temperature

A temperature reference point on the device case or a lead point adjacent to the case must be specified. In the instance of a hex base stud-mounted device, the reference temperature point should be specified at the center of the flat surface of any one of the hex faces.

Temperatures in degrees Celsius (centigrade) are to be selected when possible from the table in paragraph 4.1.2 and inserted in blanks corresponding to the symbols T_1 through T_7.

Operating temperatures are first to be inserted in ascending order, thus T_1 is the lowest operating temperature. Temperature symbol numbers higher than the one used for the highest operating temperatures are assigned to storage temperatures from the lowest to the highest temperature value. Since the minimum operating and storage temperatures are often the same, this same temperature value will often appear in two different numbered blanks, such as T_1 and T_6. Also T_1 and T_2 are quite often the same value.

The temperatures T_1 through T_7 are to be selected in accordance with the instructions listed below. T_1, T_2, and T_6 may be decreased in increments of 5°C. T_3, T_4, T_5, and T_7 may be increased in increments of 5°C. No intermediate temperatures are to be used.

T_1 and T_6 must be specified at 0°C or lower.

T_2 must be specified as 25°C or lower.

T_3 must be specified to meet the requirements of the table below, depending upon the value of maximum operating temperature (T_5) specified.

Maximum Operating Temperature (T_5)	Permissible Range of Max. Case Temperatures at Full Load (T_3)	Preferred Max. Case Temperature at Full Load (T_3)
Case 100°C	40-65	55
Case 125°C	60-85	70
Case 150°C	85-110	100
Case 175°C (for future use)	To be established	

It is desirable that all thyristors of a given general configuration be registered to have identical temperatures for T_3. It is suggested that the registrant attempt to use a value which is the same as for a similar device which has already been registered.

T_4 must be specified at least 5°C higher than T_3.

T_5 must be specified at least 5°C higher than T_4 and should conform to the standard.

T_7 must be specified equal to T_5 or higher.

Once the values to T_1 through T_5 have been established in the section on Operating Temperatures, the same values should be used whenever symbols T_1 through T_5 appear in the registration format.

A blank is provided for registering any limitation of soldering temperature that would be necessary to avoid damaging the device when soldering it into the circuit. This information is optional.

4.1.7.2 Voltage

The electrical ratings to be given are the maximum input voltage rating and the maximum on-state current rating that can be continuously handled by the device over the normal operating temperature range, T_2 to T_5.

Off-state and/or reverse voltage may be derated in the temperature range T_1 to T_2. Likewise, on-state current may be derated over the same temperature range if desired. This derating information is to be registered as additional information. As no blanks are provided for such derating information, it should be included in a manner consistent with the other parts of the registration, and given an appropriate paragraph number.

Where it is desired to use a registration format to register more than one device in a series and the devices have different voltage ratings, the information required to establish the voltage ratings may be given in the form of a note at the end of the format in which case reference shall be made to this note in appropriate blanks in the format. This note may consist of a table giving the various voltages which apply to the different devices in the series.

4.1.7.3 Current

The current rating of the thyristor is to be registered as either an average value (averaged over a full cycle of the ac input voltage) or as a pure dc value for reverse blocking thyristors and as an ac rms value for bidirectional devices, as this is of more significance with respect to their major applications. Spaces are given to register the current rating over the normal (no derating) temperature range T_2 to T_3 and also at a lower value at temperature T_4 which is above the normal temperature range. By definition the current rating at T_5 is zero so a complete current rating curve is to be registered from T_2 to T_5. This curve consists of three straight line segments. The current at T_4 should be approximately 1/3, 1/2, or 2/3 of the rated current over the normal operating range. The number registered may be rounded to eliminate fractions.

AC ratings for reverse blocking and reverse conducting thyristors are based on 50 to 400 Hz waveforms into resistive loads and a conduction angle of $180° \pm 5\%$. Bidirectional thyristor ratings are based on 50 to 60 or 400 Hz waveforms. Immediately after conducting the current specified over the normal operating temperature range and also the current specified at T_4, and after reaching equilibrium temperature, the device must be able to regain its off-state at full rated voltage, following a brief turn-off interval.

The surge current rating is the peak value of a specified half or full sine wave of current. This surge may be repeated after the device has returned to original thermal equilibrium conditions. This is a non-repetitive rating. The device is to be capable of withstanding a minimum of 100 such surges without failure. It is not required to regain ability to block off-state voltage following the current surge until the original thermal equilibrium conditions have been re-established. For the 60 Hz half-sine-wave surge rating, the current surge is to be preceded by and followed by the normal operating conditions consisting of maximum rated 60 Hz half-sine-wave current, device reference point temperature equal to

T_3, and for reverse blocking thyristors rated repetitive 60 Hz peak reverse blocking voltage if applicable. In addition, for reverse blocking thyristors the half cycle of reverse blocking voltage following the half-sine-wave surge current is to be the registered non-repetitive 60 Hz peak reverse blocking voltage, if such exists. Otherwise, rated repetitive peak reverse voltage should be applied.

4.1.7.4 Gate Power

For triode thyristors, the peak gate power dissipation should be registered. In addition, the maximum allowable average gate power dissipation is to be stated. Since gate power dissipation contributes to junction temperature rise, gate power is considered to be zero at T_5. T_5 is a zero current condition and ability to block voltage is the only required capability. At lower temperatures, the temperature rise caused by the permissible gate power dissipation should be considered when determining the maximum on-state current permitted.

4.1.8 IV. ELECTRICAL CHARACTERISTICS

4.1.8.1 Off-State and Reverse Blocking Current

In the sections under Off-State and Reverse Blocking Current, where more than one device is being registered at one time and these currents are not the same for all the devices being registered, the current values may be given in the same note which lists the voltage ratings and reference shall then be made to this note in the appropriate blanks.

4.1.8.2 Reverse Gate Current

Registration of this characteristic is optional.

4.1.8.3 On-State Voltage

In order to avoid excessive heating of the junction during the test for on-state voltage, the width of the current pulse used to make the measurement should not exceed 2 millisecond and the repetition rate of the pulses should be low enough to impose a duty cycle of no more than 2%. However, the pulse width should be wide enough to assure that the device is fully on by the time the voltage measurement is taken.

4.1.8.4 Holding Current

Both maximum and minimum holding currents may be registered, the maximum value being registered at T_2, and the minimum value at T_5. Holding current is registered under condition of low anode source voltage (12 volts preferred) and under conditions where prior to determining the holding current the on-state current has been increased to a value high enough to insure that the device is fully turned on. Then, by increasing the resistance in series with the anode of the device, the current shall be reduced until it ceases. The holding current is defined as the lowest value of current observed before current conduction ceases.

4.1.8.5 Latching Current

Spaces are provided for registering maximum latching current at T_2 and minimum latching current at T_5. Latching current is similar to holding current, but is not the same, since latching current is defined as that on-state current below which the device will not remain in conduction after the application and removal of a stated trigger pulse. The width of this pulse must be long enough so that if it is cut in half latching current will not be affected. Latching current is quite likely to be somewhat higher than the holding current. Because latching current is dependent upon the triggering excitation applied during the test, complete information must be provided concerning the triggering conditions. Also to be specified is off-state voltage prior to the appearance of the trigger pulse (12 volts preferred).

4.1.8.6 Turn-On Time

The components of turn-on time, delay time and rise time, may be registered. Blanks are provided for only maximum values because as a rule these are the significant values and minimum values are not important to the user. Under test conditions the triggering conditions are to be fully described. The temperature and off-state voltage prior to turn-on are to be stated also. Generally, the temperature is given as 25°C and the off-state voltage is the rated value. The current turned on should preferably be one of the rated values of current for the device.

4.1.8.7 Critical Rate of Rise of Off-State Voltage

The values registered in this blank are to be obtained from an exponential test voltage waveform. The numerical value of this characteristic is defined as the slope of the straight line connecting the origin and 63% magnitude point of the critical test voltage waveform. The greatest rate of rise of applied off-state voltage, as defined in the test method, which all devices can be subjected to without triggering on and the maximum temperature at which the rating will be met are to be registered. This parameter is not to be confused with the rate of rise of reapplied off-state voltage, which is one of the test conditions for measuring circuit commutated turn-off time.

4.1.9 V. THERMAL CHARACTERISTICS

The maximum steady state thermal resistance between the junction and the temperature reference point specified in the beginning of the format is to be registered. As an optional item, the transient thermal impedance characteristics may be supplied in tabular form or as a curve.

Also to be registered is the maximum allowable thermal resistance of the heat sink to which the registered device must be mounted in order to prevent thermal runaway when registered voltage is applied over the registered operating temperature range.

In the following sections the use of specific registration formats is considered in greater detail.

4.2 USE OF REGISTRATION FORMAT FOR TRIODE THYRISTORS, JC-22 RDF-1

4.2.1 I. GENERAL DESCRIPTION

The format for triode thyristors is to be used for both reverse blocking and reverse conducting triode thyristors, including those having gate turn-off characteristics. (Reverse blocking triode thyristors are also known as semiconductor controlled rectifiers, SCR's.) Whether the device is the gate turn-off type is to be stated and if this is the case, the maximum anode current which can be turned off must be specified.

4.2.2 II. MECHANICAL DATA

This section is to be completed in accordance with the instructions given in paragraph 4.1.6.

4.2.3 III. MAXIMUM RATINGS

The ratings registered can be based either on operation in a single-phase, half-wave circuit with a 50 to 400 Hz sinusoidal principal voltage source, resistive load, and a conduction angle of 180° ± 5%, or on operation in a circuit with a dc principal voltage source. These ratings are established on the basis of blocking full rated voltage in either the off-state or reverse direction immediately following conduction of rated on-state current for a period long enough to establish temperature equilibrium in the junction. However, the device is not expected to return to the off-state during the turn-off interval. It is not required to register values for both the ac and dc modes of operation. When only one mode of operation is selected for registration, all values given must be consistent with the mode chosen: For example, items III.B.1, III.C.1, III.C.5.a, IV.A.1, IV.B.1 and IV.D.1 represent ac operation and items III.B.2, III.C.2, III.C.5.d, IV.A.2, IV.B.2 and IV.D.2 represent dc operation.

4.2.3.1 A. Temperature

Follow the instructions given in paragraph 4.1.7.1. In addition, the option of registering the maximum operating junction temperature rating is given. This rating is required in conjunction with the device transient thermal impedance characteristics to calculate device repetitive overload current ratings of any desired waveshape and duty cycle.

4.2.3.2 B. Voltage at T_2 to T_5

The off-state voltage rating to be given in paragraph III.B.1 is the peak value of the 50-400 Hz sine wave voltage that can be withstood on a repetitive basis over the operating temperature range of T_2 to T_5. In paragraph III.B.2 it is the maximum dc voltage that can be withstood over the same operating temperature range. In either case the gate voltage and resistance bias conditions that are to pertain are to be specified. The non-repetitive (or transient) peak reverse blocking voltage is also to be specified under ac operation.

The peak positive anode voltage rating is the maximum positive voltage that may be applied to the device. This voltage may exceed the breakover voltage of the device in which case the applicable di/dt and current ratings of the device must be observed to avoid device damage.

The peak negative gate voltage is the limiting value which may not be exceeded if damage to the gate is to be avoided.

4.2.3.3 C. Current

The current rating to be registered is either the full cycle average on-state current for 50-400 Hz half sine wave conduction or the direct (continuous or dc) on-state current. The peak positive gate current may also be specified. The peak repetitive on-state current may be registered as a special rating for devices intended specifically for pulse operation on a repetitive basis, but with no particular turn-off time implied.

If the device is being registered for ac operation, the 60 Hz and 1.5 ms one-half-cycle sine-wave on-state surge (non-repetitive) current should be registered. (Refer to paragraph 4.1.7.3.) If the registration is for a dc rated device, the rectangular pulse on-state surge (non-repetitive) current should be registered, and the pulse width, pulse rise time, duty cycle and gate drive conditions are to be specified. This pulse is to be preceded and followed by the current specified in paragraph III.C.2.a.

If the pulse circuit commutated turn-off time characteristic is registered, then the current rating which is a necessary test condition of this characteristic must also be registered. This current rating is registered exactly as specified in Section IV.O of the registration format.

Provision is made for the registration of three critical rate of rise of on-state current ratings (di/dt ratings). The repetitive rating will generally apply to devices used primarily in phase control applications at power frequencies. This repetitive rating, as usual, implies unlimited operation at the conditions of the rating and that gate control is retained. The non-repetitive di/dt ratings apply, as usual, for abnormal, very infrequent circuit operation and therefore the device is not required to regain gate control following a current pulse until original thermal equilibrium conditions have been reestablished. Breakover voltage triggering as applied to a non-repetitive di/dt rating refers to a triggering mode produced by a voltage that exceeds the device breakover voltage. In a typical application, this type of triggering voltage might be produced by some disturbance on the ac supply lines such as high current switching or by lightning. If desired the di/dt rating may be registered with a resistor-capacitor series combination connected directly across the thyristor. This type of R-C circuit is often used to reduce the amplitude and dv/dt of unwanted transient voltages that could produce harmful effects on the thyristor. Such an R-C circuit can have a marked effect (particularly high C and low R) on the thyristor di/dt capability because of the spike of current it produces at the instant of turn-on. If the particular thyristor type being registered will be used in applications requiring R-C combinations of such value as to affect the device di/dt rating, these values of R and C should be registered as a part of the thyristor di/dt rating.

4.2.3.4 D. Gate Power Dissipation at T_3

Refer to paragraph 4.1.7.4.

4.2.4 IV. ELECTRICAL CHARACTERISTICS

4.2.4.1 A. Off-State Current

Gate bias conditions should be specified because these influence the blocking current observed. If registration is being made for ac operation then peak off-state blocking current at T_5 and rated peak off-state voltage should be given. If registration is being made for dc operation then dc off-state blocking current at T_5 and rated dc off-state voltage should be registered.

4.2.4.2 B. Reverse Current

In similar manner to the above, the reverse blocking current should be registered.

4.2.4.3 C. Peak Negative Gate Current

If peak negative gate current is registered, the value given should be that obtained at temperature T_5 with maximum rated peak negative gate voltage applied to the gate. The anode terminal should be open circuited.

4.2.4.4 D. On-State Voltage at 25°C Case or Ambient Temperature

If registration is being made for ac operation the value of on-state voltage registered should be that obtained at π times maximum rated average current (peak value of a half sine wave of rated average current) at 25°C. If registration under dc operation has been chosen, the on-state voltage at maximum rated direct current at 25°C should be given.

4.2.4.5 E. DC Gate Trigger Voltage

The gate trigger voltage registered should be the value of direct voltage which will produce the gate current required to trigger all devices of the type being registered when the anode voltage is at a low value (12 volts preferred) and at minimum operating temperature T_2. A value of load resistance should be given which will be low enough to permit the device to latch-on when the registered dc gate trigger voltage and/or current are applied and then removed.

Also in this section, there is an optional item for listing the minimum gate trigger voltage which will produce the gate current required to trigger any unit of the type being registered. This is to be specified under the conditions of maximum rated voltage applied to the device at maximum rated operating temperature, T_5. In the case of devices intended for ac operation, this optional item is ususally registered.

4.2.4.6 F. DC Gate Trigger Current

In similar fashion, the direct current required for triggering any device of the type being registered is given under the same operating conditions as was given for maximum gate trigger voltage. An optional item is the minimum dc gate current required to trigger any unit under maximum voltage and temperature conditions.

4.2.4.7 G. Holding Current

Gate bias conditions must be specified as a gate source voltage and gate source resistance, or as a gate bias resistance. The preferred anode source voltage is 12 volts. Also, the peak on-state current when the device under test is first turned on is to be specified.

4.2.4.8 H. Latching Current

Gate excitation conditions must be specified, including gate bias and gate trigger pulse conditions. The same anode voltage should be specified as was given under Holding Current.

4.2.4.9 I. Peak Gate Turn-Off Voltage at T_3

This section should be completed for devices which are of the gate turn-off type. Load inductance and range of load current are to be stated as these affect the gate turn-off voltage required. Anode source voltage, preferably rated off-state voltage, is to be specified as well as minimum gate pulse width and gate bias conditions.

4.2.4.10 J. Peak Gate Turn-Off Current at T_3

Maximum gate turn-off current is also to be registered for gate turn-off devices under the same conditions as discussed for peak gate turn-off voltage.

4.2.4.11 K. Gate-Controlled Turn-On Time

Delay time and rise time or total turn-on time may be specified. Gate excitation conditions must be specified in the blanks provided as well as the off-state voltage prior to turn-on and the on-state current. Rated repetitive or direct off-state voltage and rated peak (π times average) repetitive or direct on-state current are preferred.

4.2.4.12 L. Gate-Controlled Turn-Off Time

The value to be given in this section is the turn-off time for a gate turn-off device, and two values are to be registered, the maximum storage time and the maximum fall time. In addition, the minimum gate pulse width which will turn the device off under the conditions specified is to be given. Under test conditions, the conditions pertaining to the turn-off time test are to be given in the space provided, and the gate bias circuit is to be shown. The gate turn-off current required may be specified or else the gate turn-off pulse may be characterized by stating an open circuit voltage and a source impedance, in ohms.

4.2.4.13 M. Circuit-Commutated Turn-Off Time

In this section total circuit commutated turn-off time and the reverse recovery time may be registered. Test conditions are to be given which describe the conditions under which these times are to be measured.

The repetition rate of the on-state current pulses should be kept low enough so that the heating of the junction above the case of the device under test is negligible. The value of the peak on-state current at which the test is conducted is generally a value approximately equal to the nominal average current rating of the device being registered. The duration of the on-state current pulse should be long enough to permit current flow to equalize throughout the device junction and yet short enough to keep junction heating to a minimum.

The magnitude of the reverse voltage applied (from the instant of principal current reversal to time t_1) will influence the observed turn-off time. Higher values of reverse voltage tend to decrease the measured turn-off time. This effect is most apparent for reverse voltages below 10 volts at time t_1 and therefore the registration format requires specification of the maximum reverse voltage applied at time t_1. This value together with the specifications of a maximum peak reverse voltage control the reverse voltage to be applied throughout the turn-off time interval. Following the initial peak value of reverse voltage, the value during the remainder of the turn-off interval essentially will be that value specified at time t_1 with allowance for some decay of the reverse voltage supply. This flexibility allows, for example, the reverse voltage conditions to be specified for the case of a closely coupled anti-parallel rectifier diode or other voltage clamping circuits. The off-state voltage (starting at time t_1) is applied as a linear ramp with specified rate of rise. This voltage is to be clamped at a value specified as Off-State Voltage and is usually equal to the rated repetitive peak off-state voltage value for the device being registered.

The gate bias conditions to be specified are those which are to be maintained after the end of the gate trigger pulse which initiates on-state current conduction. The gate bias conditions must be carefully controlled since they can have a significant effect on the measured value of turn-off time. Generally, a gate bias resistance value is specified.

4.2.4.14 N. Critical Rate of Rise of Off-State Voltage

Refer to paragraph 4.1.8.7.

4.2.4.15 O. Pulse-Circuit-Commutated Turn-Off Time

This characteristic is similar to circuit-commutated turn-off time except the magnitude and rate of rise of the on-state test current is such that sufficient localized heating is produced during turn-on to have a marked effect on the turn-off time. It is also required to register the device power dissipation produced by this type of operation with high switch-on losses in order to insure device interchangeability. This turn-off time characteristic is usually only registered for thyristors designed for fast switching at high repetition rates.

4.2.5 V. THERMAL CHARACTERISTICS

Refer to paragraph 4.1.9.

4.3 USE OF REGISTRATION FORMAT FOR BIDIRECTIONAL TRIODE THYRISTORS, JC-22 RDF-2

4.3.1 I. GENERAL DESCRIPTION

The two power terminals are designated as Main Terminal 1 and Main Terminal 2. Main Terminal 1 is defined as the terminal to which the gate signal and Main Terminal 2 voltage is referenced. Four triggering modes may be possible with some types of bidirectional thyristors; that is either polarity of gate signal may cause switching for either polarity of Main Terminal 2 voltage. It is not required to select more than one mode for each polarity of Main Terminal 2 voltage but the modes identified in the General Description must be consistent with the values registered in Sections IV.C, IV.D, IV.E, and IV.F.

4.3.2 II. MECHANICAL DATA

Refer to paragraph 4.1.6.

4.3.3 III. MAXIMUM RATINGS

4.3.3.1 A. Temperature

Refer to paragraph 4.1.7.1.

4.3.3.2 B. Voltage at T_2 to T_5 and C. Current

The ratings registered are to be based on operation in a 50 to 60 Hz or 50 to 400 Hz resistive load circuit. The sine-wave supply voltage should have a peak value equal to that registered in III.B.1. When the thyristor is conducting a sine wave current having the rms value registered in III.C.1.a and the operating temperature is T_3, the thyristor must be capable of returning to the off-state at the beginning of that half cycle following gate trigger removal. In a like manner, the thyristor must be able to return to the off-state after conducting current III.C.1.b at T_4 when the gate trigger is removed. The peak principal voltage is the maximum voltage that may be applied to the device; the voltage may exceed the breakover voltage of the device in which case the applicable di/dt and current ratings of the device must be observed to avoid device damage. Provisions are made for registering repetitive and non-repetitive critical rate of rise of on-state current ratings (di/dt ratings). These ratings apply for operation in either quadrant and an explanation of these ratings is given in 4.2.3.3.

4.3.3.3 D. Gate Power Dissipation at T_3

Refer to paragraph 4.1.7.4.

4.3.4 IV. ELECTRICAL CHARACTERISTICS

The electrical characteristics are to be registered on the basis of symmetrical operation of the device and should be the limiting value for either direction of operation.

4.3.4.1 A. Repetitive Peak Off-State Current

Gate bias conditions if required must be specified because they influence the off-state currents observed.

4.3.4.2 B. Peak On-State Voltage at 25°C Case or Ambient Temperature

The peak on-state voltage is specified under pulse conditions and the voltage is measured at the peak current listed in section III.C.1a times $\sqrt{2}$ at 25°C.

4.3.4.3 C. Peak Gate Trigger Voltage, Main Terminal 2 Positive

Positive gate trigger voltage and/or negative peak gate trigger voltage may be registered. The gate trigger voltage registered should be the value which will produce the gate current that will trigger all devices of the type being registered with the Main Terminal 2 source voltage at some low value (12 volts preferred) and at temperature T_2. A value of load resistance shall be given which will be low enough to permit the device to latch on when the registered gate trigger voltage is applied. The minimum pulse width of the gate voltage pulse should also be specified since for very short pulses higher gate voltages and currents are required for triggering. Also in this section, it is optional to specify the minimum gate trigger voltage for triggering any unit of the type being registered. This minimum gate trigger voltage is to be specified under the conditions of maximum rated voltage applied to the device at maximum rated operating temperature, T_5.

4.3.4.4 D. Peak Gate Trigger Voltage, Main Terminal 2 Negative

In similar fashion to that described in paragraph 4.3.4.3, except that Main Terminal 2 voltage is reversed, the peak gate trigger voltage is to be registered. Again either or both polarities of gate trigger voltage may be registered.

4.3.4.5 E. Peak Gate Trigger Current, Main Terminal 2 Positive

Peak gate trigger current required to trigger all devices when Main Terminal 2 is positive and under the conditions registered in Section IV.C. should be registered here. The currents registered should pertain to the gate triggering voltages registered.

4.3.4.6 F. Peak Gate Trigger Current, Main Terminal 2 Negative

In similar fashion to the above, the peak gate trigger current required to trigger all devices when Main Terminal 2 is negative is to be registered in this section. The currents registered should pertain to the gate trigger voltages registered in paragraph IV.D.

4.3.4.7 G. Holding Current

Refer to paragraphs 4.1.8.4 and 4.3.4.

4.3.4.8 H. Latching Current

Refer to paragraphs 4.1.8.5 and 4.3.4.

4.3.4.9 I. Gate-Controlled Turn-On Time

Refer to paragraphs 4.1.8.6 and 4.3.4.

4.3.4.10 J. Critical Rate of Rise of Off-State Voltage

Refer to paragraph 4.1.8.7 and 4.3.4

4.3.4.11 K. Critical Rate of Rise of Commutation Voltage

It is recommended that the test conditions used for the registration of this characteristic be those that correspond to the maximum registered values of on-state current, off-state voltage and case temperature. Since the recommended duty cycle of the on-state test current is quite high, sufficient test time must be allotted for the case temperature to stabilize to the specified value which in this situation will be very close to the registered T_3 value if registered on-state test current is used. Since the characteristic to be registered involves a slope of an exponential wave shape, a definition of the numerical value of the characteristic is required. Thus the registered value of the critical rate of rise of commutation voltage is the slope ($V/\mu s$) of the straight line connecting the 10% and 63% voltage points. The registration of this characteristic is on an ac basis and therefore the single registered value must be the limiting value for device operation in either quadrant.

4.3.5 V. THERMAL CHARACTERISTICS

Refer to paragraph 4.1.9 and 4.3.4.

4.4 USE OF REGISTRATION FORMAT FOR POWER DIODE THYRISTORS, JC-22 RDF-3

This registration format applies to devices intended for power control applications. For diode thyristors intended for signal level applications refer to registration formats in the JC-20 series.

4.4.1 I. GENERAL DESCRIPTION

This registration format is intended for use with both reverse blocking and reverse conducting diode thyristors and also with bidirectional diode thyristors. In describing the thyristor, methods required to initiate switching of the device should be mentioned. The current rating can be given as the average current rating for reverse blocking or reverse conducting diode thyristors, or as the RMS current rating for bidirectional thyristors.

4.4.2 II. MECHANICAL DATA

Refer to paragraph 4.1.6.

4.4.3 III. MAXIMUM RATINGS

Maximum electrical ratings assigned to the device are to be given in this section. If a bidirectional device is being registered, the ratings are to be given on the basis of symmetrical operation of the device and should be the limiting value for either direction of operation.

4.4.3.1 A. Temperature

Refer to paragraph 4.1.7.1.

4.4.3.2 B. Voltage at T_2 to T_5

Refer to paragraph 4.1.7.2

4.4.3.3 C. Current

The current rating of the diode thyristor is to be registered as the average value for reverse blocking and reverse conducting devices, 50 to 400 Hz, and as the RMS value, 50 to 60 Hz or 50 to 400 Hz for bidirectional devices. III.C.1.a applies to the normal current range where there is no derating, III.C.1.b applies to T_4 only.

4.4.4 IV. ELECTRICAL CHARACTERISTICS

Information supplied in this section must include both a minimum and a maximum breakover voltage through the range T_2 to T_5.

4.4.4.1 A. Breakover Voltage and Current for Bidirectional Devices

The values of breakover voltages entered in this section apply to sinusoidal test voltage waveforms which do not exceed 60 or 400 Hz. Maximum breakover current is also required in this section at a reference temperature of T_2. For bidirectional devices the electrical characteristics are to be registered on the basis of symmetrical operation of the device and should be the limiting value for either direction of operation.

4.4.4.2 B. Repetitive Peak Off-State and Reverse Currents at T_5

Repetitive peak off-state current at T_5 is the characteristic of the device at its rated repetitive peak off-state voltage, III.B.1, at T_5. (Peak breakover current at T_5 will be higher than rated repetitive peak off-state current). Repetitive peak reverse current for reverse blocking devices is to be similarly registered.

4.4.4.3 C. Peak On-State Voltage

The peak on-state voltage is specified under pulse conditions and the voltage is measured at the peak of the current listed in section III.C.1.a (π times the average values for reverse blocking devices and $\sqrt{2}$ times the RMS value for bidirectional devices).

4.4.4.4 D. Holding Current

Refer to paragraphs 4.1.8.4 and 4.3.4.

4.4.4.5 E. Latching Current

Refer to paragraphs 4.1.8.5 and 4.3.4.

4.4.4.6 F. Turn-On Time at T_2

Refer to paragraphs 4.1.8.6 and 4.3.4. For the current turned on, it is preferable to state π times III.C.1.a amperes for reverse blocking or reverse conducting thyristors, and $\sqrt{2}$ times III.C.1.a amperes for bidirectional thyristors.

4.4.4.7 G. Circuit-Commutated Turn-Off Time

Circuit-commutated turn-off time is to be registered only for reverse blocking devices.

4.4.4.8 Critical Rate of Rise of Off-State Voltage

Refer to paragraph 4.1.8.7 and 4.3.4.

4.4.5 V. THERMAL CHARACTERISTICS

Refer to paragraph 4.1.9 and 4.3.4.

PART 5

RATINGS ESTABLISHMENT AND VERIFICATION TESTS

INDEX

PART 5

RATING ESTABLISHMENT AND VERIFICATION TESTS

5.1 INTRODUCTION AND REFERENCE TABLE OF RATINGS AND TEST METHODS

This section describes standard test methods to be used in establishing and verifying the maximum ratings for thyristors given in the JC-22 series of registration formats for triode thyristors (JC-22 RDF-1), bidirectional triode thyristors (JC-22 RDF-2), and diode thyristors (JC-22 RDF-3). The term "maximum rating" as used here means limiting value and thus implies that operation beyond a rating can result in device damage.

The following table cross-references maximum ratings, the registration formats for the device types to which the rating applies, the test methods used to establish the rating, and the number of the section of Part 5 which describes the test method.

Maximum Rating	Formats in which rating appears (Note 1)	Test Method in Part 5	
		Title	No.
Operating Temperatures	T, B, D	Repetitive Rating Tests (Note 2)	5.2.1
Storage Temperatures	T, B, D	Storage Life Test	5.3.1
Lead or Terminal Temperature for Soldering Purposes	T, B, D	Lead or Terminal Temperature Test	5.3.2
Repetitive Peak Off-State Voltage, 1/2 Sine Wave	T, D	Steady State Operational Life Test for Unidirectional Thyristors or Alternating Principal Voltage Life Test	5.2.1.1 or 5.2.1.3
Repetitive Peak Off-State Voltage, 1/2 Sine Wave	B, D	Steady State Operational Life Test for Bidirectional Thyristors or Alternating Principal Voltage Life Test	5.2.1.2 or 5.2.1.3

Maximum Rating	Formats in which rating appears (Note 1)	Test Method in Part 5	
		Title	No.
Repetitive Peak Reverse Voltage, 1/2 Sine Wave	T, D	Steady State Operational Life Test for Unidirectional Thyristors or Alternating Principal Voltage Life Test	5.2.1.1 or 5.2.1.3
Non-Repetitive Peak Reverse Voltage, 1/2 Sine Wave	T	Sine Wave Surge Current and Non-Repetitive Peak Reverse Voltage Test	5.2.2.1
DC Off-State Voltage and DC Reverse Voltage	T	DC Off-State or Reverse Blocking Voltage Life Test	5.2.1.4
Peak Positive Anode Voltage	T	Peak Positive Anode Voltage Test	5.2.2.5
Peak Positive Gate Voltage, Peak Negative Gate Voltage, Peak Positive Gate Current, Peak Negative Gate Current, Peak Gate Power and Average Gate Power	B	Gate Rating Life Test for Bidirectional Triode Thyristors	5.2.1.7
Peak Negative Gate Voltage Peak Positive Gate Current Peak Gate Power and Average Gate Power	T	Gate Rating Life Test for Unidirectional Triode Thyristors	5.2.1.6
Average On-State Current, 1/2 Sine Wave and Direct On-State Current	T, D T	Steady State Operational Life Test for Unidirectional Thyristors	5.2.1.1
On-State RMS Current, Full Sine Wave	B, D	Steady State Operational Life Test for Bidirectional Thyristors	5.2.1.2

Maximum Rating	Formats in which rating appears (Note 1)	Test Method in Part 5	
		Title	No.
Peak Repetitive On-State Current	T	Pulsed On-State Current Life Test	5.2.1.5
Surge (Non-Repetitive) On-State Current (60 Hz 1/2 or Full Sine Wave)	T, B, D	60 Hz Sine-Wave Surge Current Test and Non-Repetitive Peak Reverse Voltage Test	5.2.2.1
Surge (Non-Repetitive) On-State Current, 1.5 Millisecond Duration	T	Surge (Non-Repetitive) On-State Current, 1.5 Millisecond Duration Test	5.2.2.2
Surge (Non-Repetitive) On-State Current, 0.5 Millisecond Duration	T	Surge (Non-Repetitive) On-State Current, 0.5 Millisecond Duration Test	5.2.2.3
Repetitive Pulse Current Rating with Turn-Off Conditions	T	Repetitive Pulse Current Rating Under Specified Turn-Off Conditions Life Test	5.2.1.8
Surge On-State Current (Rectangular Pulse)	T	Rectangular Pulse Surge Current Test	5.2.2.4
Critical Rate of Rise of On-State Current (Repetitive and Non-Repetitive)	T, B	Critical Rate of Rise of On-State Current Test	5.2.2.6
Thermal Fatigue	None	Thermal Fatigue Life Test	5.2.1.9

Note 1: The following key is used for this column:

Symbol	Thyristor Format
T	Unidirectional Triode
B	Bidirectional Triode
D	Diode

Note 2: Operating Temperature Ratings cannot be established except in conjunction with other ratings. Operating Temperature Ratings are established by performing the tests of Section 5.2.1, Repetitive Rating Tests, which are applicable to the device type.

5.2 ELECTRICAL TESTS

5.2.1 Repetitive Rating Tests

5.2.1.1 Steady State Operational Life Test for Unidirectional Thyristors

A. Introduction

This test method is used to establish the maximum temperature, maximum voltage, and maximum current ratings for reverse blocking and reverse conducting diode and triode thyristors.

B. Operating Conditions

1. For devices registered for ac operation.

   a. Power sources shall be 60 Hz sinusoidal waveform sources.

   b. The test device shall be made to conduct rated average current at registered T_3.

   c. The conduction angle of the test current shall be 150° to 180°.

   d. The test temperature shall be T_3.

   e. Rated half sine wave repetitive peak reverse blocking voltage and rated half sine wave repetitive peak off-state voltage shall be applied during alternate non-conducting half cycles starting no later than 5° after conduction has ceased.

      Note: For devices which do not have a reverse blocking voltage rating, rated repetitive peak off-state voltage shall be applied during each non-conducting half cycle.

      For devices which have asymmetrical voltage ratings, the high voltage half wave supply can be replaced by two half wave thyristor supplies which would be synchronized to the high voltage reversing control. This would allow for independent off-state and reverse voltage ratings. The suggested test circuit shown in Figs. 5.1 and 5.2 would only test one bank of devices with the desired waveform. Therefore, the other bank could be replaced by one large device or a bank of devices having full symmetrical blocking voltage capability.

   f. The conduction angle of the blocking voltage shall be 175° ± 5°.

   g. A suggested test circuit is shown in Figs. 5.1 and 5.2.

2. For devices registered for dc operation

   a. Power sources shall be dc.

   b. The test device shall be made to conduct rated dc current at registered T_3, and then block rated dc off-state voltage alternately. The time at each condition shall be one hour.

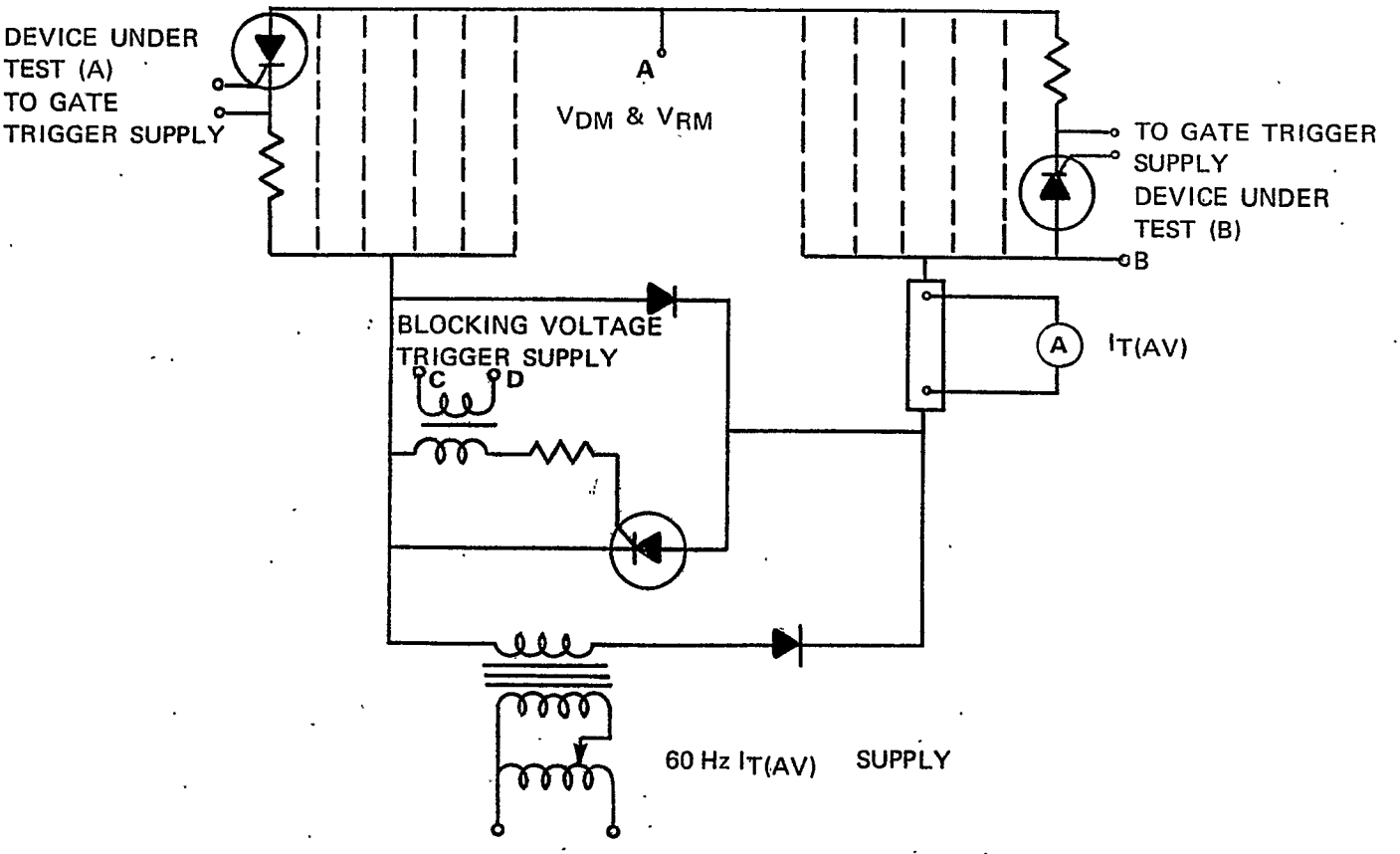
   c. The test temperature shall be T_3.

C. The duration of the life test shall be 1000 hours.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

FIGURE 5.1 – UNIDIRECTIONAL THYRISTOR LIFE TEST CIRCUIT



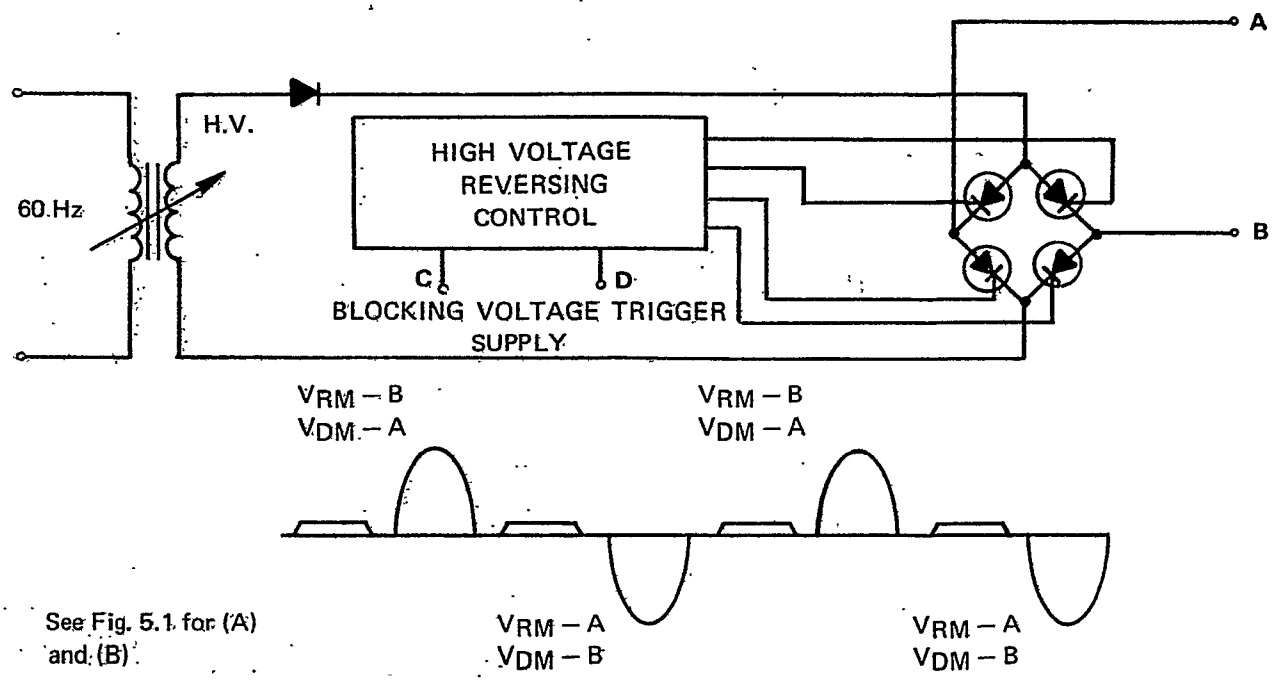


FIGURE 5.2 – HIGH VOLTAGE V_{DM} AND V_{RM} SUPPLY

5.2.1.2 Steady State Operational Life Test for Bidirectional Thyristors

A. Introduction

This test method is used to establish the maximum temperature, maximum voltage, and maximum current ratings for diode and triode bidirectional thyristors.

B. Operating Conditions

1. Power sources shall be 60 Hz sinusoidal wave form sources.

2. The device shall be made to conduct in one chosen direction a half cycle of current of peak value equal to twice its rated RMS current at registered T_3. Following the next half cycle interval in which there is no current flow the device shall be made to conduct the test current in the opposite direction.

3. The conduction angle of the test current shall be 150° to 180°.

4. The test temperature shall be T_3.

5. Rated half sine wave peak off-state voltage shall be applied during the non-conducting half cycles starting no later than 5° after conduction has ceased. The half cycle off-state voltage shall always be applied in the opposite direction from that of the current flow during the preceding half cycle.

6. The duration of the off-state voltage shall be 175° ± 5°.

C. The duration of the life test shall be 1000 hours.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.1.3 Alternating Principal Voltage Life Test

A. Introduction

This test method is used to establish the half sine wave repetitive peak off-state or reverse blocking voltage ratings for all types of thyristors.

B. Operating Conditions

1. Power source shall be a 60 Hz sinusoidal waveform source.

2. Test temperature shall be T_5.

3. Test voltage shall be rated half sine wave repetitive blocking voltage applied in both directions on alternate half cycles.

Note: For devices with asymmetrical voltage ratings, two independent half wave power sources would be required.

When testing reverse conducting devices, a single half wave power source would be required which would apply principal off-state voltage only in the positive direction.

4. Gate conditions shall be specified as

a. Gate source voltage and resistance or

b. Gate bias resistance.

5. Maximum thermal resistance from case to ambient shall be specified. (This requirement is to insure thermal stability).

C. The duration of the life test shall be 1000 hours.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.1.4 DC Off-State or Reverse Blocking Voltage Life Test

A. Introduction

This test method is used to establish the dc off-state and reverse voltage ratings for all types of unidirectional thyristors.

B. Operating Conditions

1. Power source shall be dc with 1% maximum ripple.

2. Test temperature shall be T_S.

3. Test voltage shall be rated dc value and the direction of application of the voltage shall be specified.

4. Gate bias conditions shall be specified as

a. Gate source voltage and resistance

or

b. Gate bias resistance

5. Maximum thermal resistance from case to ambient shall be specified. (This requirement is to insure thermal stability).

C. The duration of the life test shall be 1000 hours.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.1.5 Pulsed On-State Current Life Test

A. Introduction

This test method is used to establish the maximum pulsed on-state current ratings for thyristors.

B. Operating Conditions

1. The test current magnitude, waveform, duty cycle, and device test temperature shall be as given in the device registration data. If all of this information is not contained in the registration data, the device manufacturer must supply the missing information.

The rate of rise of on-state current must be limited to safe values as determined by the manufacturer.

The gate current pulse used to initiate conduction must be of sufficient amplitude and width to assure complete turn on of the test device, without exceeding any of the maximum gate ratings.

C. The test duration shall be 1000 hours.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.1.6 Gate Rating Life Test for Unidirectional Triode Thyristors

A. Introduction

This test method is to be used in establishing the Maximum Peak Positive Gate Current, Maximum Peak Negative Gate Voltage, Maximum Peak Gate Power and Maximum Average Gate Power Ratings for Unidirectional Triode Thyristors.

B. Operating Conditions

1. For ac rated thyristors

a. The test device will be operated at the Steady State Operational Life Test conditions of Section 5.2.1.1.

b. The positive gate pulse applied at 60 pps to initiate conduction will be of rectangular waveform and adjusted in amplitude so that either the peak positive gate power or the peak positive gate current is equal to the maximum rated value.

Note: For any one device it may not be possible to apply rated peak gate power without exceeding rated peak gate current, or vice versa. Therefore the general test method for gate ratings will require adjusting the gate pulse amplitude for one or both of these ratings without exceeding the other. When it is desirable to test for only one of these ratings, selection of devices having the proper gate characteristics must be made.

c. During the non-conducting intervals a pulse of negative voltage will be applied to the gate which is equal in amplitude to the Maximum Peak Negative Gate Voltage rating.

d. The positive and negative gate pulses will be adjusted in width so that the average gate power dissipated is equal to the Maximum Average Gate Power rating or so that the pulses last for the entire half cycle during which they are applied, whichever is smaller.

2. For dc rated thyristors

a. The procedure will be the same as for ac rated thyristors.

b. The value of $I_{T(AV)}$ to be used will be found from the value of I_T registered at T_3 using the following formula:

$$I_{T(AV)} = I_T/1.57$$

c. The peak off-state and peak reverse principal voltage which will be applied will be equal to the registered dc values.

C. The test duration will be 1000 hours.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.1.7 Gate Rating Life Test for Bidirectional Triode Thyristors

A. Introduction

This test method is to be used in establishing the Maximum Peak Positive (or Negative) Gate Voltage rating, the Maximum Peak Positive (or Negative) Gate Current rating and the Maximum Peak Gate Power and Maximum Average Gate Power ratings for Bidirectional Triode Thyristors.

B. Operating Conditions

1. The test device will be operated at the Steady State Operational Life Test conditions of section 5.2.1.2.

2. The current pulse applied to the gate to initiate conduction will be of rectangular waveform. For devices registered with triggering capability for either direction of gate current, the gate current pulse will be alternately positive and negative for each successive conducting half cycle. For devices registered with triggering capability for only one direction of gate current, all gate pulses will be applied in that one direction.

3. The gate current pulse amplitude will be adjusted such that one or more of the following ratings is reached but none is exceeded:

   Max. Peak Positive (or Negative) Gate Voltage
   Max. Peak Positive (or Negative) Gate Current
   Max. Peak Positive (or Negative) Gate Power

   Note: For any one device it may not be possible to apply a gate pulse of either polarity which satisfies all three ratings simultaneously. Therefore, the general test method for gate ratings will require adjusting the gate current pulse amplitude for one or all of these ratings without exceeding any of the others. When it is desirable to test for only one of these ratings, selection of devices having the proper gate characteristics must be made.

4. The pulse widths of the positive and negative gate current pulses will be equal. Pulse widths will be adjusted so that the rated Maximum Average Gate Power is dissipated, or so that the pulses last for the entire conducting half cycle during which they are applied, whichever is smaller.

C. The test duration shall be 1,000 hours.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.1.8 Repetitive Pulse Current Rating, Under Specified Turn-Off Conditions, Life Test for Reverse Blocking Thyristors.

A. Introduction

This test method is used to establish the repetitive pulse current rating under specified turn-off conditions. This current rating is actually a test condition called for in the pulse circuit commutated turn-off time characteristics. This characteristic is repetitive and therefore its current rating test condition must also be repetitive.

B. Operating Conditions

The test device is operated exactly as specified in Section IV.0 of the registration format.

C. The test duration shall be such that 10^9 cycles minimum is achieved.

D. All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.1.9 Thermal Fatigue Life Test for Thyristors

A. Introduction

This is a reference test method used to establish the ability of a thyristor to withstand the thermal cycling produced by alternately applying and removing on-state current. Blocking voltages are not involved in this test except as required by the ac heating current source operating into a very light load. This test method applies to unidirectional and bidirectional thyristors whose temperature reference point is on the device case.

B. Operating Conditions

1. The heating current source shall be 50/60 Hz sinusoidal ac supply.

2. The heating current conduction angle shall be 150° to 180° when testing unidirectional thyristors and 150° to 180° for each operating quadrant when testing bidirectional thyristors.

3. The heating current magnitude shall be that value registered at temperature T_3.

4. The case temperature reached at the end of the heating period shall be T_3 $^{+10°C}_{-0}$

5. The case temperature reached after the cooling period shall be 30 ± 10°C.

6. The change in case temperature produced by the conditions specified in 4 and 5 must be 50°C minimum. If this cannot be achieved using the heating current-case temperature specified in 3, the current may be reduced (but not less than 50% of registered value) so that the case temperature can be raised. Consult manufacturers current rating curves.

7. The heating period shall be greater than the device thermal time constant* but less than 6 minutes.

8. The cooling period shall be greater than the device thermal time constant* but less than 8 minutes.

9. The total time for one heating-cooling cycle shall be 10 minutes maximum. See Fig. 5.3.

*Thermal time constant is defined here as the time for the test device case temperature and junction temperature differential to stabilize.

10. A suggested test circuit for testing many devices at a time is shown in Fig. 5.4. The test devices are connected in series with two inverse parallel strings when testing unidirectional thyristors and one string when testing bidirectional thyristors. To obtain identical case temperature excursion, the power dissipation and thermal resistance of the test devices must be matched or the individual heat dissipators must be made adjustable.

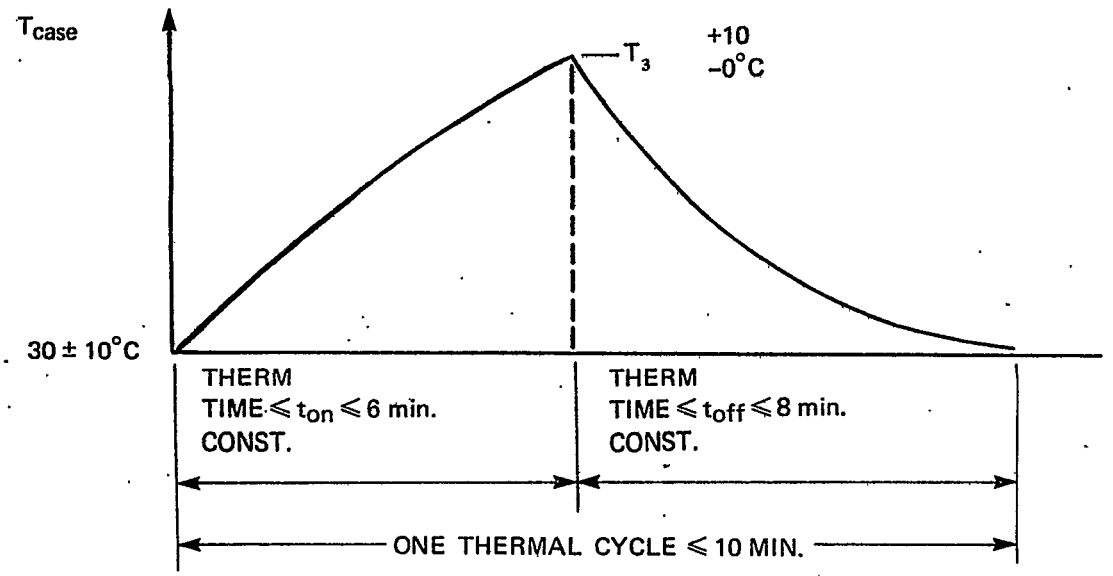
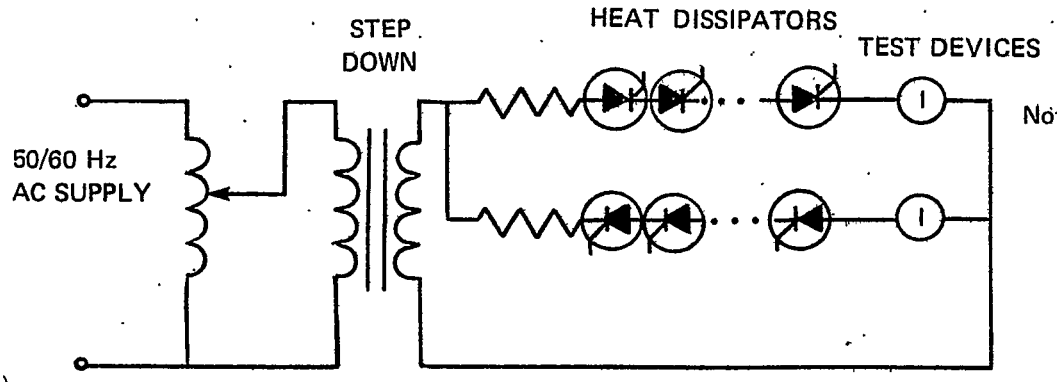


FIGURE 5.3



Note: (1) Any convenient gate triggering may be used including anode triggering.
(2) Resistors improve test current waveform and balance and effects of changing on-state voltage.

FIGURE 5.4

C. Test Duration

The duration of the test is to be specified as a number of complete thermal cycles.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type in addition to thermal resistance.

5.2.2 Non-Repetitive Rating Tests

5.2.2.1 60 Hz Sine-Wave Surge Current Test and Non-Repetitive Peak Reverse Voltage Test

A. Introduction

This test method is used to establish the sine-wave surge current ratings for all types of thyristors except those registered with dc ratings only, and to establish the non-repetitive peak reverse voltage rating for reverse blocking thyristors. The thyristor is not required to regain gate control during or immediately following this current surge test. However, gate control must be regained after the device has cooled to its original thermal equilibrium conditions.

B. Test Method

The test device is operated under steady state rated current and voltage conditions before and after the application of the surge current. In testing reverse blocking thyristors, immediately following the half cycle surge current, a half sine wave of reverse voltage of magnitude equal to the device non-repetitive peak reverse voltage rating is applied. In testing bidirectional thyristors, the test current is full cycle and no reverse voltage is involved in the test. (See Fig. 5.5 thru 5.8 for surge test circuits and waveforms). The time between current surges shall be long enough to permit the device temperature to return to its original thermal equilibrium.

C. Operating Conditions

1. The power sources shall be 60 Hz sinusoidal waveform sources.

2. The test device shall be made to conduct rated average forward current at T_3 and rated repetitive peak reverse voltage, half wave, shall be applied. The half cycle conduction angle of test current and voltage must be 150° – 180°.

Note:

a. For bidirectional devices, the current shall be rated RMS value and no reverse voltage is applied.

b. For reverse conducting thyristors no reverse voltage is applied.

3. The steady state thermal equilibrium test temperature shall be T_3.

4. Gate bias conditions shall be specified as:

a. Gate source voltage and resistance

or

b. Gate bias resistance

5. The peak value of the surge current shall be specified. For unidirectional thyristors, the test current waveform is a single half cycle sine wave. For bidirectional thyristors, the test current waveform is a full cycle sine wave. Test current half cycle conduction angles must be 150° – 180°.

6. Rated non-repetitive peak reverse voltage half sine wave shall be applied during the half cycle immediately following the half cycle of rated surge current.

Note:

a. If a reverse blocking device does not have this voltage rating registered, use as test voltage the repetitive peak reverse voltage, half-sine-wave rating.

b. This test condition is deleted when surge current testing bidirectional or reverse conducting thyristors.

7. The number of current surges to be applied shall be 100.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

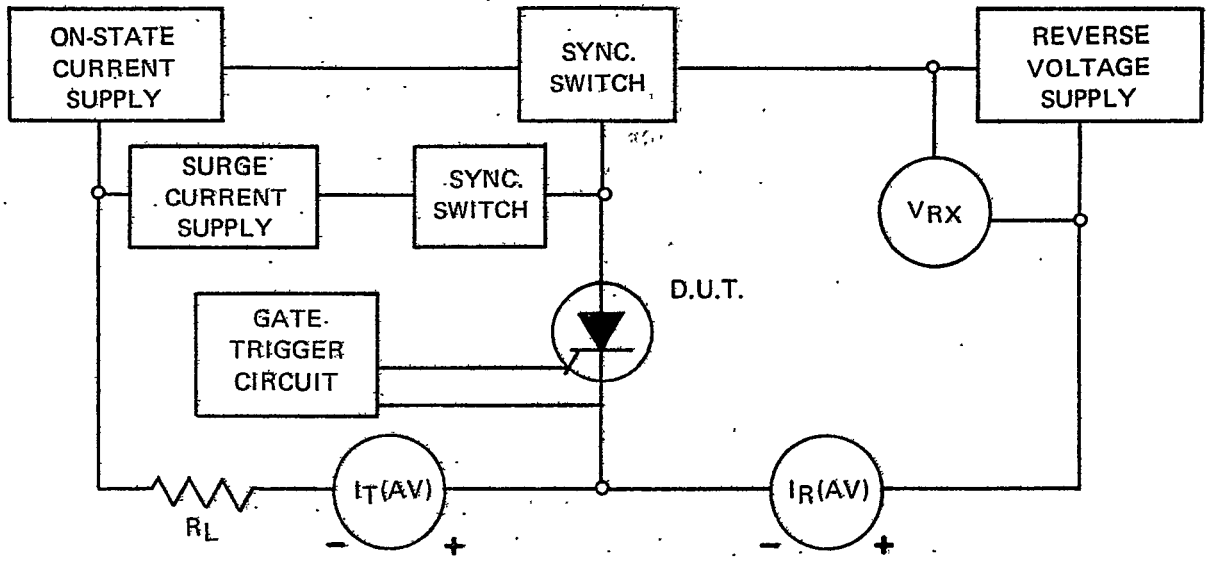


FIGURE 5.5 – BASIC TEST CIRCUIT FOR THE 60 HZ SINE-WAVE SURGE CURRENT AND NON-REPETITIVE PEAK REVERSE BLOCKING VOLTAGE TEST

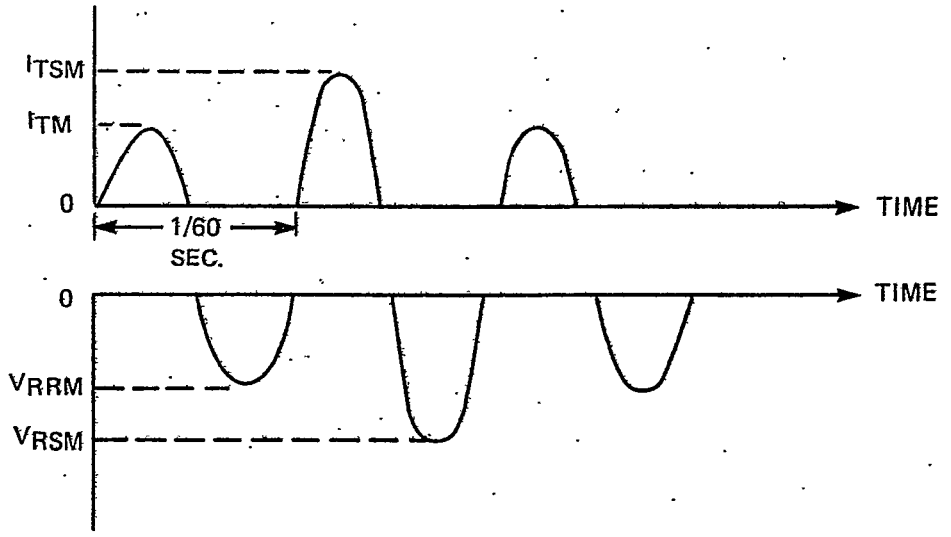


FIGURE 5.6 – VOLTAGE AND CURRENT WAVEFORMS APPLIED TO THE DEVICE UNDER TEST

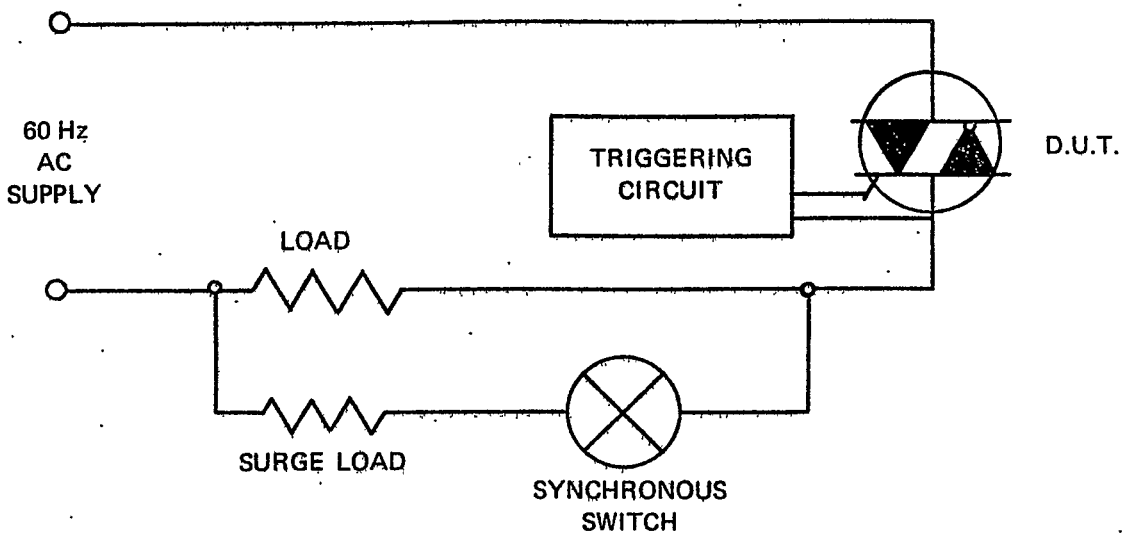


FIGURE 5.7 – BASIC TEST CIRCUIT FOR THE BIDIRECTIONAL THYRISTOR SURGE CURRENT TEST

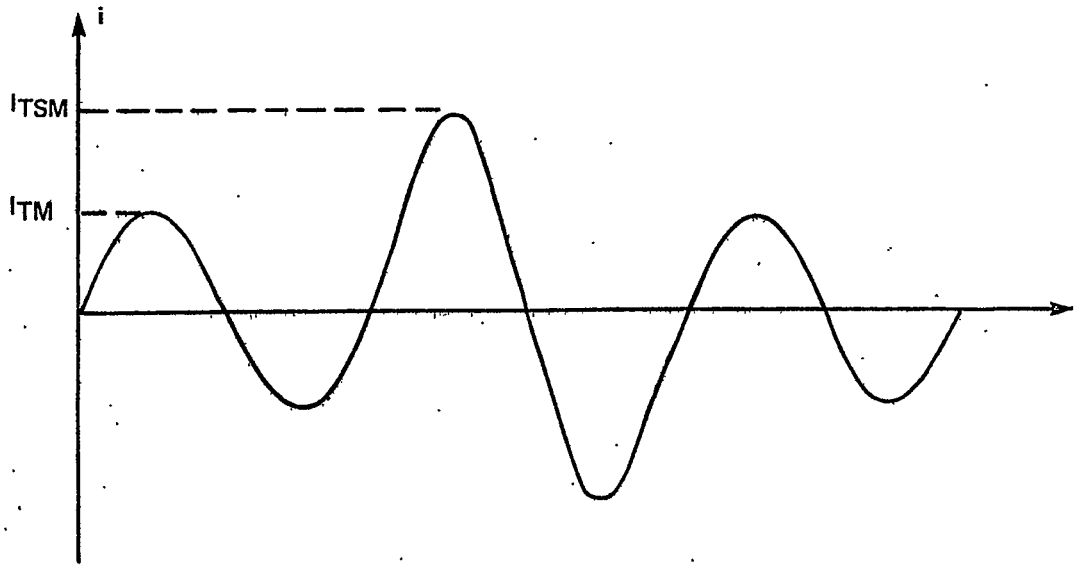


FIGURE 5.8 – CURRENT WAVEFORM APPLIED TO THE THYRISTOR UNDER TEST

5.2.2.2 Surge (Non-Repetitive) On-State Current, 1.5 Millisecond Duration, Test

A. Introduction

This test method is used to establish the 1.5 millisecond half-sine-wave surge current ratings for all types of thyristors except those registered with dc ratings only. The thyristor is not required to block voltage or retain gate control during or immediately following this current surge test. However, the thyristor must regain gate control and rated blocking voltage capabilities after it has cooled to its original thermal equilibrium conditions.

B. Test Method

The test device is to be brought up to steady state thermal equilibrium temperature before the application of the surge current. Following the current surge, no reverse or off-state voltage is to be applied until the device has cooled to the original steady state thermal equilibrium condition. (See Fig. 5.9 and 5.10 for surge current test circuits and wave forms.) The time between current surges shall be long enough to permit the device virtual junction temperature to return to its original thermal equilibrium value.

The gate signal duration to the test device and initiating device should be less than 1.5 milliseconds to prevent a possible second pulse due to circuit oscillations.

The values of L (total discharge circuit inductance), C, and E_C must be set to produce the specified peak surge current and specified pulse width.

C. Operating Conditions

1. The power source shall be suitable to charge C to the necessary value to produce the specified peak surge current.

2. Prior to application of surge current, the device temperature shall be brought up to the specified case temperature by use of an external heat source, such as a temperature-controlled mounting block.

3. The specified case temperature shall be T_S.

4. Gate bias conditions shall be specified as:

   a. Gate source voltage and resistance, or

   b. Gate bias resistance.

5. The peak value of the surge current shall be specified. The test current waveform is a single half-cycle sine wave. The single half-cycle sine-wave test current pulse width must be 1.5 milliseconds ± 0.15 millisecond.

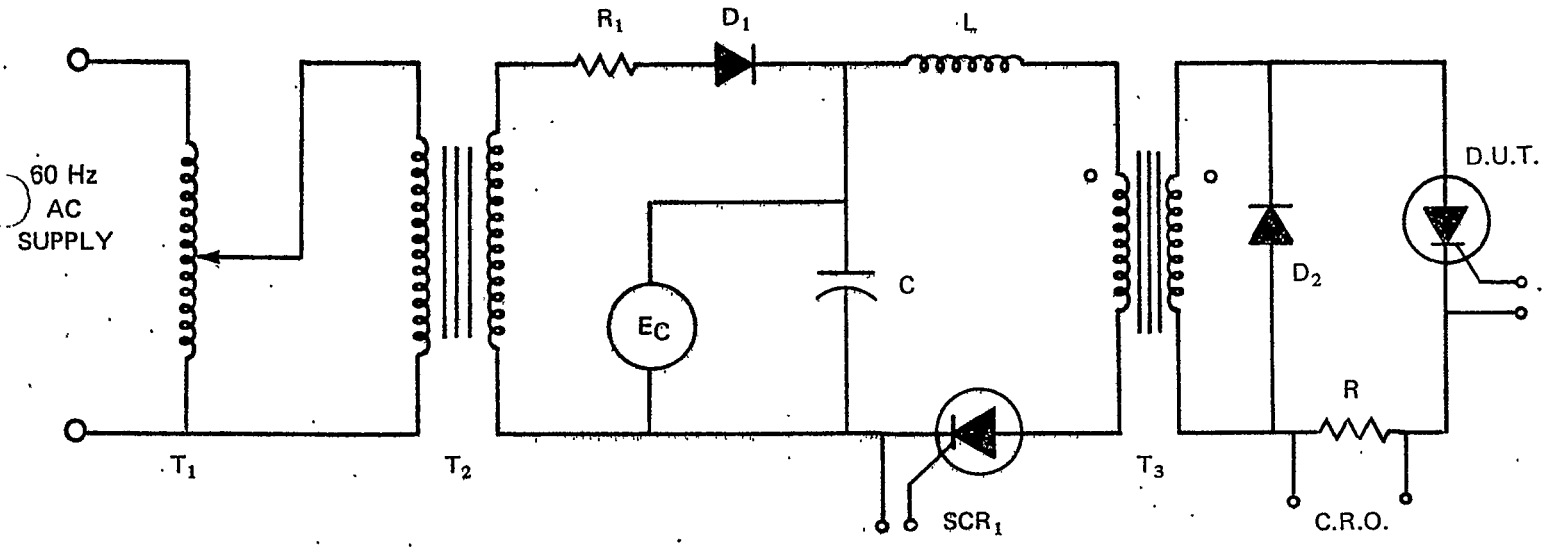
6. No voltage shall be applied immediately following the half cycle of surge current.

7. The minimum time between each surge current pulse shall be 20 seconds.

8. The number of current surges to be applied shall be 100 for unidirectional thyristors. For bidirectional thyristors, the number of pulses shall be 100 in one direction then 100 in the opposite direction.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.



R_1	=	Charging current limiting resistor
R	=	Non-inductive current viewing resistor
T_1	=	Variable autotransformer
T_2	=	Isolation transformer
T_3	=	Current step-up transformer
D_1	=	Charging diode
D_2	=	Bypass diode
C, L, E_C	=	Values set for specified surge current and pulse width. L includes total discharge circuit inductance.
SCR_1	=	Initiating SCR. Trigger SCR_1 and DUT simultaneously

FIGURE 5.9 – BASIC TEST CIRCUIT FOR SURGE (NON-REPETITIVE) ON-STATE CURRENT, 1.5 MILLISECOND DURATION, TEST

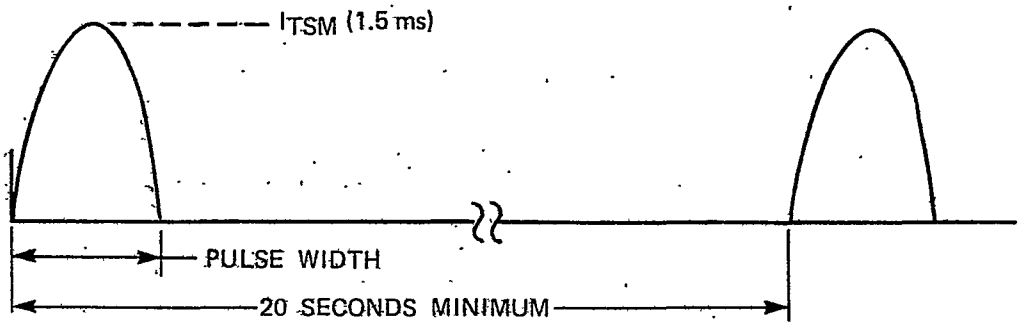


FIGURE 5.10—CURRENT WAVEFORM APPLIED TO THE DEVICE UNDER TEST

5.2.2.3 Surge (Non-Repetitive) On-State Current, 0.5 Millisecond Duration, Test

A. Introduction

This test method is used to establish the 0.5 millisecond half-sine-wave surge current ratings for all types of thyristors except those registered with dc ratings only. The thyristor is not required to block voltage or retain gate control during or immediately following this current surge test. However, the thyristor must regain gate control and rated blocking voltage capabilities after it has cooled to its original thermal equilibrium conditions.

B. Test Method

The test device is to be brought up to steady state thermal equilibrium temperature and the voltage across the device must be the rated V_{DRM} before the application of the surge current. The device is to be gated on by the specified gate trigger pulse conditions. Following the current surge, no reverse or off-state voltage is to be applied until the device has cooled to the original steady state thermal equilibrium condition. (See Fig. 5.11 and 5.12 for surge current test circuits and waveforms.) The time between current surges shall be long enough to permit the device virtual junction temperature to return to its original thermal equilibrium value.

The gate signal duration to the initiating device should be less than 0.5 milliseconds to prevent a possible second pulse due to circuit oscillations.

The values of L_1 (total high current discharge circuit inductance), C_1 and E_{C1} must be set to produce the specified peak surge current and specified pulse widths. The values of L_2 (total high voltage discharge circuit inductance), C_2 and E_{C2} must be set to produce 5 per cent of the specified peak surge current and 5 per cent of the specified pulse width. E_{C2} must be rated V_{DRM} for the device under test.

C. Operating Conditions

1. The power source for C_1 shall be suitable to charge C_1 to the necessary value to produce the specified peak surge current. The power source for C_2 shall be suitable to charge C_2 to V_{DRM} rating of the device under test and to produce 5 per cent of the specified peak surge current.

2. Prior to application of surge current:

   a. The device shall be brought up to the specified case temperature by use of an external heat source, such as a temperature-controlled mounting block.

   b. The high voltage circuit shall supply the specified voltage across the device.

3. The specified case temperature shall be T_S.

4. The voltage across the device prior to conduction shall be V_{DRM}. Prior to gating the device on, the high voltage charging circuit must be inactivated to avoid stressing the device with voltage after the surge.

5. The device shall be gated on by a gate trigger pulse specified as to:

   a. Pulse width, t_W

   b. Rise time, t_r

   c. Gate source voltage and resistance.

6. The peak value of the surge current shall be specified.

   a. The high current circuit test current waveform is a single half-cycle sine wave. The peak value of the current is the specified surge current. The pulse width of the current must be 0.5 millisecond ± 0.05 millisecond.

   b. The high-voltage-circuit test current waveform is a single half-cycle sine wave. The peak value of the current is 5 per cent of the specified surge current. The pulse width of the current must be 0.025 millisecond ± 0.0025 millisecond.

   c. The high-current-circuit test current and the high-voltage-circuit test current must be initiated simultaneously.

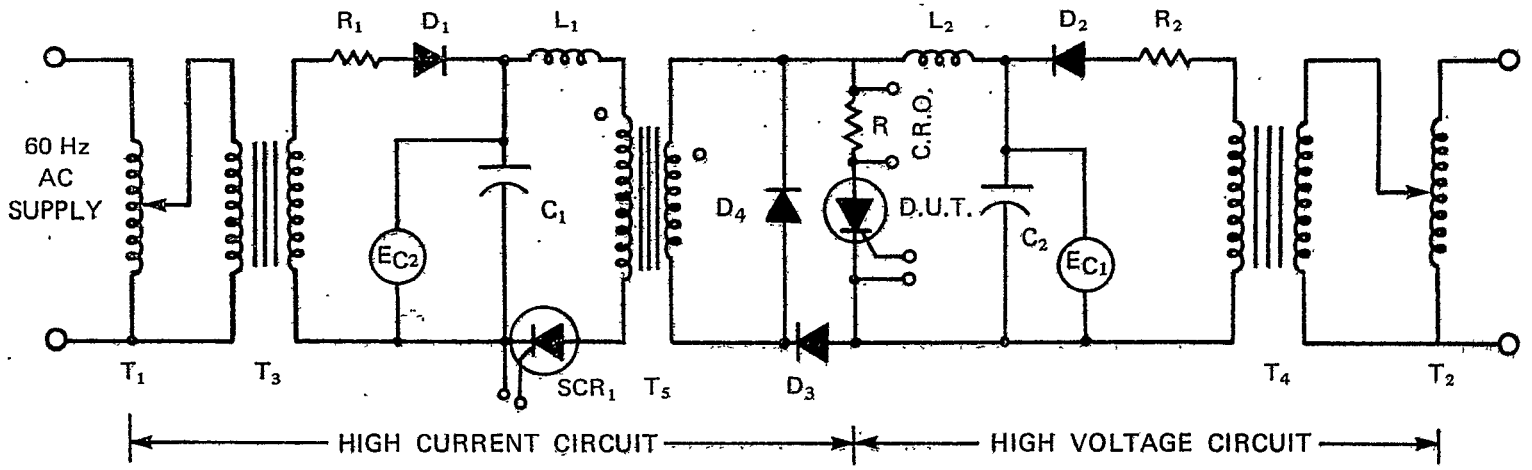
7. No voltage shall be applied immediately following the half cycle of surge current.

8. The minimum time between each surge current pulse shall be 20 seconds.

9. The number of current surges to be applied shall be 100 for unidirectional thyristors. For bidirectional thyristors, the number of pulses shall be 100 in one direction then 100 in the opposite direction.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.



R_1, R_2	=	Charging current limiting resistors
R	=	Non-inductive current viewing resistor
T_1, T_2	=	Variable autotransformers
T_3, T_4	=	Isolation transformers
T_5	=	Current step-up transformer
D_1, D_2	=	Charging diodes
D_3,	=	Isolating diode
D_4	=	Bypass diode
C_1, L_1, E_{C1}	=	Values set for specified surge current and pulse width
$C_2, L_2, C2$	=	E_{C2} set to V_{DRM} of Device Under Test. E_{C2}, L_2, C_2 set for 1/20 specified Surge Current and 1/20 specified Pulse Width
SCR_1	=	Initiating SCR

FIGURE 5.11 – BASIC TEST CIRCUIT FOR SURGE (NON-REPETITIVE) ON-STATE CURRENT, 0.5 MILLISECOND DURATION, TEST

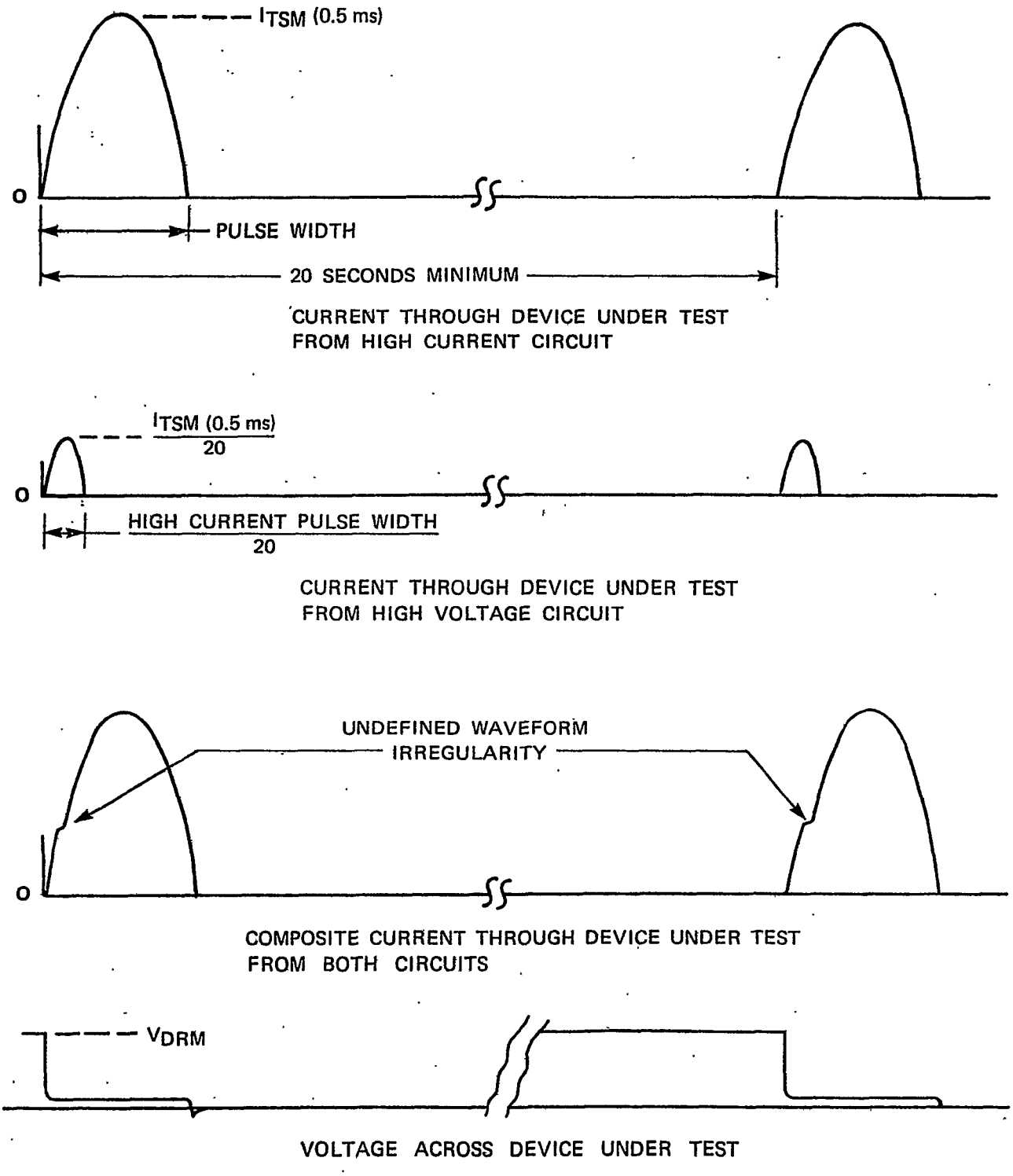


FIGURE 5.12 – VOLTAGE AND CURRENT WAVEFORMS APPLIED TO THE DEVICE UNDER TEST

5.2.2.4 Rectangular Pulse Surge Current Test

A. Introduction

This test method is used to establish the square wave surge current rating for thyristors registered with continuous dc ratings.

B. Test Method

The test device is operated under its steady state continuous current rating at T_3 before and after the application of the surge current. The time between current surges shall be long enough to permit the device temperature to return to its original thermal equilibrium. No reverse or off-state voltage conditions are involved in this test.

C. Operating Conditions

1. Power sources shall be dc with $\leqslant$ 5% ripple.

2. The test device shall be operated at its continuous current rating.

3. The steady state thermal equilibrium test temperature shall be T_3.

4. The single rectangular pulse of surge current shall be specified as to:

   a. Amplitude

   b. Width as measured at 50% points

   c. Rise time

5. The number of current surges to be applied shall be 100.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.2.5 Peak Positive Anode Voltage Test

A. Introduction

This test method is used for establishing the peak positive anode voltage rating for triode thyristors which are registered either for ac or dc operation. This is a non-repetitive rating and it represents the maximum value of off-state voltage which may be applied to a thyristor without causing permanent damage even if breakover turn-on occurs.

B. Test Method

The test device shall be connected through a load resistance to a source of voltage capable of delivering a single voltage pulse of peak value equal to the peak positive anode voltage rating of the device. The test voltage shall be a half sine wave for ac rated thyristors and shall be a square wave for dc rated thyristors. The duration of the test voltage is not to exceed 8.3 milliseconds. The test voltage pulses are applied at a rate slow enough to permit the test device to return to its original thermal equilibrium between pulses. The series load resistance must limit conduction current to within rated value in the event of device turn-on. The load resistor is computed as follows:

$$R_L = \frac{\text{Pk. Pos. Anode Voltage Rating}}{\pi \text{ X (Avg Current Rating at } T_3)} \text{ for AC Rated Thyristors}$$

$$R_L = \frac{\text{Pk. Pos. Anode Voltage Rating}}{\text{Cont. Current Rating at } T_3} \text{ for DC Rated Thyristors}$$

It is important to observe in performing this test that the rate of rise of blocking voltage and rate of rise of conduction current does not exceed the device rating or capability.

C. Operating Conditions

1. The peak test voltage shall be specified as the peak positive anode voltage rating of the device with pulse width not to exceed 8.3 milliseconds. The test voltage waveform shall be half sinusoidal for ac rated thyristors and square wave for dc rated thyristors.

2. The steady state thermal equilibrium test temperature shall be T_5.

3. Gate bias conditions shall be specified as.

   a. Gate source voltage and resistance

   or

   b. Gate bias resistance

4. The load resistance shall be specified.

5. The number of pulses to be applied shall be 100.

6. The minimum time between pulses is to be two minutes.

D. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.2.2.6 Critical Rate of Rise of On-State Current Test

A. Introduction

The rate at which on-state current can be increased in a thyristor is limited by the initial turned on area and the rate of increase and modulation of the active area during turn on. This test method may be used to apply a rate of rise of on-state current (di/dt) stress to a triode thyristor for the purpose of establishing a rating. This rating is necessary for those devices unable to withstand the rate of rise of on-state current determined by their turn-on characteristics in a non-inductive circuit.

This rating may be either repetitive or non-repetitive which means respectively that the rating may be applied an unlimited or a limited number of times. Two different non-repetitive ratings may be assigned to triode thyristors: one for gate triggering and one for triggering by exceeding the thyristor breakover voltage. The time between on-state current pulses in the non-repetitive rating case shall be long enough to insure that the device temperature has returned to its original thermal equilibrium. For bidirectional devices, these ratings apply for operation in either quadrant.

B. Test Circuit

A suitable test circuit is shown in Fig. 5.13. The di/dt stress is applied using the device under test to discharge a capacitor through a series resistor and inductor to produce a damped on-state current pulse. Reverse switching transients may be suppressed as this method is intended to be a test of on-state switching capability only. Approximate values of R, L and C in terms of the test conditions are given in Fig. 5.13. For those values of circuit constants to apply in the case of breakover voltage triggering, V_{DM} is replaced by the $V_{(BO)}$ of the test device.

C. Operating Conditions

1. Fig. 5.14 illustrates the on-state current wave shape, and identifies several test conditions.

2. The time t_1 shall be $\geqslant$ 1 microsecond.

3. I_{TM} shall be $\geqslant$ twice the rated value of on-state current at T_3. (The rated value of on-state current at T_3 will be an average value for ac rated devices and a dc value for dc rated devices).

4. The pulse repetition rate for establishment of the repetitive rating for unidirectional thyristors and for bidirectional thyristors shall be 60 p/s.

5. The off-state voltage V_{DM}, when applicable, shall be equal to the rated value at T_5.

6. The temperature shall be T_5.

7. The gate trigger pulse, when applicable, shall be specified as to:

   a. Pulse width, t_w

   b. Rise time, t_r

   c. Gate source voltage and resistance

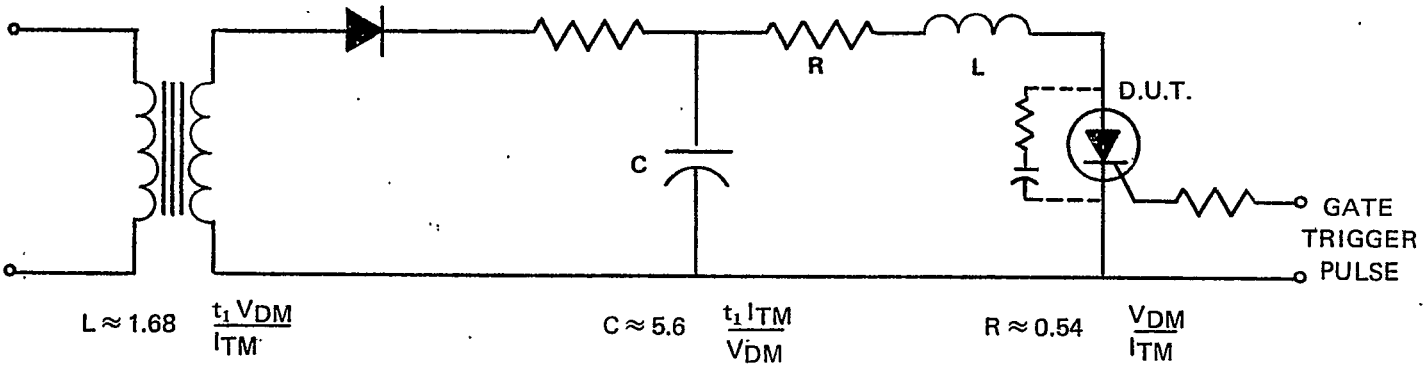


FIGURE 5.13 – BASIC TEST CIRCUIT FOR THE CRITICAL RATE OF RISE OF ON-STATE CURRENT TEST

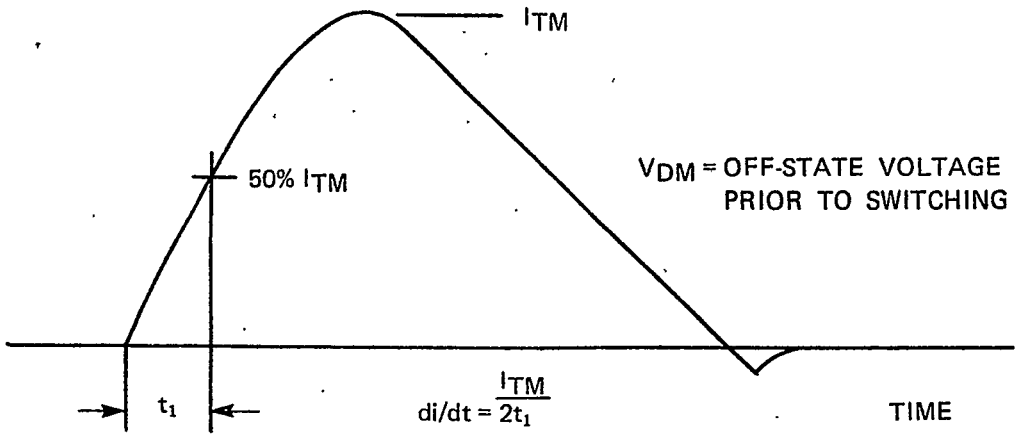


FIGURE 5.14 – ON-STATE CURRENT WAVESHAPE FOR THE CRITICAL RATE OF RISE OF ON-STATE CURRENT TEST

D. Test Duration

1. The test duration shall be 1000 hours in establishing the repetitive rating.

2. The number of on-state current pulses shall be 100 in establishing the breakover-voltage-triggered non-repetitive rating.

3. The number of on-state current pulses shall be 300 at a 60 Hz repetition rate in establishing the gate-triggered non-repetitive rating.

E. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.3 ENVIRONMENTAL TESTS

5.3.1 Storage Life Test

A. Introduction

This test method is used to establish the storage temperature range rating for all types of thyristors. Since the maximum storage temperature (T_7) represents the greatest stress condition to the test device, the storage life test is usually performed at this temperature.

B. Operating Conditions

1. The storage temperature, usually T_7, shall be specified.

2. The test duration shall be 1000 hours.

C. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish the rating.

5.3.2 Lead or Terminal Temperature Test

A. Introduction

This test is to be used to verify the maximum lead or terminal temperature rating for soldering purposes for a specified distance from the case of the device for a specified time.

B. Operating Conditions

A solder pot, containing lead – tin alloy with a nominal tin content of at least 50 per cent – shall be used. This apparatus shall be capable of maintaining the liquid at the temperature specified. The device leads shall be immersed for the specified time at the specified temperature to the specified distance from the case of the device. The leads shall be immersed individually or simultaneously.

After immersion, units shall be allowed to cool and stabilize at room ambient conditions before final examination and measurement are made.

C. Post Test Measurements

All of the characteristics given in Section 5.4 which are indicated as being applicable to the device type shall be measured to establish to rating.

5.4 POST TEST MEASUREMENTS

Measurements of the characteristics given in this section shall be made following any of the Rating Performance Tests of Sections 5.2 and 5.3 to establish the ratings. Only those characteristics which are indicated as being applicable to the device type being tested shall be measured. The test conditions for measurement of each characteristic shall preferably be as registered.

A. Off-State Current (All Devices)
Test Conditions to be Specified:

1. Gate source voltage and resistance, or gate bias resistance.

2. Temperature

3. Off-state voltage

B. Reverse Blocking Current (Reverse Blocking Thyristors Only)
Test Conditions to be Specified:

1. Gate source voltage and resistance, or gate bias resistance.

2. Temperature

3. Reverse blocking voltage

C. On-State Voltage (All Devices)
Peak value under pulse conditions shall be used.
Test Conditions to be Specified:

1. Temperature (shall be 25°C ambient)

2. Pulse width (shall be 1 to 2 ms).

3. Duty cycle (shall be $\leq$ 2%)

4. Peak on-state current

D. Peak Gate Trigger Current (Triode Thyristors Only)
Test Conditions to be Specified:

1. Minimum gate pulse width.

2. Source voltage ($\leq$ 12 volts) and load resistance for the principal current.

3. Polarity of main terminal 2 (for bidirectional devices only).

4. Temperature (T_2).

E. Breakover Characteristics (Diode Thyristors Only)

1. Peak breakover voltage at a specified temperature from T_2 to T_5.

2. Peak breakover current at a specified temperature from T_2 to T_5.

PART 6

CHARACTERISTIC TESTS

INDEX

6.3.1.1.6 Latching Current

6.3.1.1.7 DC Holding Current

6.3.1.1.8 Gate Trigger Current and Voltage

6.3.1.1.9 Gate Non-Trigger Current and Voltage

6.3.1.1.10 DC Negative Gate Current

6.3.2 AC Tests (Dynamic)

6.3.2.1 Test Circuits and Procedures

6.3.2.1.1 AC Reverse Blocking Current

6.3.2.1.2 AC Off-State Current

6.3.2.1.3 AC On-State Voltage

6.3.3 Instantaneous or Pulse Tests

6.3.3.1 Test Methods

6.3.4 Switching Time Tests

6.3.4.1 Gate-Controlled Turn-On Time Test Method

6.3.4.2 Circuit-Commutated Turn-Off Time Test Method for Reverse Blocking Thyristors.

6.3.4.3 Gate Turn-Off Time Test Method for Gate Turn-Off Thyristors.

6.3.4.4 Pulse-Circuit-Commutated Turn-Off Time Test Method for Reverse Blocking Triode Thyristors.

6.3.5 Critical Rate of Rise of Off-State Voltage Test

6.3.5.1 Exponential Voltage Rise Test Method

6.3.5.2 Linear Voltage Rise Test Method

6.3.6 Thermal Resistance and Transient Thermal Impedance Test Method

6.3.7 Critical Rate of Rise of Commutation Voltage for Bidirectional Thyristors

PART 6

CHARACTERISTIC TESTS

6.1 GENERAL

The purpose of this section is to set forth accepted test practices as a guide in making thyristor characteristic tests.

6.2 ELECTRICAL MEASUREMENTS – GENERAL

Electrical measurements of semiconductor thyristors will, to a large extent, depend upon equipment circuit parameters such as source impedance, type of load and type of circuit. For this reason, measurements will be confined mainly to measurements of single thyristor parameters. Where it is necessary, an arbitrary choice of associated circuit parameters may be made to provide the necessary standardization between the user's and the manufacturer's testing procedure. Correlation between these tests and specific equipment tests will be the responsibility of the user.

6.2.1 Choice of Meters

The current wave into and the voltage and current waves out of a thyristor circuit may be distorted due to inherent action of the circuit and/or the circuit element. The selection of the proper type of instrument is important for accuracy of measurement. Conventional sinusoidal conversion factors are not applicable in converting between reverse and off state currents and on state voltages from average to rms or peak values.

6.2.1.1 Input

The input alternating voltage and current shall be measured with instruments which respond to the root-mean-square values of the quantities being measured. Rectifier-type meters are satisfactory only with undistorted wave forms.

6.2.1.2 Output

Unless otherwise specified the output voltage and current of a thyristor circuit shall be measured with permanent-magnet moving-coil-type direct-current instruments. Such instruments will indicate the average values of the quantities measured. If the root-mean-square values are to be measured, dynamometer-type instruments should be used. (Iron-vane-type instruments may be used with some sacrifice in accuracy.) Rectifier-type instruments should not be used to measure these quantities because of inaccuracies on distorted wave forms.

6.2.2 Ripple Voltage

The root-mean-square value of the ripple voltage may be measured with a root-mean-square indicating meter in series with a capacitor having sufficiently low impedance so as not to affect appreciably the indication of the voltmeter. Rectifier-type instruments should not be used.

6.2.3 Thermal Equilibrium Conditions

When measuring a temperature sensitive static parameter under conditions such that the product of the applied voltage and current at the test point produces a dissipation level which would cause significant heating of the junction, the measured result may be subject to errors due to thermal drift. In order to avoid such errors, the measurement should be made under defined conditions of thermal equilibrium. Thermal equilibrium may be achieved under either of two conditions, steady state dc or short pulse. The criteria for determining when thermal equilibrium has been reached are described below:

6.2.3.1 Steady State DC Measurements

When making measurements under conditions of steady state dc, a condition of thermal equilibrium may be considered to have been achieved if halving the time between the application of power and the taking of the reading causes no error in the indicated result within the required accuracy of measurement. For these purposes very long pulses or step functions may be considered as steady state dc.

6.2.3.2 Pulse Measurements

When measurement is made under pulse conditions, thermal equilibrium may be considered to have been achieved immediately upon application of power provided that the pulse width is short enough to that doubling causes no error within the required accuracy of measurement. When making measurements under pulse conditions, the pulse width should be long enough to insure that the reading is taken after carrier equilibrium has been achieved.

6.2.4 Gate Trigger and Bias Conditions

6.2.4.1 Gate Trigger Pulse

The gate trigger pulse is defined as a rectangular voltage pulse applied to the device under test through a series resistance. The specification of the pulse should be in terms of the load line presented to the gate and reference terminals of the device under test as _____ volts and _____ ohms. If additional circuitry is connected to the gate – reference terminals for bias purposes, its effect on the specified load line must also be included. If the dynamic impedance of the generator is less than 5% of the specified series resistance, its effect on the test may be considered negligible and the gate pulse amplitude may be observed at the generator terminals during the test. If the generator does not have a low dynamic impedance, the pulse voltage should be set with the test device disconnected and the resistance should be determined by measuring the pulse current with gate shorted to reference. The total series resistance is calculated from open circuit voltage divided by short circuit current equals R, the total resistance. The gate pulse width is measured between the 50% points of the rising and falling wave form as shown in Figure 6-1. Gate pulse rise time is measured between the 10% and 90% points of the rising wave form. When the dynamic impedance of the gate pulse generator is negligible, the rise time of the trigger pulse voltage is measured on the open-circuited pulse generator output waveform. When the dynamic

impedance of the pulse generator is not negligible, the rise time of the pulse generator voltage is taken as the rise time of the current produced when the output of the pulse generator is short-circuited or as the rise time of the voltage across a non-inductive resistor connected to the output of the gate pulse generator of such ohmic value as to approximate the thyristor gate resistance.

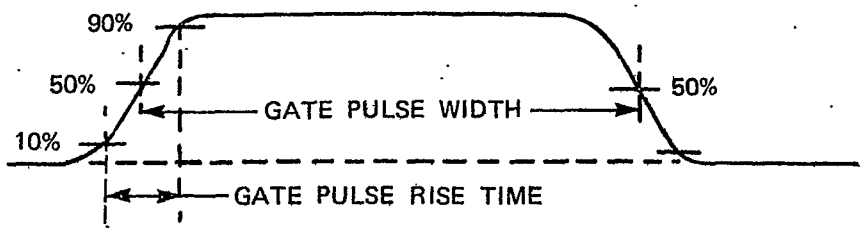


FIGURE 6.1 – GATE TRIGGER PULSE WAVE FORM

6.2.4.2 Gate Bias

The load line presented to the gate and reference terminals of the device under test during the interval between trigger pulses acts as gate bias. This gate bias load line is specified as _____ volts and _____ ohms. If the voltage is other than zero, the polarity of the gate terminal must be specified. Unless some means is provided for isolating the trigger pulse generator from the device under test, it will provide gate bias and should be specified accordingly.

The following example, Figure 6.2, illustrates the specification of gate bias and gate trigger pulse for a typical circuit:

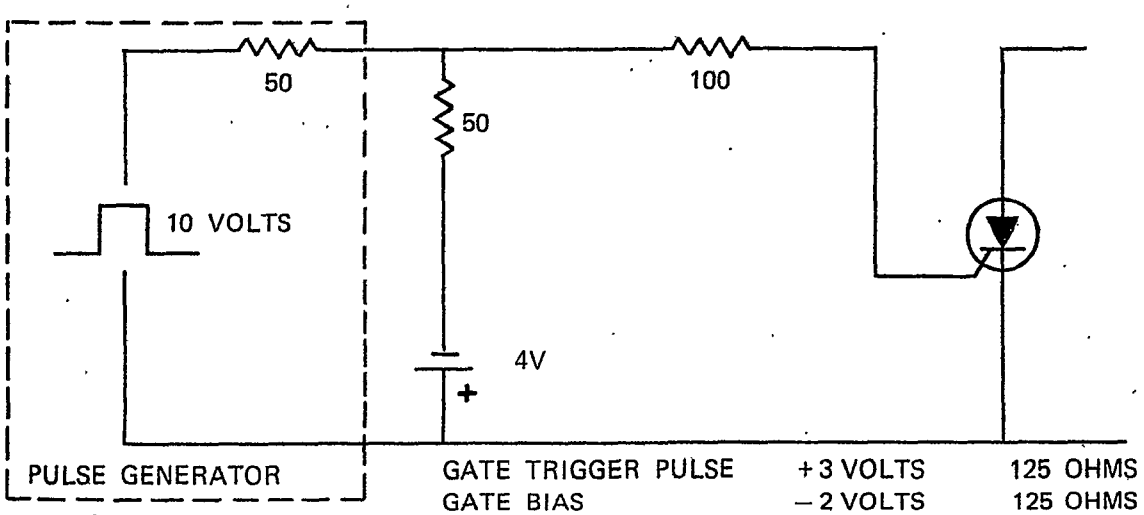


FIGURE 6.2 – EXAMPLE OF GATE BIAS CIRCUIT

6.3 TYPES OF TESTS

The types of tests which may be performed on thyristors are specified to provide a standard of reference between the manufacturer and user. Some of the tests are useful only as inspection tests while others are useful in the extensive evaluation of device characteristics.

The listing of these tests does not imply that any specific test, or all of the tests, must be performed by either the manufacturer or the user. It is the responsibility of the user and manufacturer to agree upon any series of specific tests or test conditions, and the further responsibility of the user to establish the relationship between these tests and the performance of the thyristor in a particular application.

In the test methods given below, the test device is a reverse blocking triode thyristor (SCR). These testing methods in general will also be bi-directional triode thyristors for either operational quadrant when proper gate signal and principal voltage polarities are observed. These test methods will also apply for diode thyristors if gate triggering and biasing conditions are deleted and replaced by applicable voltage triggering specifications.

6.3.1 Direct-Current Tests (Static)

Reverse and off-state characteristic tests are made by applying a direct voltage to a thyristor while in a blocking state and measuring the current which flows. Characteristic tests in the on-state are made by passing a given value of direct conduction current through a thyristor and measuring the on-state voltage. For recommended values of tests voltages and currents, the manufacturer of the particular thyristor should be consulted. Unless otherwise specified, direct current measurements are taken after thermal equilibrium is reached because of the temperature sensitivity of characteristics.

In testing thyristors, the source of direct current for on-state voltage testing is not considered important providing the ripple is less than 5%. In testing the reverse, off-state, and gate trigger characteristics of thyristors, ripple of the voltage source should not exceed 1% and particular care must be taken to prevent voltage transients from exceeding the thyristor voltage rating. Measuring thyristor characteristics may require the use of an attached heat dissipator. Heat dissipator recommendations of the manufacturer should be followed.

6.3.1.1 Test Circuits and Procedures

6.3.1.1.1 DC Breakover Voltage ($V_{(BO)}$)

6.3.1.1.1.1 Test Description

The manufacturers literature must be consulted before this test is performed because a particular thyristor type can have a peak off-state voltage limit which could restrict the applied test voltage to less than the breakover voltage of the device. The test is performed by slowly increasing the supply voltage until the device switches from the off-state to the on-state. The highest dc voltage thus achieved across the device is

called the dc breakover voltage. Breakover voltage is quite temperature dependent and for certain device types quite sensitive to gate bias. If testing is done at elevated temperature, the device must be mounted on a heat dissipator sufficient size to prevent thermal runaway.

6.3.1.1.1.2 Test Circuit

The test circuit is shown in Figure 6.3. The resistance R is used to limit device current to a very low value when switching to the on-state occurs. The dc breakdown voltage is read on dc voltmeter V.

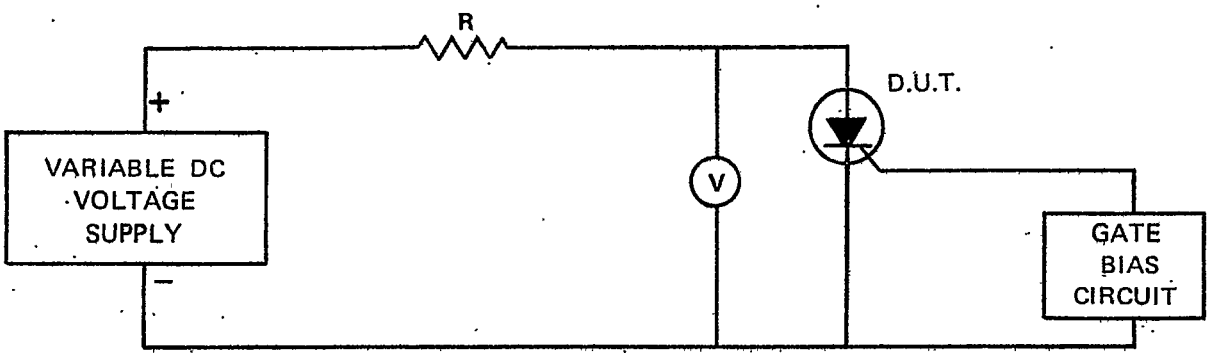


FIGURE 6.3 – DC BREAKOVER VOLTAGE TEST CIRCUIT

6.3.1.1.1.3 Test Conditions to be Specified

a. Case Temperature = _____°C

b. Gate Bias Conditions

1. Source Voltage = ± _____ V and
Source Resistance = _____ Ohms

2. Or Gate Bias Resistance = _____Ohms

c. Thermal Resistance of Minimum Heat Dissipator Upon Which Test Device Is Mounted _____°C/W.

6.3.1.1.1.4 Characteristics to be Measured

DC Breakover Voltage $V_{(BO)}$ = _____ Volts

6.3.1.1.2 DC Reverse Breakdown Voltage ($V_{(BR)R}$)

6.3.1.1.2.1 Test Description

The manufacturers' literature must be consulted before the test is performed because a particular thyristor type can have a peak reverse voltage limit which could restrict the applied test voltage to less than the reverse breakdown voltage of the device. The test is performed by slowly increasing the supply voltage until the device changes from the reverse blocking state to a low resistance state and reaches a specified reverse test current level. The resulting voltage across the device is the dc reverse breakdown voltage. This voltage is quite temperature dependent and for certain device types may be sensitive to gate bias. If testing is done at elevated temperature, the device must be mounted on a heat dissipator of sufficient size to prevent thermal runaway.

6.3.1.1.2.2 Test Circuit

The test circuit is shown in Figure 6.4. The resistance R is for current limiting purposes. The specified dc reverse current is read on dc milliammeter I and the dc breakdown voltage is read on dc voltmeter V. The milliammeter drop should be taken into account when measuring the breakdown voltage of the test device.

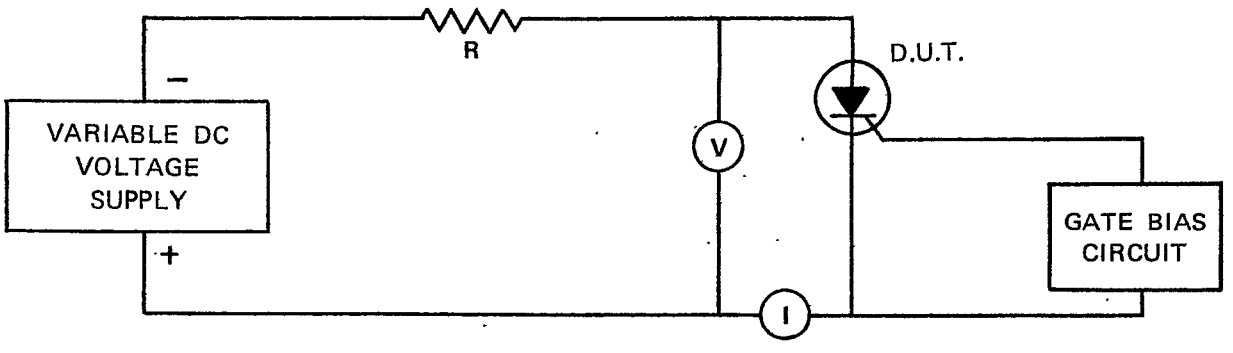


FIGURE 6.4 – DC REVERSE BREAKDOWN VOLTAGE TEST CIRCUIT

6.3.1.1.2.3 Test Conditions To Be Specified

a. Case Temperature = _____°C

b. Gate Bias Conditions

1. Source Voltage = ± _____ V and
Source Resistance = _____ Ohms

2. Or Gate Bias Resistance = _____ Ohms

c. DC Reverse Test Current = _____ mA

d. Thermal Resistance of Minimum Heat Dissipator Upon Which Test Device Is Mounted = _____°C/W

6.3.1.1.2.4 Characteristic To Be Measured

DC Reverse Breakdown Voltage $V_{(BR)R}$ = _____V.

6.3.1.1.3 DC Reverse Blocking Current (I_R)

6.3.1.1.3.1 Test Description

Specified reverse voltage is applied to the test device and the resulting current flow through the test device is measured. Reverse blocking current is quite temperature sensitive and for certain device types is also sensitive to gate bias. If testing is done at elevated temperature, the device must be mounted on a heat dissipator of sufficient size to prevent thermal runaway.

6.3.1.1.3.2 Test Circuit

The test circuit is shown in Figure 6.4 which is the same one as is used for the dc reverse breakdown voltage test. The test voltage is read on dc voltmeter V and the resulting reverse blocking current on dc milliammeter I.

6.3.1.1.3.3 Test Conditions To Be Specified

a. Case Temperature = _____°C

b. Gate Bias Conditions

1. Source Voltage = ± _____ V and
Source Resistance = _____ Ohms

2. Or Gate Bias Resistance = _____ Ohms

c. DC Reverse Test Voltage (V_R) = _____ V

d. Thermal Resistance of Minimum Heat Dissipator Upon Which Test Device Is Mounted = _____ °C/W

6.3.1.1.3.4 Characteristic To Be Measured

DC Reverse Blocking Current (I_R) = _____ mA

6.3.1.1.4 DC Off-State Current (I_D)

6.3.1.1.4.1 Test Description

Specified off-state voltage is applied to the test device and the resulting current flow through the test device is measured. Off-state current is quite temperature sensitive and for certain device types is also sensitive to gate bias. If testing is done at elevated temperature, the device must be mounted on a heat dissipator of sufficient size to prevent thermal runaway.

6.3.1.1.4.2 Test Circuit

The test circuit is shown in Figure 6.4 except that the polarity of the source voltage and meters must be reversed. With this exception, this is the same test circuit that is used for measuring dc reverse breakdown voltage and reverse blocking current. The test voltage is read on dc voltmeter V and the resulting off-state current on dc milliammeter I.

6.3.1.1.4.3 Test Conditions To Be Specified

a. Case Temperature = _____ °C

b. Gate Bias Conditions

1. Source Voltage = ± _____ V and
Source Resistance = _____ Ohms

2. Or Gate Bias Resistance = _____ Ohms

c. DC Off-State Test Voltage (V_D) = _____ Ohms

d. Thermal Resistance of Minimum Heat Dissipator Upon Which Test Device Is Mounted = _____ °C/W

6.3.1.1.4.4 Characteristic To Be Measured

DC Off-State Current (I_D) = _____ mA

6.3.1.1.5 DC On-State Voltage (V_T)

6.3.1.1.5.1 Test Description

Specified on-state current is made to flow through the test device and the resulting voltage across the test device is measured. The on-state voltage is somewhat temperature sensitive and so test device thermal equilibrium should be achieved before the measurement is made. The manner in which the test device is triggered into the on-state is unimportant as long as the test current is near rated value. The test device may be triggered by connecting the gate terminal through a suitable resistor to the supply voltage or by use of a conventional gate triggering source. The gate triggering signal, whatever it may be, is removed prior to measuring the on-state voltage.

6.3.1.1.5.2 Test Circuit

The test circuit is shown in Figure 6.5. Closing SW momentarily switches the test device to the on-state. The test current is adjusted to specified value by adjusting the supply voltage magnitude and/or the resistance R. The test current is read by means of ammeter I and the on-voltage is measured by means of dc voltmeter V. The voltmeter connections are made at specified points on the test device and always within the current connection points.

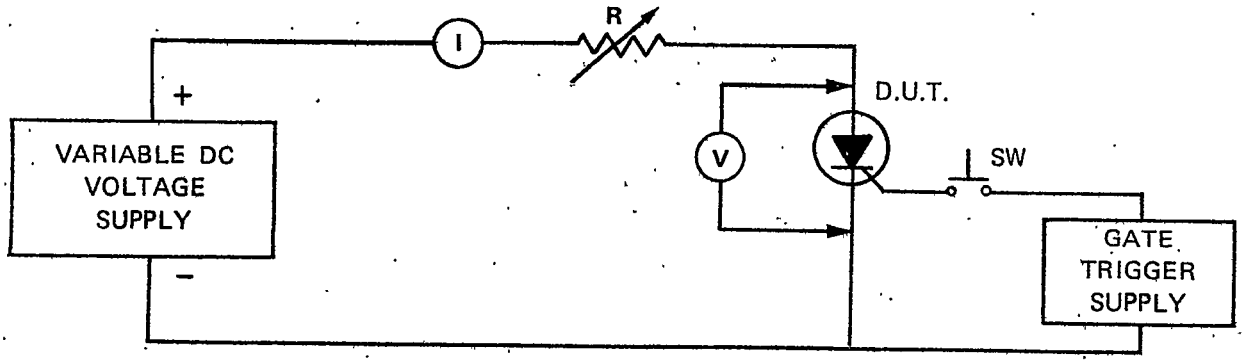


FIGURE 6.5 – DC ON-STATE VOLTAGE TEST CIRCUIT

6.3.1.1.5.3 Test Conditions To Be Specified

a. Case Temperature = _____°C

b. Location of voltage measuring probes

c. DC On-State Test Current (I_T) = _____ A

6.3.1.1.5.4 Characteristic To Be Measured

DC On-State Voltage (V_T) = _____ V

6.3.1.1.6 Latching Current (i_L)

6.3.1.1.6.1 Test Description

This test is used to determine the minimum on-state current which will maintain the device in the on-state subsequent to triggering from the off-state to the on-state. It is performed by applying a specified gate pulse at a low repetition rate and then decreasing the circuit resistance until the on-state current will remain flowing following the removal of the triggering signal. Test temperature, gate trigger signal, and gate bias between trigger pulses all affect the latching current level and therefore all three must be specified. The circuit L/R should be essentially zero if ammeter is to read correct i_L at the cessation of the gate trigger pulse.

6.3.1.1.6.2 Test Circuit

The test circuit is shown in Fig. 6.6. The dc source voltage is fixed and the resistance R is used to adjust the on-state current. The latching current (minimum on-state current) is read on milliammeter I. The gate trigger pulse width should be long compared with the rise time of the on-state current. If the gate trigger signal is $\geqslant 100\ \mu s$ in duration, the measured value of latching current will be the same as in the case where the gate trigger signal is applied continuously.

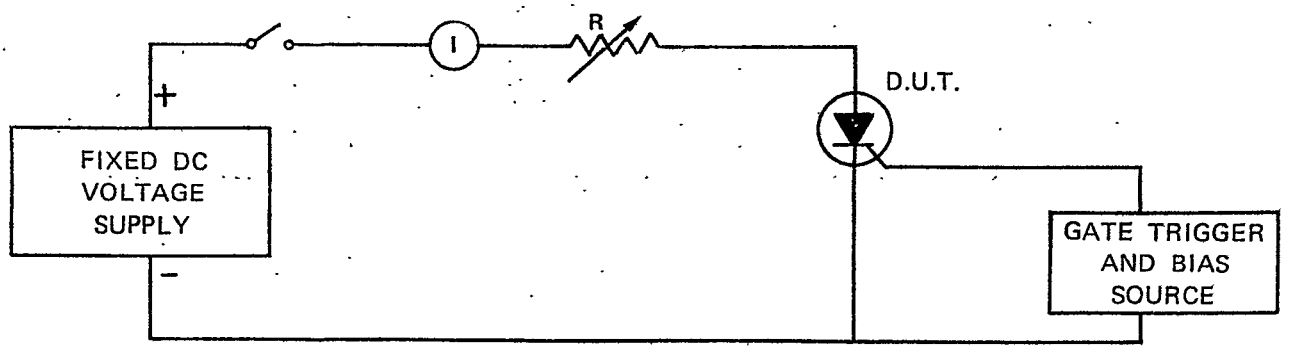


FIGURE 6.6 – LATCHING AND HOLDING CURRENT TEST CIRCUIT

6.3.1.1.6.3 Test Conditions To Be Specified

a. Case Temperature = _____°C

b. DC Source Voltage = _____V
(Test Device Off-State Voltage)

c. Gate Trigger Pulse (See 6.2.4)

1. Source Voltage = _____ V and
   Source Resistance = _____ Ohms

2. Rise Time = _____ μs

3. Width = _____ μs

4. Fall Time = _____ μs

5. Repetition Rate = _____ pps

d. Gate Bias Conditions (See 6.2.4)

Source Voltage = ± _____ V and Source
Resistance = _____ Ohms

6.3.1.1.6.4 Characteristic To Be Measured

Latching Current (i_L) = _____ mA

6.3.1.1.7 DC Holding Current (I_H)

6.3.1.1.7.1 Test Description

This test is used to determine the minimum on-state current that will sustain device current conduction following operation at normal conduction (on-state) current levels. It is performed by turning the device on and establishing a specified on-state current for an instant and then reducing the current until the device switches from the on-state to the off-state. The lowest on-state current thus attained is the holding current. The initial on-state current level should be high enough to insure that the device is fully turned-on and of short enough duration to insure that self heating is negligible. A fixed dc supply voltage is used and the test current is controlled by a variable series resistance. The temperature of the test device and the gate bias conditions affect the holding current and therefore must be specified. The gate trigger signal used to turn the test device on initially can be of any sufficient magnitude to turn the device on and must be removed before the actual measurement of holding current is made.

6.3.1.1.7.2 Test Circuit

The test circuit is shown in Figure 6.6. The resistance R is adjusted to achieve the initial on-state current level subsequent to triggering and then

is readjusted to reduce the test current and make the holding current measurement. The holding current is measured on the milliammeter I.

6.3.1.1.7.3 Test Conditions To Be Specified

a. Case Temperature = _____°C

b. DC Source Voltage = _____V

c. Peak initial on-state current = _____ mA

d. Gate Bias Conditions

1. Source Voltage = ± _____V and
Source Resistance = _____ Ohms

2. Or Gate Bias Resistance = _____Ohms

6.3.1.1.7.4 Characteristic To Be Measured

DC Holding Current (I_H) = _____mA

6.3.1.1.8 DC Gate Trigger Current and Voltage Test (I_{GT}), (V_{GT})

6.3.1.1.8.1 Test Description

This test is used to measure the magnitude of the dc gate current and voltage signals required to trigger a triode thyristor from the off-state to the on-state. The gate current actually performs the triggering function and the gate trigger voltage represents the drive required to achieve the triggering current. The test is performed by first establishing the load circuit conditions and then increasing the dc voltage applied to the gate until the test device triggers. The gate trigger current and voltage are the maximum values achieved prior to triggering. The magnitude of the gate trigger current and voltage is dependent upon temperature, load circuit conditions and for some device types the gate resistance bias looking back into the gate trigger circuit from the test device gate to reference terminals. Sufficient resistance in series with the gate voltage supply is required to insure that the test device (particularly low current devices) will not turn back off subsequent to triggering because of a gate impedance increase at the instant of turn-on.

6.3.1.1.8.2 Test Circuit

The test circuit is shown in Fig. 6.7. The gate supply voltage should contain < 1% ripple. Resistance R is used to limit the on-state current to low value subsequent to triggering. The measured gate trigger voltage

should be corrected for the voltage drop across the milliammeter I. The dc gate trigger voltage is read on dc voltmeter V_1 and the dc gate trigger current is read on milliammeter I. DC voltmeter V_2 may be used to detect the triggering of the test device.

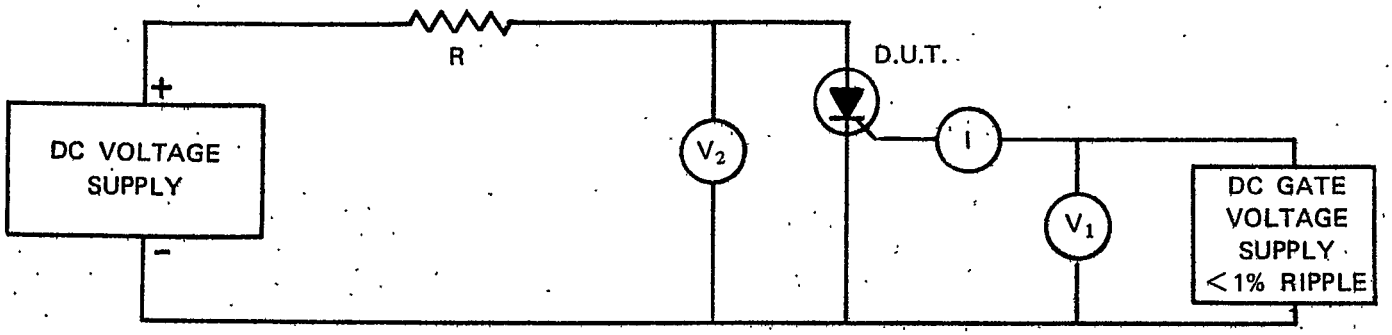


FIGURE 6.7 – DC GATE TRIGGER CURRENT AND VOLTAGE TEST CIRCUIT

6.3.1.1.8.3 Test Conditions To Be Specified

a. Case Temperature = _____ °C.

b. DC Supply Voltage = _____ V

c. Load Resistance (R) = _____ Ohms

d. Gate Bias Resistance = _____ Ohms

6.3.1.1.8.4 Characteristics To Be Measured

DC Gate Trigger Current (I_{GT}) = _____ mA

DC Gate Trigger Voltage (V_{GT}) = _____ V

6.3.1.1.9 DC Gate Non-Trigger Current and Voltage Test (I_{GD}), (V_{GD})

6.3.1.1.9.1 Test Description

The test is identical to the dc gate trigger current and voltage test (6.3.1.1.8) except the characteristics measured are the gate trigger current and voltage magnitudes immediately prior to the switching of the test device. The purpose of this test is to determine the magnitude of unwanted gate signals that can be tolerated before spurious triggering occurs.

6.3.1.1.9.2 Test Circuit

Same as that given in Figure 6.7

6.3.1.1.9.3 Test Conditions To Be Specified

Same as those given in 6.3.1.1.8.3.

6.3.1.1.9.4 Characteristics To Be Measured

DC Gate Non-Trigger Current (I_{GD}) = _____ mA

DC Gate Non-Trigger Voltage (V_{GD}) = _____ V

6.3.1.1.10 DC Negative Gate Current (I_G)

6.3.1.1.10.1 Test Description

This test is applicable to reverse blocking triode thyristors only. The purpose of the test is to measure the negative (blocking) current resulting when a negative gate to cathode voltage is applied to the test device. The anode terminal of the test device is open circuited.

6.3.1.1.10.2 Test Circuit

The test circuit is shown in Figure 6.8. The specified dc voltage applied to the test device may be read on dc voltmeter V. The dc negative gate current is read on milliammeter I. The resistance R limits current in the event of test device breakdown. The ripple of the dc supply voltage should be < 1%. The measured applied voltage to the test device should be corrected for the voltage drop across the milliammeter.

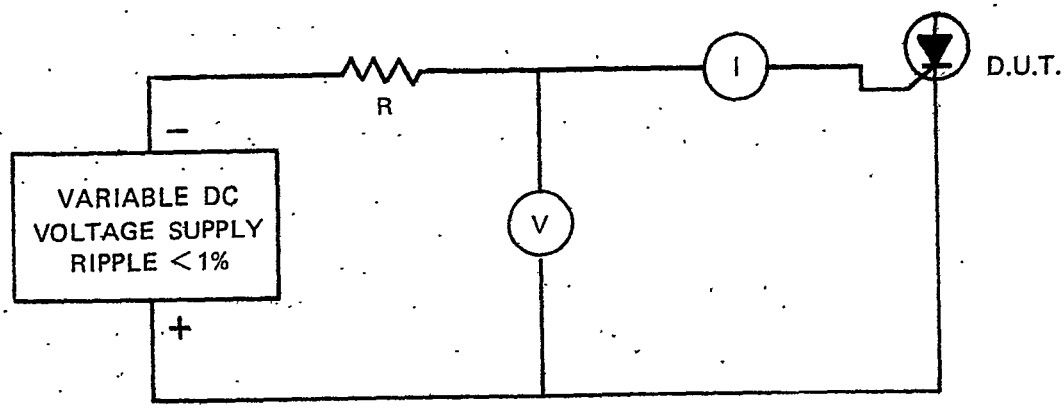


FIGURE 6.8 – DC NEGATIVE GATE CURRENT TEST CIRCUIT

6.3.1.1.10.3 Test Conditions To Be Specified

a. Case Temperature = _____°C

b. DC Negative Gate Voltage = _____V

6.3.1.1.10.4 Characteristic To Be Measured

DC Negative Gate Current (I_G) = _____mA

6.3.2 Alternating Current Tests (Dynamic)

These tests are performed with the semiconductor thyristor connected in the appropriate test circuit and energized with 60 Hz alternating current. For recommended values of test voltage and current, the manufacturer of the particular thyristor should be consulted. Unless otherwise specified, alternating current measurements should be taken after thermal equilibrium is reached.

6.3.2.1 Test Circuits and Procedures

6.3.2.1.1 Peak AC Reverse Blocking Current (I_{RM})

6.3.2.1.1.1 Test Description

Specified peak reverse voltage is applied to the test device and the resulting peak current flow through the device is measured. Reverse blocking current is quite temperature sensitive and for certain device types is also sensitive to gate bias. If testing is done at elevated temperature, the device must be mounted on a heat dissipator of sufficient size to prevent thermal runaway.

6.3.2.1.1.2 Test Circuit

The test circuit is shown in Figure 6.9. The test voltage is of half sine

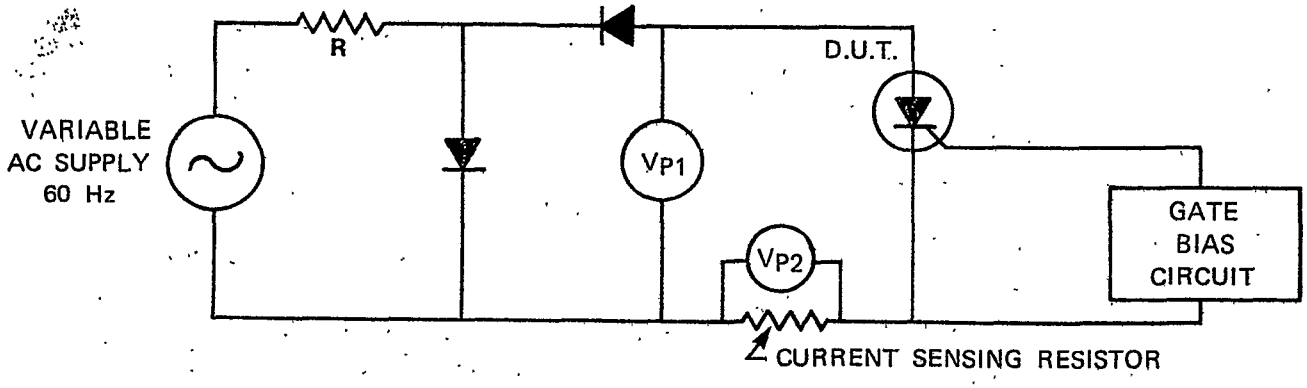


FIGURE 6.9 – AC REVERSE BLOCKING CURRENT TEST CIRCUIT

wave, 60 Hz, waveform and its peak value is read on peak reading voltmeter V_{P1}. The peak reverse blocking current may be measured by means of a current sensing resistor with a peak reading voltmeter V_{P2} connected across it. Resistance R is used to limit the current through the test device in the event of breakdown.

6.3.2.1.1.3 Test Conditions To Be Specified

a. Case Temperature = _____ °C

b. Gate Bias Conditions

1. Source Voltage = ± _____ V and
   Source Resistance = _____ Ohms

2. Or Gate Bias Resistance = _____ Ohms

c. Peak AC Reverse Test Voltage (V_{RM}) = _____ V

d. Thermal Resistance of Minimum Heat Dissipator
Upon Which Test Device Is Mounted = _____ °C/W

6.3.2.1.1.4 Characteristic To Be Measured

Peak AC Reverse Blocking Current (I_{RM}) = _____ mA

6.3.2.1.2 Peak AC Off-State Current (I_{DM})

6.3.2.1.2.1 Test Description

Specified peak off-state voltage is applied to the test device and the resulting peak current flow through the device is measured. Off-state current is quite temperature sensitive and for certain device types is also sensitive to gate bias. If testing is done at elevated temperature, the device must be mounted on a heat dissipator of sufficient size to prevent thermal runaway.

6.3.2.1.2.2 Test Circuit

The test circuit is shown in Figure 6.10. The test voltage is of half sine wave, 60 Hz, waveform and its peak value is read on peak reading voltmeter V_{P1}. The peak off-state current may be measured by means of a current sensing resistor with a peak reading voltmeter, V_{P2}, connected across it. Resistance R is used to limit the current to a very low value through the test device in the event of breakover.

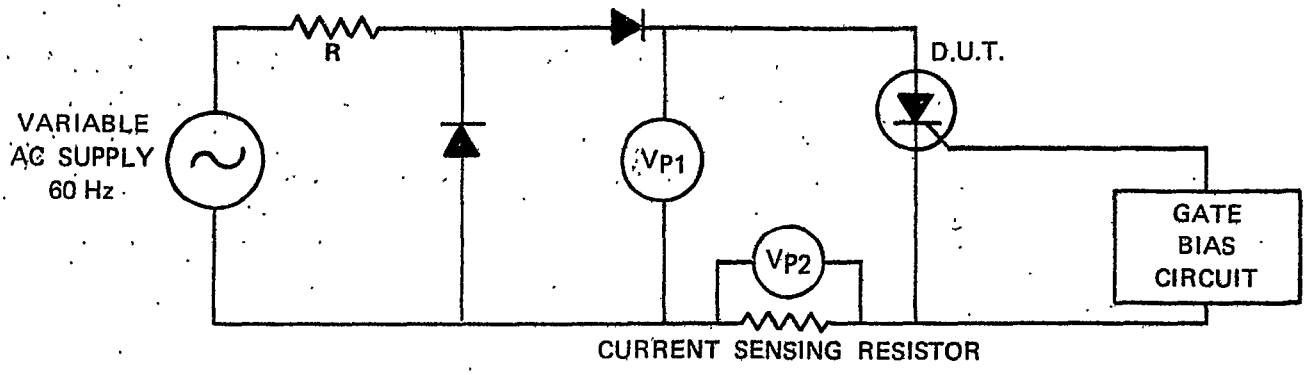


FIGURE 6.10 – AC OFF-STATE CURRENT TEST CIRCUIT

6.3.2.1.2.3 Test Conditions To Be Specified

a. Case Temperature = _____ °C

b. Gate Bias Conditions

1. Source Voltage = ± _____ V and
   Source Resistance = _____ Ohms

2. Or Gate Bias Resistance = _____ Ohms

c. Peak AC Off-State Test Voltage (V_{DM}) = _____ V

d. Thermal Resistance of Minimum Heat Dissipator
Upon Which Test Device is Mounted = _____ °C/W

6.3.2.1.2.4 Characteristic To Be Measured

Peak AC Off-State Current (I_{DM}) = _____ mA

6.3.2.1.3 Peak AC On-State Voltage (V_{TM})

6.3.2.1.3.1 Test Description

A specified average on-state current of half sine, 60 Hz, waveform is passed through the test device and the resulting peak on-state voltage across the test device is measured. The manner in which the test device is triggered into the on-state is unimportant as long as approximately 180 degree conduction is achieved and the gate signal has been removed by the time the test current reaches peak value. Test device thermal equilibrium should be achieved before the voltage measurement is made.

6.3.2.1.3.2 Test Circuit

The test circuit is shown in Figure 6.11. The ac supply voltage and resistance R determines the test current magnitude. The supply voltage should be of sufficient magnitude to insure a test current conduction angle of not less than 175 degrees. The on-state voltage is read on peak reading voltmeter V_P. The average test current is read on dc ammeter I_O. The voltmeter, V_P, connections are made at specified points on the test device and always within the current connection points.

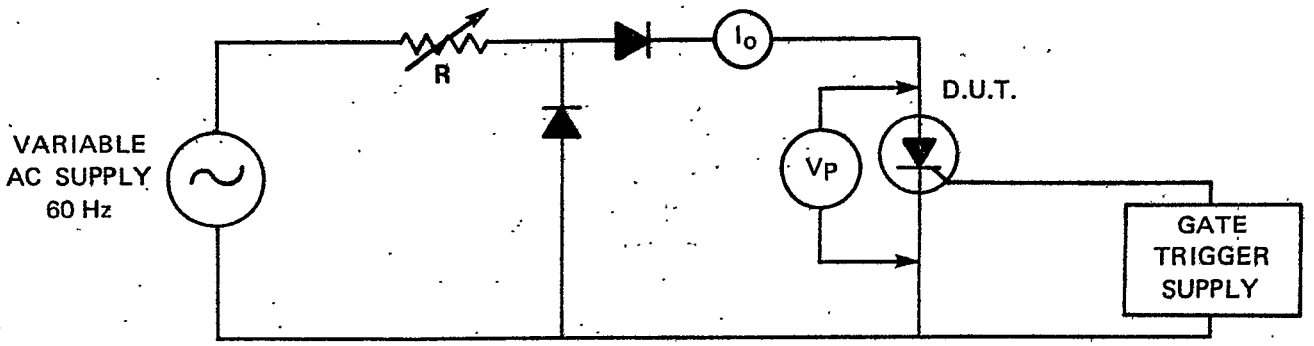


FIGURE 6.11 – AC ON-STATE VOLTAGE TEST CIRCUIT

6.3.2.1.3.3 Test Conditions To Be Specified

a. Case Temperature = _____ °C

b. Location of Voltage Measuring Probes

c. Average On-State Test Current ($I_{T(AV)}$) = _____ A

6.3.2.1.3.4 Characteristic To Be Measured

Peak On-State Voltage (V_{TM}) = _____ V

6.3.3 Instantaneous or Pulse Tests

Pulse tests are normally used for measuring isothermal instantaneous voltampere characteristics of thyristors for one or more of the following purposes:

Obtain characteristics under conditions of negligible internal heating:

Measure characteristics at current levels that would damage the thyristor if maintained continuously.

6.3.3.1 Peak On-State Voltage (V_{TM})

This test provides a method of measuring peak on-state voltage at high current levels without heat sinking. Test currents can be obtained by applying a single half cycle from a 60 Hz source to the thyristor through a suitable switching device or by using a square wave pulse generator. One alternate method of generating a half-sine wave of current consists of discharging a capacitor through a series inductor using a suitable switching device. The latter method permits narrower test pulses with less heating and better control of amplitude. Suitable indicating devices for measuring current and voltage values are oscilloscopes, oscillographs, and peak reading voltmeters. The pulses may be applied singly or repetitively, providing the repetition rate is low enough to limit device heating to a negligible value. The leading edge di/dt of the test current pulse should be less than the repetitive di/dt rating of the test device in order to eliminate any possibility of device damage or unpredictable device heating.

6.3.3.1.1 Test Circuit

A circuit used for this test is shown in Figure 6.12. The pulse generator output voltage is adjusted in conjunction with

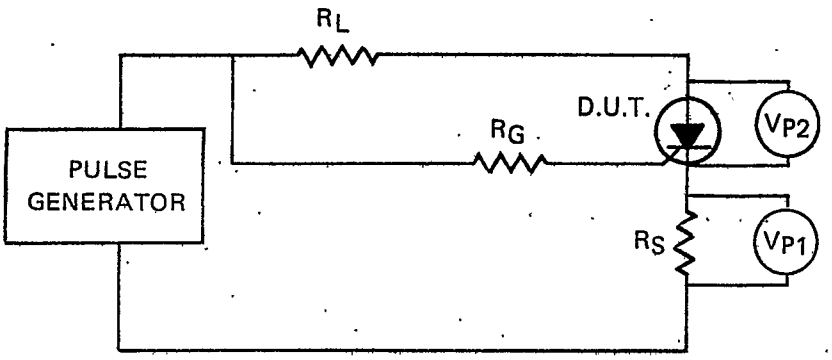


FIGURE 6.12 – PEAK ON-STATE VOLTAGE TEST CIRCUIT

R_L to obtain the specified value of peak on-state current. R_g serves to provide gate current to turn the thyristor on. An independent gate trigger source may be used if desired. The on-state current is determined by the peak voltage drop, as read on peak reading voltmeter V_{P1}, across the current sensing resistor R_S. The peak on-state voltage is read on peak reading voltmeter V_{P2} which is triggered on after the test current starts to increase.

Generation of a high current pulse by the discharge of a capacitor through an inductor is accomplished with the circuit shown in Figure 6.13. After the thyristor switch is turned on an instant following turn-on of the test thyristor, the L-C circuit causes a high current pulse to flow through the test thyristor, then attempts to reverse its flow. The reverse bias causes both thyristors to turn-off. The dc

power supply is adjusted to regulate the on-state current amplitude. L and C determine the pulse width. The pulse width must be wide enough to insure that the device is fully on at the time the peak current is reached. Typical waveshapes are shown in Figure 6.14.

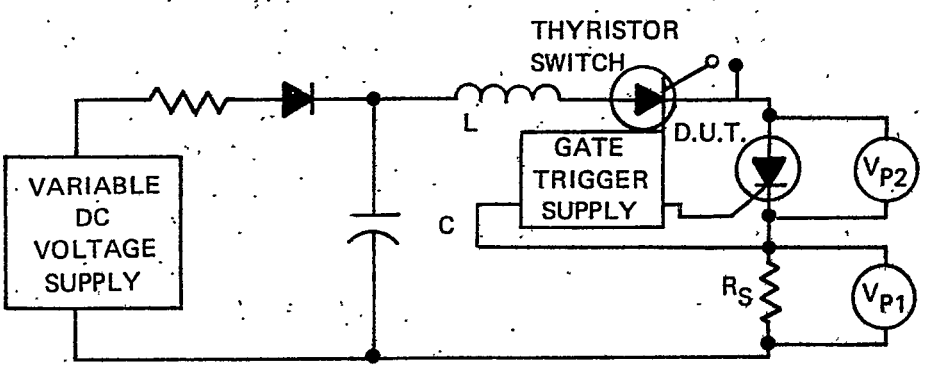


FIGURE 6.13 – PEAK ON-STATE VOLTAGE TEST CIRCUIT

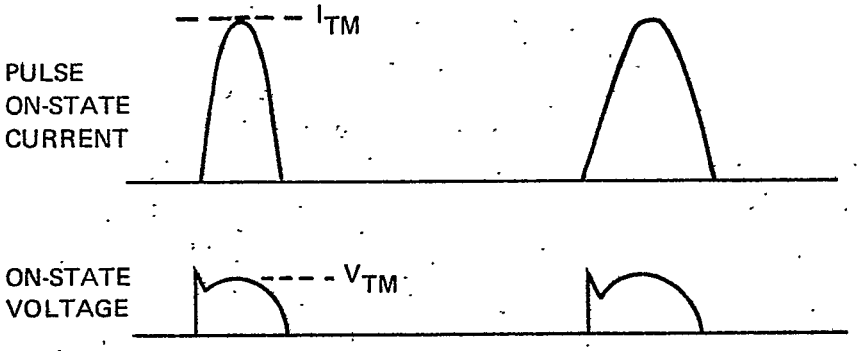


FIGURE 6.14 – PULSE CURRENT AND VOLTAGE WAVEFORMS

6.3.3.1.2 Test Conditions to be Specified

A. On-State Current Magnitude (I_{TM}) _____ A

B. On-State Current Pulse Width _____ μs

C. Case Temperature _____ °C

6.3.3.1.3 Characteristic to be measured

A. Peak On-State Voltage (V_{TM}) _____ V

6.3.4 Switching Time Tests

6.3.4.1 Gate-Controlled Turn-On Time (t_{gt})

6.3.4.1.1 Test Description

This test method applies to all triode thyristors and for either polarity of applied voltage in the case of bidirectional devices.

The delay and rise times of anode current during the turn on of a triode thyristor are affected by gate trigger pulse variations and anode circuit inductance. This test method establishes a test circuit and provision for specification of critical test conditions.

6.3.4.1.2 Test Circuits

The circuit used for the test is shown in Figure 6.15. The capacitor C_1 is charged on one-half cycle of the 60 Hz supply voltage through T_1, D_1, R_1 and R_2. On the next half cycle, the gate trigger pulse is delivered to the device under test which causes it to turn on, discharging C_1 through R_2. The gate trigger pulse generator must be synchronized so that the gate trigger pulse is applied while the charging supply is negative.

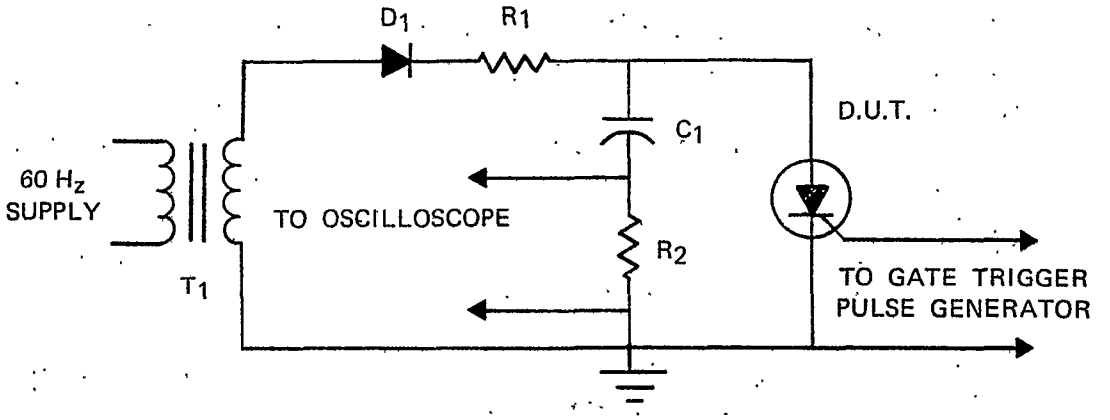


FIGURE 6.15 – TEST CIRCUIT FOR TURN-ON TIME

The delay and rise times can be observed by means of an oscilloscope connected across R_2. The delay time is the interval between the 10% point on the leading edge of the gate trigger pulse and the time when the resulting on-state current reaches 10% of its maximum value. The rise time is the time interval during which the on-state current increases from 10% to 90% of its maximum value. An alternate method to observe delay and rise time is to observe the voltage across the test thyristor using an oscilloscope. This is illustrated in the waveforms shown in Figure 6.16.

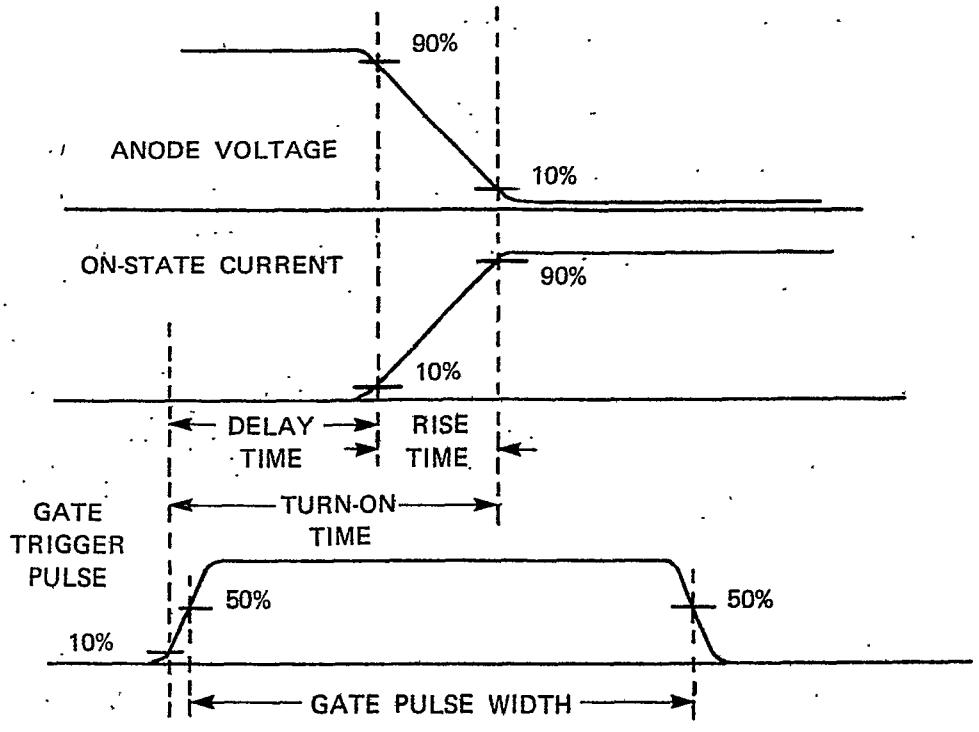


FIGURE 6.16 – TURN-ON TIME WAVEFORMS

The following criterion should be used in selecting the component values in the test circuit:

A. The rise time of the gate trigger pulse should not exceed 10% of the specified delay time.

B. The product of R_2 and C_1 should be equal to or greater than ten times the specified rise time but less than 25-30 times to minimize self heating.

C. When on-state current waveform is observed the inductance of the capacitor discharge loop including all its components should be equal to or less than 0.1 times the product of R_2 and the specified rise time.

D. R_1 is a surge limiting resistor to protect D_1.

6.3.4.1.3 Test Conditions To Be Specified

A. Gate Trigger Pulse (See 6.2.4) _____ V _____ ohms

B. Gate Bias (See 6.2.4) _____ V _____ ohms

C. Gate Pulse Width _____ μs

D. Case Temperature _____ °C

E. Off-State Voltage _____ V

F. On-State Current Magnitude _____ A

G. On-State Current di/dt (10-90%)
if using D.U.T. voltage to measure rise time _____ A/μs

H. Specify whether on-current or D.U.T. voltage is to be observed when measuring delay and rise time.

6.3.4.1.4 Characteristics To Be Measured (See Note)

	Maximum
A. Delay Time (t_d)	_____ μs
B. Rise Time (t_r)	_____ μs

Note – Turn on time (t_{gt}) may be specified as a time equal to or less than the sum of the delay and rise times.

6.3.4.2 Circuit-Commutated Turn-Off Time Test Method For Reverse Blocking Thyristors (t_q)

6.3.4.2.1 Test Description

This test is performed by first causing the thyristor under test to conduct the specified on-state current at the specified thermal condition. This current is conducted for the specified time (a period long enough to establish carrier equilibrium). Next, the current is reversed through the thyristor at the specified rate (di/dt) by means of an externally applied reverse blocking voltage. The reverse current recovers stored charge from the anode and cathode junctions of the thyristor, allowing the thyristor to support the specified reverse blocking voltage. A further waiting time is required for the collector junction charges to re-combine before the thyristor is capable of blocking forward voltage. Since this re-combination cannot be observed directly, the test is performed by applying an off-state voltage at the specified rate of rise (dv/dt) after successively shorter waiting times until it is observed that the thyristor is unable to support the off-state voltage (without switching to the on-state). The thyristor current and voltage waveforms are illustrated in Figure 6.17.

6.3.4.2.2 Test Circuits

A. The simplified circuit diagram in Figure 6.18 illustrates the operating principles of a circuit used to generate the waveforms illustrated in Figure 6.17. The circuit diagram utilizes current generators, ideal switches and no provision for repetitive test cycles for purposes of clarity.

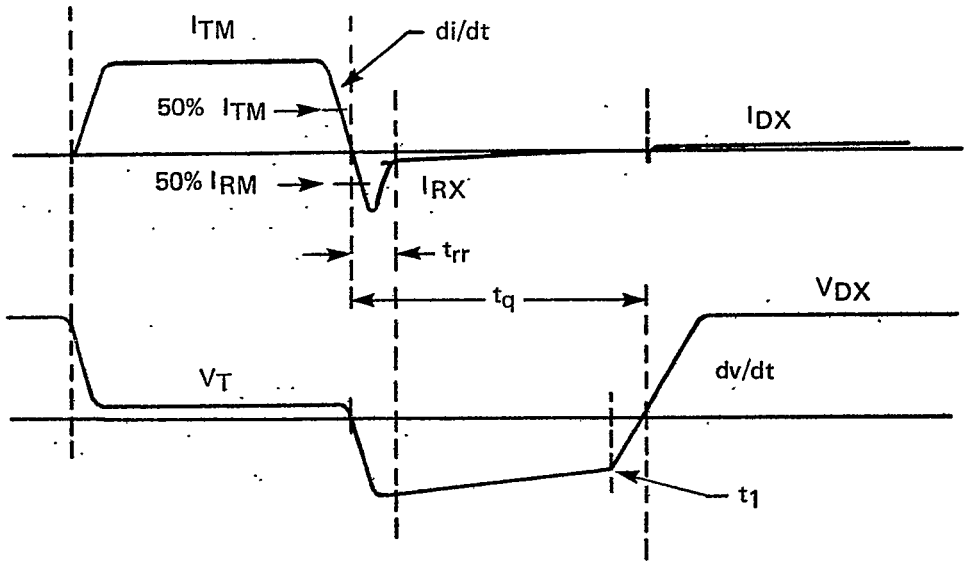


FIGURE 6.17 – THYRISTOR CURRENT AND VOLTAGE WAVEFORMS DURING CIRCUIT-COMMUTATED TURN-OFF

The operation of the circuit of Figure 6.18 is as follows:

1. S_2 and S_4 are closed simultaneously causing the thyristor under test to switch to the on-state and conduct the specified current I_T, S_4 is then opened to disconnect the gate trigger supply R_1 and V_3.

2. After the specified conduction time, S_3 is closed to cause current reversal. The rate of current change (di/dt) is determined by V_2, L_1 and R_2. Diode D_2 prevents a commutation voltage transient when the thyristor under test begins to recover its reverse blocking capability. Diode D_1 must have a longer reverse recovery time than the thyristor under test so that the reverse blocking voltage appears across the thyristor under test.

3. The application of off-state voltage is initiated by closing S_1. The Current I_1 completes the reverse recovery of D_1 and is then diverted to C_1. C_1 charges linearly with time at a rate equal to I_1/C_1 producing the required dv/dt illustrated in Figure 6.17. This voltage rises to a value equal to V_1 which is adjusted to the specified off-state voltage.

B. The circuit of Figure 6.19 is shown as an example which accomplishes the circuit functions of Figure 6.18 on a repetitive basis. The gate trigger generator is synchronized with the supply frequency to supply trigger pulses on the half cycle following the charging of C_5 and C_2. Trigger pulses are supplied to thyristors a, b and c in that order to accomplish the switching functions of Sw1, Sw2, Sw3 and Sw4 of Figure 6.18.

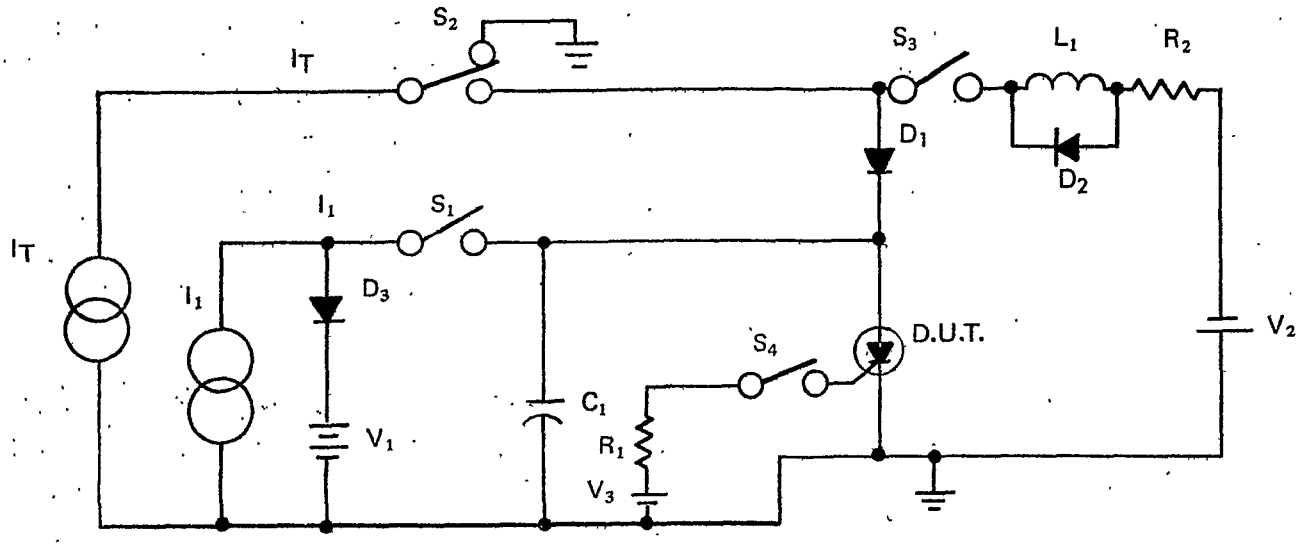


FIGURE 6.18 – SIMPLIFIED TEST CIRCUIT

Current I_T is provided by Capacitor C_5, discharging through R_1. C_2 serves the function of the reverse blocking voltage battery of Figure 6.18. The voltage V_1 is provided by C_4 and the constant current I_1 is provided by L_2. The current through L_2 has a magnitude determined by the voltage on C_3 and resistor R_3. Triggering thyristor c reverses the bias on D_3 causing the current through L_2 to be diverted through thyristor c. The inductance of L_2 should be large enough to maintain a substantially constant current until capacitor C_1 has charged to the voltage of C_4. At this point, D_3 will conduct and prevent further increase of voltage on C_1. D_3 should be a fast recovery diode.

In addition, the following considerations are applicable:

1. The time constant R_1 C_5 must be large enough to maintain essentially constant current during the conducting period. For test currents above 100 amperes, a properly designed lumped constant transmission line and a reduced repetition rate may result in a more practical source of conduction current.

2. As shown, thyristor b does not turn off until the charges on C_2 and C_5 reach equilibrium. This results in considerable power loss in R_1 and R_2. This loss can be considerably reduced by adding additional circuitry for turning off thyristor b following the triggering of thyristor c or by reducing the pulse repetition rate.

3. Resistor R_4 provides a discharge path for capacitor C_1. The current drawn by R_4 must be less than the holding current of thyristor c so that it may turn off after C_1 becomes charged. C_1 should be small or have a resistor connected in series with it to protect the thyristor under test.

4. Effects of distributed capacitance in L_2, reverse recovery of Diodes D_1 and D_3 and wiring inductance may cause undesirable oscillations in the re-applied forward voltage waveform. These effects can be minimized by good design practices including the use of suitable damping resistances.

5. The gate bias and trigger circuit design must recognize that current from the reverse voltage supply will flow through these circuits. For example, a series diode will not adequately decouple the trigger circuit from a parallel connected bias circuit.

6. Good design practice should be used to avoid exceeding ratings of the components selected.

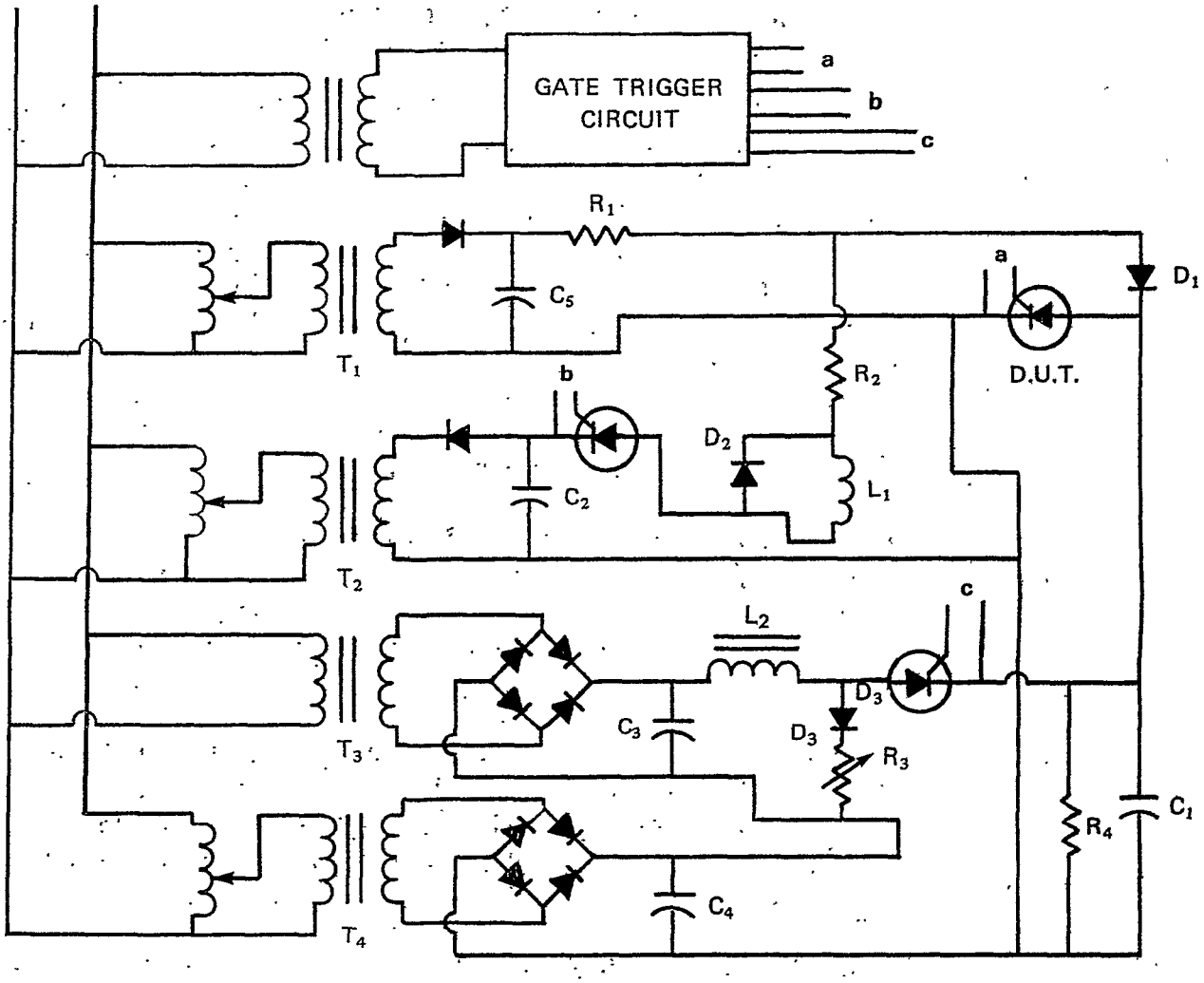


FIGURE 6.19 – PRACTICAL TEST CIRCUIT

6.3.4.2.3 Test Conditions To Be Specified

A. On-state current amplitude (di/dt low enough to assure negligible turn-on heating) _____ A

B. On-state current duration _____ μs

C. Commutation rate (di/dt) (the slope of the line from 50% of + peak to 50% of – peak) _____ A/μs

D. Peak reverse voltage (max.) _____ V

E. Reverse voltage at t_1 (max.) _____ V

F. Operating temperature _____ °C

G. Test repetition rate _____ pps

*H. Rate of rise of re-applied off-state voltage (dv/dt) _____ V/μs

I. Off-state voltage _____ V

J. Gate bias conditions

1. Gate Source Voltage _____ V

2. Gate Source Resistance _____ ohms

*If other than linear ramp waveform is used, specify wave shape.

6.3.4.2.4 Characteristics To Be Measured

A. Turn-off time (t_q) _____ μs

B. Reverse Recovery Time (t_{rr}) (i_{RX} =_____mA) _____ μs

6.3.4.3 Gate-Controlled Turn-Off Time Test Method for Gate Turn-Off Thyristors (t_{gq})

6.3.4.3.1 Test Description

A turn-off thyristor can be switched from the on-state to the off-state with a control signal of appropriate polarity applied to the gate terminal. The delay and fall times of anode current during the turn-off of the thyristor are affected by gate pulse

variations and anode circuit conditions. This test method establishes a test circuit and provision for specification of critical test conditions.

6.3.4.3.2 Test Circuit

The circuit used for the test is shown in Figure 6.20. The thyristor is turned on by the gate pulse delivered by the "on-pulse" generator. On-state current is determined by the off-state supply voltage and the load resistor R_L.

After a predetermined time a specified Gate Turn-Off Current is supplied to the gate terminal by the "off-pulse" generator.

The storage time and fall time may be observed by means of an oscilloscope connected across the current sensing resistor.

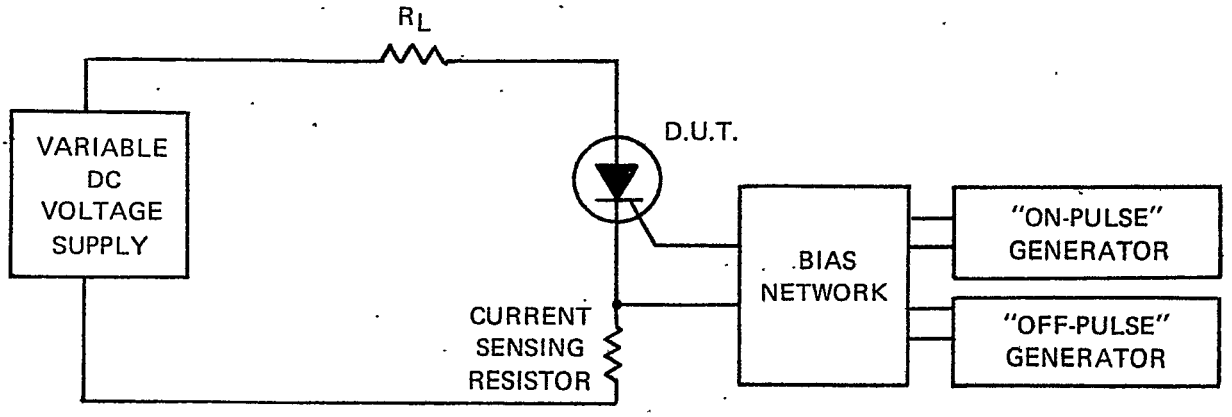


FIGURE 6.20 – GATE TURN-OFF TEST CIRCUIT

Storage time is the time interval between the 10% point on the leading edge of the gate pulse and the 90% point on the on-state current waveform. Fall time is the time interval between the 90% and 10% points on the on-state current waveform. Turn-off time is the sum of storage time and fall time. Typical waveforms are shown in Figure 6.21.

General Notes:

1. Gate current or gate source voltage rise time shall not exceed 10% of the Storage Time interval.

2. Duty cycle should be chosen considering heating effects of switching power losses. Sufficient anode current off time of at least 10 times the pulse width must be allowed to insure that the device under test remains turned off after the turn-off pulse ends.

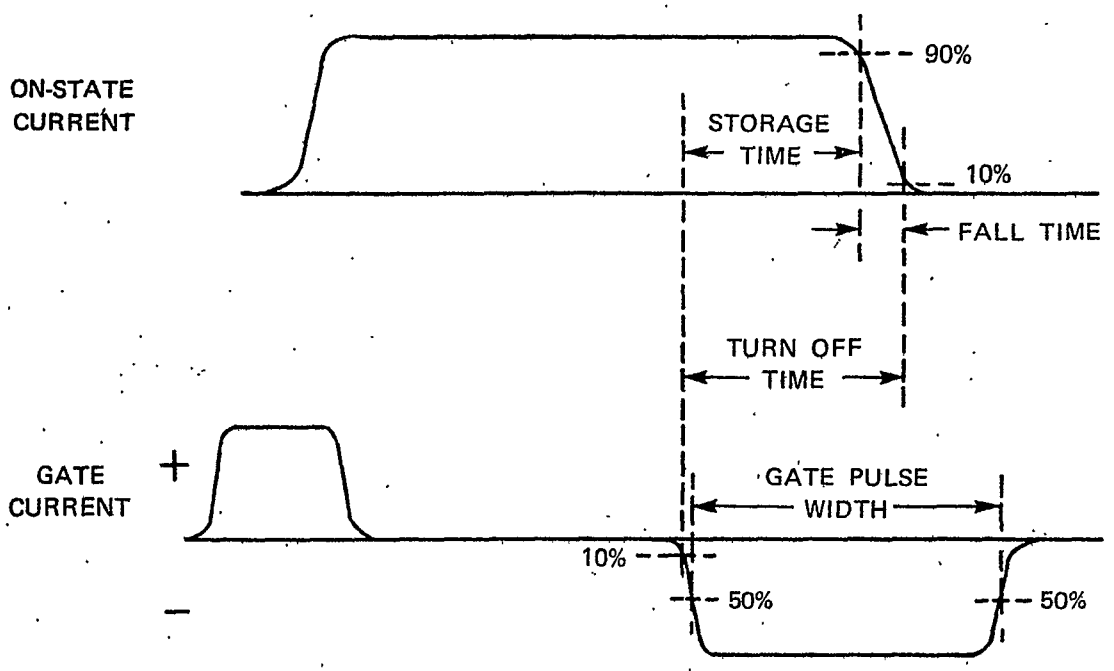


FIGURE 6.21 – TYPICAL GATE TURN-OFF CIRCUIT WAVEFORMS

3. The inductance of the anode circuit should be minimized to prevent anode voltage overshoot on turn-off.

6.3.4.3.3 Test Conditions To Be Specified

1. Off-State Voltage _____ V
2. On-state Current _____ A
3. Switching Repetition Rate _____ pps
4. Duty Cycle (percent on time) _____ %
5. Operating Temperature (case or ambient). _____ °C
6. Bias Network (show circuit)
7. Gate Turn-off Current (peak) _____ mA

or

Gate Source Voltage and _____ V
Gate Source Resistance _____ ohms

6.3.4.3.4 Characteristics To Be Measured

1. Storage Time (t_s) _____ μs

2. Fall time (t_f) _____ μs

3. Gate Pulse Width _____ μs

6.3.4.4 Pulse-Circuit-Commutated Turn-Off Time Test Method for Reverse Blocking Triode Thyristors

6.3.4.4.1 Test Description

This test is similar to the circuit-commutated turn-off test described in 6.3.4.2 except the magnitude and rate of rise of the on-state current is such that considerable localized heating is produced during the switch-on interval. This has an effect on turn-off time which must be defined. The test current and voltage waveforms used in this test are shown in Figure 6.22.

The average power dissipation may be measured in several ways. If the instantaneous device voltage and current is measured for the purpose of obtaining average power by integration of the instantaneous voltage current product, the current sensing resistor should be noninductive and the effect of the device inductance on its instantaneous voltage measurement should be considered. Another average power measurement procedure is to attach the test device to a calibrated thermal resistance which in turn is attached to any suitable heat sink. The test device and the calibrated thermal resistance are thermally insulated so that all the device power dissipation flows uniformly and unidirectionally through the calibrated thermal resistance to the heat sink. After thermal equilibrium is established, the temperature drop is measured, by means of two thermocouples, across the calibrated thermal resistance. This temperature drop divided by the known thermal resistance yields the device average power dissipation.

6.3.4.4.2 Test Circuit

A simplified test circuit diagram is given in Fig. 6.23 and it operates as follows. The test current waveform is obtained by first charging capacitor C from the dc supply through switch S-1, inductor L and resistor R. R is a very low resistance non-inductive current sensing resistor. After C is fully charged, S-1 is opened and the device under test (D.U.T.) is then triggered. The test current waveform results from C discharging through rectifier diode D1, R, L and D.U.T. The values of L and C control the test current waveform. The oscillatory nature of the test current will back bias D.U.T., thus turning it off. Off-state voltage can then be applied to the D.U.T. at any subsequent time by closing switch S-2. Rectifier diode D1 must have a recovery time longer than that of the D.U.T. (so that back bias will develop across D.U.T.) but shorter than the shortest turn-off time to be measured. Rectifier diode D3 and voltage regulator diode D4 are shown to illustrate one method of

controlling the reverse test voltage at time t_6. With this circuit arrangement an overshoot reverse voltage as depicted at time t_4 may result if D3 is slow in turning on or appreciable inductance is present in the D3, D4 circuit loop. For lower reverse test voltage values at time t_6, voltage regulator diode D4 can be replaced by any number of rectifier diodes connected in series with D3. The test circuit may be made to operate repetitively by the proper timing and sequencing of S-1, S-2 and the triggering of D.U.T.

6.3.4.4.3 Test Conditions To Be Specified

1. On-state current pulse time to peak ($t_2 - t_1$) _____ μ s
2. On-state current pulse base width ($t_3 - t_1$) _____ μs
3. Peak on-state current (t_2) _____ A
4. On-state current pulse repetition rate _____ pps
5. Peak reverse voltage (t_5) _____ V
6. Reverse voltage (t_6) _____ V
7. Peak off-state voltage (t_0, t_8) _____ V
8. Peak reverse current (t_4) Min. _____ A
   Max. _____ A
9. Rate of rise of off-state voltage (Linear ramp) (t_6 to t_8) _____ V/μs
10. Case temperature _____ °C
11. Gate Trigger pulse
    Source Voltage _____ V
    Source Resistance _____ ohms
12. Gate trigger pulse width (90% points) (base width must be less than $t_3 - t_0$ but greater than $t_1 - t_0$) _____ μs
13. Gate trigger pulse rise time (10% to 90%) _____ μs
14. Gate bias conditions
    Source Voltage ± _____ V
    and Source Resistance _____ ohms
    or Gate Bias Resistance _____ ohms

15. Reapplied voltage duration ($t_9 - t_8$) 50 μs min.

16. Off-state voltage supply decay (t_8 to t_9) 5% of Test Condition 7 max.

6.3.4.4.4 Characteristic To Be Measured

1. Turn-off Time (t_q) _____ μs max.

2. Average Power Dissipation _____ W max.

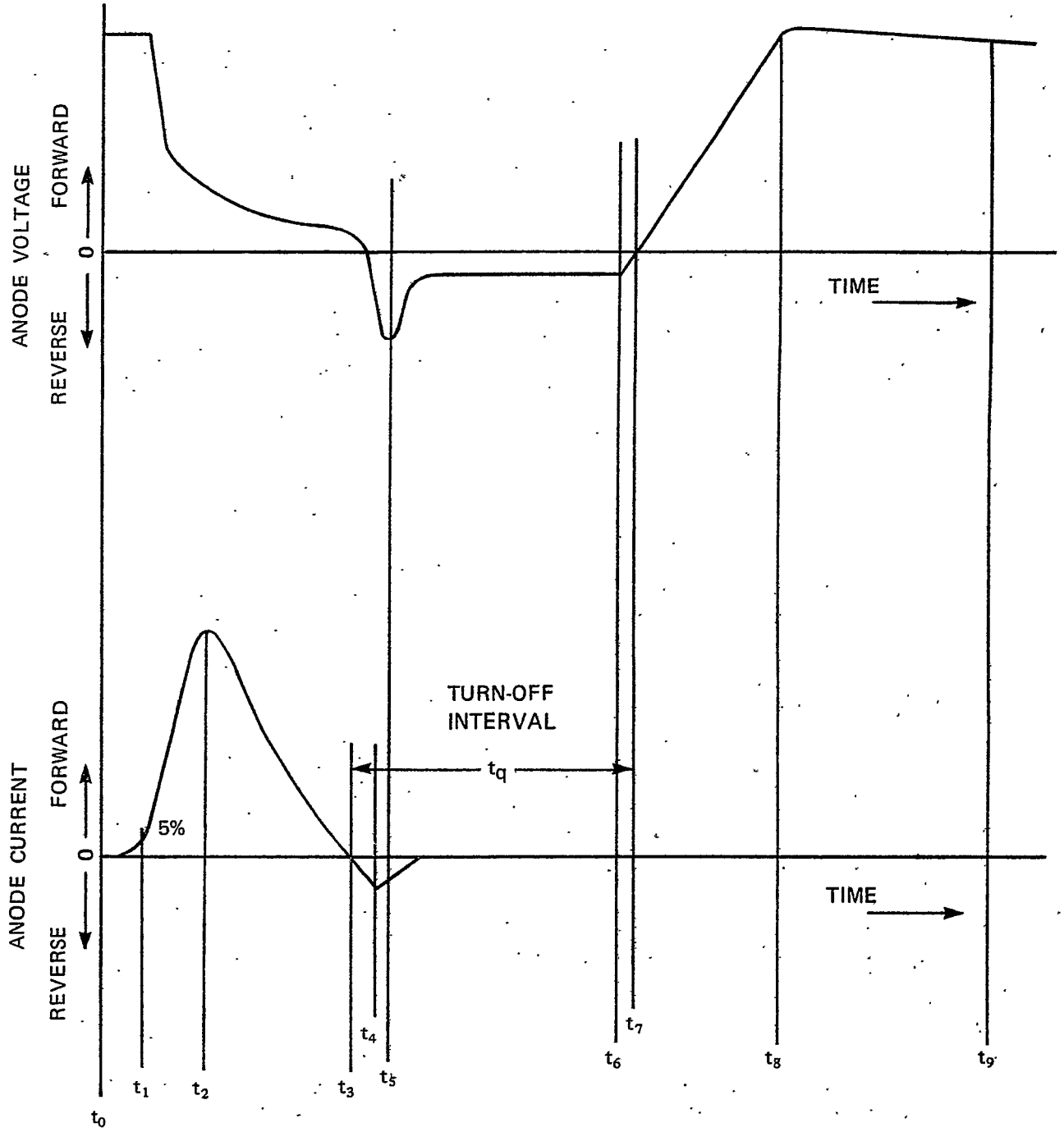


FIGURE 6.22

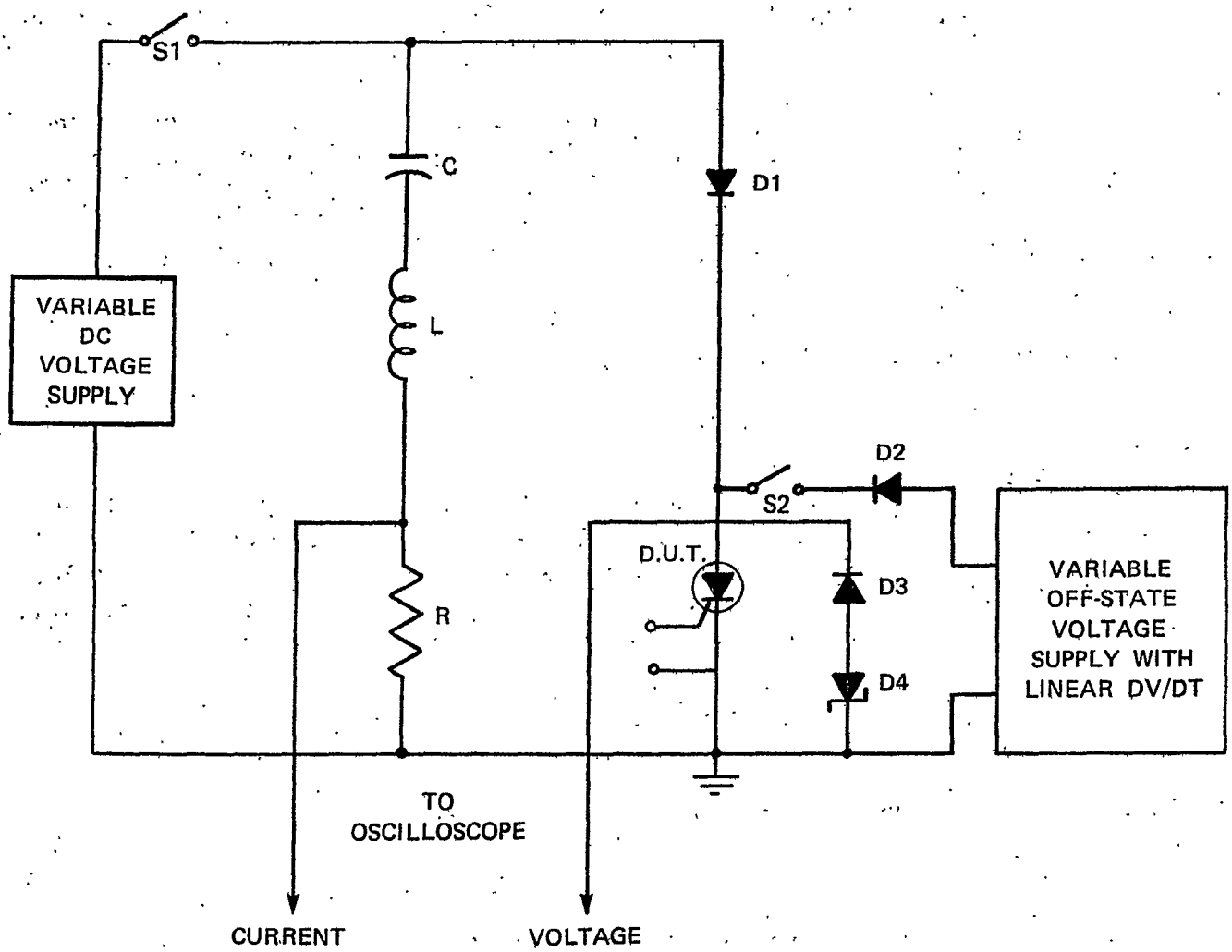

S1
C
D1
VARIABLE
DC
VOLTAGE
SUPPLY
L
D2
S2
D.U.T.
D3
R
D4
VARIABLE
OFF-STATE
VOLTAGE
SUPPLY WITH
LINEAR DV/DT
TO
OSCILLOSCOPE
CURRENT
VOLTAGE

FIGURE 6.23

6.3.5 Critical Rate of Rise of Off-State Voltage Test Method

This test applies to all thyristors including the bidirectional for both polarities of applied voltage.

The off-state stability of a thyristor is sensitive to the rate at which the off-state voltage is applied. Off-state voltages applied faster than a given rate will cause the device to break-over prematurely into the on-state.

Critical rate of rise of off-state voltage is defined as the minimum value of the rate of applied off-state voltage which will cause the thyristor to switch from the off-state to the on-state under specified conditions.

Generally two types of rates of voltage rise are referred to, exponential and linear. The exponential method is the method used for registration of dv/dt.

6.3.5.1 Exponential Voltage Rise Test Method

6.3.5.1.1 Test Description

This test is performed with an exponential waveform of specified amplitude with the device initially unenergized. The rate is increased until the thyristor breaks over. The rate of rise at breakover is the critical value. The exponential method produces a changing rate of rise which requires an arbitrary definition of numerical value. The numerical value of this rate of rise is calculated as follows:

$$\text{Critical rate of rise} = \frac{\text{Peak Off-State Voltage) X 0.632}}{T}$$

The test voltage waveform is shown in Figure 6.24.

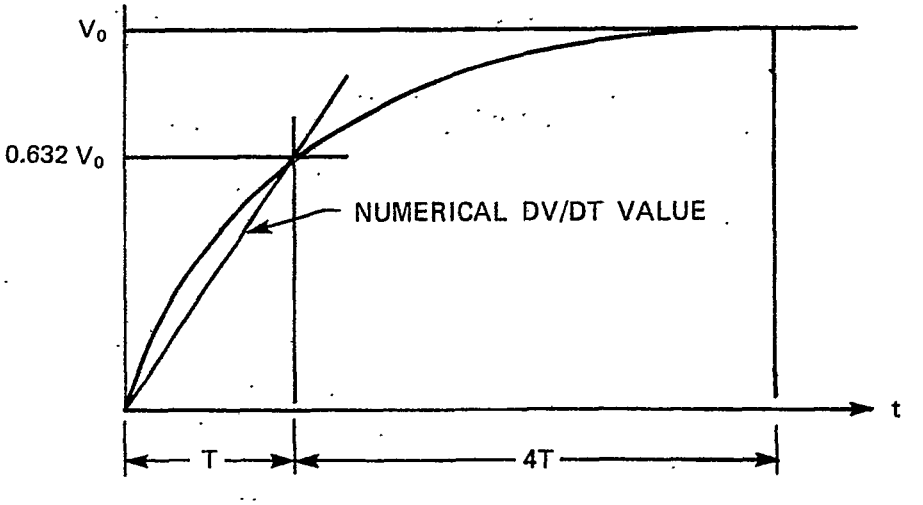


FIGURE 6.24 – TEST VOLTAGE WAVEFORM

6.3.5.1.2 Test Circuit

A circuit diagram is shown in Figure 6.25. The following precautions are recommended:

a. The values of R_2 and C_1 must be selected to minimize waveform distortion due to thyristor and circuit wiring impedances.

b. The switch S_1 should have a closure time (including bounce) of not more than 0.1 T (critical time constant). The switch should be closed for a minimum of 5 T.

c. The current limiting resistor R_2, or other protective circuitry may be required to prevent damage to the thyristor under test in the event of breakover.

d. The purpose of R_3 is to discharge C_1 while S_1 is open so that the test may be performed on a repetitive basis. The repetition rate should be low enough so that halving the repetition rate does not change the results within the accuracy limits of the test.

e. The rate of rise is increased by lowering the capacitance of C_1.

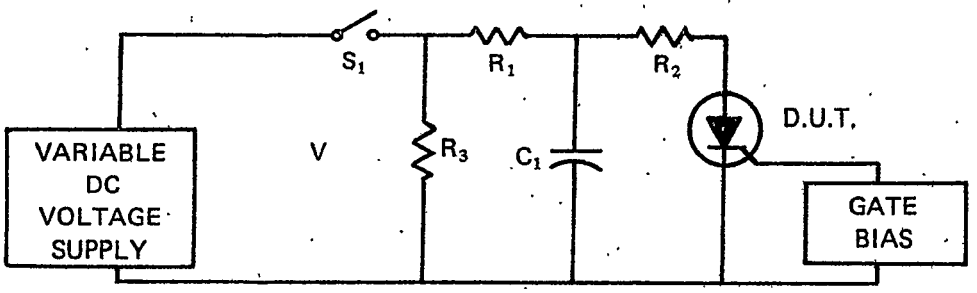


FIGURE 6.25 – CIRCUIT DIAGRAM

6.3.5.1.3 Test Conditions To Be Specified

A. Off-State Voltage (Rated Preferred) _____ Volts

B. Case Temperature _____ °C

C. Gate Bias Conditions

1. Source Voltage = ± _____V and Source Resistance = _____Ohms.

2. Or Gate Bias Resistance = _____Ohms.

6.3.5.1.4 Characteristic To Be Measured

A. Numerical Value of Critical Rate of Rise (dv/dt) Exponential_____V/μs

6.3.5.2 Linear Voltage Rise Test Method

6.3.5.2.1 Test Description

This test is performed with a linear voltage waveform of specified amplitude with the device initially unenergized. The rate is increased until the thyristor breaks over. The rate of rise at breakover is the critical value. The test voltage waveform is shown in Figure 6.26. The numerical value of the critical rate of rise = $\frac{0.8\ V_O}{t_2 - t_1}$

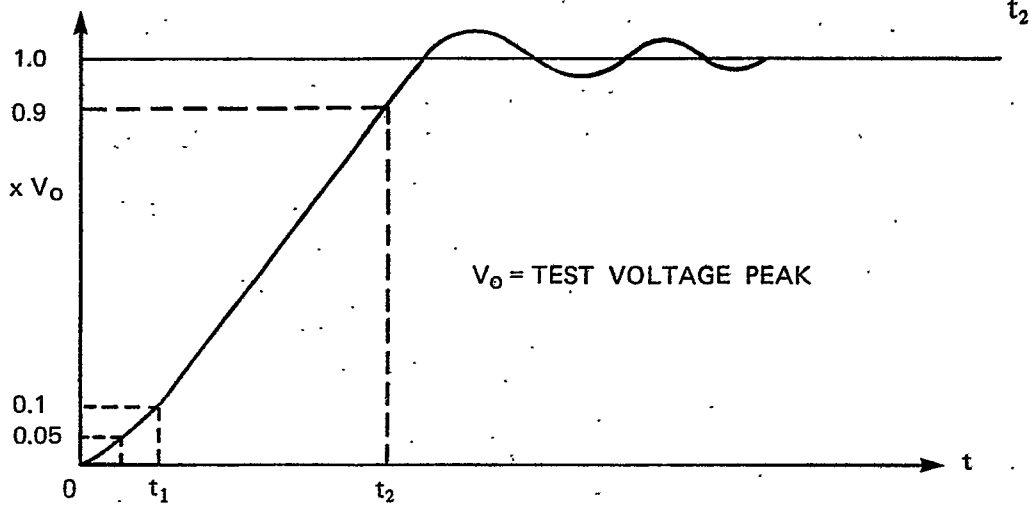


FIGURE 6.26 – TEST VOLTAGE WAVEFORM

The linearity of this waveform is specified as follows:

a. The instantaneous test voltage between 10% and 90% V_O shall not vary by more than ± 10% from the corresponding value on the straight line connecting the 10% and 90% V_O points.

b. The instantaneous slope of the test voltage between 10% and 90% V_O shall not vary by more than ± 100% from the slope of the line connecting the 10% and 90% V_O points.

c. The slope of the straight line connecting the 5% and 10% V_O points shall not be less than 75% of the slope of the straight line connecting the 10% and 90% V_O points.

d. The peak of the test voltage overshoot shall not exceed 10% V_O.

6.3.5.2.2 Test Circuit

A circuit diagram is shown in Figure 6.27. The basis of the circuit operation is the flow of a constant current into a capacitor giving rise to a linear dv/dt.

Initially, S_1 (which may be an SCR) is open and C_1 and C_2 are charged to their full voltage. A constant current, with amplitude dependent on Supply I setting, is

flowing through loop L_1, D_1. At some time later, S_1 is closed and the constant current flows through R_3 and into C_3 generating a voltage across C_3, which is in parallel with the thyristor under test. The slope of this ramp can be varied by adjusting the magnitude of the constant current and/or adjusting the capacitance of the C_3 branch by adding capacitance with S_2. The voltage amplitude to which this ramp rises is determined by the sum of the voltage across C_1 and C_2. The dv/dt measurement is made on an oscilloscope connected across the thyristor under test.

The following precautions are recommended:

a. Slow switching of S_1 can cause an undesirable non-linearity in the voltage waveform (see interval $t = 0$ to t_1 in Figure 6.26). It is possible to eliminate this by the addition of R_5,D_2 and the negative voltage supply. However, should this addition be utilized, the reverse voltage across the thyristor under test, when S_1 is open, must be less than .02 V_O.

b. During the test, S_1 should be closed for a minimum of 50 μs.

c. R_6 may be required to prevent damage to the device under test in the event of breakover. However, R_6 should be as small as possible in order to minimize test voltage waveform distortion.

d. In the test circuit provision is made for the discharge of C_3, while S_1 is open so that the test may be performed on a repetitive basis. The repetition rate should be low enough so that halving the repetition rate does not change the results within the accuracy limits of the test.

e. Inductance due to wiring should be kept at a minimum in the loop containing C_2, D_1, S_1, R_3. D_1 should be a fast recovery rectifier diode(s).

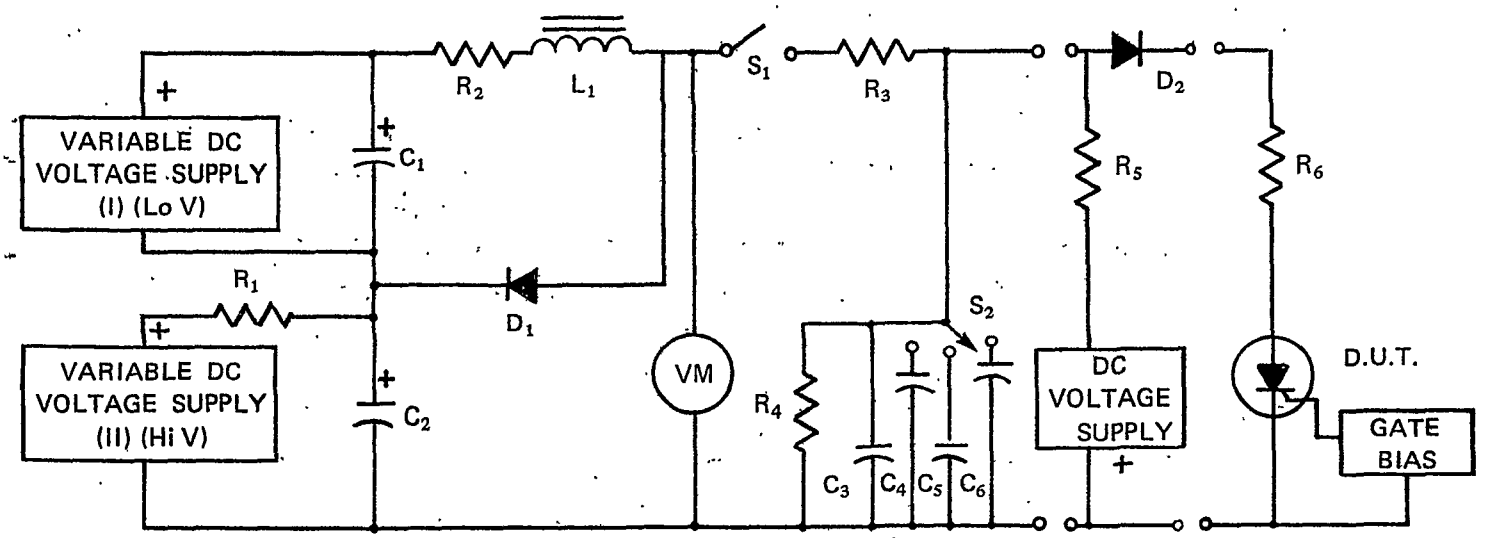


FIGURE 6.27 – CIRCUIT DIAGRAM

6.3.5.2.3 Test Conditions To Be Specified

A. Off-State Voltage (Rated Preferred) _____ V

B. Case Temperature _____ °C

C. Gate Bias Conditions

1. Source Voltage = ± _____ V and
   Source Resistance = _____ Ohms.

2. Or Gate Bias Resistance = _____ Ohms.

6.3.5.2.4 Characteristic To Be Measured

A. Numerical Value of Critical Rate of Rise (dv/dt) Linear _____ V/μs.

6.3.6 Thermal Resistance and Transient Thermal Impedance Test Method

The thermal resistance of a thyristor is a measure of the ability of the thyristor package to remove heat from the junction and therefore an indication of the power handling capability of the thyristor. Thermal resistance is measured in Celsius degrees of temperature rise of the junction, per watt of power dissipated in the junction. (°C/W)

Three thermal resistance measurements are common: $R_{\theta JC}$ – steady state thermal resistance from junction to case, $R_{\theta JA}$ – steady state thermal resistance from junction to ambient with device unattached to a heat sink or attached to a specified heat sink, and $Z_{\theta(t)}$ – transient thermal impedance to a specified reference (case, heat sink, ambient, etc.), a measure of junction temperature rise for a specified power pulse.

6.3.6.1 Test Description

The measurement of these characteristics is based on the use of a temperature sensitive parameter as an indicator of virtual junction temperature. On-state voltage at a small percentage of rated current is normally used as the temperature sensitive parameter. The low level on-state voltage is monitored immediately after the device has dissipated a known power pulse. The junction temperature rise is determined from the measured low level on-state voltage. Thermal resistance is calculated as:

$$\text{Thermal resistance} = \frac{\text{Junction temperature rise}}{\text{Power}}.$$

A calibration curve should be prepared for the thyristor by measuring on-state voltage as a function of virtual junction temperature at the selected value of measuring current. Discontinuities in this curve as shown in curve B, Figure 6.28 indicate partial switching which should be corrected by selecting a higher value of measuring current.

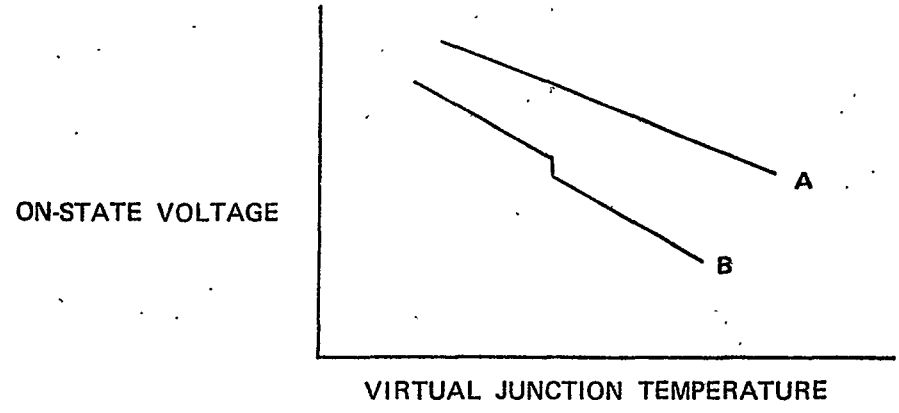


FIGURE 6.28 – CALIBRATION CURVE

6.3.6.2 Test Circuit

A test circuit as illustrated in Figure 6.29 may be used to obtain the data required for calculating the transient thermal impedance characteristic curve. After establishing thermal equilibrium, the power dissipated in the thyristor should be measured and recorded. The heating current supply is then interrupted and the on-state voltage produced by the measuring current supply is recorded as a function of time as shown in Figure 6.30. This may be accomplished by photographing the oscilloscope trace. The test may be repeated at different oscilloscope sweep rates in order to adequately measure the on-state voltage over the entire time range. Reference point temperature should also be monitored as a function of time. Since this change is relatively small and slow, a thermistor or thermocouple measuring system should be adequate.

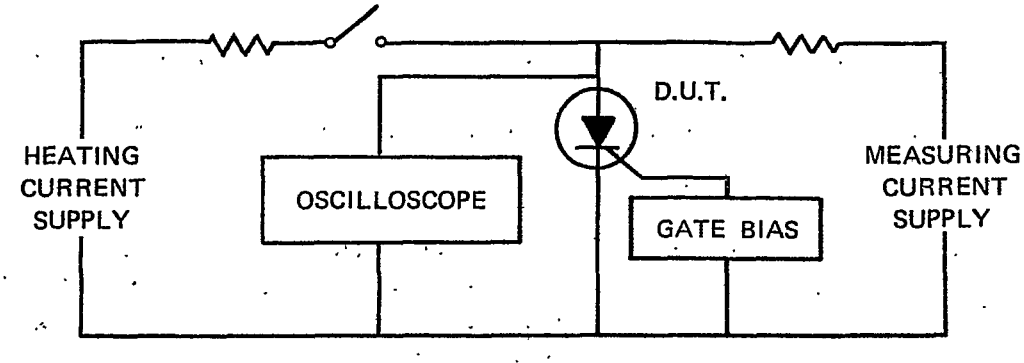


FIGURE 6.29 – TEST CIRCUIT

The curve of on-state voltage as a function of time can be converted to virtual junction temperature versus time by means of the calibration curve. Transient thermal impedance junction to case is then calculated as follows:

$$Z_{\theta JC(t)} = \frac{(T_J - T_C) - (T_J' - T_C')}{P}$$

Where T_J = The virtual junction temperature at the time of heating current interruption.

T_J' = Virtual junction temperature at a specified time after heating current interruption.

P = The power dissipation which caused the change of temperature difference.

T_C = Case temperature at the time of heating current interruption.

T_C' = Case temperature at the specified time after heating current interruption.

$Z_{\theta JC(t)}$ = Transient thermal impedance, junction to case for the specified time interval.

Figure 6.31 illustrates the shape of a typical transient thermal impedance curve.

Thermal resistance is the value of $Z_\theta(t)$ when the time is long compared to the thermal time constants of the thyristor and may be computed from:

$$R_{\theta JC} = \frac{T_J - T_C}{P}$$

For transient thermal impedance, or thermal resistance, junction to ambient substitute ambient temperature for case. Transient thermal impedance or thermal resistance between any two points is obtained by substituting temperature measurement at these points for T_j and T_C in the equations.

Difficulties with this measurement method are due to ambiguity in determining the value of virtual junction temperature at the time of current interruption. Nonthermal voltage transients occur due to the excess charge carriers present after the heating current is interrupted. This difficulty can be avoided by extrapolating the on-voltage versus time curve back to zero time from a time known to be in charge equilibrium. This time can be estimated from life time observations or by performing the measurements at different power levels and noting the shortest time where the virtual junction temperature is a linear function of power dissipated. The dotted portion of the on-state voltage curve illustrates the extrapolation to the point shown as V_T in Figure 6.30.

Another source of non-thermal transients in the on-state voltage characteristic is due to the collapse of the magnetic field around the thyristor when the heating current is interrupted. This problem may be significant when currents of ten amperes or more are used with thyristors housed in packages having a magnetic material encircling the conductor. Decay times in the order of one-half to one milli-second have been observed due to this phenomenon.

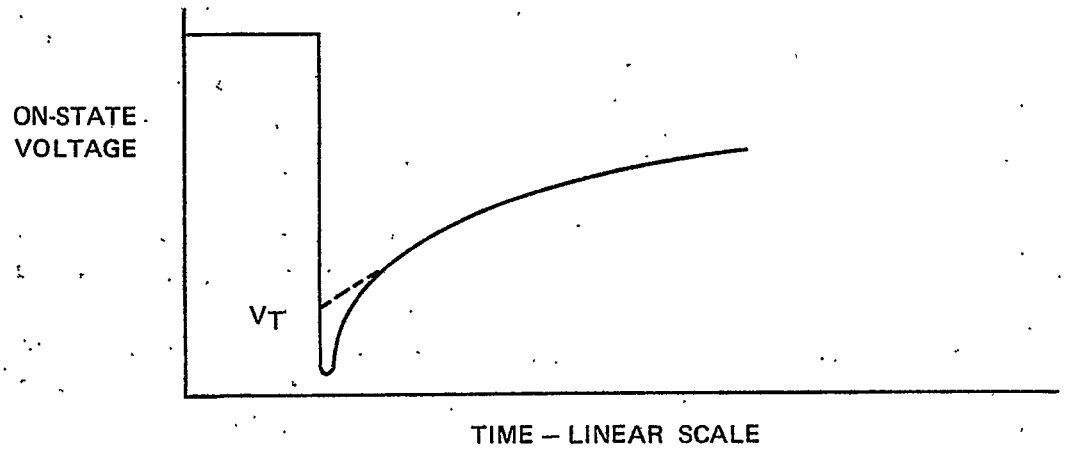


FIGURE 6.30 – ON-STATE VOLTAGE CURVE

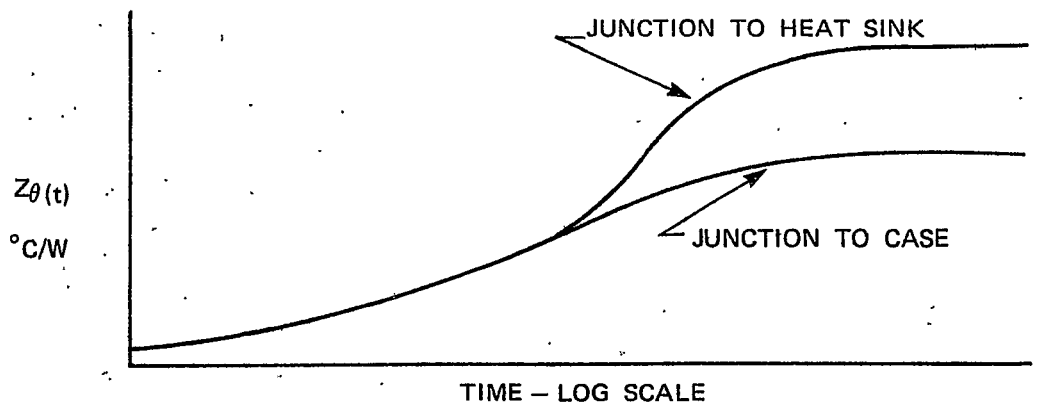


FIGURE 6.31 – TRANSIENT THERMAL IMPEDANCE CURVE

6.3.7 Critical Rate of Rise of Commutation Voltage for Bidirectional Thyristors

6.3.7.1 Test Description

This test applies to all bidirectional thyristors for both polarities of applied voltage.

The bidirectional thyristor, in its usual mode of operation, is required to switch to the opposite polarity off-state following current conduction in the on-state. In common 50/60 Hz or 400 Hz ac phase control applications utilizing sinusoidal voltage sources, this switching occurs each half cycle at the current zero point. This switching action is termed "commutation" and it is brought about by the reversal of the source voltage. The ability of the thyristor to maintain the off-state as this commutation voltage builds up in the opposite direction is determined by: (1) device operating temperature, (2) rate of reversal of current, (3) magnitude and time rate of application of commutation voltage.

This test method establishes the on-state current magnitude, duration, repetition rate, and rate of reversal; the device case temperature; and commutation voltage magnitude as test conditions and measures the critical rate of rise of the commutation voltage. The critical rate of rise of commutation voltage is the rate above which the device will not maintain the off-state but will conduct current in the opposite direction in the absence of a gate trigger signal. While this failure to switch to the off-state is not detrimental to the thyristor, it does result in loss of control of power to the load.

The voltage, current and temperature test conditions selected for this test are recommended to be the maximum registered values for the thyristor under test. The device under test may be triggered by means of any convenient trigger pulses of either polarity.

6.3.7.2 Test Circuit

The test circuit to be used is shown in Fig. 6.33 and the test current and voltage waveforms are shown in Fig. 6.32.

The power source for the test circuit is a 50/60 Hz or 400 Hz single phase sinewave supply which produces sinusoidal test current. The X/R for the entire test circuit shall be $\geqslant 10$ so that the supply voltage and current are essentially in quadrature. The time rate of application of commutation voltage (test device off-state voltage) is essentially exponential and is determined by the setting of R_1 and C_1. This voltage may be observed by means of an oscilloscope connected across the test device. The numerical value assigned to the dv/dt of the exponential voltage waveform is defined here as the slope of the straight line connecting the 10% and 63% points on the test voltage waveform. The 10% voltage point is used instead of zero because of the difficulty in determining the time point at which zero voltage occurs. The test voltage overshoot should be limited to 10% of the specified peak value of the test voltage.

In this test method the rate of reversal of test current (di/dt) is quite circuit limited. Hence for thyristors with very good switching capability during commutation, the test device may

maintain the off-state even when R_1 and C_1 are removed. In this case the dv/dt of the test voltage waveform is determined by the capacitance of the thyristor and distributed capacitance of other circuit components, particularly the reactor.

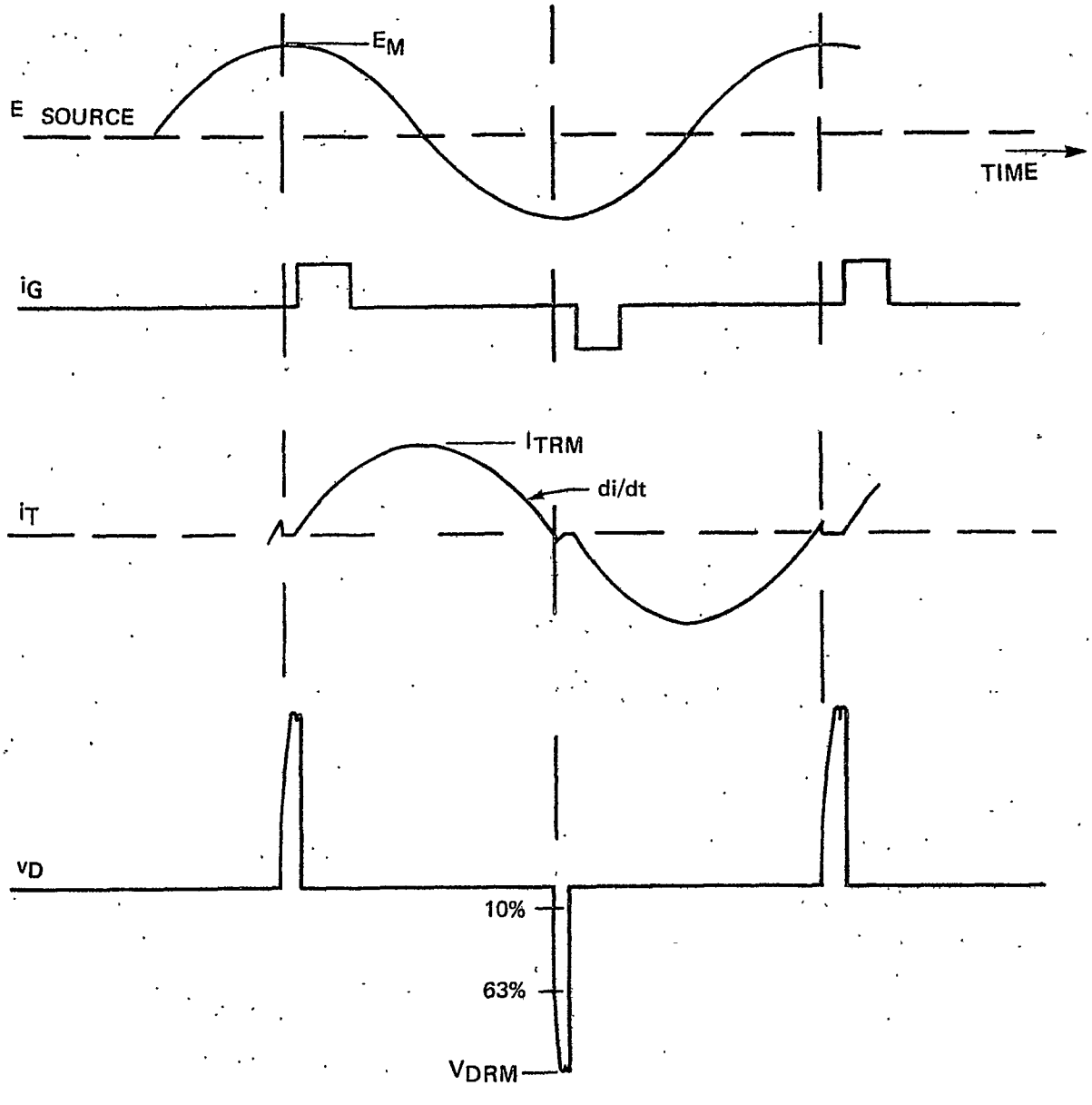


FIGURE 6.32 – TEST WAVEFORMS

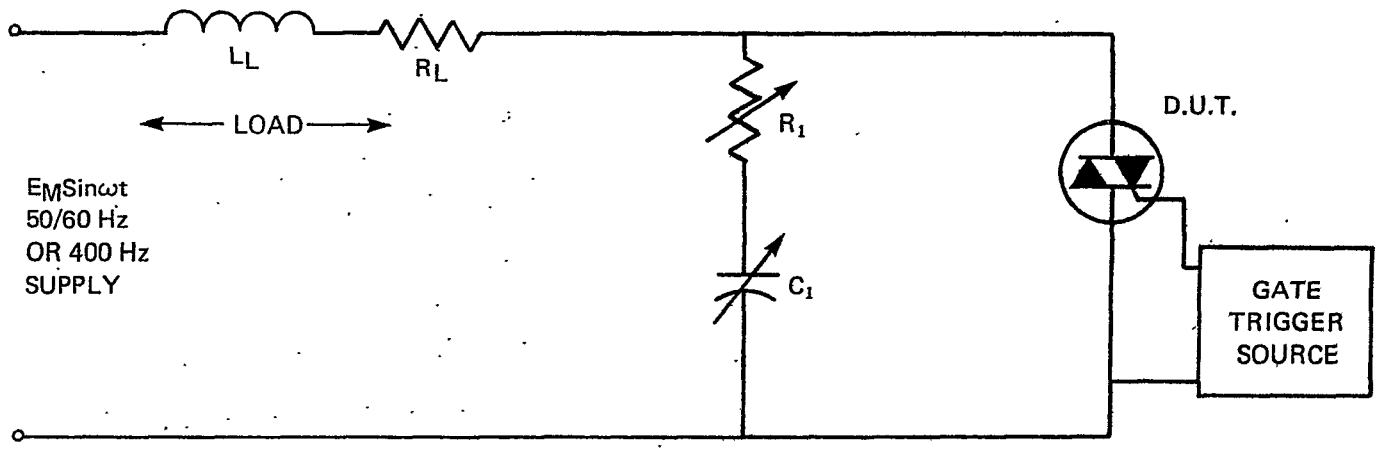


FIGURE 6.33 – CRITICAL RATE OF RISE OF COMMUTATION VOLTAGE TEST CIRCUIT

6.3.7.3 Test Conditions To Be Specified

These specifications apply for each half cycle of the test voltage and current.

1. Frequency of Single Phase Sinusoidal AC Supply (50 or 60 Hz, or 400 Hz recommended) _____ Hz

2. Peak On-State Current ($I_{TM} \approx \frac{E_M}{Z_L}$) _____ A

3. On-State Current Duration (90% of half cycle recommended) _____ ms

4. Rate of Reversal of On-State Current (di/dt) (The slope of the line connecting the 50% and 0% I_{TM} points; $di/dt \approx (6fI_{TM} \times 10^{-6})$ _____ A/μs

5. Peak Off-State Voltage ($D_{RM} \approx E_M$) _____ V

6. Off-State Voltage Duration (200 μs min recommended) _____ μs

7. Gate Bias Conditions (between current pulses)
   Gate Source Voltage _____ V
   Gate Source Resistance _____ ohms
   or Gate Bias Resistance _____ ohms

8. Case Temperature _____ °C

6.3.7.4 Characteristic To Be Measured

Critical Rate of Rise of Commutation Voltage (The slope of the line connecting the 10% and 63% test voltage points) _____ V/μs

PART 7

USER'S GUIDE

INDEX

PART 7

USER'S GUIDE

7.1 INTRODUCTION

The optimum use of thyristors requires considerable knowledge of the device on the part of the user. The purpose of this section is to give some explanation of thyristors ratings and characteristics and to point out how these ratings and characteristics must be considered in actual thyristor applications. This section will not give minute device or applications detail. Rather it will serve as a guide or outline from which the user may proceed to additional technical information sources.

7.2 THYRISTOR SAFETY CONSIDERATIONS

The designer, maker and user of electrical equipment containing thyristors should give attention to the following points relative to the safety of personnel who may operate the equipment:

1. The electrical potentials on the anode, cathode and gate terminals on the thyristor present an electrical shock hazard when the equipment is energized.

2. The normal operating case temperature of energized thyristors is often high enough to present burn hazards to both operating personnel and flammable material touching the thyristor.

3. If the thyristor is falsely triggered (for example, conducting films produced by certain environments appearing across the thyristor insulation) or fails (see 7.10 and 7.11), power, of course, will be applied to the equipment load. Operator safety may be affected by an unexpected energizing of the load.

4. In the event that an equipment output short or internal fault condition develops, very high surge current can be passed through the thyristors. If this surge current exceeds thyristor ratings for magnitude and duration, the thyristor may be damaged; and if the surge is severe enough, internal heating can cause the thyristor to rupture and perhaps sustain an arc.

7.3 VOLTAGE CONSIDERATIONS

7.3.1 Basis for and Comparison of Thyristor Voltage Ratings

There are four common voltage ratings assigned to thyristors.

7.3.1.1 Repetitive Peak Reverse Voltage

This is the normal maximum allowable value of reverse voltage which may be applied to the thyristor. At this voltage, reverse power dissipation is generally small and contributes little to the total dissipation in the thyristor.

The repetitive peak reverse voltage occurring in a thyristor circuit is a known or measurable periodic function and may be considered to be under the control of the equipment

designer. Any repetitive peak voltages occurring in the circuit even of short duration, such as those due to switching action of the thyristor, should be included in this category.

7.3.1.2 Non-Repetitive Peak Reverse Voltage

For short time intervals, the reverse voltage may be permitted to exceed the steady state ratings. During this time the instantaneous power dissipation may become significant, but still remain below the level which the manufacturer has found to be destructive. While the energy dissipated during this time causes an increase of junction temperature, the level reached is not sufficient to cause thermal runaway, and removing the excess voltage within the time period specified will allow the junction temperature to rapidly drop back to the steady state operating level. In addition to considerations of thermal runaway, non-repetitive peak reverse voltage ratings are often limited by the manufacturer for other reasons, such as an abrupt change in slope of the reverse blocking volt-ampere characteristic or hysteresis, discontinuities (including sharp knees) or instability exhibited in the same characteristic. Non-repetitive reverse voltages may occur as random circuit transients, which may or may not originate within the equipment. These voltages may often be minimized by the provision of voltage surge suppression components as discussed in the following paragraphs.

7.3.1.3 Repetitive Off-State Voltage

This is the maximum repetitive value of off-state voltage, either transient or steady state, which the thyristor is rated to block under stated conditions. Above this voltage, the thyristor may switch to the conducting or on-state. The blocking capability of thyristors is sensitive to temperature and for most types is lowest at the highest operating temperature (T_S). The gate bias present from gate to cathode external to the thyristor also may affect blocking capability, and in some types, the rating of the device requires a specific gate bias.

While triode thyristors are generally designed to be turned on only by gate signals, turn-on by exceeding the blocking voltage may not be destructive. Manufacturers will generally specify whether or not this is the case for a specific device type. Limitations on rate-of-rise of anode current must be observed after turn-on, as discussed in Section 7.6.2, and it should be noted that device di/dt capability may be lower under turn-on from excess off-state voltage than when gate triggered.

Undesirable circuit action may result from inadvertent turn-on and should be considered in equipment design.

7.3.1.4 Peak Principal Voltage

As discussed in the previous paragraph, thyristors are to some degree self-protecting from overvoltages in the off-state, since they can switch to the on-state at excessive voltage levels. However, there may be secondary effects, such as surface field stresses, which require that an upper limit be placed on the principal voltage applied to the thyristor in the off-state. For instance, a reverse blocking device having an off-state voltage rating of two hundred (200) volts at 100°C may not turn on at 700 volts at 25°C. The device may carry a Peak

Positive Principal Voltage (or Peak Positive Anode Voltage) rating which requires that no more than 600 volts be applied, even if it is capable of blocking this voltage under certain conditions. If the Peak Positive Principal Voltage rating is exceeded, either continuously or transiently, device degradation or destruction may result.

Bidirectional thyristors are not subject to the reverse voltage considerations noted in paragraphs 7.3.1.1 and 7.3.1.2 above, since they will turn on in either direction. Therefore, the remarks concerning off-state voltage and peak principal voltage may be considered to apply to bidirectional devices in both polarities.

7.3.2 Overvoltages

Because of the sensitivity of silicon thyristors to voltage transients in excess of their ratings, proper circuit design may require some built-in means to afford safe operation. Transient voltages generally are caused by the following:

1. De-energizing a transformer primary.
2. Energizing a transformer primary.
3. External disturbances caused by lightning, motors, solenoids, relay circuits, etc., which share the same alternating-current source with the thyristor circuit.
4. Alternating-current switching.
5. Reverse recovery transients (See 7.6.4).
6. Opening dc load switches when using an LC filter with high L/C ratio.
7. Regenerative types of load.
8. Fuse blowing when used for isolating a defective thyristor in a parallel-connected group.

Each transient voltage source produces a different degree of voltage oscillation, e.g., some generate up to twice the working peak reverse voltage of the circuit, while others can generate as high as eight or ten times this value. The surest method to observe transients is with a high-speed oscilloscope. It should have a frequency response of at least 40 MHz. Peak reading voltmeters are also used to measure transient voltages but generally with a lesser degree of certainty. However, they are very useful when the occurrence of the transient is unpredictable.

In order to maintain peak voltages within thyristor ratings, the following points should be considered:

1. The speed of current interruption by the switching elements, (circuit breaker, fuse, etc.)
2. The location of switching elements or the sequence of switching.

3. Provision for additional energy storage or dissipation means in the circuit. (Examples: capacitive filters or voltage clipping devices, such as those made from silicon-carbide, selenium, etc., across transformer windings, across the thyristor and, sometimes, across output terminals.)

4. Provision of peak voltage capability equal to the maximum anticipated transient by the use of thyristors with adequate voltage ratings or the use of an adequate number of thyristors in series.

7.3.3 Series Operation

The usual series operation techniques for obtaining higher voltage outputs can be readily used for thyristors without difficulty providing the device manufacturer's recommended procedures are followed. Generally, these procedures depend on the type of electrical characteristics which are considered typical of the device as manufactured and, also, on the actual application conditions.

It is important when thyristors are operated in series that the proper division of voltage is assured. Generally, manufacturers will recommend one or more of the following procedures:

1. Factory matched off-state and reverse characteristics.

2. Resistive voltage dividers shunting the thyristors.

3. Capacitive voltage dividers shunting the thyristors.

4. Multiple transformer windings supplying rectifier circuits having outputs connected in series.

Thyristors which have been factory-matched with respect to off-state and reverse breakdown characteristics, reverse current, and temperature coefficient have operated successfully with no voltage dividers. The use of resistors placed across each thyristor, the magnitude of which is equal to some fraction, say one-half, of the minimum blocking resistance of the thyristor, will force voltage division during steady-state operation. For some applications, differences in reverse recovery time may be an important factor as this affects the proper division of voltage during transient switching. Moreover, the variation of the capacitance between the individual devices and even the variation of capacitance to ground (when many units in series are used) can cause an unequal voltage division. In both of these cases, a capacitive voltage divider is required and can be provided by connecting a capacitor across each thyristor.

When capacitive dividers are used, a damping resistance should be used in series with each capacitor to prevent oscillatory overvoltages and avoid excessive di/dt or peak current in the thyristor when it is turned on with off-state voltage present.

When only a few thyristors are in series, multiple transformer windings may be used where each winding supplies a thyristor assembly consisting of one thyristor in each circuit leg. The outputs of each thyristor assembly are then connected in series to obtain the desired voltage. Generally, the choice of circuit will depend upon the application and number of units in series. The manufacturer should be consulted for recommendations.

Gate triggering provisions for units operated in series require special attention. Adequate magnitude and rise time of the gate signal must be used to minimize differences in delay time and rise time between the units during turn-on of the series string. Otherwise, voltages exceeding the peak principal voltage ratings might be applied to the slower units. It is often difficult to obtain adequate rise time characteristics in multiple secondary pulse transformers used to trigger a large number of thyristors in series.

7.4 CURRENT CONSIDERATIONS

7.4.1 Maximum Operating Junction Temperature

Thyristor steady-state current ratings are ultimately limited by the maximum allowable junction temperature rating of the device. The semiconductor manufacturer determines the maximum junction temperature rating by evaluating the following factors and then deciding upon the best compromise:

1. The melting temperatures or temperatures of physical change of device materials. This consideration places the absolute upper limit on device operating temperatures.

2. The temperature dependence of the off-state breakover voltage. Above a certain temperature the breakover voltage decreases rapidly with temperature.

3. The temperature dependence of the off-state and blocking current. Off-state and reverse blocking current are exponential functions of temperature and this produces an exponential blocking power generation relationship with temperature. If blocking power losses become too high, the device may run away destructively in the reverse direction (or switch to the on-state from the off-state) because of the regenerative blocking power-junction temperature rise relationship.

4. Reliability considerations – In general, the lower the operating junction temperature, the greater the life expectancy of any semiconductor device. This fact is, of course, in conflict with the users' and manufacturers' desire to obtain the greatest power output from a given semiconductor device size.

5. Effect on device characteristics – Since minority carrier lifetime is quite temperature dependent, any thyristor characteristic such as dv/dt capability or turn-off time which depends on lifetime will likewise be temperature dependent. dv/dt capability and turn-off time are both enhanced as the operating junction temperature is reduced. Again, this conflicts with the desire for the highest power rating.

To complete this discussion of junction temperature effects, it should be mentioned that the low junction temperature limits are generally determined by mechanical stress exerted on the silicon crystal. This stress is produced by the imperfect matching of thermal expansion coefficients of the various materials used in the fabrication of the device.

7.4.2 Junction Heat Generation

The conduction current flowing through the thyristor causes a power or heat generation. The heat produced in the device by the flow of steady direct conduction current is simply this current multiplied by the voltage drop across the device. The heat produced in the device by a periodic current may be determined by integrating the instantaneous product of device current and voltage as follows:

$$P = \frac{1}{T}\int_0^T e(t)\, i(t)\, dt$$

P — Average power generated in the device.
T — Period of the current.
i(t) — Instantaneous conduction current
e(t) — Instantaneous voltage across the device.

Since the thyristor conduction current and voltage are related in a nonlinear manner, this integration must be carried out by such means as graphical integration or by determining a mathematical approximation for the thyristor volt-ampere characteristic which will permit integration in closed form.

Other sources of device heat generation include power losses when the device is in the off-state or reverse blocking state. Gate signal power losses are quite small compared to the power loss produced by conduction current. The same is true of switching losses except at very high operating frequencies. To simplify various calculations, all heat generated in the thyristor is assumed to be uniformly generated at the center plane of the silicon crystal.

7.4.3 Thermal Resistance

A measure of the effectiveness with which a semiconductor device is able to get rid of heat is called thermal resistance. The lower the device thermal resistance figure, the lower the junction temperature rise for a given conduction current and resulting junction power generation. When thermal resistance is specified, the beginning and end of the thermal path must be clearly indicated. The common thyristor device thermal resistance specification is the value from the junction to a particular point on the case. For stud-mounted thyristors, this point is generally the center of one of the hex flats. (Refer to paragraph 7.9.3.3)

The heat flow associated with thyristor junction-to-case thermal resistance may be considered unidirectional. For the direct conduction current situation, Fourier's steady state heat flow relations are analogous to Ohm's steady state direct current flow relations.

Ohm's Law	Fourier's Law
$I = \frac{\Delta V}{R}$	$P = \frac{\Delta T_{JC}}{R_{\theta JC}}$

I = Direct current flow through R in Amperes

R = Electrical resistance in Ohms

ΔV = Voltage difference across R in Volts

P = Power or heat flow in Watts

$R_{\theta JC}$ = Thermal resistance from junction to case in °C/W

ΔT_{JC} = Temperature difference across $R_{\theta JC}$ in degrees C.

When the heat flow (and device current flow) is periodic or pulsating, the small thermal capacitance (heat storage capability) of the silicon crystal in the thyristor causes the junction temperature to rise and fall with the pulsating power generation. Thus, if the thyristor dc or effective junction-to-case thermal resistance is multiplied by the average power generated by a pulsating current, the result will be the average junction temperature rise above the case temperature. To find the peak junction temperature in this case, the thyristor transient thermal impedance characteristic must be used in a power superposition calculation. The reader is referred to the literature where this procedure is adequately covered. Now, it is possible to answer the question as to which instantaneous junction temperature is used by the manufacturer to establish the device maximum operating junction temperature rating. For this rating, different manufacturers may use any one of the following:

a. Peak junction temperature – That is, the highest instantaneous junction temperature produced by periodic conduction current waveforms.

b. Average junction temperature – That is, the average junction temperature produced by periodic conduction current waveforms.

c. The instantaneous temperature at the conclusion of the conduction current – That is, the junction temperature at the instant the blocking voltage is applied.

7.4.4 Steady State Current Ratings

The current rating assigned a thyristor by its manufacturer depends upon its maximum allowable junction temperature rating, the internal device power generation produced by the conduction current, the total thermal resistance from junction to ambient, and finally the ambient temperature. Since the manufacturer has no control over the user's ambient temperature, the size of the heat dissipator that he attaches to the thyristor or how the heat dissipator is cooled, the manufacturer prefers to assign a current rating based upon the case temperature of the device. Since maximum operating junction temperature is fixed, the thyristor current rating will be a curve relating allowable current to case temperature. The lower the case temperature maintained by the user, the higher the allowable device current, and vice versa. The allowable current will approach zero as the case temperature approaches the maximum operating junction temperature. This is true, of course, because the difference between the case and maximum operating junction temperature is the product of the conduction power and the junction-to-case thermal resistance. For lead-mounted thyristors, the current rating curves are often presented as a function of ambient temperature by assuming that no heat dissipator is attached to the device.

The basic current ratings for reverse blocking thyristors are generally given in terms of average current with the current waveforms being either half sine wave of frequency 50 to 400 Hz, or square waves with duty cycle or conduction period as a parameter. Since the half sine wave current waveform can be conduction delayed as determined by the user, the conduction angle of this waveform is generally taken as a parameter in the presentation of the average current rating. These basic current waveforms apply for resistive or inductive loads. Capacitive loads may cause very high peak current for a given average value because the thyristor can only conduct when the supply voltage exceeds the voltage presented by the capacitor.

The current ratings for bidirectional thyristors cannot practically be given in terms of average current. For these devices, rms current is presented as a function of case temperature. The conduction angle of this waveform is generally taken as a parameter. The ratings apply to resistive or inductive loads.

7.4.5 Overload Current Ratings

Overload current ratings may be divided into two types: non-repetitive and repetitive.

Non-repetitive overloads are those which occur rarely and are not a part of the normal application of the device. Examples of such overloads are faults in the equipment in which the devices are used and accidental shorting of the load. Non-repetitive overload ratings permit the device to exceed its maximum operating junction temperature for short periods of time because this overload rating applies following any rated load condition. In the case of a reverse blocking thyristor, the device must block rated voltage in the reverse direction during the current overload. However, no type of thyristor is required to block off-stage voltage at any time during or immediately following the overload. Thus, in the case of a bidirectional thyristor, the device need not block in either direction during or immediately following the overload. Usually only approximately one hundred such current overloads are permitted over the life of the device. These non-repetitive overload ratings just described may be divided into two types: multicycle (which includes single cycle) and subcycle. For a reverse blocking thyristor, the multicycle overload current rating, or surge current rating as it is commonly called, is a curve giving the maximum peak values of half sine wave on-state current as a function of overload duration measured in number of cycles on a 60 Hz basis. Usually these ratings are given for some one to sixty cycles. For a bidirectional thyristor, the current waveform used in the rating is a full sine wave and the current is again specified in terms of peak amperes. For both types of thyristor surge rating curves, the current curves can be converted from peak values to rms current values by using conventional mathematical relationships. Multicycle surge curves are used to select proper circuit breakers and series line impedances to prevent damage to the thyristor in the event of an equipment fault.

The subcycle overload or subcycle surge rating curve is so called because the time duration of the rating is usually from about one to eight milliseconds which is less than the time of one cycle of a 60 Hz power source. Again, overload current is given in curve form as a function of overload duration. RMS current is used rather than average or peak value in order to make the curves as general as possible. This rating also applies following any rated load condition and neither off-state nor reverse blocking capability is required on the part of the thyristor immediately following the overload current. The subcycle surge current rating may be used to select the proper

current-limiting use for protection of the thyristor in the event of an equipment fault. Since this use of the rating is so common, the manufacturer often uses this curve to calculate the i^2t rating for the device and then may simply publish the i^2t rating for the device in place of the subcycle current overload curve. The reason for this is that fuses are commonly rated in terms of i^2t. Incidentally, the "i" in this rating is rms current computed over the time base "t" which is the duration of the overload current.

Repetitive overloads are those which are an intended part of the device application. An example of such an overload would be in a dc motor drive application where the motor furnishes the drive for an electric locomotive used for commuter service. This type of overload may occur any number of times during the life of the thyristor. Therefore, its rated maximum operating junction temperature must not be exceeded during the overload if long thyristor life is required. Since this type of overload can have any conceivable complex current waveform and duty cycle, a current rating analysis involving the use of the transient thermal impedance characteristics is the only practical approach. In this type of analysis, the thyristor junction-to-case transient thermal impedance characteristic is added to the user's heat dissipator transient thermal impedance characteristic. Then by the superposition of power waveforms in conjunction with the composite thermal impedance curve, the overload current rating can be obtained. The exact calculation procedure is found in the power semiconductor literature.

7.4.6 Parallel Operation

Sometimes it is desirable to operate thyristors in parallel to obtain higher circuit output current. The primary design consideration to achieve successful paralleling is to balance the current in the parallel paths. This may be accomplished in two ways:

1. Add sufficient identical impedance in each path to force current sharing even if the very low impedance thyristor conduction E-I characteristics and individual path impedances are grossly mismatched. The addition of resistance to each path will produce this current sharing, but of course, it is a very inefficient method. The use of series reactors affords a method by which the efficiency is improved.

2. Introduce "paralleling reactors" (which actually function as transformers) which induce the proper correcting voltage in response to the current unbalance in the parallel paths. The use of paralleling reactors can only be used in ac phase control applications and not in dc chopper applications.

3. Factory match the thyristor conduction characteristics and very carefully design the parallel paths so that their impedances (self inductance, mutual inductance and resistance) are balanced without the addition of lumped impedances. (A circular device configuration and coaxial power leads may be required to achieve this objective.) Since thyristor conduction E – I characteristics are somewhat temperature dependent, it is well to mount all paralleled thyristors on a common heat dissipator to insure the same operating junction temperature.

Perfect current sharing seldom can be achieved using any matching method, so the average current per parallel thyristor should be reduced accordingly. Generally this derating is about 10%.

In parallel operation, the thyristor triggering must also be carefully handled. If pulse triggering is used, it must be of sufficient duration to permit all thyristor conduction currents to build up to greater than latching current values. The trigger pulses should be very fast rising and of high magnitude to insure good current sharing during the turn-on interval. If the load is inductive and thus produces slow rising output current, a gate signal applied throughout the conduction period should be considered. If it is necessary to switch the thyristor on from a very large conduction delay angle, continuous gate drive should again be considered because of the mismatch of device latching and holding current levels even when conduction characteristics are matched by the manufacturer. In certain circuits, such as the three phase, double-way (bridge) circuit, a long gate pulse is necessary to insure conduction of load current through two thyristors whose principal voltage waves are phase displaced with respect to each other.

7.5 TRIGGERING

7.5.1 Gate Triggering Triode Thyristors

The triode thyristor is specifically designed to be triggered by means of a gate current signal of sufficient magnitude to turn on the device. The trigger voltage source should be designed to supply this gate current into the impedance exhibited by the device from gate terminal to reference terminal (usually cathode). The variation of gate trigger current and gate trigger voltage among devices of the same family are presented on the data sheets as a curve of gate voltage vs. gate current. The boundary lines of maximum gate impedance and minimum gate impedance on the characteristic curves represent the limits between which the gate characteristics of all devices of the same family lie. The gate characteristic diagram shows the locus of all possible triggering points of thyristors conforming to a certain specification and shows limits for the minimum dc triggering requirements which must be met to turn on all of these devices. When using very short duration trigger current pulses, the minimum magnitude required to trigger may be estimated from the dc gate trigger specifications using a constant charge approximation. Assume that the published dc current-to-trigger values are applicable for pulse durations down to about twenty microseconds. Then, for shorter trigger current pulse widths, scale up the current magnitude to produce the same charge as produced by the twenty microsecond trigger current pulse.

The gate trigger characteristics vary inversely with temperature. The lower the junction temperature, the more gate drive is required for triggering and conversely, the higher the junction temperature the less the gate drive required for triggering. For actual applications, the lowest operating temperature should be considered when determining the gate trigger requirements.

Related to the gate trigger characteristics is the maximum gate voltage that will not trigger the thyristor. This is a measure of the gate noise tolerance of the device and is dependent upon the junction temperature. The gate noise tolerance should be considered at the maximum rated junction temperature because the gate voltage to trigger is lowest at this temperature. Undesirable noise signals may be shunted around the gate terminal by an impedance from the gate to its reference terminal as long as undo attenuation of the gate trigger signal does not occur.

While the minimum gate triggering requirements are adequate to turn on the thyristor from a dc source, in many applications the gate should be overdriven by fast rising pulses to minimize and reduce variations in turn-on time. The magnitude of the trigger signal when overdriving the gate should not exceed the maximum allowable gate current and maximum peak and average gate

power dissipation ratings. Where reverse gate power is dissipated, the total gate power dissipation will be the sum of both the positive and negative average gate power losses. Also in the negative direction, the maximum gate ratings should be observed. Both positive and negative gate limits are given on the data sheets and they may indicate that protective devices such as voltage clamps and current limiters may be required in some applications.

The gate pulse width required to trigger a thyristor will depend upon the time required for the anode current to reach the latching value. It may be necessary to maintain a gate signal throughout the conduction period in applications where the load is so highly inductive that the time required to reach the latching level is very long and in applications where the anode current may swing below the holding value within the conduction period.

Further reasons for overdriving the gate may be found in 7.6.2 on di/dt capability, 7.3.3 on series voltage sharing and 7.4.6 on parallel current sharing.

7.5.2 Triggering Diode Thyristors

This type of device is triggered from an off-state to an on-state by exceeding the breakover voltage of the device. Sufficient current (called breakover current) must be available at the breakover voltage point to produce triggering. In this discussion, the breakover voltage should be considered as the maximum blocking voltage the device will sustain prior to switching and the breakover current the highest blocking current the device will sustain prior to switching. Generally, these points are coincident, but if they are not, the device user will have safe specifications from which to design triggering circuitry. It should be mentioned here that this device may also be triggered on by applying anode voltage at a rate which exceeds the critical rate of applied off-state voltage (dv/dt) limit of the device.

Generally, a pulse transformer is used to produce the high voltage necessary to trigger on a diode thyristor. Hence, the dynamic or pulse breakover current specification is needed by the circuit designer. If such values are not given on the device specification sheets, they may be obtained approximately from the static ($\geqslant$ 20 μs pulse width) breakover current specification as follows: Assume the static breakover current specification applies to a 20 μs triggering pulse. Then, for shorter pulse widths, maintain the trigger charge the same. That is, the area under the triggering current-time curve is to be held constant. The triggering current required on the low voltage (primary) side of the pulse transformer will be the particular required value of the device dynamic breakover current times the turns ratio of the step-up pulse transformer times a factor greater than one which accounts for the inefficiency of the pulse transformer. Faster device turn-on will generally result if the triggering voltage pulse is applied at a fast enough rate to produce some dv/dt triggering effect.

Thyristor breakover voltage is temperature dependent and will vary somewhat with the particular design of the device. Generally, starting at very low temperatures, breakover voltage will increase very slightly with temperature and then at fairly high temperatures the voltage will decrease. At quite high temperatures ($\geq$ 150°C) the decrease in breakover voltage with temperature can be quite sharp. On the other hand, breakover current will always decrease with increasing operating temperature.

7.6 SWITCHING

General

There are three distinct switching conditions which can occur with thyristors: 1) turn-on, 2) reverse recovery, and 3) turn-off (off-state recovery). As phenomena, these can be considered separately, though in many applications such as high frequency or pulse circuits, the three effects become inter-related.

7.6.1 Turn-On of Triode Thyristors

In applications such as radar pulse modulators, power supply crowbars, or control and alarm circuits, where the speed-of-response of the thyristor becomes a measure of performance, the gate controlled (t_{gt}) turn-on time may be reduced significantly by overdriving the gate with signals larger than the dc gate current which will just accomplish triggering (as specified by the manufacturer). Curves relating t_{gt} to the magnitude of the gate signal are generally available. Overdriving the gate by two to ten times the minimum signal level will usually accomplish most of the reduction in turn-on time possible and will reduce the variation in t_{gt} between thyristors of the same type and between subsequent pulses applied to the same unit (jitter). Increasing temperature and voltage will generally reduce the delay time interval, though not by an appreciable amount.

The rise-time portion of the total turn-on interval is affected strongly by the circuit conditions during turn-on. In higher voltage, lower current, noninductive circuits, the dynamic impedance of the thyristor is a small percentage of overall circuit impedance and the rise of current to the 90% point occurs more rapidly.

7.6.2 Rate-of-Rise of On-State Current in Triode Thyristors

At the end of the delay and rise time periods, as defined by the gate-controlled turn-on time, the thyristor will be in conduction through only a portion of its total available conduction area. A further interval is required for the current to spread from the initial area turned on, which is close to the gate, to the rest of the conduction area. During this time, the rate-of-rise of the on-state current should be kept within the critical rate of rise of on-state current (di/dt) rating of the device so that excessive localized heating of that portion of area which is in conduction will not be encountered. The di/dt ratings may be either repetitive or non-repetitive types and will therefore apply respectively to continuous operation or infrequent overload situations.

The use of a fast rising gate pulse of large magnitude will usually improve the thyristor's di/dt capability by increasing the area initially entering conduction. It should be emphasized that the specified conditions of the di/dt rating should include a gate current magnitude which generally will represent some overdriving of the gate beyond the minimum requirements for dc triggering. Turn on of the thyristor at other gate currents or by other mechanisms such as exceeding the breakover voltage or by dv/dt may result in a different di/dt capability.

After an appreciable on-state current is reached, the gate signal has little influence on the rate of current spreading to the remaining conduction area. In cases where di/dt stresses exceed the

device capability, linear or self-saturating reactors may be inserted in the circuit to lower di/dt or to delay the onset of the bulk of the load current until device current spreading is nearly complete.

Among the circuits which are very likely to produce di/dt problems are those where capacitors are being discharged. The capacitor discharge may be the prime function of the thyristor or it may be a secondary consideration, such as the discharge of a capacitor used for transient overvoltage protection. In any case, di/dt must be controlled by adequate impedance in the discharge loop.

However, even in such low frequency circuits as 60 Hz phase control applications, situations can arise where di/dt is beyond device capability. For example, in SCR circuits feeding inductive dc loads, the rate of current commutation from one phase to another in three phase systems is inversely proportional to the ac system impedance. Where such thyristor circuits are directly connected to an ac system of low short-circuit impedance, di/dt stresses in the thyristor when turning on should be considered. This kind of problem may be encountered more often in large ac/dc power conversion equipments since di/dt capability is not generally proportional to the current rating of the thyristor.

7.6.3 Turn-On Dissipation

Apart from the limitations of di/dt ratings, the power dissipation during turn-on may become a limiting factor in the high frequency performance of a thyristor. As switching frequency increases, turn-on losses may become large compared to on-state losses. This may necessitate operation at lower than rated 60 Hz current or reduction of turn-on losses by control of di/dt.

7.6.4 Reverse Recovery

In switching from the on-state to reverse blocking, a large initial reverse current will flow through a reverse blocking thyristor. The rate of rise of this current is determined only by the external circuit. After a short interval, less than a few microseconds, the thyristor will become able to block reverse voltage and the reverse current will decay to the normal blocking level. The magnitude of the reverse recovery current may be large enough to warrant consideration in determining the rating of other circuit components which supply this current, particularly with respect to turn-on dissipation in another thyristor. In addition, the decay of the peak reverse recovery current may be abrupt enough to generate large transient overvoltages in inductive circuit components feeding this current. Such overvoltages may be controlled in a variety of ways, the simplest of which is often the use of capacitor in parallel with the thyristor of sufficient size to accept the stored inductive energy from the circuit without excessive voltage rise. This capacitor should have a resistor in series to limit turn-on dissipation in the thyristor when it is switched on again.

7.6.5 Turn-Off

The turn-off time of a thyristor describes the minimum interval of time after the end of conduction of on-state current before off-state voltage can be reapplied without the device turning on. If adequate turn-off time is not provided and the thyristor inadvertently switches to the on-state when off-state voltage is reapplied, this is not in itself damaging to the device. The circuit action resulting from failure to turn off may produce undesirable effects, however, such as high dc fault currents which may exceed the device capability. In dc switching circuits such as

inverters and switching regulators, the magnitude of the turn-off time which must be provided for the thyristor directly influences the upper limit of operating frequency, and the size of the commutating components which provide for turn-off.

Factors causing an increase in turn-off time are: high junction temperature, high forward current prior to turn-off, rapid reduction of forward conduction to zero, limited reverse recovery current, low reverse blocking voltage, a fast rate of rise of voltage from reverse blocking to off-state, and a large magnitude of off-state voltage. Thyristors which are optimized for fast turn-off are available and are generally less sensitive to the above conditions, than are normal designs. It should be noted that turn-on dissipation may influence turn-off time in two ways. First, the rate of decay of turn-on-induced hot spot temperatures in silicon material is generally slow compared to the interval between turn-on and turn-off in circuits above a few kilohertz. Therefore, some portions of the device may not turn off under high frequency operation. Secondly, turn-on dissipation may, at high frequencies, increase the average power loss appreciably and therefore raise the average junction temperature, leading to increased device turn-off time.

Conservative design practice should provide some safety factor in circuit turn-off interval beyond the device turn-off time rating to allow for abnormal circuit operating conditions, such as greater than normal supply voltage and load magnitude, high current during start-up conditions, etc. It should be recognized that the numerous circuit influences on turn-off time may differ in an operating circuit from those used in manufacturer's specification of turn-off time.

7.7 FUNDAMENTAL THYRISTOR CIRCUITS

The circuits shown in the tables listed are presented only as an aid in understanding the application of reverse blocking thyristors in various circuits. The calculations shown are theoretical and based on undistorted input waveforms, no power loss in the semiconductor devices and no reactance or losses in the transformers or associated heads.

The reader may find these circuit tables useful in approximating the values of circuit voltages and currents but must also consider transformer and lead impedances, semiconductor device losses, voltage transients, surge current conditions, etc., for proper circuit design.

The following symbols apply to the circuits listed in the figures below:

E_ℓ – RMS line voltage – volts

E_D – Average load voltage – volts

E_A – RMS load voltage – volts

F.F. – Form factor – ratio of rms load voltage to average load voltage

I_D – Average load current – amperes

TABLE 1 – FUNDAMENTAL CIRCUIT VALUES – SINGLE PHASE, HALF WAVE, RESISTIVE LOAD

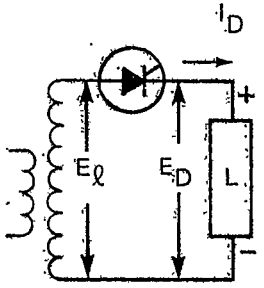
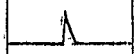
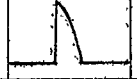
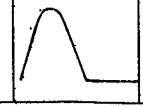
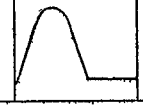
Circuit Diagram	Conduction Angle	Output Wave Values					Thyristor Wave Values						Transformer VA Capacity	
		Voltage Wave Form	E_D	E_A	F.F.	Ripple Current %	Current Wave Form	I_T (AV)	I_T (AV)	I_t (rms)	V_{DM}	V_{RM}	Pri	Sec
	30°		.030 E_ℓ	.120 E_ℓ	3.99	387		.0426 I_{TM}	1.00 I_D	3.99 I_D	1.41 E_ℓ	1.41 E_ℓ	133 $E_D I_D$	133 $E_D I_D$
	60°		.109 E_ℓ	.302 E_ℓ	2.78	258		.092 I_{TM}	1.00 I_D	2.78 I_D	1.41 E_ℓ	1.41 E_ℓ	25.5 $E_D I_D$	25.5 $E_D I_D$
	90°		.225 E_ℓ	.508 E_ℓ	2.26	202		.159 I_{TM}	1.00 I_D	2.26 I_D	1.41 E_ℓ	1.41 E_ℓ	10.0 $E_D I_D$	10.0 $E_D I_D$
	120°		.338 E_ℓ	.635 E_ℓ	1.88	159		.239 I_{TM}	1.00 I_D	1.88 I_D	1.22 E_ℓ	1.41 E_ℓ	5.56 $E_D I_D$	5.56 $E_D I_D$
	150°		.420 E_ℓ	.698 E_ℓ	1.66	133		.297 I_{TM}	1.00 I_D	1.66 I_D	.71 E_ℓ	1.41 E_ℓ	3.96 $E_D I_D$	3.96 $E_D I_D$
	180°		.450 E_ℓ	.707 E_ℓ	1.57	121		.318 I_{TM}	1.00 I_D	1.57 I_D	0	1.41 E_ℓ	3.49 $E_D I_D$	3.49 $E_D I_D$

TABLE 2 – FUNDAMENTAL CIRCUIT VALUES – SINGLE PHASE, FULL WAVE, RESISTIVE LOAD

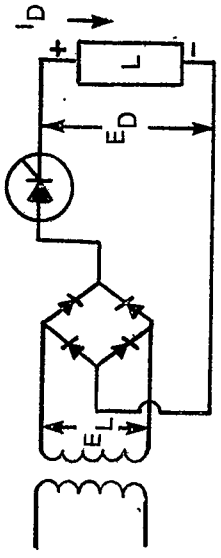
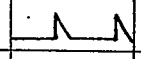
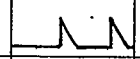
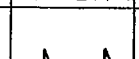
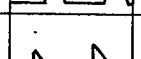
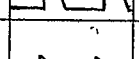
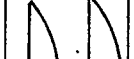
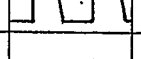
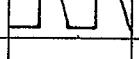
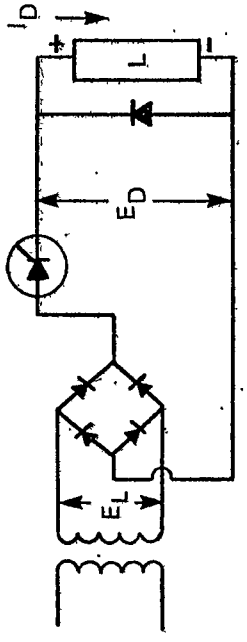
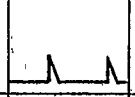
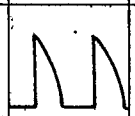
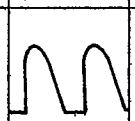
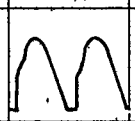
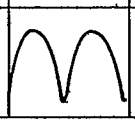
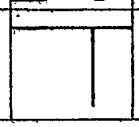
Circuit Diagram	Conduction Angle	Output Wave Values						Thyristor Wave Values					Transformer VA Capacity	
		Voltage Wave Form	E_D	E_A	F.F.	Ripple Current %	Current Wave Form	I_T (AV)	I_T (AV)	I_t (rms)	V_{DM}	V_{RM}	Pri	Sec
	60°		.060 E_ℓ	.170 E_ℓ	2.82	265		.095 I_{TM}	1.00 I_D	2.82 I_D	1.41 E_ℓ	0	47 E_DI_D	47 E_DI_D
	120°		.218 E_ℓ	.427 E_ℓ	1.97	170		.184 I_{TM}	1.00 I_D	1.97 I_D	1.41 E_ℓ	0	9.05 E_DI_D	9.05 E_DI_D
	180°		.450 E_ℓ	.720 E_ℓ	1.57	124		.318 I_{TM}	1.00 I_D	1.57 I_D	1.41 E_ℓ	0	3.49 E_DI_D	3.49 E_DI_D
	240°		.676 E_ℓ	.900 E_ℓ	1.20	88		.578 I_{TM}	1.00 I_D	1.20 I_D	1.22 E_ℓ	0	1.77 E_DI_D	1.77 E_DI_D
	300°		.840 E_ℓ	.988 E_ℓ	1.17	62		.594 I_{TM}	1.00 I_D	1.17 I_D	.71 E_ℓ	0	1.39 E_DI_D	1.39 E_DI_D
	360°		.900 E_ℓ	1.000 E_ℓ	1.11	48.5		.636 I_{TM}	1.00 I_D	1.11 I_D	0	0	1.23 E_DI_D	1.23 E_DI_D

TABLE 3 – FUNDAMENTAL CIRCUIT VALUES – SINGLE PHASE, FULL WAVE, INDUCTIVE LOAD

Circuit Diagram	Conduction Angle	Output Wave Values					Thyristor Wave Values						Transformer VA Capacity	
		Voltage Wave Form	E_D	E_A	F.F.	Ripple Current %	Current Wave Form	I_T (AV)	I_T (AV)	I_t (rms)	V_{DM}	V_{RM}	Pri	Sec
	60°		0.60 E_ℓ	1.70 E_ℓ	2.82			.167 I_{TM}	1.00 I_D	2.45 I_D	1.41 E_ℓ	0	6.7 E_DI_D	6.7 E_DI_D
	120°		.218 E_ℓ	.427 E_ℓ	1.97			.333 I_{TM}	1.00 I_D	1.73 I_D	1.41 E_ℓ	0	2.68 E_DI_D	2.68 E_DI_D
	180°		.450 E_ℓ	.720 E_ℓ	1.57			.500 I_{TM}	1.00 I_D	1.41 I_D	1.41 E_ℓ	0	1.57 E_DI_D	1.57 E_DI_D
	240°		.676 E_ℓ	.900 E_ℓ	1.20			.667 I_{TM}	1.00 I_D	1.22 I_D	1.22 E_ℓ	0	1.21 E_DI_D	1.21 E_DI_D
	300°		.840 E_ℓ	.988 E_ℓ	1.17			.883 I_{TM}	1.00 I_D	1.11 I_D	.71 E_ℓ	0	1.07 E_DI_D	1.07 E_DI_D
	360°		.9 E_ℓ	1.0 E_ℓ	1.11			1.00 I_{TM}	1.00 I_D	1.00 I_D	0	0	1.11 E_DI_D	1.11 E_DI_D

7.8 HEAT DISSIPATOR CONSIDERATIONS

7.8.1 General

In order to achieve the full current carrying capability of stud- or base-mounted thyristors, it is required that they be attached to heat dissipators (heat sinks). Exceptions to this are those thyristors which are lead-mounted or possess large integral heat dissipators. These types of devices have their current ratings referred to ambient temperature. Of course, these types of thyristors may also be assigned current ratings based upon their case temperatures.

7.8.2 Attachment of Stud-Mounted Thyristors to Heat Dissipators

7.8.2.1 Consideration When Using Aluminum Heat Dissipators

Galvanic action between the aluminum and copper (if plating has been scored) can occur and impede the heat flow. Therefore, grease having corrosion inhibiting properties should be applied to the contact surfaces. Moreover, the unequal temperature coefficients of aluminum and copper can cause the mounting to gradually loosen as the assembly is cycled through temperature extremes. A spring washer on the reverse side of the fin minimizes this effect by allowing the aluminum to expand against the washer compression rather than the copper.

7.8.2.2 Hole and Surface Preparation

When thyristors possessing studs with machine threads are mounted through a clearance hole, optimum heat transfer depends on adequate contact between the thyristor base and heat dissipator surfaces. Care should be taken, therefore, to insure a clean flat area for contact, free of ridges or high spots, burrs, etc. The base surface itself should be checked for removal of all burrs or peened over corners that may have occurred during previous handling.

7.8.2.3 Lubrication of Contact Surfaces

Any practical thermal joint will have trapped air pockets in the inevitable depressions and voids between the surfaces. Since air is a relatively poor thermal conductor, the heat transfer can be improved by applying a thin layer of silicone grease or similar joint compound to the thermal contact surfaces before joining. Bulked greases may impair heat transfer as the bulk material may interfere with intimate contact of the mating surfaces.

7.8.2.4 Mounting Torque

Good thermal contact between the base of the thyristor and the heat dissipator requires adequate pressure between the two contact surfaces. This is produced by torque on the threads of the device. However, a torque beyond a certain point no longer improves the thermal contact and may mechanically stress the semiconductor crystal and associated materials inside the housing. For this reason, precise adherence to the manufacturer's torque recommendation is necessary, and this should be verified by using a torque wrench.

The torques specified for lubricated and non-lubricated stud threads may be different; the device manufacturer's recommendation on mounting torque should be followed.

7.9 TEMPERATURE MEASUREMENTS

7.9.1 General

Thermal measurements of thyristors are direct measurements of ambient and/or surface temperatures or indirect measurements of internal temperatures. Since the temperature rise of components above ambient temperatures will depend upon parameters such as dissipated power, air velocity, altitude, and ambient temperature, an arbitrary choice of these parameters may be made to provide the necessary standardization between the user's and the manufacturer's testing procedures. Correlation between these tests and specific equipment tests is the responsibility of the user.

Acceptable methods of temperature measurement such as thermocouples, thermometers, pyrometers, temperature-sensitive resistors, and temperature-sensitive paints may be used. Where specific temperatures may be measured accurately only with specific methods, these methods will be specified.

NOTE: For further details covering procedures and instruments for temperature measurements, refer to 7.9.5.2 and 7.9.5.3 and to the IEEE Master Test Code for Temperature Measurement of Electric Apparatus, Publication No. 551.

7.9.2 Ambient Temperature

Ambient temperature, as herein used, is the temperature of the medium used for cooling the thyristor.

1. Natural-Air Cooling Systems (Natural convection cooling) — The ambient temperature is the temperature of the air immediately below the thyristor when operating under specified conditions.

2. Forced-Air Cooling Systems (Forced convection cooling) — The ambient temperature is the temperature of the air immediately before its entry into the vicinity of the thyristor.

3. Cooling Medium Other Than Air — The manufacturer should be consulted for his recommendation.

7.9.3 Thyristor Temperatures

7.9.3.1 General

Since a thyristor consists of a multi-junction semiconductor material enclosed in a housing, direct measurement of junction temperature is not possible. Ambient temperature, heat dissipator temperature, or case temperature may be measured directly.

7.9.3.2 Thyristor Junction Temperature

The effective temperature rise of the thyristor junction above a stated external reference point may be obtained from the product of the effective thermal resistance, junction to reference, and the total power loss of the thyristor.

If the on-state current of the thyristor is pulsating, the junction temperature may fluctuate as shown in Figure 7.1. Because of the low thermal capacity of the semiconductor material, calculation of peak or some instantaneous junction temperature may require the use of transient thermal response characteristics.

The average junction temperature rise as shown in Figure 7.1 may be calculated by multiplying average power loss by the value of effective thermal resistance for direct current. (The value usually given on manufacturer's data sheets.)

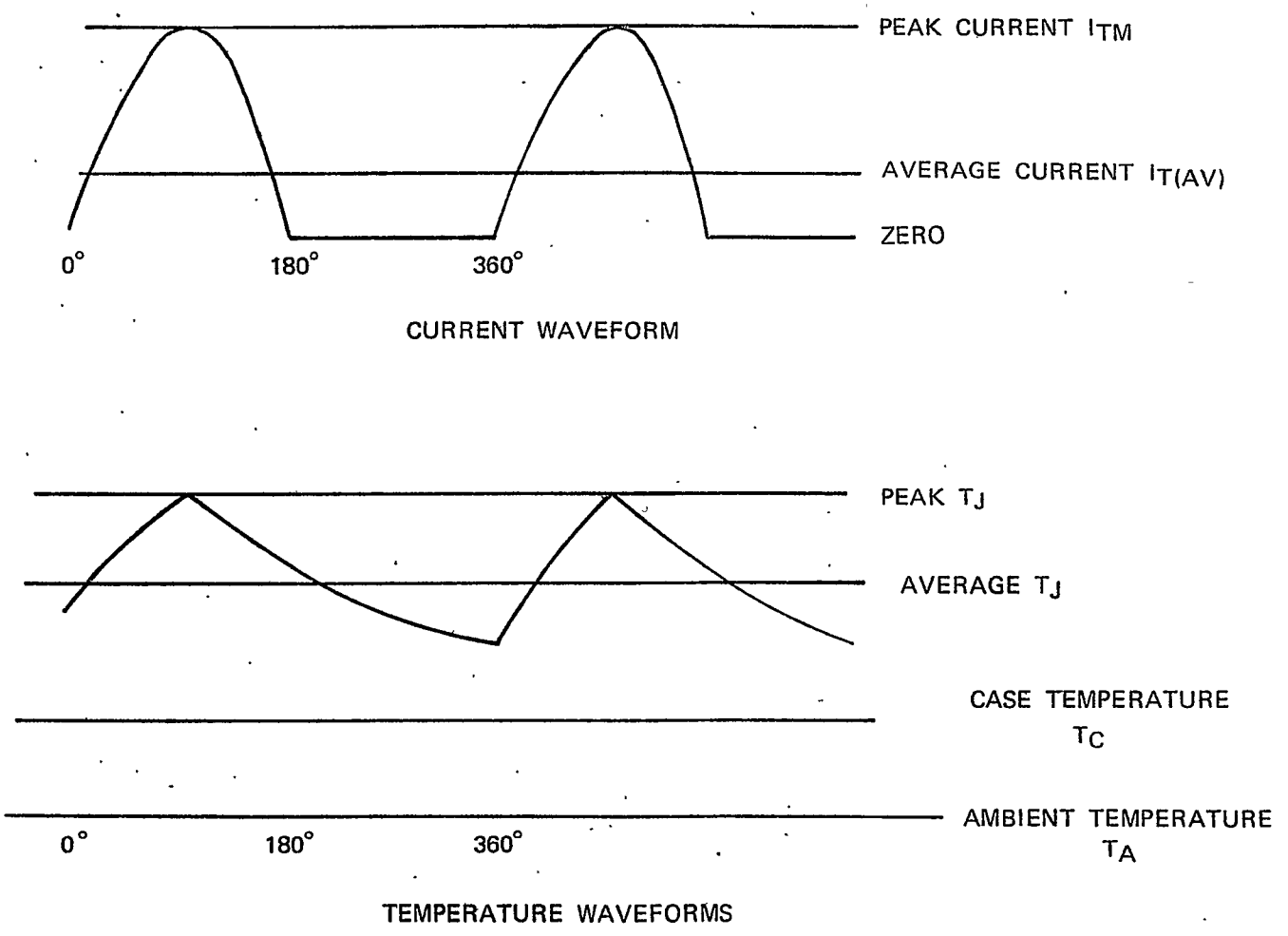


FIGURE 7.1 – TYPICAL ON-STATE CURRENT AND CORRESPONDING JUNCTION AND CASE TEMPERATURE WAVEFORMS IN A HALF-WAVE AC CIRCUIT

If an effective thermal resistance for some other specified waveform (single phase, three phase, etc.) is given, the product of this value and the average power loss for the particular current waveform will give the peak junction temperature.

7.9.3.3 Case Temperature

The case temperature of a stud-mounted, hexagonal base thyristor is measured at the center of any flat on the hex. The case temperature of other base-mounted thyristors is measured at a point specified by the manufacturer. The recommended case temperature test method employs the use of thermocouples and is defined as follows:

1. *Type of Thermocouple* – The thermocouple material shall be copper-constantan as recommended by the Standard Handbook for Electrical Engineers (A.E. Knowlton, 9th Edition, 1957, Section 3-325, page 195) for the range of –190C to 350C. The wire size shall be no larger than #30 Awg. The junction of the thermocouple shall be welded together to form a bead rather than soldered or twisted.

2. *Mounting Method* – A small hole, just large enough to insert the thermocouple, shall be drilled approximately 1/32 inch deep in the flat of the case hex at the point specified by the manufacturer. The edge of the hole should then be peened with a small center punch to force a rigid mechanical contact with the welded bead of the thermocouple. If forced-air cooling is used, the thermocouple shall be mounted away from the air stream, and the thermocouple leads close to the junction shall be shielded.

3. *Accuracy* – An accuracy of plus or minus 1/2°C should be expected of the thermocouple. Under load condition, slight variations in the temperature of different points on the case may reduce this accuracy to plus or minus 1.0°C for free convection cooling, and plus or minus 2.0°C for forced-air cooling.

4. *Other Methods of Mounting* – Other methods of mounting thermocouples, with the possible exception of the thermocouple welded directly to the case, will result in temperature readings lower than the actual temperature. These deviations will result from:

   a. Inadequate contact with the case when using cemented thermocouples.

   b. External heat dissipator in contact with the thermocouple when using pressure contacts.

7.9.4 Temperature Measurements Involving Thyristors Mounted on Heat Dissipators

7.9.4.1 Free-Air Convection Measurements

The heat dissipator should be suspended vertically in a cubic enclosure whose dimensions are a minimum of four times the dissipator height. The enclosure should be so designed that the inside walls are insulated from ambient, i.e., they are substantially at the inside ambient temperature. See Figure 7.2.

The ambient temperature should be measured by means of a thermocouple mounted at a distance 1/4 the dissipator height directly below the center of the bottom of the heat dissipator.

The heat dissipator temperature should be measured by means of a peened thermocouple attachment to the dissipator at a radius of 1/4 inch greater than the maximum thyristor base radius.

The case temperature of the thyristor should be measured by means of a peened thermocouple attachment to the center of one of the flats on the hex base where a copper-base device is used, or to a point on the base specified by a manufacturer if another type of base is used. Care should be exercised in installing thermocouples so that the thyristors are not damaged.

7.9.4.2 Forced-Air Convection Measurements

The heat dissipator, oriented parallel to the air stream, should be rigidly fastened inside a rectangular duct which has a width 1 inch or 25% (whichever is smaller) greater than the dissipator width and a height 1 inch or 25% (whichever is smaller) greater than the distance measured from the bottom of the dissipator to the top of the dissipator. Any additional parts of the thyristor and/or test lead may protrude through a sealed hold in the duct or out of the duct as shown in Figure 7.3. The dissipator should be supported by the mounting brackets, using insulating material. Mounting brackets and high current leads should not cover more than 2% of the duct cross section area. The length of the duct, from air input end to air exhaust end, should be seven times the dissipator length. The inside duct walls should have a smooth surface. The dissipator should be located in the duct so that its leading edge is four fin lengths downstream from the air input end of the duct.

The air velocity should be measured one dissipator width upstream from its leading edge. The recommended test air velocity will be considered the average of all point velocities over the air stream cross section. The dissipator air pressure drop should be measured between one dissipator length upstream from its leading edge and one length downstream from its trailing edge.

The ambient temperature should be measured one dissipator length upstream from its leading edge by means of a thermometer or thermocouple.

The dissipator temperature should be measured by means of a peened thermocouple attachment to the dissipator at a radius of 1/4 inch greater than the maximum thyristor base radius. This measurement point should also be located on the dissipator centerline parallel to the air flow and on the downstream side of the thyristor.

The case temperature of the thyristor should be measured by means of a peened thermocouple attachment to the center of one of the flats on the hex base where a copper-base device is used, or to a point on the base specified by the manufacturer if another type base is used. The thermocouple connection to the thyristor base should be on the downstream side of the thyristor. Care should be exercised in installing thermocouples so that the thyristors are not damaged.

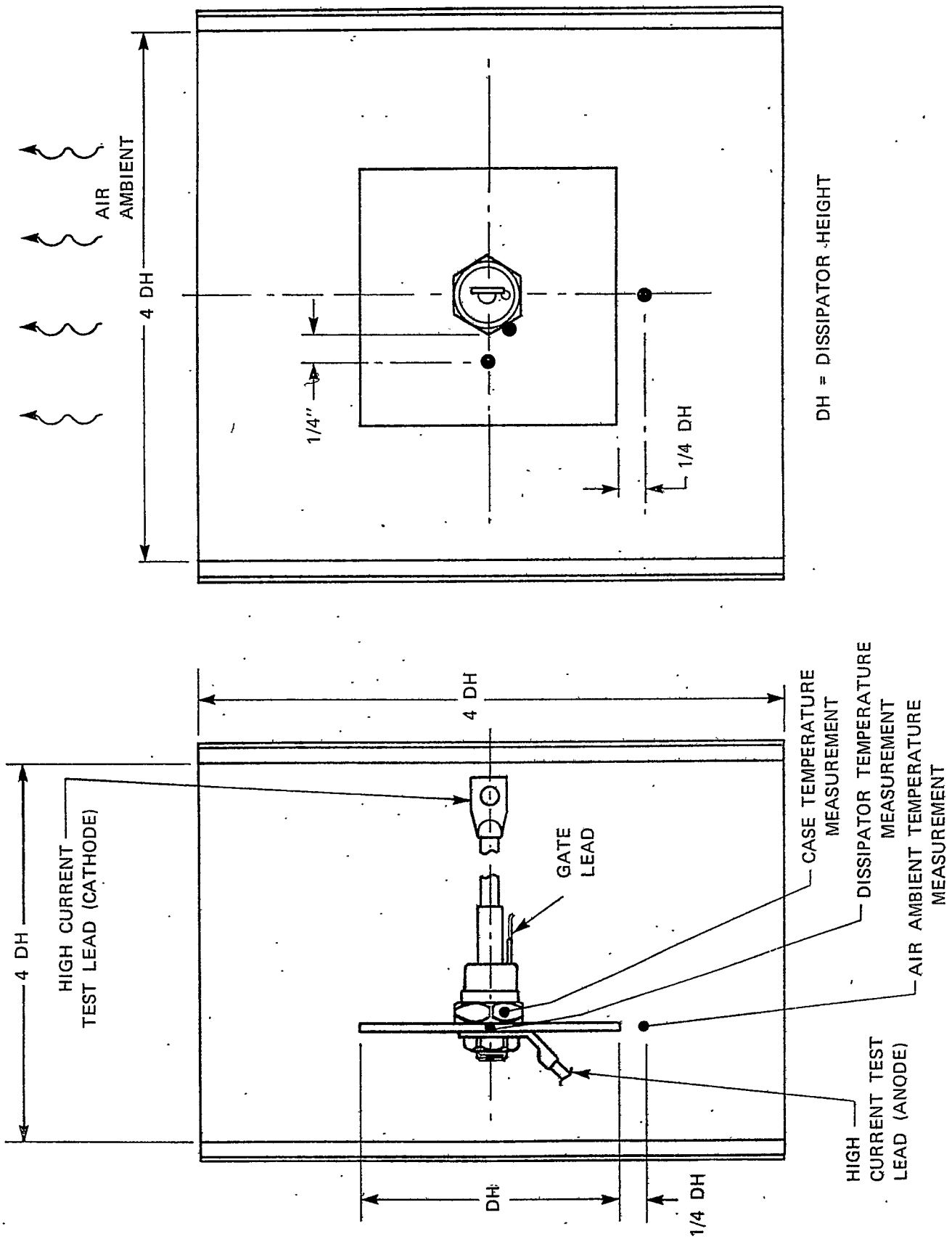


FIGURE 7.2 – FREE-AIR CONVECTION MEASUREMENT

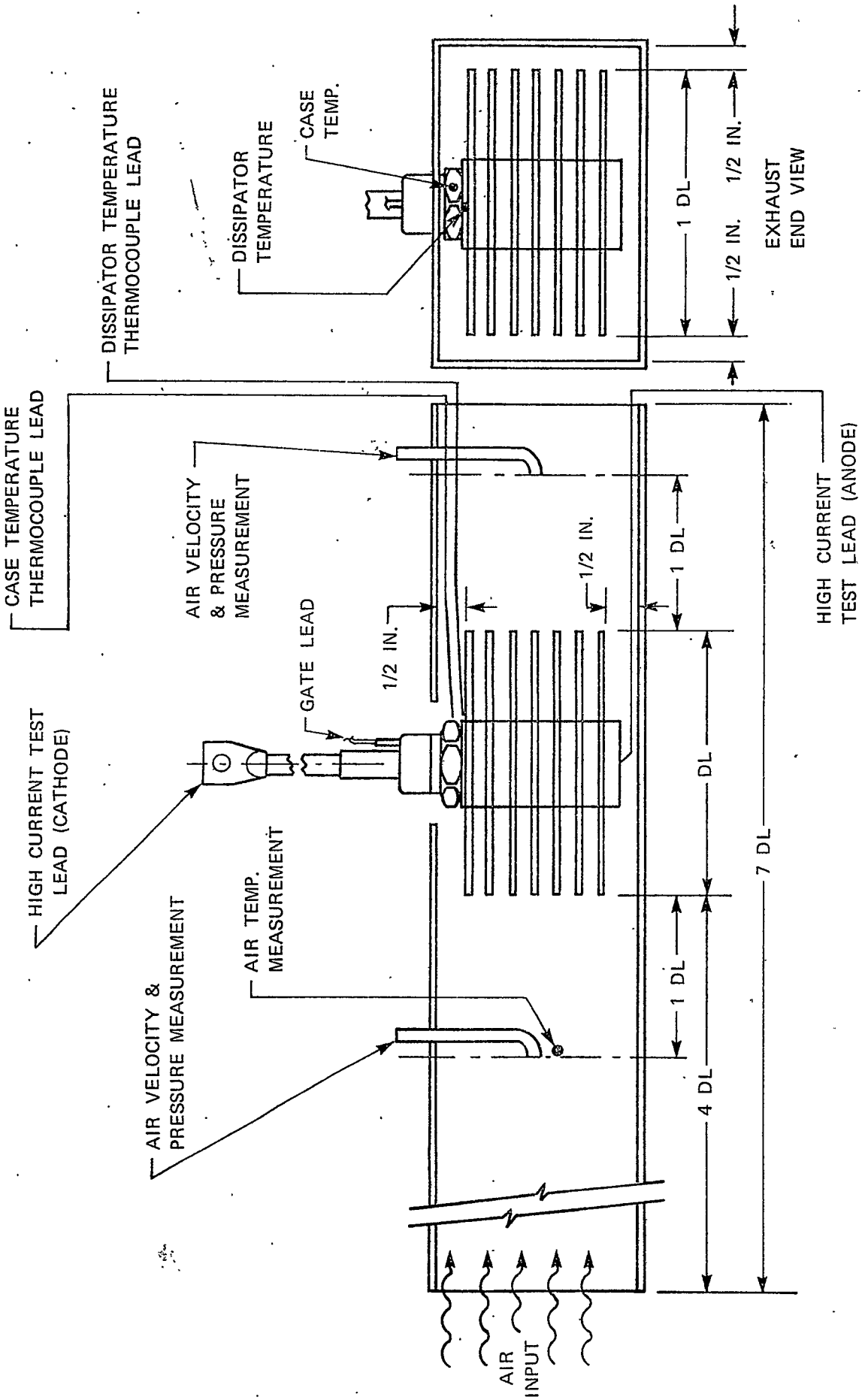


FIGURE 7.3 – FORCED CONVECTION MEASUREMENT DL = DISSIPATOR LENGTH

7.9.5 User Temperature Measurement Methods

7.9.5.1 General

The thermocouple temperature measuring method given in 7.9.3.3 is the most accurate method for measuring surface temperatures. However, in an actual field application, a faster, less accurate method may be more desirable.

7.9.5.2 Typical Methods of Temperature Measurement

1. A thermocouple cemented or peened to the case or heat sink of the thyristor.

2. A hand pyrometer such as the Type 4100 manufactured by Alnor.

3. Temperature-sensitive paint such as Tempilaq or, in the solid form, such as Tempilsticks.

7.9.5.3 Comments and Limitations of Each Method

1. Thermocouples

   a. Most accurate method.

   b. Permits measurements in closed cubicles.

   c. Most time consuming.

   d. Care must be taken to insure solid contact of the thermocouple on the surface of the component.

   3. Thermocouple leads must be shielded in forced drafts.

2. Hand Pyrometer

   a. Accurate within 5 to 8 percent.

   b. Component must be accessible during measurements.

   c. Quick and simple technique.

   d. Adaptable to measurements on only the larger hex base thyristors and heat dissipators.

   e. Hazard. Use with care so that the metal parts of the pyrometer do not ground or short any part of circuit.

3. Temperature Sensitive Paint

   a. Accurate within plus or minus one percent.

   b. Component must be visible and accessible.

   c. Quick and simple technique.

   d. Adaptable to all devices regardless of size.

   e. Will measure only specific temperatures.

7.10 THYRISTOR FAILURE MODES

7.10.1 General

Thyristor failures may be broadly classified as either catastrophic or degradation failures. Catastrophic failure occurs when a device exhibits a sudden change in characteristic which renders it inoperable. A degradation failure is generally a failure by definition because it is the result of a defined change in some characteristic. The device may still function satisfactorily in the circuit.

7.10.2 Catastrophic Failure

Catastrophic failure can occur whenever the thyristor is operated beyond its published ratings or it contains an unknown fabrication defect. This type of failure generally results in an electrical short between principal terminals. However, if the resulting short-circuit current is high enough, device internal parts may melt and thus render the device an open circuit.

Generally, it is over voltage or over current operation that produces catastrophic failures. Over voltage failures may be due to excessive circuit transient voltages which were not accounted for in the circuit design. Voltage failure may also occur if inadequate device cooling raises the operating junction temperature above rated value and thereby invalidates the steady state voltage rating of the thyristor. Over current catastrophic failures are generally caused by improper fusing or circuit protection coordination in the event of a circuit fault condition. Of course, rough handling during the installation of thyristors into equipment can mechanically damage the devices to the extent that they fail catastrophically as soon as electric power is applied. Excessive device mounting torque and excessive force applied to the insulated terminals or leads are two common causes of physical damage to thyristors.

7.10.3 Degradation Failures

Any significant degradation of thyristor on-state, gate or switching characteristics is quite rare. The characteristics most vulnerable to degradation are the reverse blocking and off-state voltage characteristics. This effect is outside the control of the user, assuming that the device is operated at all times within all of its maximum ratings. It should be pointed out however, that this type of degradation increases with increasing operating voltage and temperature levels. Hence, the user

can reduce the possibility of blocking voltage degradation effects by operating beneath the maximum temperature and/or voltage ratings of the device. Thus, the probability of long thyristor operating life can be increased simply by using heat sinks which are somewhat oversized and selecting thyristors of a voltage grade somewhat in excess of the actual maximum circuit voltage.

7.11 RADIO FREQUENCY INTERFERENCE (RFI)

As with all fast switching devices, thyristors with their rapid turn-on capability can shock excite the circuits in which they are used. Such shock excitation of power distribution lines many times produces voltage oscillations in the radio frequency range. This radio frequency energy may be radiated, or circuit conducted, from its source; and if of sufficient magnitude, it can interfere with the operation of other electrical (especially communications) equipment. Various military specifications have been issued which define acceptable RFI generation levels for various types of military equipment. Test procedures are also given in these specifications.

Since it is the fast switching that produces RFI problems, the addition of any inductance to the load will work toward reducing RFI. To minimize radiated RFI, the best approach is to use electrostatic shielding with the shield connected to a solid RF ground. To minimize conducted RFI the best approach is to isolate the thyristor from the rest of the circuit with series inductors. These inductors may be of the saturating type since they are needed only during the switch-on interval. If a good RF ground is available, a capacitor connected to this ground in an "L" filter is effective in suppressing conducted RFI.

RFI, if of sufficient magnitude, can adversely affect the operation of other thyristors in a system in two ways:

1. If the RFI finds its way into the thyristor anode circuit, the high dv/dt can trigger the device. Thus, R-C suppression may have to be used across the thyristor to prevent dv/dt triggering. Incidentally, negative gate bias is effective with many thyristors for increasing dv/dt withstand capability sufficiently to overcome the spurious triggering problem.

2. If RFI gets into the gate circuit, the thyristor again can be triggered on. In this case, the gate circuit must be adequately decoupled.

7.12 SIMPLE MEASUREMENTS IN TROUBLE SHOOTING

7.12.1 Off-State and Reverse Blocking Voltage Checks

An ohmmeter may be used to determine if a thyristor is shorted in either the off-state or reverse direction. Disconnect the gate and cathode terminals from the circuit and then measure the device resistance in both directions. Use the highest resistance range of the ohmmeter to assure that the driving voltage is greater than several volts. Resistance readings will range from 10 kilohms to greater than 1 megohm depending upon the particular device blocking characteristics.

The ohmmeter test will not determine whether the thyristor blocking characteristics have degraded. There may be times when it is believed that the thyristor has been over-stressed and

thus there is some doubt as to whether it will block rated voltage. In this case, rated dc voltage should be applied to the device (starting at zero volts) through a suitable resistor and dc milliammeter. The thyristor specification sheets should be consulted for typical values of room temperature blocking current at rated dc voltage. The supply voltage used in this test and the series resistor and ammeter should be chosen so that if the thyristor breaks over during the blocking voltage test, the resistor will limit the current to the full scale value of the milliammeter. Thus, blocking current will be read low on the milliammeter scale, but no particular accuracy is required in this test. The dc supply should be free of voltage transients.

7.12.2 Gate Trigger Check

To determine whether the gate of a triode thyristor is operational, the following check may be used. Apply about 6V dc, through a suitable resistance, from anode to cathode of the device, anode positive with respect to cathode. Then connect a low dc voltage source (3 to 6V dc) through a suitable series resistance between gate and reference terminal. The thyristor should trigger on. Turn-on may be detected by monitoring the voltage across the anode circuit resistor. The manufacturer's specification sheets may be consulted to calculate a suitable value of anode circuit resistance to limit device current to about 10% of rated value, and to determine suitable values of gate supply voltage and source resistance.

The simple tests mentioned above will generally determine whether a thyristor is operational. The comments also apply to bidirectional thyristors for both operating quadrants. If precise device rating or characteristic information is required, refer to the test information given in Parts 5 and 6 of this publication.

PART 8

MILITARY SPECIFICATIONS

INDEX

APPENDIX I

MILITARY SPECIFICATIONS

8.1 PURPOSE AND STRUCTURE

Military specifications are prepared as procurement documents to describe various items purchased by the United States Government. Semiconductors are covered under Military Specification, MIL-S-19500, "Semiconductor Devices, General Specification for." This document contains the general requirements and provisions for such things as materials, marking, formation of lots, qualification provisions, quality conformance inspection requirements, preparation for delivery, etc., which are applicable to all types of semiconductors. It also references other specifications and standards which are applicable such as MIL-STD-750, MIL-S-19491, MIL-STD-105, etc. These are considered to be a part of the specification to the extent specified, which may be the entire document or a single provision such as a particular test method taken from MIL-STD-202.

Particular semiconductor device types are covered by detail specifications prepared under and referencing MIL-S-19500. These detail specifications bear a MIL-S-19500/XXX number and the device types covered are shown in the title. The body of these specifications completely describes the device in terms of its mechanical and electrical characteristics and ratings, and its quality and reliability test requirements. Also, any necessary exceptions to the general specification are taken in the detail specification. A periodic supplement to MIL-S-19500 is available which lists the detail device specifications which have been issued and have remained in active status.

8.2 OTHER SPECIFICATIONS

In addition to those mentioned above which apply only to products, a particular procurement contract or customer order may invoke the requirements of any of several other general Government specifications issued by the DoD agencies.

One of particular importance is MIL-Q-9858A, "Quality Program Requirements." This requires that the contractor establish and maintain a completely documented Quality Control System including control of design, changes, manufacturing processes, product test and shipping. Another is MIL-I-45208, "Inspection System Requirements." A Government Representative will usually conduct a survey before permitting shipment against a contract which requires compliance to MIL-Q-9858A or MIL-I-45208.

8.3 MILITARY STANDARDS

A number of standards may be referred to in military specifications. These are general-purpose descriptions of requirements or testing procedures which are applicable to many classes or types of items; as such, they refer the detailed requirements to the detailed specifications for the particular item. These standards serve these dual purposes:

1. Reduce the amount of repetitious printing which would be required if all of the procurement information about an item were included in each detail specification.

2. Standardize test methods and equipment, material requirements, etc., in the interests of economy and of interchangeability of items supplied by different manufacturers.

8.4 PREPARATION, REVISION AND COORDINATION

MIL-S-19500 and referenced documents are revised or amended as required to incorporate new concepts and to accomplish necessary changes. The formal revision is handled at a joint meeting of the Military Services with invited members of the supplier and user industry present. Suggestions and comments from industry associations such as EIA are given due consideration during these meetings; however, the Services reserve the authority to make all final decisions. Revision of specifications is indicated by a suffix letter, e.g., MIL-S-19500E, where E is the revision letter. Unless called out otherwise, it is understood that reference to MIL-S-19500 or other document, means the latest revision.

8.5 MILITARY PREPARING ACTIVITIES

Naval Electronics System Command
Washington, D.C. 20360
Attn: Code 05143, Mr. C. E. Suman

U. S. Army Electronics Command
Fort Monmouth, New Jersey 07703
Attn: AMSEL-PP-EM-2, Mr. J. Deisler

Rome Air Development Center
Griffiss Air Force Base
Rome, New York 13442
Attn: EMNRB, Mr. E. J. Wojnas

Defense Electronics Supply Center
Dayton, Ohio 45401
Attn: DESC-ECS, Mr. N. A. Hauck

Note: DESC acts as Preparing Activity when requested.

Each of the above agencies issues specifications for the use of its Service. When they are issued without formal review and concurrence by the other Services, they are referred to as "single service" or limited coordination (LC) specifications, and may be recognized as such by a parenthetical designation following the slash number such as (NAVY), (EL), or (USAF) to indicate Navy, Army, or Air Force respectively.

When devices specified in LC specifications are found to be of interest to the other Services, the specification is formally reviewed and concurrence for use by all Services is reached. The document is then revised and considered to be coordinated and the parenthetical service designator is dropped.

8.6 QUALIFIED PRODUCTS

The "JAN" brand is registered as a U.S. Government certification mark as number 504860 by the U.S. patent office.

Before a manufacturer may sell products which bear the military JAN brand, he must meet the qualification requirements of the general specification and the applicable detail specification and be approved for listing on the QPL (see Section 8.9). Qualification approval is granted by the Qualifying Activity mentioned in the specification after the necessary tests have been successfully conducted and reported.

8.7 QUALIFICATION APPROVAL

The procedure for obtaining qualification approval is detailed in "Provisions Governing Qualification" and in DESC publication "Qualification Information for Manufacturers." It is essential that any manufacturer who expects to offer qualified products for sale be familiar with these qualification procedures, and that he obtain copies of all pertinent specifications including amendments and referenced documents before initiating testing.

The test facilities that the manufacturer desires to use for qualification testing must be approved by the Qualifying Activity. These facilities may be either in the manufacturer's plant or in a commercial laboratory. If the facilities have not been previously found suitable for qualification testing, a list of test facilities and other information about the laboratory must be sent to the Qualifying Activity prior to a survey of the facilities. The time involved may vary considerably depending on the completeness of the information furnished, availability of qualifying activity personnel to conduct a facilities survey, etc.

A manufacturer who desires to qualify a product requests authorization to conduct qualifying tests by submitting the appropriate forms. He receives authorization to conduct the test a short time later. Qualification inspection involves testing specific samples of units in accordance with procedures of the agency involved and under cognizance of a government inspector. A maximum number of allowed defectives is prescribed; excessive failures at this point are a serious setback. Under best possible conditions, testing requires at least six weeks because of 1000-hour life tests. When the testing has been completed, the manufacturer makes a detailed report of test results to the cognizant agency. If he has experienced trouble, he must explain the reasons and outline the corrective action taken. Depending upon the nature of the trouble, he may be required to do only a retest of the sample on the test failed, or a complete qualification test on a new sample.

Qualification is granted two to three weeks after the manufacturer submits a satisfactory report. The total time for this process is usually four to five months if all goes well.

8.8 RESPONSIBILITY FOR TESTING

The current military specification practice places the responsibility for the conduct of the required qualification and quality conformance inspection testing on the supplier, under the surveillance of a Government Quality and Assurance Representative (QAR) who is assigned to cover a particular order. Equipment contractors are permitted to request Government Procurement Quality Assurance (PQA) action at subcontract level on items which they purchase for use in military equipment. Government

inspection at subcontract level can only be contractually required when authorized by the equipment contractor's QAR.

8.9 QPL LISTING

A "qualified" item of a supplier is placed on a continually updated "Qualified Products List" (QPL), which is used by the Government and by its contractors to determine the eligible suppliers of a particular item covered by a military specification. If a supplier is not listed on the QPL for the desired item, he will ordinarily not be solicited for bids to supply the item. An exception to this status occurs when the Military Qualifying Activity has advised a supplier that his product has passed the qualification testing procedure, but he is not yet listed on the QPL for the item because of QPL revision and printing time. In this case he may publicize his qualifications, accept orders for the item, and proceed with acceptance testing using his authorization from the Qualifying Activity as evidence of his qualification status.

8.10 APPLICABLE REVISION AND ORDER OF PRECEDENCE

In Government procurement practice, the issue of a military specification or standard which is in effect on the date of invitation for bids for an item is considered to apply to the resulting contract or order for the item.

It should be noted that this practice applies to all referenced documents as well as to the detail specification. Since the different documents are revised independently, it is occasionally found that conflicting requirements exist in the detail specification and reference documents. These cases are ultimately resolved by revision of the detail specification, but in the interim relief is usually afforded by means of suitable interpretation by the preparing activity for the detail specification (listed in 8.5 above). Such interpretation may be requested when the question cannot be resolved by considering the order of precedence of the documents involved, which is:

1. The contract or purchase order. Its requirements take precedence over all others except as limited by the JAN branding provisions of MIL-S-19500.
2. The detail specification for the item.
3. The general specification for the item.
4. The referenced documents.

8.11 MILITARY SPECIFICATION FORMAT

Though each component category will have its unique requirements, most specifications follow similar patterns whether they are prepared as a "general" or as a "detailed" specification. Format guidelines, policies, and procedures are strictly governed by Defense Standardization Manual 4120.3-M (formerly M200). Because some "detailed" specifications can become rather lengthy, the front page is devoted to giving a summary of the device's maximum ratings and primary characteristics. This provides the potential user with a quick check list to determine if the devices covered therein can be applied to his circuit design. DESC-ECS (see address in 8.5) has available, upon request, limited quantities of "detail" specification formats covering the more common semiconductor devices.