CONNECTOR PERFORMANCE STANDARD FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS

PS-008

DDR5 CAMM2 Connector Performance Standard

JEDEC
SOLID STATE TECHNOLOGY ASSOCIATION

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DDR5 CAMM2 Connector Performance Standard

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DDR5 CAMM2 Connector Performance Standard

(From JEDEC Board Ballot JCB-15-30, formulated under the cognizance of the JC-11.14 Subcommittee on Microelectronic Assemblies.)

Scope

This standard defines the form, fit and function of DDR5 CAMM2 connectors, variations xBxx, xCxx and xDxx defined in SO-032 to support channels with DDR5 transfer rates. It contains mechanical, electrical and reliability requirements for connector mated to a module defined in MO-358. The intent of this document is to provide performance standards to enable connector, system designers and manufacturers to build, qualify and use the DDR5 CAMM2 connectors in client platforms.

1.1 Connector Overview

DDR5 CAMM2 connector is compress-mount technology (CMT) connector. Retention is needed to ensure the function of the connector, which is defined for applications where a CAMM2 module card mounted over the connector, parallel to the system board.

References

The following references provide normative requirements as specified in the body of this document:

- JEDEC MO-358: Module Outline
- JEDEC SO-032: Socket Outlines
- EIA-364-1000: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Controlled Environment
- EIA-364-05: Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors
- EIA-364-09: Durability Test Procedure for Electrical Connectors and Contacts
- EIA-364-13: Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets
- EIA 364-23: Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets
- EIA-364-27: Shock Test Procedure for Electrical Connectors
- EIA-364-28: Vibration Test Procedure for Electrical Connectors and Sockets
- EIA-364-29: Contact Retention Test Procedure for Electrical Connectors
- EIA-364-31: Humidity Test Procedure for Electrical Connectors and Sockets
- EIA-364-32: Thermal Shock Test Procedure for Electrical Connectors and Sockets
- EIA 364-70: Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
- JEDEC JESD22-B108: Coplanarity Test for Surface-Mount Semiconductor Devices
- JS709A Defining “Low-Halogen” Electronic Products

2 Acronyms, terms, and definitions

Table 1 - Terms and Definitions

Term	Description
BOL	Beginning of Life
dB	Given in dB-volts, i.e., 20log10(V2/V1)
CAMM2	Compression Attached Memory Module
CMT	Compress Mount Technology
DUT	Device under test
EIA	Electronics Industry Alliance
EOL	End of Life
JEDEC	JEDEC Solid State Technology Association
LP DDR	Low Power Double Data Rate
System board	PCB on which the DDR5 connector is mounted
Vertical connector	A connector that accepts a module perpendicular to the system board

3 Pin Numbering

Connector pin numbering sequence information is provided in SO-032. Please refer to the note.Connector Socket Outline

3.1 DDR5 CAMM2 Connector Overview

A primary consideration for DDR5 CAMM2 development is to support modular DDR5 solution, rather than relying solely on SODIMM socket on the motherboard.

The DDR5 CAMM2 connector refers to 3 height variations defined in SO-032: xBxx (1.85mm), xCxx (2.85mm) and xDxx (7.50 mm). It features three posts, with two serving as alignment features and the third providing guidance to improve serviceability. The connector also includes six mounting holes, but only the three holes located at the edge in the width direction are used for DDR5 CAMM2 retention. The other three holes, located at the center, are reserved for other applications.

3.2 Socket outline

A general view of the DDR5 CAMM2 connector is shown in Figure 1 . For the detailed outlines, refer to JEP95, SO-032, variation xBxx, xCxx and xDxx.

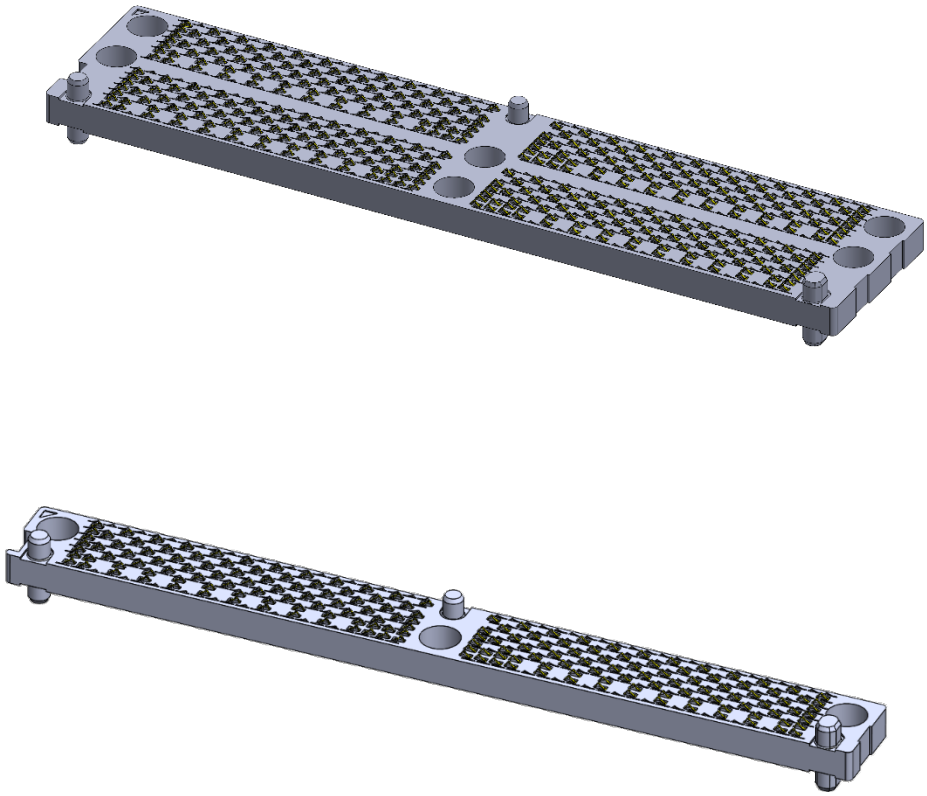


Figure 1 Examples of DDR5 CAMM2 connector (Top: Dual channel. Bottom: Single channel)

4 Module Outline

4.1 Module mechanical dimensions

A general view of the DDR5 CAMM2 module is shown in Figure 2. For the detailed outline, refer to JEDEC JEP95, MO-358.

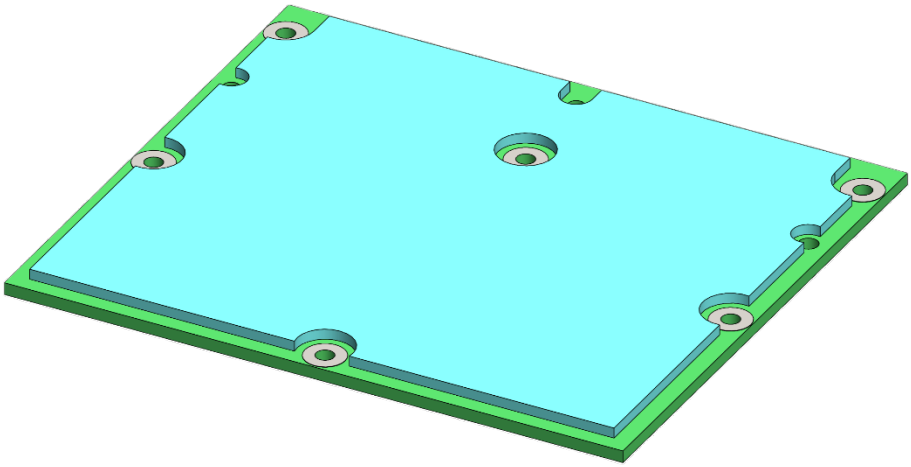


Figure 2 Example of a DDR5 CAMM2 Dual Channel Module

5 Assembly

5.1 CAMM2 Module assembly

Figure 3 depicts an example of CAMM2 module assembly. To provide additional support, it is advisable to place a backplate beneath the motherboard. Embedded M2 nuts on the backplate are aligned through the system board and the DDR5 CAMM2 connector. The CAMM2 module is placed onto the connector and then fastened with three M2 screws to secure it in place.

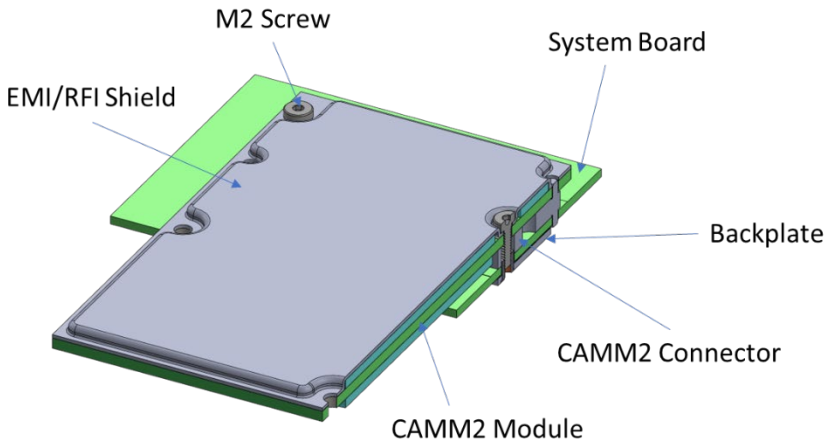


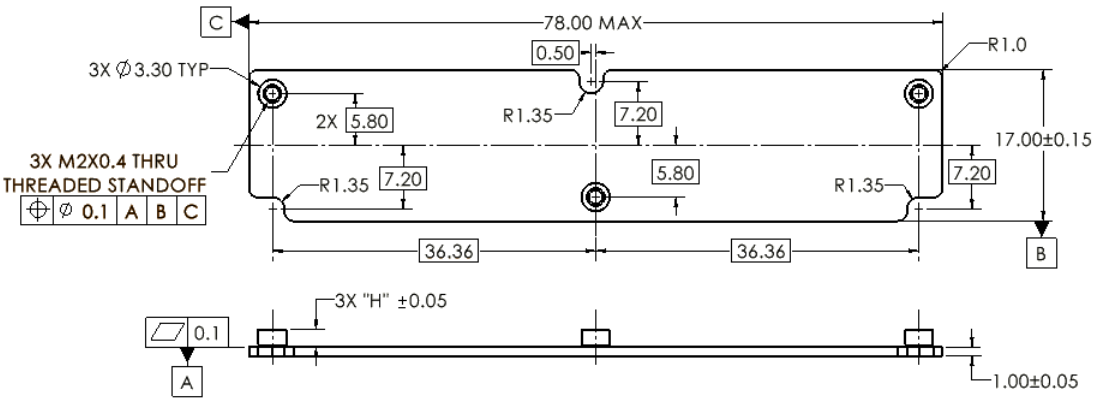
Figure 3 Reference assembly scheme (Dual channel)

5.2 Reference Backplate

A backplate is required to ensure the connector works properly, a reference backplate (material: stainless steel) is provided and shown in Figure 5.

A thin adhesive material may be placed between the backplate and the system board to improve the serviceability. Dimension H will be adjusted accordingly to accommodate the adhesive material thickness.

The three nuts on the back plate can be used as a ground return when a gasket used to ensure conductive connection to motherboard ground plane.



STANDOFF HEIGHT TABLE	
SYSTEM BOARD THICKNESS (MM)	H (MM)
0.8	1.60
0.9	1.70
1.0	1.80
1.1	1.90
1.2	2.00

Figure 4 Reference backplate design (Dual channel)

5.3 Reference assembly (with shield)

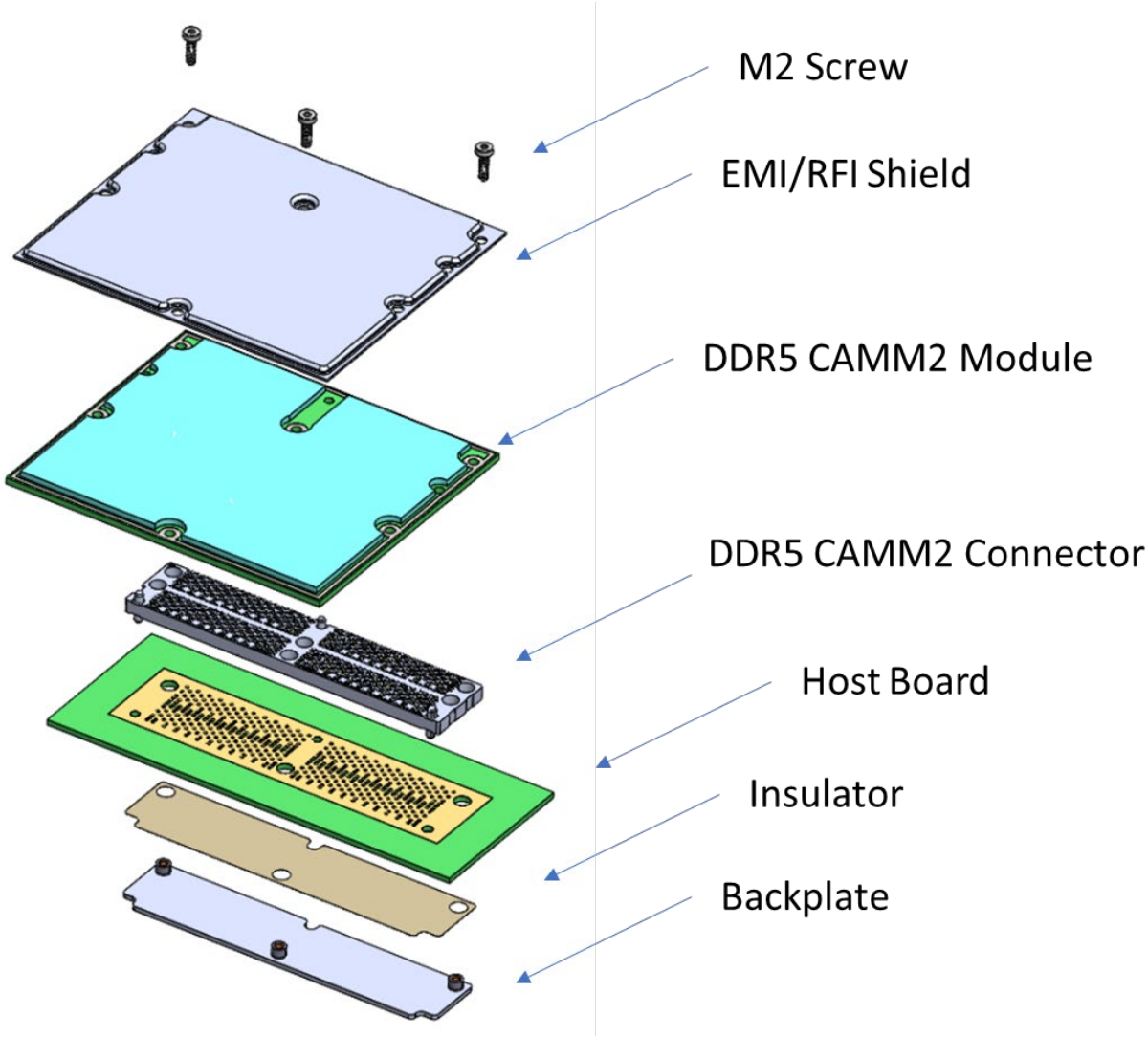


Figure 5 Assembly reference view (Dual channel)

6 Performance requirements

Reliability benchmark testing shall be performed per EIA 364-1000 test groups 1, 2, 3, and 4 for 3, 5, or 7-year life cycle requirements. A minimum 5 samples are to be tested per subgroup.

6.1 Mechanical and other requirements

Table 2 - Mechanical and other requirements

Mechanical Test Description	**Procedure**	**Requirement**
Normal Force – Terminal (fully compressed)	EIA 364-29	Max 35 gf per pin
Retention Force - Terminal (Optional)	EIA 364-29	50 gf minimum per pin; maximum movement of contact of 0.50 mm
Durability (mating/unmating)	EIA-364-09 Perform 25 cycles installation cycles	LLCR and no nickel plating exposed at contact interface
Additional Tests	Procedure	Requirement
Recommended fastening torque (mounting)		0.1~0.2 N.m (14.2~28.3 oz.in)
Recommended retention torque (un-mounting)		0.08 N.m. (11.3 oz.in) minimum
Module component reliability (optional)	IPC-TM-650 Dye and Pry	<25% solder joint crack

6.2 Reliability test conditions

Table 3 - Reliability test sequence

Test	Test Group			
	1	2	3	4
Low Level Contact Resistance	1,4,6	1,4,6,8	1,3,5,7	1,4,6,8,10
Reseating	5	7		9
Vibration			4	
Mechanical Shock			6	
Durability (preconditioning)	2	2	2	2
Temperature Life	3			
Temperature Life (preconditioning)				3
Thermal Shock		3		
Cyclic Temp and Humidity		5		
Mixed Flowing Gas				5
Thermal Disturbance				7

6.3 Reliability test conditions (cont'd)

Table 4 - Reliability test conditions

Reliability Test Description	Procedure	Requirement
Durability (preconditioning)	EIA-364-09, perform 5 plug/unplug cycles	no evidence of physical damage
Temperature Life Temperature Life (preconditioning)	EIA-364-17, Method A (without electrical load) 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 8 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 9	electrical, mechanical and environmental criteria
Low Level Contact Resistance (LLCR)	EIA-364-23 (termination of connector to board carrier shall be included in the measurements)	Refer to Table 5.4.2
Shock Unpackaged	EIA-364 -27 Trapezoidal shock 50 g, ± 10% Duration 11 ms Velocity change 170 inch/sec, ± 10% Three drops in each of six directions are applied to each of the three samples Detail in Annex C	electrical, mechanical and environmental criteria
Vibration Unpackaged	EIA-364 -28 Random profile: 5 Hz @ 0.01 g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up) 20 Hz to 500 Hz @ 0.02 g^2/Hz (flat) Input acceleration is 3.13 g RMS 10 minutes per axis for all 3 axes on all samples Random control limit tolerance is ± 3 dB Detail in Annex C	no discontinuities of ≥ 1 microsecond electrical, mechanical and environmental criteria
Cyclic Temperature and Humidity	EIA-364-31B, Method III without conditioning, initial measurements, cold shock and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 24 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Shock	EIA-364-32, Method A, Table 2, Test Condition 1, -55 °C to 85 °C, perform 5 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Disturbance	EIA-364-1000 Cycle the connector between 15 ±3 °C and 85 ±3 °C, as measured on the part. Ramps should be a minimum of 2 °C/minute. Dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled; perform 10 cycles in mated condition.	electrical, mechanical and environmental criteria
Mixed Flowing Gas	EIA-364-65, class IIA, Option 4. Expose all specimens in the mated condition for the total mixed flowing gas exposure duration per EIA 364-1000 Table 4.	electrical, mechanical and environmental criteria
Reseating	Manually unplug/plug the connector. Perform 3 cycles	No evidence of physical damage

6.4 Environmental requirements

Table 5 - Connector environmental requirements

Environmental Requirements	Procedure	Requirement
Flammability	UL 94	V-0
Lead Free	RoHS compliant per IEC 62474	RoHS directive (2011/65/EU)
Low Halogen	1000 ppm max Cl when used in a flame retardant 1000 ppm max Br when used in a flame retardant Per JS-709A Standard (Clause 4)	Sample combustion followed by ion chromatography as specified in British Standard Methods BS EN 114582/2007, Characterization of waste – Halogen and sulfur content – Oxygen combustion in closed systems and determination methods OR US EPA-5050 (BOM Preparation Method for Solid Waste)

6.5 Electrical requirements

Table 6 - Connector electrical requirements

DC Electrical Requirements	Procedure	Requirement
LLCR Contact resistance, Initial	EIA-364 -23 Detail in Annex A	50 mΩ Max for SO-032 variation xBxx and xCxx. 150 mΩ Max for SO-032 variation xDxx
LLCR (Contact resistance)	EIA364-23B Subject mated contacts assembled in housing to 20 mV maximum voltage at 100 mA maximum current	Post Stress: the resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading shall not exceed 20 mΩ
Withstanding Voltage	EIA-364-20, Condition I. 500 V ac at sea level.	One minute hold with no breakdown or flashover.
Insulation resistance	EIA-364 -21	1M Ω minimum
Current carrying capability at 30 °C temperature rise per contact	EIA-364 Test Procedure 70 Detail in Annex B	1.0 amp/pin

7 Signal Integrity requirements

The signal integrity requirements are measured by the connector and its interfaces with baseboard and module. The device under test (DUT) includes short stripline trace on baseboard, a ø0.25mm micro-via, a short trace between the micro-via to contact pad, the contact pad on baseboard, the connector pin, the contact pad on module, a short trace between contact pad to a micro-via, ø0.25mm micro-via, and short stripline on module.

The detail of the DUT is shown in in Figure 1 and the detail of the testboard is described in Annex A.

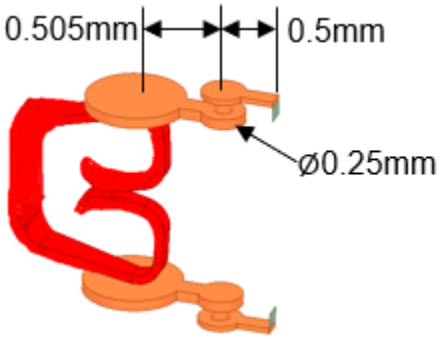


Figure 6: Device under test (DUT)

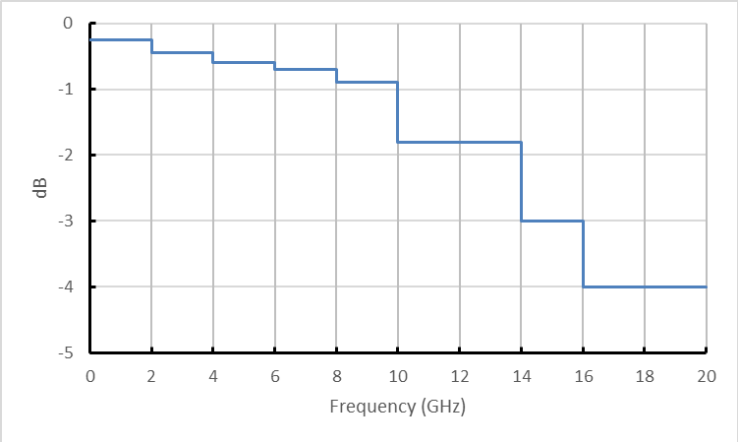
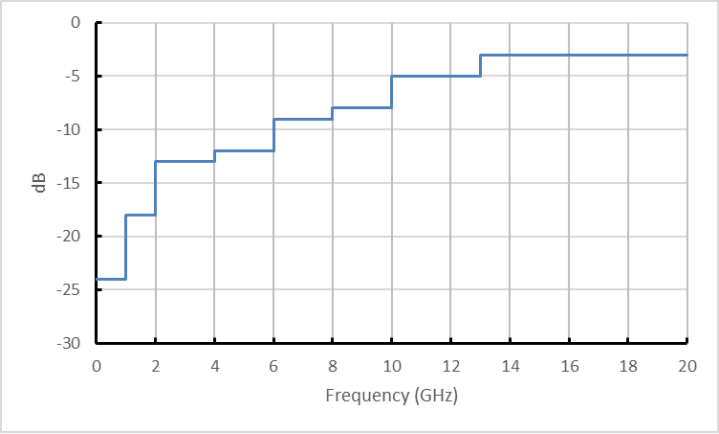
7.1 Frequency domain requirements

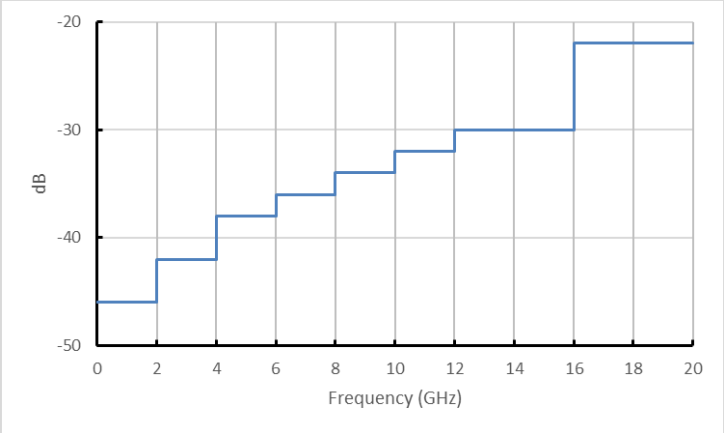
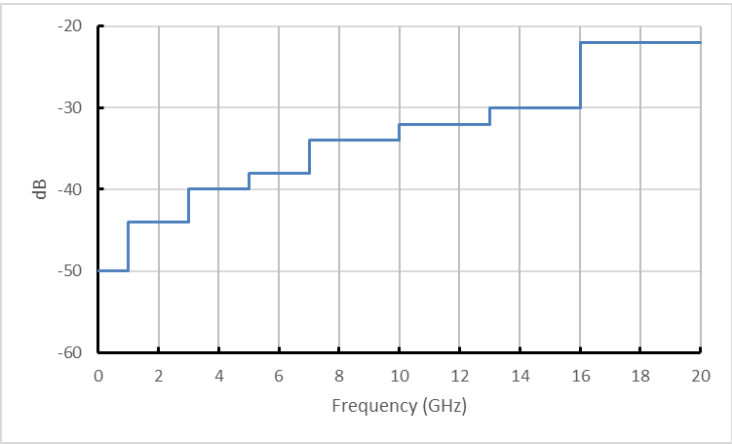
The S-parameter requirements for 1.85mm, 2.85mm and 7.5mm height CAMM2 connector are shown in Table 7.

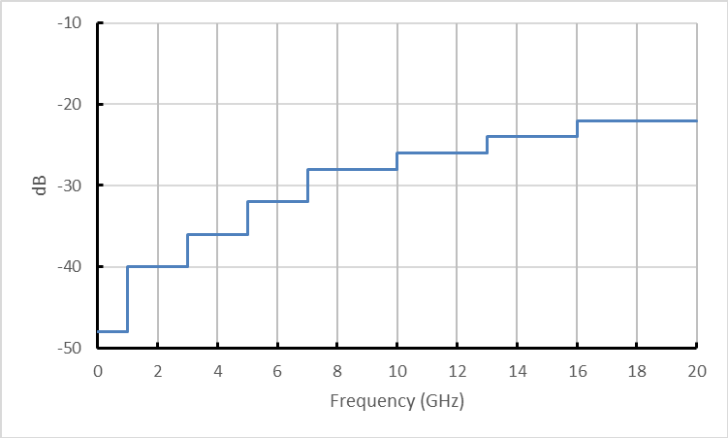
Notes:

- Effects of both baseboard and module pads, connector pin and micro-vias are included
- Reference impedance = 40ohm

Table 7 - S-parameter requirements

S-Parameter	Target Value
Insertion Loss (IL) **Note:** • Detail in Annex	> -0.25 dB (f <= 2.0 GHz) > -0.45 dB (2.0 GHz < f <= 4.0 GHz) > -0.60 dB (4.0 GHz < f <= 6.0 GHz) > -0.70 dB (6.0 GHz < f <= 8.0 GHz) > -0.90 dB (8.0 GHz < f <= 10.0 GHz) > -1.80 dB (10.0 GHz < f <= 14.0 GHz) > -3.0 dB (14.0 GHz < f <= 16.0 GHz) > -4.0 dB (16.0 GHz < f <= 20.0 GHz) 
Return Loss (RL) **Note:** • Detail in Annex	< -24.0 (f <= 1.0GHz) < -18.0 (1.0 GHz < f <= 2.0 GHz) < -13.0 (2.0 GHz < f <= 4.0 GHz) < -12.0 (4.0 GHz < f <= 6.0 GHz) < -9.0 (6.0 GHz < f <= 8.0 GHz) < -8.0 (8.0 GHz < f <= 10.0 GHz) < -5.0 (10.0 GHz < f <= 13.0 GHz) < -3.0 (13.0 GHz < f <= 20.0 GHz) 

Near End Crosstalk (NEXT) **Note:** • Detail in Annex	< -46.0 dB (f <= 2.0 GHz) < -42.0 dB (2.0 GHz < f <= 4.0 GHz) < -38.0 dB (4.0 GHz < f <= 6.0 GHz) < -36.0 dB (6.0 GHz < f <= 8.0 GHz) < -34.0 dB (8.0 GHz < f <= 10.0 GHz) < -32.0 dB (10.0 GHz < f <= 12.0 GHz) < -30.0 dB (12.0 GHz < f <= 16.0 GHz) < -22.0 dB (16.0 GHz < f <= 20.0 GHz) 
Far End Crosstalk (FEXT) Note: • Detail in Annex	< -50.0 dB (f <= 1.0 GHz) < -44.0 dB (1.0 GHz < f <= 3.0 GHz) < -40.0 dB (3.0 GHz < f <= 5.0 GHz) < -38.0 dB (5.0 GHz < f <= 7.0 GHz) < -34.0 dB (7.0 GHz < f <= 10.0 GHz) < -32.0 dB (10.0 GHz < f <= 13.0 GHz) < -30.0 dB (13.0 GHz < f <= 16.0 GHz) < -22.0 dB (16.0 GHz < f <= 20.0 GHz) 

Power Sum FEXT (PSFEXT) **Note:** • Detail in Annex	< -48.0 dB (f <= 1.0 GHz) < -40.0 dB (1.0 GHz < f <= 3.0 GHz) < -36.0 dB (3.0 GHz < f <= 5.0 GHz) < -32.0 dB (5.0 GHz < f <= 7.0 GHz) < -28.0 dB (7.0 GHz < f <= 10.0 GHz) < -26.0 dB (10.0 GHz < f <= 13.0 GHz) < -24.0 dB (13.0 GHz < f <= 16.0 GHz) < -22.0 dB (16.0 GHz < f <= 20.0 GHz) 

Annex A (informative) LLCR Measurements

A.1 Reference equipment

- Micro-ohmmeter (such as Keithly 580; Keysight/Agilent 4338B)
- Cable with clamper or pogo pins

A.2 4-wire measurement

Figure A.1 illustrates 4 wire LLCR measurement

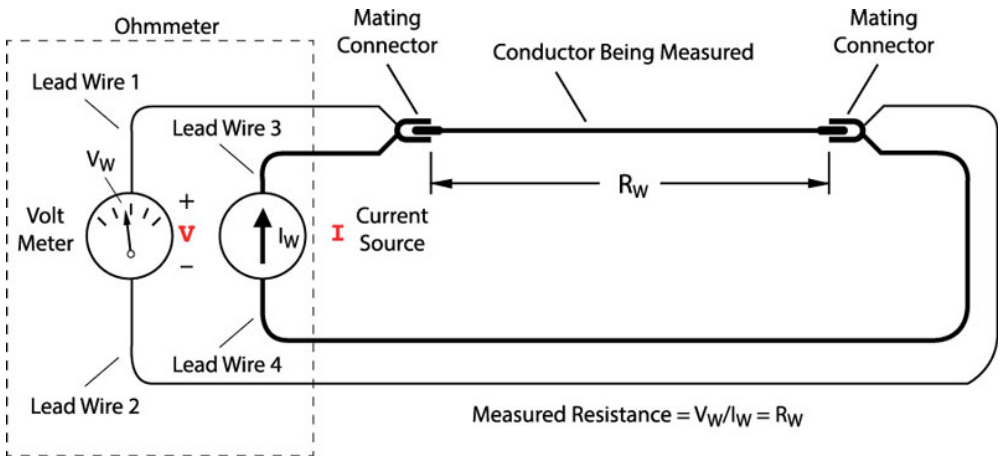


Figure A.1 — 4-wire measurement

A.2 Test fixture example

Figure A.2 and Figure A.3 illustrate LLCR measurement examples using 4-wire measurement.

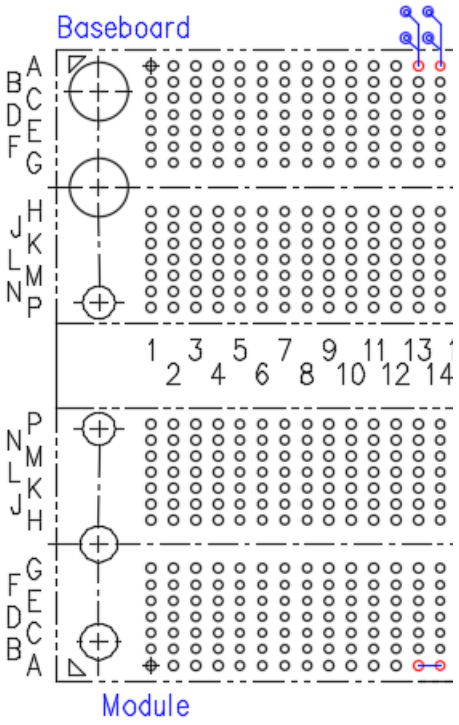


Figure A.2 — 4-wire connection example (2 pins in series)

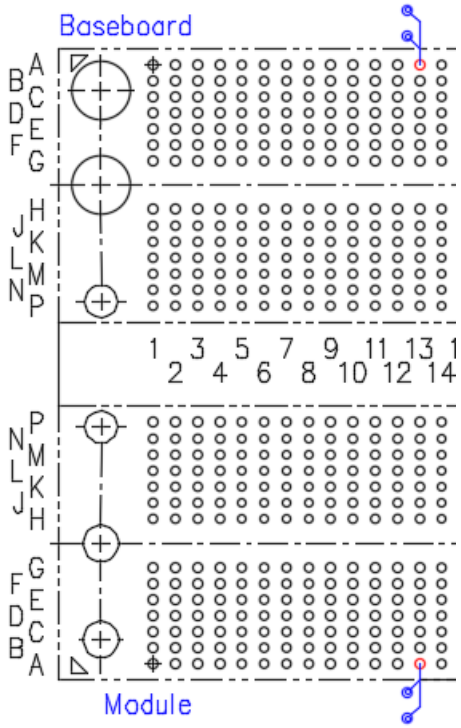


Figure A.3 — 4-wire connection example (single pin)

Annex B (informative) Current Carrying Capability Testing

B.1 Reference equipment

T-Rise Method (Reference EIA 364-70 Method 2)

B.2 Test procedure

The method is summarized as follows: Minimum of 5 connector samples.

- Ambient system temperature stabilized (testing to occur at ambient system temperature)
  - Current necessary to produce the specified temperature of 30C. (Do not exceed maximum connector temperature rating e.g. 105C)
  - Test multiple contacts (F23, G23, N23, P23, F24, G24, N24, P24) in housing per wiring diagram (current through wire 1 and wire 2).
- Report results per EIA 364-70 table “test documentation Annex”.

B.3 Test board daisy chain connection

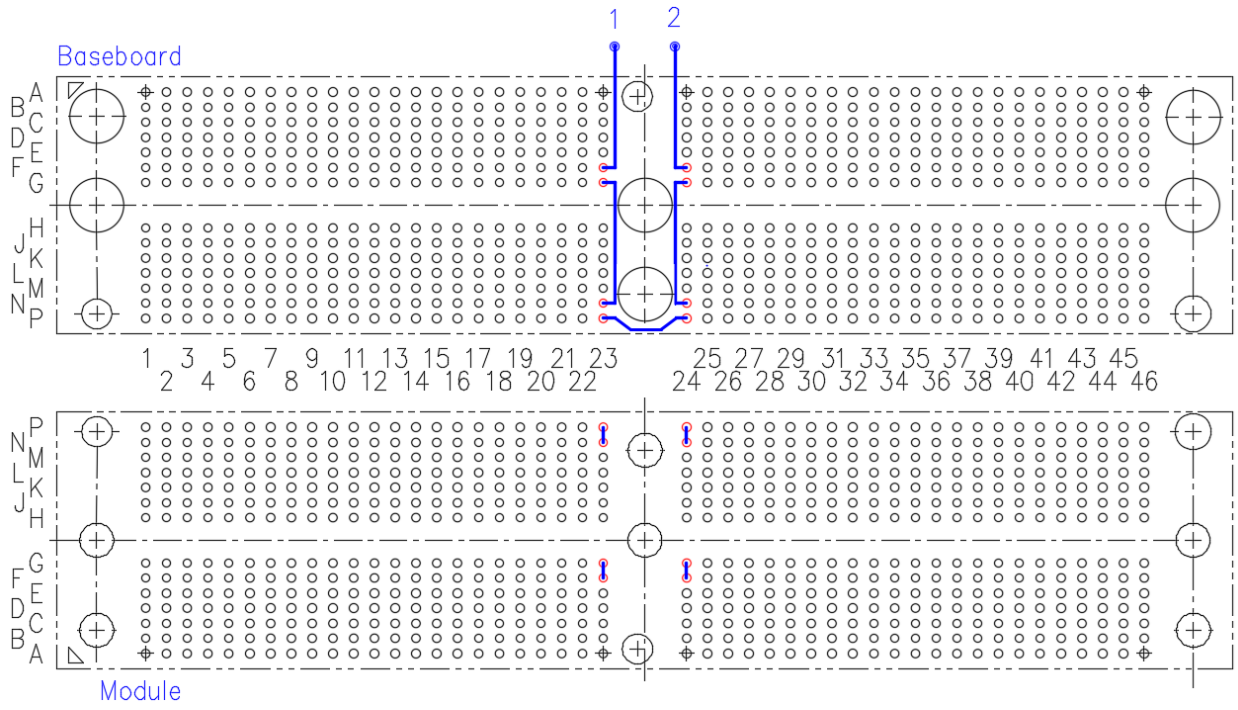


Figure B.1 — Daisy chain connection

Annex C (informative) Shock and vibration test board

C.1 Shock and vibration

Shock and vibration base board to be specified by OEM/ODM due to various system layouts.

C.2 Test Module - weight and center of gravity

- Module weight: 15 grams
- Top cover weight: 10 grams
- Module shape: Follow MO-357 on module size and form factor
- Center of gravity of module: 15 mm from the module straight edge.
- Module thickness: 1.20 +0/-0.10 mm.
- Module to check connector continuity and DRAM solder joint reliability

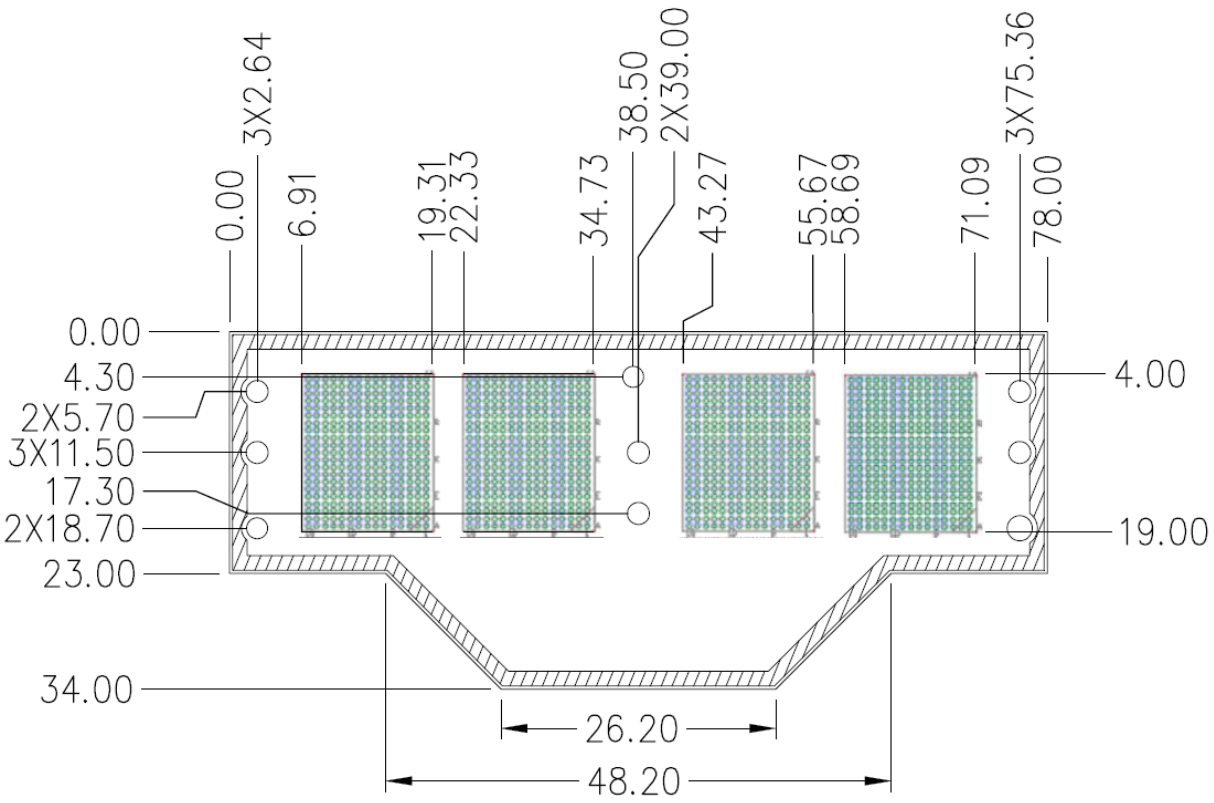


Figure C.1 —Example of the test module with DRAM location

C.3 Shock unpackaged

C.3.1 Purpose

To ensure the boards are sufficiently robust to withstand shocks when shipped in a system. Board un-packaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.3.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.3.3 Test Conditions

- Trapezoidal shock 50 g ± 10%.
- Velocity change 170 inch/sec, ± 10%.
- Three drops in each of six directions are applied to each of the three samples.

C.4 Vibration unpackaged

C.4.1 Purpose

To ensure the board is sufficiently robust to withstand vibration when mounted in a system, which is being shipped. Board unpackaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.4.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.4.3 Test Conditions

Random profile:

- 5 Hz @ 0.01 g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up)
- 20 Hz to 500 Hz @ 0.02 g^2/Hz (flat)
- Input acceleration is 3.13 g RMS
- 10 minutes per axis for all 3 axes on all samples
- Random control limit tolerance is ± 3 dB

Annex D (informative) Signal integrity test board

D.1 Reference Equipment

Vector Network Analyzer (VNA) System

2X through calibration capability required.

Connectors: Molex 2.92mm connector (# 0732520090) or equivalent connector

Two 50 Ω high frequency, low loss phase-matched cables. Recommended cables are offered by Micro Coax (part number UFB197C) or equivalence. The cables are used to connect the 2.92mm connector to the measurement ports on the VNA.

D.2 Test board

The testboard includes base board and module card. 2X through calibration traces are included on the base board to save PCB space. There is 1X through trace on base board as well for rise time setup for TDR impedance measurement.

D.2.1 Test board stackup

Figure D.1 describe details of the 6-layer DUT board and DUT module PCB stackup to be used. The DUT board and DUT module impedance are defined as 50 (± 5%) ohms, recommended trace width for the testboard is 6.5mil.

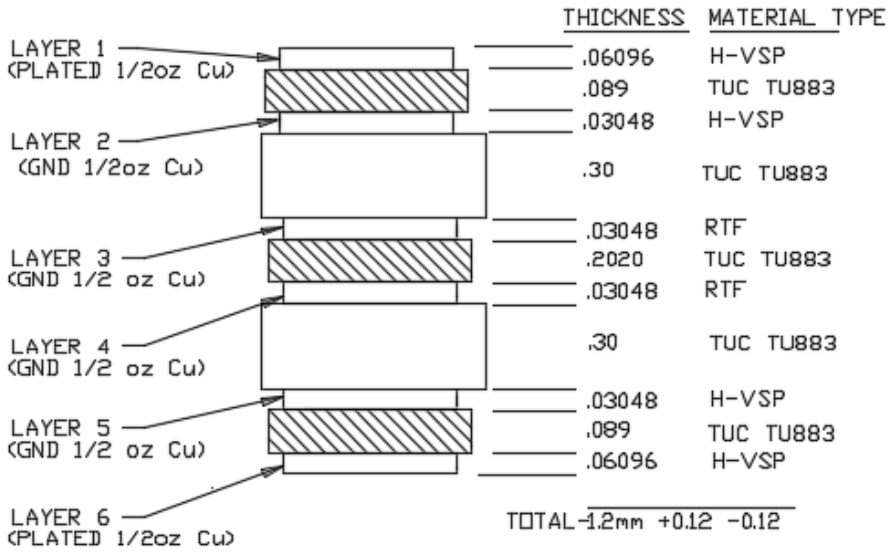


Figure D.1 Stackup of CAMM2 connector testboard

D.3.2 Baseboard and CAMM2

The reference plane for deembeded is set to be 0.5mm from micro-via pad on L2. The trace length from reference plane to 2.92mm connector is 19.5mm.

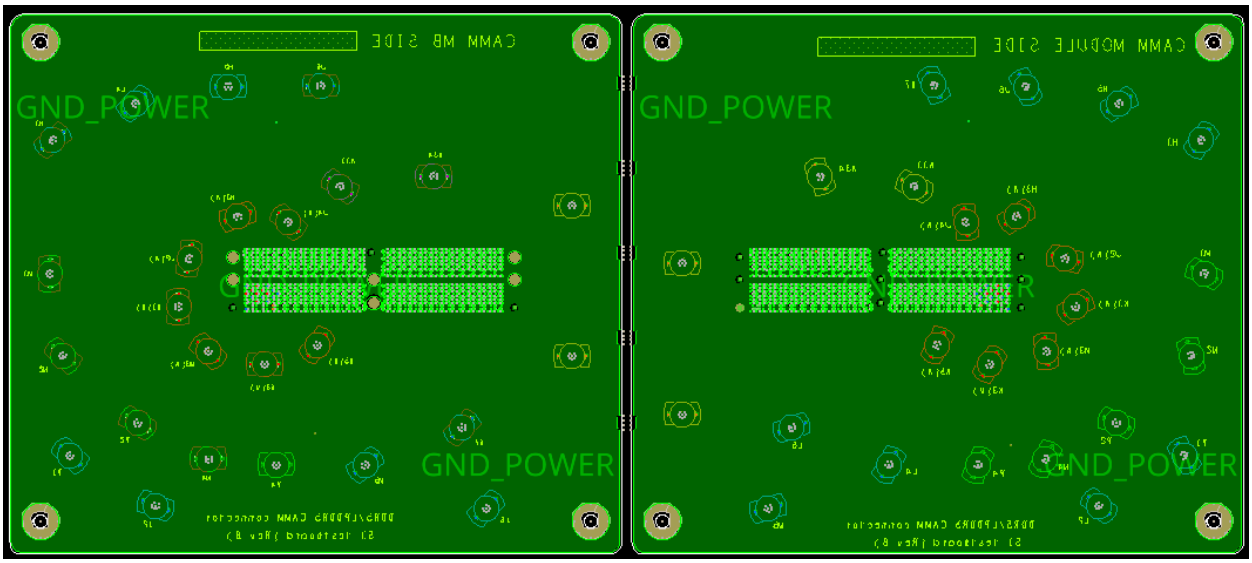


Figure D.2 CAMM2 base board

D.3.4 2.92mm connector

Molex 2.92mm connector (# 0732520090) or equivalence is recommended to use, as shown in Figure D.4. The 2.92mm connector will be screw mounted on the PCB for cable vertical access.

A low profile 0-80 screw (screw head <0.9mm) is used to fasten the 2.92mm connector on the board to avoid any interference during CAMM2 testboard assembly.

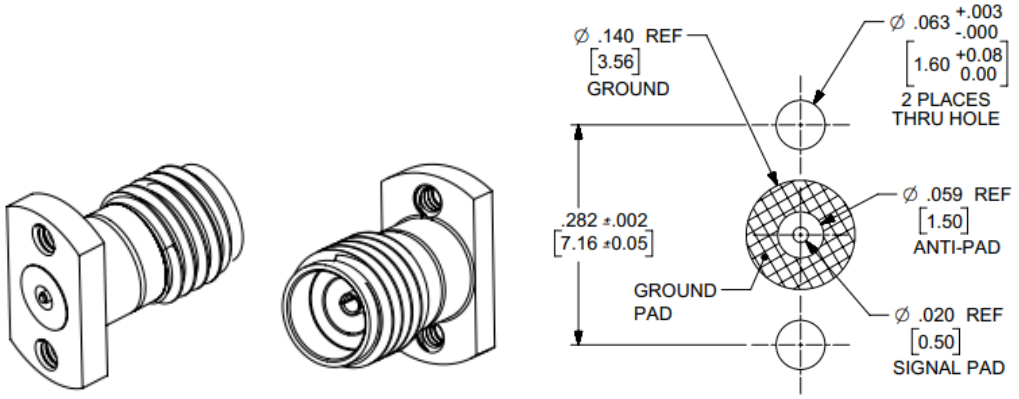


Figure D.3 (a) 2.92mm connector (b) Recommended footprint of the 2.92mm connector

D. 4 Testing

Any 2.92mm connectors not connected to VNA for testing should be terminated with 50-ohm load.

D. 5 Data processing

The pins used for testing include K1, J2, H3, K3, M3, J4 and K5. K3, J2 are selected as the victim for single pin near end crosstalk and far end crosstalk calculations. K3 is selected as victim for power sum far end crosstalk calculation.

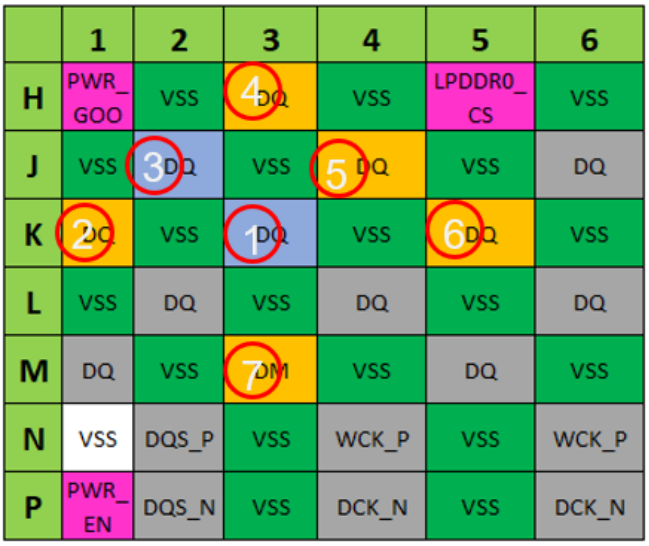


Figure D.4 Pins selected for testing

- Impedance: All 7 DQ pins
- Insertion loss: All 7 DQ pins
- Return loss: All 7 DQ pins
- NEXT: 1) K3 as victim, the rest 6 pins as aggressors 2) J2 as victim, K1, H3 as aggressors
- FEXT: 1) K3 as victim, the rest 6 pins as aggressors 2) J2 as victim, K1, H3 as aggressors
- PSFEXT: K3 as victim. The rest 6 pins as aggressors, pin J2 and pin J4 to be counted twice (to cover L2 and L4 which are not tested

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