CONNECTOR PERFORMANCE STANDARD FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS

PS-005

DDR5 288 Pin U/R/LR DIMM Connector Performance Standard

(Double Data Rate 5)

JEDEC
SOLID STATE TECHNOLOGY ASSOCIATION

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DDR5 288 Pin U/R/LR DIMM Connector Performance Standard

Contents

Tables

Figures

DDR5 288 Pin U/R/LR DIMM Connector Performance Standard

(From JEDEC Board Ballot JCB-15-30, formulated under the cognizance of the JC-11.14 Subcommittee on Microelectronic Assemblies.)

1 Scope

This standard defines the form, fit and function of DDR5 connectors for U/R/LR modules supporting channels with transfer rates up to 6.4 GT/S. It contains mechanical, electrical and reliability requirements for connector mated to a module with nominal thickness of 1.27 mm. The intent of this document is to provide Performance Standards to enable connector, system designers and manufacturers to build, qualify and use the DDR5 connectors in client and server platforms.

1.1 Connector Overview

DDR5 U/R/LR DIMM connectors share the same mechanical definition and dimensions. The 288 pin, 0.85 mm pitch vertical connector is defined for applications where a 1.27 mm nominal thickness module card vertically enters the connector, perpendicular to the system board.

2 References

The following references provide normative requirements as specified in the body of this document:

- JEDEC MO-329: Module Outline - 288 pin DDR5 DIMM, 0.85 mm pitch
- JEDEC SO-023: Socket Outlines - 288 pin DDR5 connector, 0.85 mm pitch
- JEDEC GS-010: DDR4 and DDR5 DIMM Socket Insertion and Extraction Force Gauge
- EIA-364-1000: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Controlled Environment
- EIA-364-05: Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors
- EIA-364-09: Durability Test Procedure for Electrical Connectors and Contacts
- EIA-364-13: Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets
- EIA 364-23: Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets
- EIA-364-27: Shock Test Procedure for Electrical Connectors
- EIA-364-28: Vibration Test Procedure for Electrical Connectors and Sockets
- EIA-364-29: Contact Retention Test Procedure for Electrical Connectors
- EIA-364-31: Humidity Test Procedure for Electrical Connectors and Sockets
- EIA-364-32: Thermal Shock Test Procedure for Electrical Connectors and Sockets
- EIA 364-70: Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
- JEDEC JESD22-B102 Solderability
- JEDEC JESD22-B108: Coplanarity Test for Surface-Mount Semiconductor Devices
- JESD22-B112: Package Warpage Measurement of Surface-Mount Integrated Circuits at Elevated Temperature
- JS709A Defining “Low-Halogen” Electronic Products
- SPP-023 Standard Practices and Procedures - Module Insertion/Extraction Procedure for DIMM and Mini DIMM Connectors

3 Acronyms, terms, and definitions

Table 1 - Terms and Definitions

Term	Description
BOL	Beginning of Life
dB	Given in dB-volts, i.e., 20log10(V2/V1)
DDR	Double Data Rate
DUT	Device under test
EIA	Electronics Industry Alliance
EOL	End of Life
JEDEC	JEDEC Solid State Technology Association
System board	PCB on which the DDR5 connector is mounted
Vertical connector	A connector that accepts a module perpendicular to the system board

4 Pin Numbering

This section describes pin numbers in DDR5 U/R/LR DIMM connectors. The DDR5 U/R/LR DIMM connector pin list is shown in Table 2.

Table 2 - DDR5 U/R/LR DIMM Number Sequence

Pin#			Pin#
1	Pin	Pin	145
2	Pin	Pin	146
3	Pin	Pin	147
4	Pin	Pin	148
5	Pin	Pin	149
6	Pin	Pin	150
7	Pin	Pin	151
8	Pin	Pin	152
9	Pin	Pin	153
10	Pin	Pin	154
11	Pin	Pin	155
12	Pin	Pin	156
13	Pin	Pin	157
14	Pin	Pin	158
15	Pin	Pin	159
16	Pin	Pin	160
17	Pin	Pin	161
18	Pin	Pin	162
19	Pin	Pin	163
20	Pin	Pin	164
21	Pin	Pin	165
22	Pin	Pin	166
23	Pin	Pin	167
24	Pin	Pin	168
25	Pin	Pin	169
26	Pin	Pin	170
27	Pin	Pin	171
28	Pin	Pin	172
29	Pin	Pin	173
30	Pin	Pin	174
31	Pin	Pin	175
32	Pin	Pin	176
33	Pin	Pin	177
34	Pin	Pin	178
35	Pin	Pin	179
36	Pin	Pin	180
37	Pin	Pin	181
38	Pin	Pin	182
39	Pin	Pin	183
40	Pin	Pin	184
41	Pin	Pin	185
42	Pin	Pin	186
43	Pin	Pin	187
44	Pin	Pin	188
45	Pin	Pin	189
46	Pin	Pin	190
47	Pin	Pin	191
48	Pin	Pin	192
49	Pin	Pin	193

Pin#			Pin#
50	Pin	Pin	194
51	Pin	Pin	195
52	Pin	Pin	196
53	Pin	Pin	197
54	Pin	Pin	198
55	Pin	Pin	199
56	Pin	Pin	200
57	Pin	Pin	201
58	Pin	Pin	202
59	Pin	Pin	203
60	Pin	Pin	204
61	Pin	Pin	205
62	Pin	Pin	206
63	Pin	Pin	207
64	Pin	Pin	208
65	Pin	Pin	209
66	Pin	Pin	210
67	Pin	Pin	211
68	Pin	Pin	212
69	Pin	Pin	213
70	Pin	Pin	214
71	Pin	Pin	215
72	Pin	Pin	216
73	Pin	Pin	217
74	Pin	Pin	218
75	Pin	Pin	219
Key			
76	Pin	Pin	220
77	Pin	Pin	221
78	Pin	Pin	222
79	Pin	Pin	223
80	Pin	Pin	224
81	Pin	Pin	225
82	Pin	Pin	226
83	Pin	Pin	227
84	Pin	Pin	228
85	Pin	Pin	229
86	Pin	Pin	230
87	Pin	Pin	231
88	Pin	Pin	232
89	Pin	Pin	233
90	Pin	Pin	234
91	Pin	Pin	235
92	Pin	Pin	236
93	Pin	Pin	237
94	Pin	Pin	238
95	Pin	Pin	239
96	Pin	Pin	240
97	Pin	Pin	241

Pin#			Pin#
98	Pin	Pin	242
99	Pin	Pin	243
100	Pin	Pin	244
101	Pin	Pin	245
102	Pin	Pin	246
103	Pin	Pin	247
104	Pin	Pin	248
105	Pin	Pin	249
106	Pin	Pin	250
107	Pin	Pin	251
108	Pin	Pin	252
109	Pin	Pin	253
110	Pin	Pin	254
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136	Pin	Pin	280
137	Pin	Pin	281
138	Pin	Pin	282
139	Pin	Pin	283
140	Pin	Pin	284
141	Pin	Pin	285
142	Pin	Pin	286
143	Pin	Pin	287
144	Pin	Pin	288

5 Connector Socket Outline

5.1 DDR5 Connector Overview

A primary consideration for DDR5 development was to maintain the form factor continuity with DDR4. The objective was to scale the connector in an evolutionary manner to fit within the platform volumetric limit for more bandwidth. The signaling scalability requires surface mount (SMT) type, not only to reduce the crosstalk of connector itself, but also to reduce the crosstalk of transmission lines on motherboard (MB). DDR5 connectors are uniquely keyed to prevent interchangeability with the previous connector generations. The pin count keeps 288 pins and 0.85mm pitch, same as DDR4 connector.

5.2 Socket outline

A general view of the DDR5 U/R/LR DIMM connector with inserted module is shown in Figure 1 . The socket outlines are shown in Figure 2. Detailed outlines refer to JEP95, SO-023. All dimensions are in millimeters.

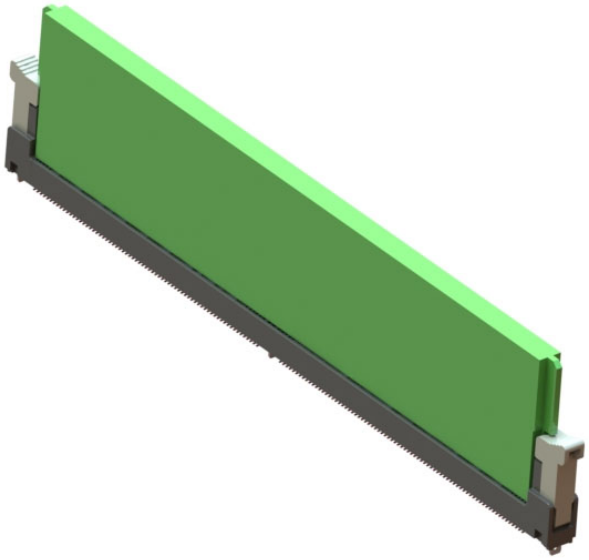


Figure 1 DDR5 socket and module (SMT)

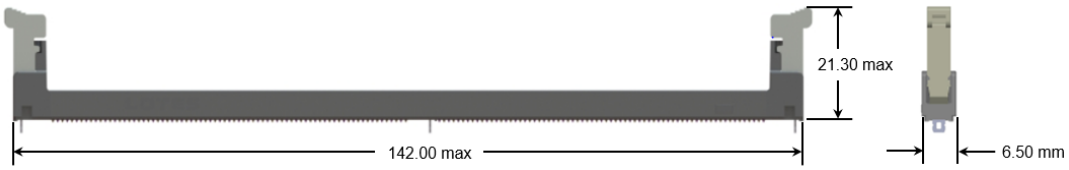


Figure 2 DDR5 U/R/LR DIMM Surface Mount (SMT) Connector Socket Outline

6 Module Outline

6.1 Module mechanical dimensions

DDR5 U/R/LR DIMM modules share the same mechanical definition and dimensions. The DDR5 U/R/LR DIMM outline is shown in Figure 3

For the detailed outline, refer to JEDEC JEP95, MO-329.

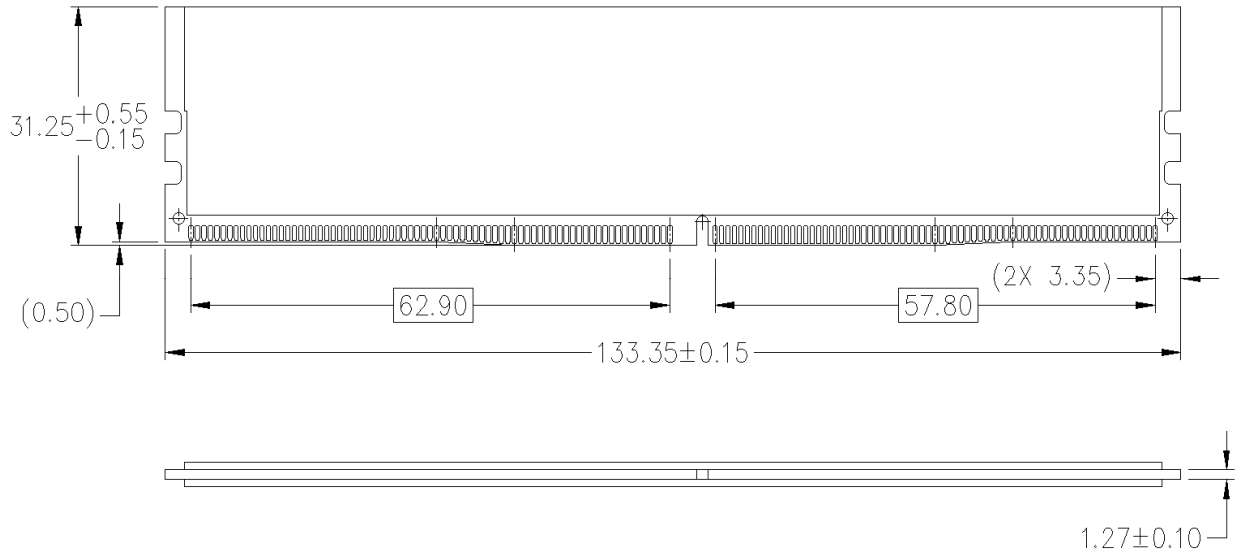


Figure 3 DDR5 U/R/LR DIMM Module Outline

6.2 Step and ramp feature

In order to reduce the insertion force, a step and ramp feature is required on the DDR5 U/R/LR DIMM module. The step and ramp feature allows the connector pins to engage the module gold fingers in a sequential manner. There are two step and ramp zones at the bottom edge of the module.

For the detailed outline, refer to JEDEC JEP95, MO-329.

6.3 DIMM gold finger shape and plating options

External tie bar will be needed on DIMM top/bottom layer, inner tie bar is not allowed for plating. Selective gold plating is not allowed.

The gold finger shape is shown in Figure 4 DDR5 U/R/LR DIMM Gold finger shape. The chamfer on the top edge of gold finger helps to keep ground via close to gold finger for better connector performance. An example of ground via placement is shown in Figure 5

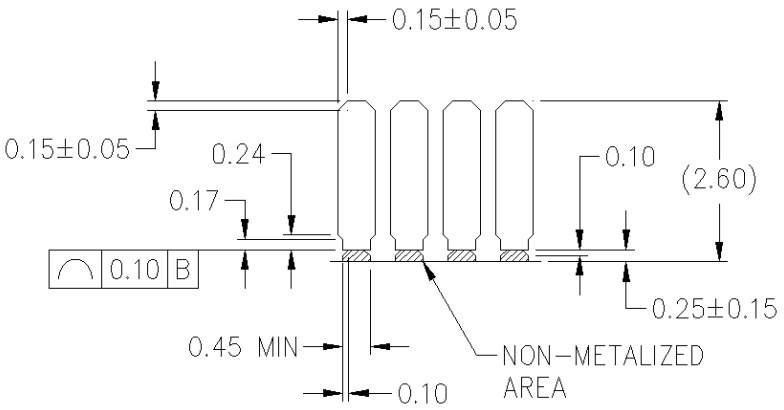


Figure 4 DDR5 U/R/LR DIMM Gold finger shape

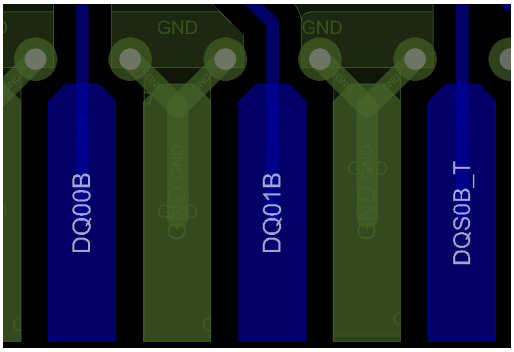


Figure 5 An example for ground via placement near gold finger

For the detailed gold finger and plating options, refer to JEDEC JEP95, MO-329.

7 Reliability requirements

Reliability benchmark testing shall be performed per EIA 364-1000 test groups 1, 2, 3, and 4 for 3, 5, or 7-year life cycle requirements. A minimum 5 samples are to be tested per subgroup.

7.1 Mechanical and other requirements

Table 3 - Mechanical and other requirements

Mechanical Test Description	Procedure	Requirement
Insertion Force (Module to Connector)	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 25.4 mm/min. Use the JEDEC GS-010-3 Insertion Gauge.	106.8 N Maximum
Retention Force - Terminal	EIA 364-29	300 gf minimum per pin; maximum movement of contact of 0.38 mm
Retention Force – Forklock/Metal tab	EIA 364-29	13.3 N minimum per forklock or metal tab; maximum movement of 0.38 mm
Insertion Force - Connector to Board	EIA-364-05 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 12.7 mm/min.	35 N maximum
Unmating Force	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 12.7 mm/min. Use the JEDEC GS-010-4 Extraction Gauge.	19.77 N minimum
Durability (mating/unmating)	EIA-364-09 GS-010-3 Insertion Gauge. Perform 25 cycles plug and unplug cycles at a rate of 25.4 mm/minute	LLCR and no nickel plating exposed at contact interface
Additional Tests	**Procedure**	**Requirement**
Solderability - Lead Free	JESD22-B102; Condition C, 8 hours ± 15 minutes steam precondition.	95% coverage minimum
Lead Free Process ability	260 °C, 5 seconds.	No physical damage to connector per visual inspection at 24 inches. No magnification

Reflow flatness (Optional)	Adapt JESD22-B112 215±5C before and after reflow peak temperature Adapted method detail in Annex E	Lead co-planarity less than (or equal to) 0.1mm OR Housing (side) warpage less than (or equal) 0.08mm
Ejector reliability	Detail in Annex F	No broken piece, no obvious wear or burr observed from 12 inch distance by naked eye

7.2 Reliability test conditions

Table 4 - Reliability test sequence

Test	Test Group			
	1	2	3	4
Low Level Contact Resistance	1,4,6	1,4,6,8	1,3,5,7	1,4,6,8,10
Reseating	5	7		9
Vibration			4	
Mechanical Shock			6	
Durability (preconditioning)	2	2	2	2
Temperature Life	3			
Temperature Life (preconditioning)				3
Thermal Shock		3		
Cyclic Temp and Humidity		5		
Mixed Flowing Gas				5
Thermal Disturbance				7

7.2 Reliability test conditions (cont'd)

Table 5 - Reliability test conditions

Reliability Test Description	Procedure	Requirement
Durability (preconditioning)	EIA-364-09, perform 5 plug/unplug cycles	no evidence of physical damage
Temperature Life Temperature Life (preconditioning)	EIA-364-17, Method A (without electrical load) 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 8 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 9	electrical, mechanical and environmental criteria
Low Level Contact Resistance (LLCR)	EIA-364-23 (termination of connector to board carrier shall be included in the measurements)	Refer to Table 5.4.2
Shock Unpackaged	EIA-364 -27 Trapezoidal shock 50 g, ± 10% Duration 11 ms Velocity change 170 inch/sec, ± 10% Three drops in each of six directions are applied to each of the three samples Detail in Annex C	electrical, mechanical and environmental criteria
Vibration Unpackaged	EIA-364 -28 Random profile: 5 Hz @ 0.01 g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up) 20 Hz to 500 Hz @ 0.02 g^2/Hz (flat) Input acceleration is 3.13 g RMS 10 minutes per axis for all 3 axes on all samples Random control limit tolerance is ± 3 dB Detail in Annex C	no discontinuities of ≥ 1 microsecond electrical, mechanical and environmental criteria
Cyclic Temperature and Humidity	EIA-364-31B, Method III without conditioning, initial measurements, cold shock and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 24 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Shock	EIA-364-32, Method A, Table 2, Test Condition 1, -55 °C to 85 °C, perform 5 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Disturbance	EIA-364-1000 Cycle the connector between 15 ±3 °C and 85 ±3 °C, as measured on the part. Ramps should be a minimum of 2 °C/minute. Dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled; perform 10 cycles in mated condition.	electrical, mechanical and environmental criteria
Mixed Flowing Gas	EIA-364-65, class IIA, Option 4. Expose all specimens in the mated condition for the total mixed flowing gas exposure duration per EIA 364-1000 Table 4.	electrical, mechanical and environmental criteria
Reseating	Manually unplug/plug the connector. Perform 3 cycles	No evidence of physical damage

7.3 Environmental requirements

Table 6 - Connector environmental requirements

Environmental Requirements	Procedure	Requirement
Flammability	UL 94	V-0
Lead Free	RoHS compliant per IEC 62474	RoHS directive (2011/65/EU)
Low Halogen	1000 ppm max Cl when used in a flame retardant 1000 ppm max Br when used in a flame retardant Per JS-709A Standard (Clause 4)	Sample combustion followed by ion chromatography as specified in British Standard Methods BS EN 114582/2007, Characterization of waste – Halogen and sulfur content – Oxygen combustion in closed systems and determination methods OR US EPA-5050 (BOM Preparation Method for Solid Waste)

7.4 Electrical requirements

Table 7 - Connector electrical requirements

DC Electrical Requirements	Procedure	Requirement
LLCR (Contact resistance)	EIA364-23B Subject mated contacts assembled in housing to 20 mV maximum voltage at 100 mA maximum current	Post Stress: the resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading shall not exceed 20 mΩ
LLCR Contact resistance, Initial	EIA-364 -23 Detail in Annex A	40 mΩ Max
Withstanding Voltage	EIA-364-20, Condition I. 500 V ac at sea level.	One minute hold with no breakdown or flashover.
Insulation resistance	EIA-364 -21	1M Ω minimum
Current carrying capability at 30 °C temperature rise per contact	EIA-364 Test Procedure 70 Detail in Annex B	1.0 amp/pin

8 Signal Integrity requirements

The electrical requirements are measured by the connector and its interfaces with baseboard and module as shown in Figure 6. The device under test (DUT) includes 25 mil microstrip from SMT pad, SMT pad on baseboard, connector pin, gold finger and 25 mil microstrip from gold finger edge. The detail of the DUT is shown in Figure 7 and the detail of the testboard is described in Annex D.

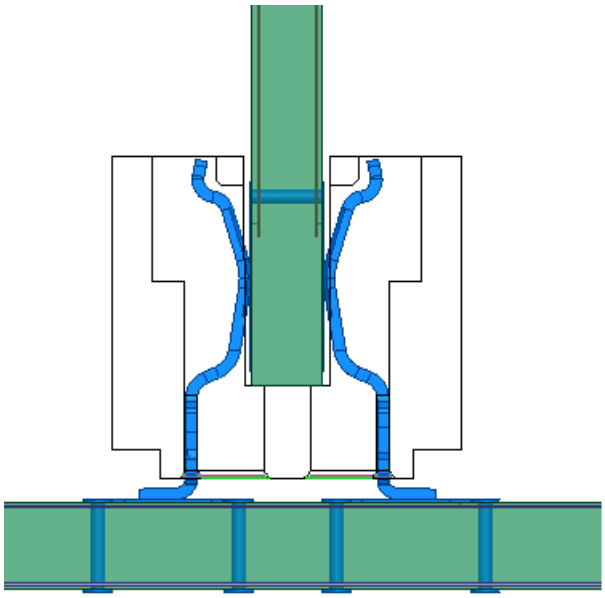


Figure 6: DDR5 288-pin connector.

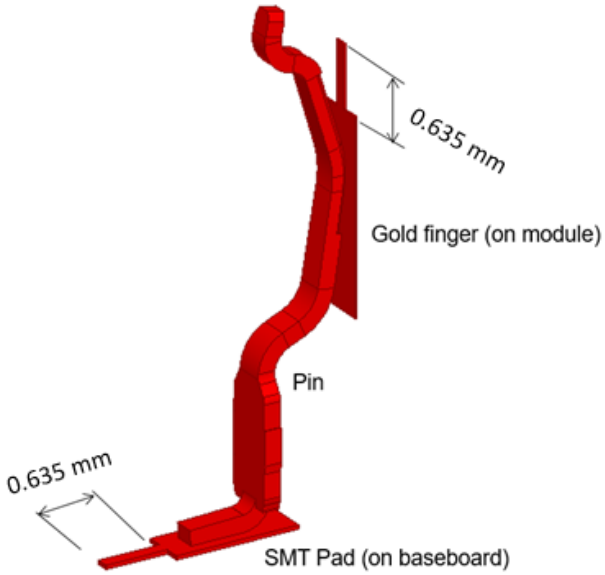


Figure 7: Device under test (DUT)

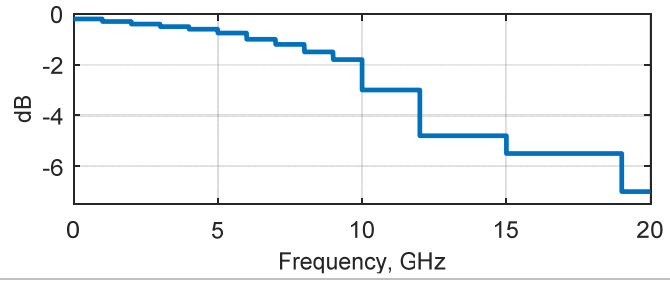
8.1 Frequency domain requirements

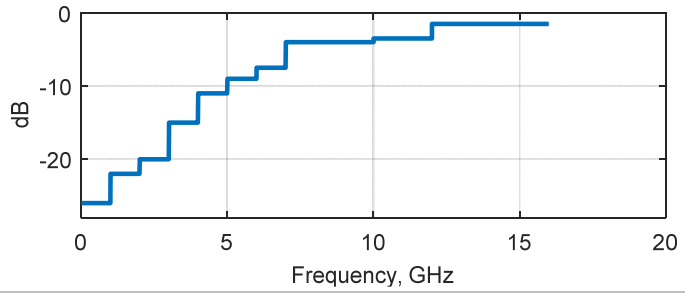
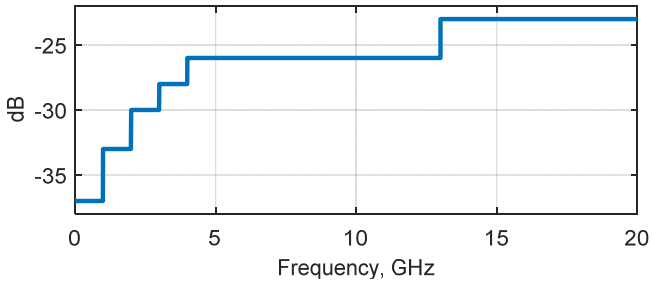
The S-parameter requirements for 288-pin U/L/LR DIMM connector are shown in Table 8.

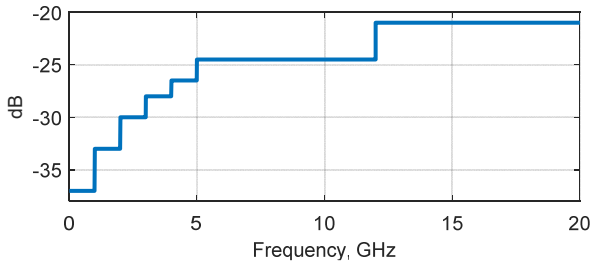
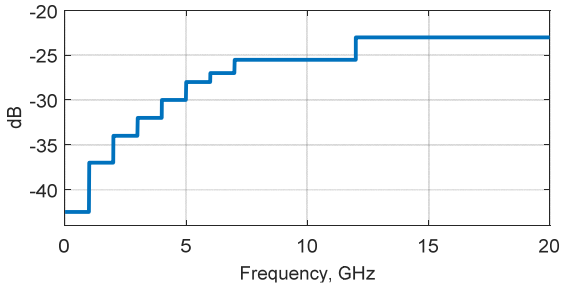
Notes:

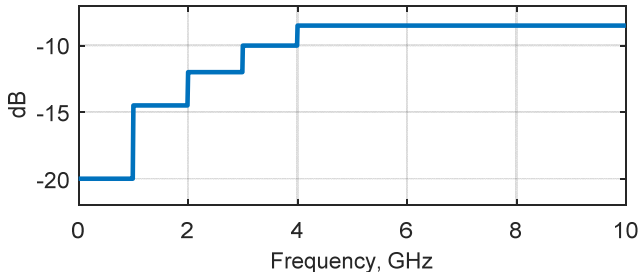
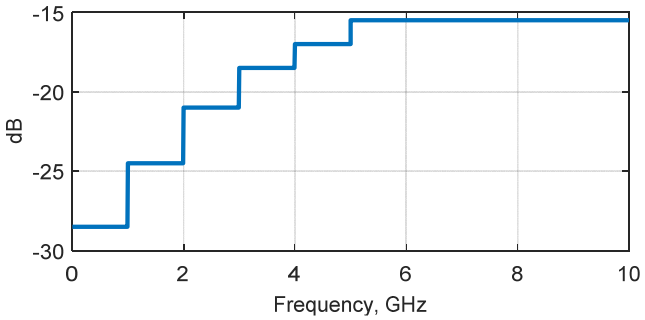
- Effects of the baseboard SMT pad and module gold finger are included
- Reference impedance = 50ohm

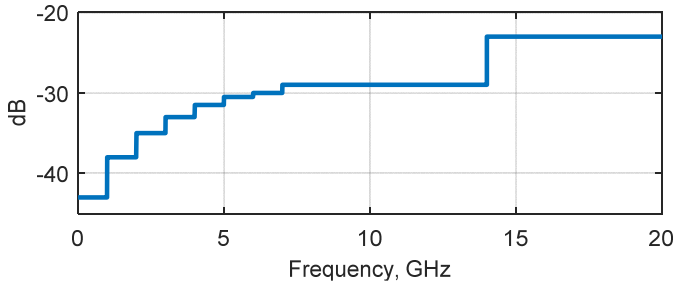
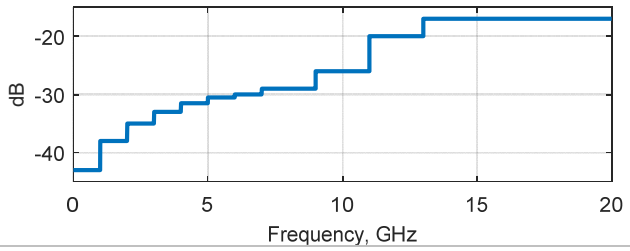
Table 8 - S-parameter requirements

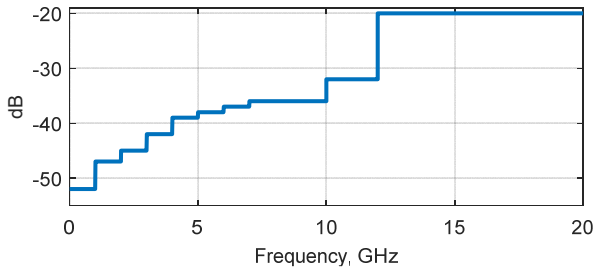
S-Parameter	Target Value
Insertion Loss **Note:** • Signals with 1:1 S/G • Measure from both the baseboard side and module side	> -0.20 dB (f <= 1.0 GHz) > -0.30 dB (1.0 GHz < f <= 2.0 GHz) > -0.40 dB (2.0 GHz < f <= 3.0 GHz) > -0.50 dB (3.0 GHz < f <= 4.0 GHz) > -0.60 dB (4.0 GHz < f <= 5.0 GHz) > -0.75 dB (5.0 GHz < f <= 6.0 GHz) > -1.00 dB (6.0 GHz < f <= 7.0 GHz) > -1.20 dB (7.0 GHz < f <= 8.0 GHz) > -1.50 dB (8.0 GHz < f <= 9.0 GHz) > -1.80 dB (9.0 GHz < f <= 10.0 GHz) > -3.0 dB (10.0 GHz < f <= 12.0 GHz) > -4.8 dB (12.0 GHz < f <= 15.0 GHz) > -5.5 dB (15.0 GHz < f <= 19.0 GHz) > -7.0 dB (19.0 GHz < f <= 20.0 GHz) 

Return Loss **Note:** • Signals with 1:1 S/G • Measure from both the baseboard side and module side	< -26.0 dB (f <= 1.0 GHZ) < -22.0 dB (1.0 GHz < f <= 2.0 GHz) < -20.0 dB (2.0 GHz < f <= 3.0 GHz) < -15.0 dB (3.0 GHz < f <= 4.0 GHz) < -11.0 dB (4.0 GHz < f <= 5.0 GHz) < -9.0 dB (5.0 GHz < f <= 6.0 GHz) < -7.5 dB (6.0 GHz < f <= 7.0 GHz) < -4.0 dB (7.0 GHz < f <= 10.0 GHz) < -3.5 dB (10.0 GHz < f <= 12.0 GHz) < -1.5 dB (12.0 GHz < f <= 16.0 GHz) 
1:1 S/G Same Side NEXT **Note:** • Both the victim and the aggressor are located at the same side • Measure from the baseboard side	< -37.0 dB (f <= 1.0 GHz) < -33.0 dB (1.0 GHz < f <= 2.0 GHz) < -30.0 dB (2.0 GHz < f <= 3.0 GHz) < -28.0 dB (3.0 GHz < f <= 4.0 GHz) < -26.0 dB (4.0 GHz < f <= 13.0 GHz) < -23.0 dB (13.0 GHz < f <= 20.0 GHz) 

1:1 S/G Same Side NEXT **Note:** • Both the victim and the aggressor are located at the same side • Measure from the module side	< -37.0 dB (f <= 1.0 GHz) < -33.0 dB (1.0 GHz < f <= 2.0 GHz) < -30.0 dB (2.0 GHz < f <= 3.0 GHz) < -28.0 dB (3.0 GHz < f <= 4.0 GHz) < -26.5 dB (4.0 GHz < f <= 5.0 GHz) < -24.5 dB (5.0 GHz < f <= 12.0 GHz) < -21.0 dB (12.0 GHz < f <= 20.0 GHz) 
1:1 S/G Same Side FEXT **Note:** • Both the victim and the aggressor locate at the same side • Measure from both the baseboard side and module side	< -42.5 dB (f <= 1.0 GHZ) < -37.0 dB (1.0 GHz < f <= 2.0 GHz) < -34.0 dB (2.0 GHz < f <= 3.0 GHz) < -32.0 dB (3.0 GHz < f <= 4.0 GHz) < -30.0 dB (4.0 GHz < f <= 5.0 GHz) < -28.0 dB (5.0 GHz < f <= 6.0 GHz) < -27.0 dB (6.0 GHz < f <= 7.0 GHz) < -25.5 dB (7.0 GHz < f <= 12.0 GHz) < -23.0 dB (12.0 GHz < f <= 20.0 GHz) 

2:1 S/G Same Side NEXT **Note:** • Both the victim and the aggressor locate at the same side • Measure from both the baseboard side and module side	< -20.0 dB (f <= 1.0 GHZ) < -14.5 dB (1.0 GHz < f <= 2.0 GHz) < -12.0 dB (2.0 GHz < f <= 3.0 GHz) < -10.0 dB (3.0 GHz < f <= 4.0 GHz) < -8.5 dB (4.0 GHz < f <= 10.0 GHz) 
2:1 S/G Same Side FEXT **Note:** • Both the victim and the aggressor locate at the same side • Measure from both the baseboard side and module side	< -28.5 dB (f <= 1.0 GHZ) < -24.5 dB (1.0 GHz < f <= 2.0 GHz) < -21.0 dB (2.0 GHz < f <= 3.0 GHz) < -18.5 dB (3.0 GHz < f <= 4.0 GHz) < -17.0 dB (4.0 GHz < f <= 5.0 GHz) < -15.5 dB (5.0 GHz < f <= 10.0 GHz) 

1:1 S/G Opposite Side NEXT **Note:** • The victim and the aggressor locate at the opposite side • Measure from the baseboard side	< -43.0 dB (f <= 1.0 GHZ) < -38.0 dB (1.0 GHz < f <= 2.0 GHz) < -35.0 dB (2.0 GHz < f <= 3.0 GHz) < -33.0 dB (3.0 GHz < f <= 4.0 GHz) < -31.5 dB (4.0 GHz < f <= 5.0 GHz) < -30.5 dB (5.0 GHz < f <= 6.0 GHz) < -30.0 dB (6.0 GHz < f <= 7.0 GHz) < -29.0 dB (7.0 GHz < f <= 14.0 GHz) < -23.0 dB (14.0 GHz < f <= 20.0 GHz) 
1:1 S/G Opposite Side NEXT **Note:** • The victim and the aggressor locate at the opposite side • Measure from the module side	< -43.0 dB (f <= 1.0 GHZ) < -38.0 dB (1.0 GHz < f <= 2.0 GHz) < -35.0 dB (2.0 GHz < f <= 3.0 GHz) < -33.0 dB (3.0 GHz < f <= 4.0 GHz) < -31.5 dB (4.0 GHz < f <= 5.0 GHz) < -30.5 dB (5.0 GHz < f <= 6.0 GHz) < -30.0 dB (6.0 GHz < f <= 7.0 GHz) < -29.0 dB (7.0 GHz < f <= 9.0 GHz) < -26.0 dB (9.0 GHz < f <= 11.0 GHz) < -20.0 dB (11.0 GHz < f <= 13.0 GHz) < -17.0 dB (13.0 GHz < f <= 20.0 GHz) 

1:1 S/G Opposite Side FEXT **Note:** • The victim and the aggressor locate at the opposite side • Measure from both the baseboard side and module side	< -52.0 dB (f <= 1.0 GHz) < -47.0 dB (1.0 GHz < f <= 2.0 GHz) < -45.0 dB (2.0 GHz < f <= 3.0 GHz) < -42.0 dB (3.0 GHz < f <= 4.0 GHz) < -39.0 dB (4.0 GHz < f <= 5.0 GHz) < -38.0 dB (5.0 GHz < f <= 6.0 GHz) < -37.0 dB (6.0 GHz < f <= 7.0 GHz) < -36.0 dB (7.0 GHz < f <= 10.0 GHz) < -32.0 dB (10.0 GHz < f <= 12.0 GHz) < -20.0 dB (12.0 GHz < f <= 20.0 GHz) 

8.2 Time domain requirements

The DDR5 288-pin connector impedance requirement is shown in Table 9.

Notes:

- Effects of the baseboard SMT pad and module gold finger are included
- Reference impedance = 50ohm
- Rise time: 80ps (10%~90%) or 60ps (20%-80%) at reference plane. Faster rise time on SMA connector will be extracted from the 1X through trace on the testboard.
- TDR launch is from both baseboard side and module side

Table 9 - Connector time domain requirement

Specification	Pass Criteria
Impedance	45~55Ω

Annex A (informative) LLCR Measurements

A.1 Reference equipment

- Micro-ohmmeter (such as Keithly 580; Agilent 4338B)
- Cable with clamper or pogo pins

A.2 Test fixture

Figure A.1 and Figure A.2 illustrate LLCR measurement examples using 4-terminal technique.

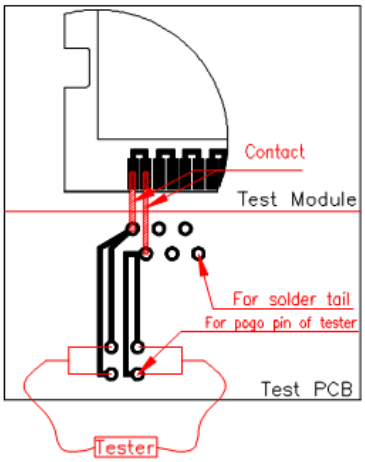


Figure A.1 — 4-wire connection example (two pins in series)

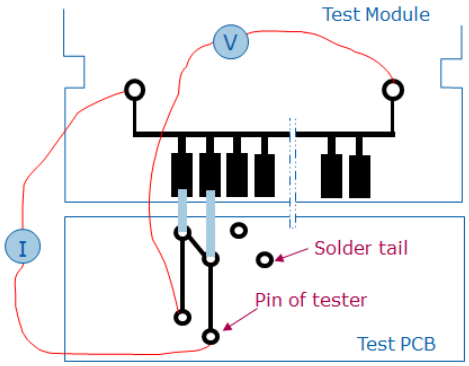


Figure A.2 — 4-wire connection example (two pins in parallel)

Annex B (informative) Current Carrying Capability Testing

B.1 Reference equipment

T-Rise Method (Reference EIA 364-70 Method 2)

B.2 Test procedure

The method is summarized as follows: Minimum of 5 connector samples.

- Ambient system temperature stabilized (testing to occur at ambient system temperature)
  - Current necessary to produce the specified temperature of 30C. (Do not exceed maximum connector temperature rating e.g. 105C)
  - Test multiple contacts (pin 146) and single contact (pin1) in housing per wiring diagram (current through wire 1 and wire 2).
- Report results per EIA 364-70 table “test documentation Annex”.

B.3 Test board daisy chain connection

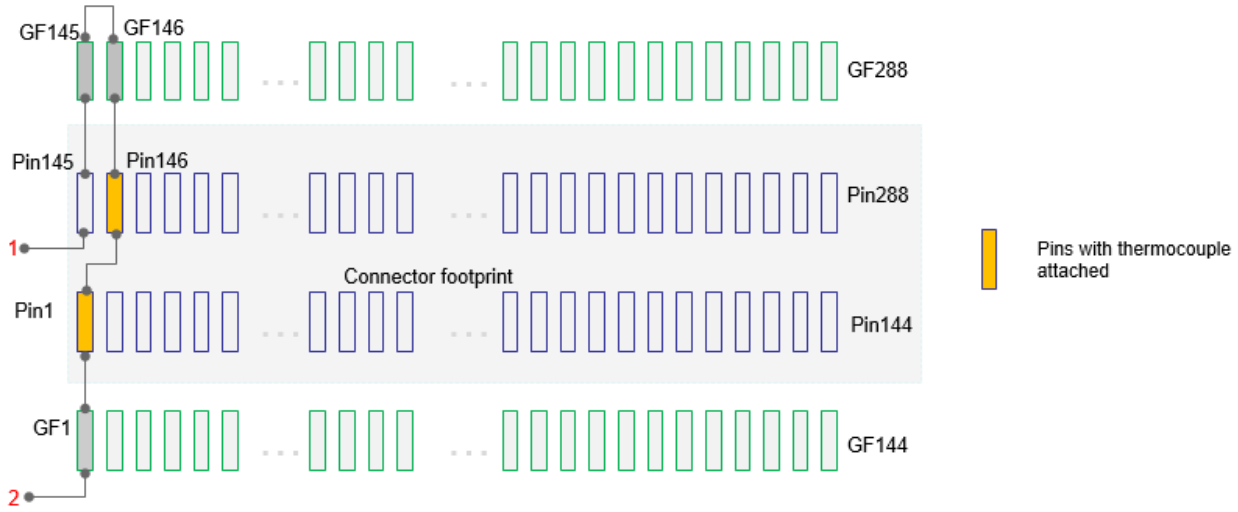


Figure B.1 — Daisy chain connection

Annex C (informative) Shock and vibration test board

C.1 Shock and vibration

Shock and vibration test board to be specified by OEM/ODM due to various system layouts.

C.2 Test Module - weight and center of gravity

- Module 1 weight 53 ± 2 grams and module 2 weight 40 ± 2 grams.
- Module 1 and module 2 are staggered placed, no same module next to each other.
- Center of gravity of module: 18-20 mm from the module mating edge (bottom of the module where gold fingers reside).
- Module thickness: 1.27 +0/-0.10 mm.
- Module to check continuity.

C.3 Shock unpackaged

C.3.1 Purpose

To ensure the boards are sufficiently robust to withstand shocks when shipped in a system. Board Un-packaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.3.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.3.3 Test Conditions

- Trapezoidal shock 50 g ± 10%.
- Velocity change 170 inch/sec, ± 10%.
- Three drops in each of six directions are applied to each of the three samples.

C.4 Vibration unpackaged

C.4.1 Purpose

To ensure the board is sufficiently robust to withstand vibration when mounted in a system, which is being shipped. Board unpackaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.4.2 Quantity

- Investigation: 1 Board
- Validation: 3 Boards

C.4.3 Test Conditions

Random profile:

- 5 Hz @ 0.01 g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up)
- 20 Hz to 500 Hz @ 0.02 g^2/Hz (flat)

- Input acceleration is 3.13 g RMS
- 10 minutes per axis for all 3 axes on all samples
- Random control limit tolerance is ± 3 dB

Annex D (informative) Signal integrity test board

D.1 Reference Equipment

Vector Network Analyzer (VNA) System

2X through calibration capability required.

Connectors: Molex 2.92mm connector (# 0732520090) or equivalent connector

Two 50 Ω high frequency, low loss phase-matched cables. Recommended cables are offered by Micro Coax (part number UFB197C) or equivalence. The cables are used to connect the 2.92mm connector to the measurement ports on the VNA.

D.2 Test board

The testboard includes base board and module card. 2X through calibration traces are included on the base board to save PCB space. There is 1X through trace on base board as well for rise time setup for TDR impedance measurement.

D.2.1 Test board stackup

Figure D.1 describe details of the 4-layer DUT board and DUT module PCB stackup to be used. The DUT board and DUT module impedance are defined as 50 (± 5%) ohms, recommended trace width for the testboard is 6.5mil.

DDR5 U/R/LR DIMM Connector SI Test Board					
Layer Name	Plane Description	Material	Layer Thickness (mm)	Copper Weight (oz)	Impedance (ohm)
	Solder mask		0.015		
Signal 1	SIGNAL		0.045		50 ± 5%
	Core	Rogers (RO4350B) or equivalent	0.100		
Plane 2	GND		0.030	1.0	
	Prepreg	FR4 (S1000-2M) or equivalent	0.890		
Plane 3	GND		0.030	1.0	
	Core	Rogers (RO4350B) or equivalent	0.100		
Signal 4	SIGNAL		0.045		50 ± 5%
	Solder mask		0.015		
			1.27	(+/-0.1)	

Figure D.1 Stackup of DDR5 U/R/LR DIMM connector testboards

D.3.2 Baseboard

The reference plane for deembedded is set to be 0.635mm from SMT pad edge on the baseboard. The trace length from reference plane to 2.92mm connector is 33.48mm. There is a cut out on L2 ground layer underneath for each signal pad, the size of the cut out is the same as the SMT pad.

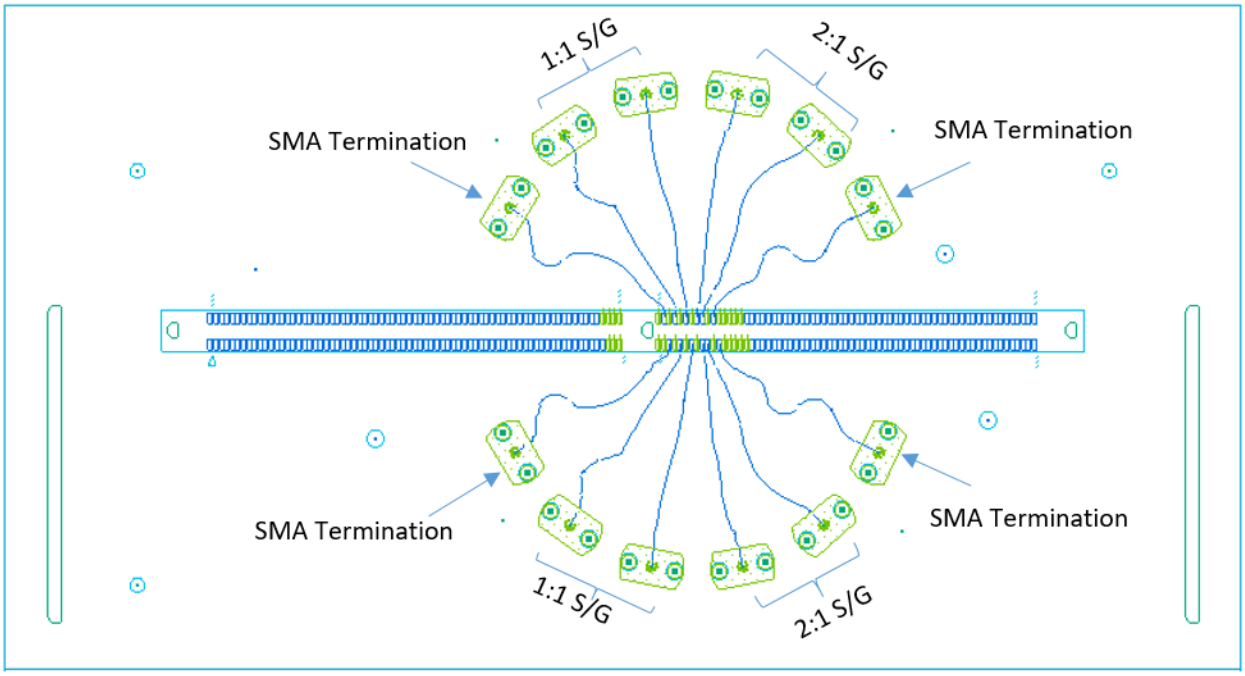


Figure D.2 DDR5 base board

D.3.3 Module card

The reference plane for deembedded is set to be 0.635mm from gold finger pad edge on the module card. The trace length from reference plane to 2.92mm connector is 33.48mm. The L2/L3 ground layer was cut up to the gold finger inside edge.

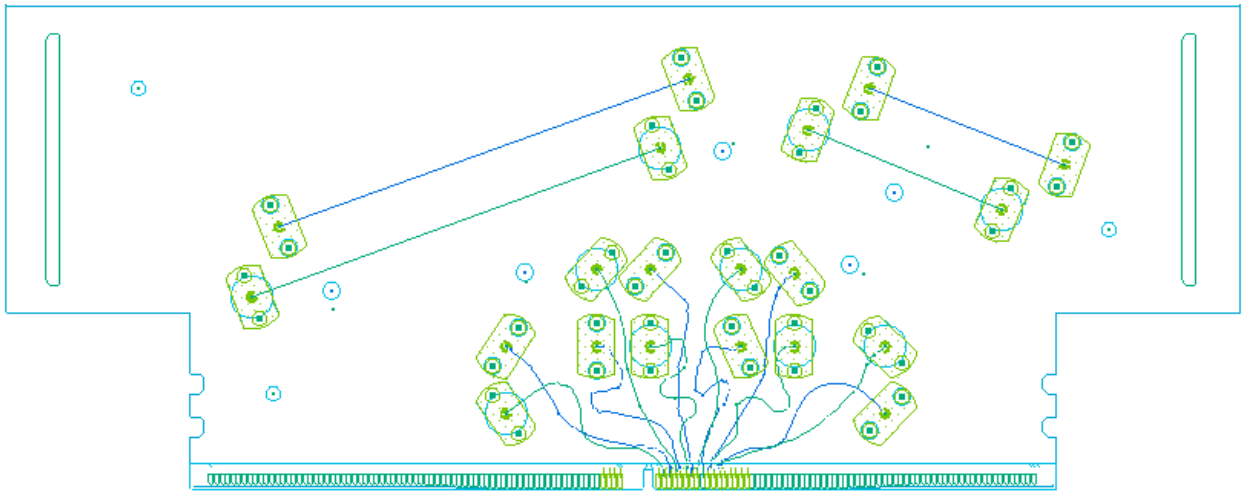
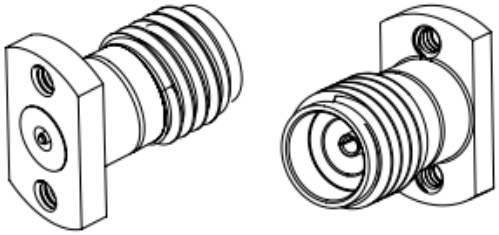


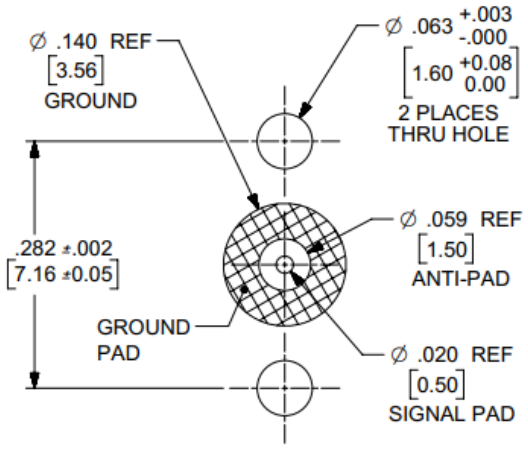
Figure D.3 DDR5 module card

D.3.4 2.92mm connector

Molex 2.92mm connector (# 0732520090) or equivalence is recommended to use, as shown in Figure D.4. The 2.92mm connector will be screw mounted on the PCB for cable vertical access.



(a)



(b)

Figure D.3 (a) 2.92mm connector (b) Recommended footprint of the 2.92mm connector

D. 4 Testing

Any 2.92mm connectors not connected to VNA for testing should be terminated with 50-ohm load.

Annex E (informative) Connector Warpage Measurement at High Temperature

E.1 Reference Equipment

- Refer to JESD22-B112

E.2 Sample Preparation

- A minimum of 3 samples shall be measured to determine variation within an assembly lot.
- The samples are vacuum packed in hard tray before testing

E.3 Test Procedure

- Thermocouple Placement: It is recommended that a thermocouple of gauge 30 or finer is used and that the thermocouple is attached to the center of the connector body using either a thermally conductive epoxy or attached using high temperature polyimide tape.
- Temperature Ramp Rate: The temperature ramp rate during both heating and cooling will influence the measured warpage. Ideally, a temperature ramp rate that can closely match the thermal profile response as seen during board assembly should be used. However, if equipment limitations prevent the achievement of assembly matched ramp rates, the equipment should be configured to achieve as fast a ramp rate as possible without introducing significant temperature differences between the top and bottom of the connector housing body. The temperature profiles in IPC/JEDEC J-STD 020 are useful targets, if achievable. The temperature profiles should be included in the test report.
- Area of measurement
    - Lead coplanarity measurement: The measurement point of each lead at the same side locates at a straight line and 0.1mm - 0.3mm from lead tip, as shown in Figure E.1. The samples can be measured either live bug orientation or dead bug orientation.

Figure E.1 Measurement point and sample orientation

    - Housing warpage: 0.7mm - 1.0mm from bottom of housing at the shaded area as shown in Figure E.2.

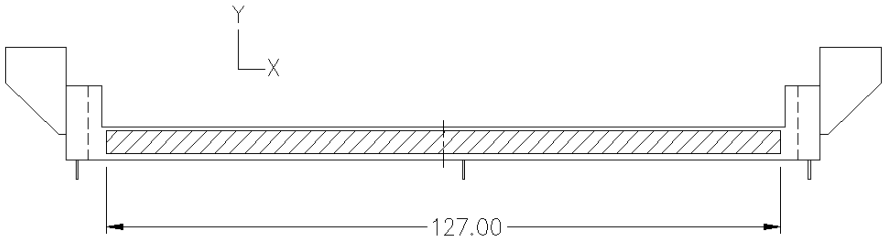


Figure E.2 Measurement point

Annex F (informative) Connector Ejector Reliability

F.1 Test Module

- The outline of the printed circuit board follows MO-329
- The module thickness: 1.27~1.37 mm.

F.2 Sample Preparation

- A minimum of 8 connector samples shall be measured to determine the variation within an assembly lot.
- The samples are mounted on a large baseboard for testing

F.3 Test Procedure

- Step 1: Check both connector and module are at new condition, the module test edge dimensions are compatible to MO-329.
- Step 2: Place the module near the tested connector, align the module edge to the connector tower and the module key to the connector key
- Step 3: Apply force on left corner of module top edge to lock the left side ejector, then press the module to close the right side ejector. Check to make sure the module installation is completed. The unbalanced installation applies to the worse case operation.
- Step 4: Apply force on left ejector to pop up the module, then press the right ejector to uninstall the module. The unbalanced uninstallation applies to the worse case operation.
- Step 5: Repeat step 2 to step 4 with the same module for 25 cycles, at minimum rate of 20 second/cycle
- Step 6: Examine the left ejector for any failure mode. An example of the failure modes is shown in Figure F.2
- Step 7: Repeat the step 1 to step 6 for additional three test samples, using a new module for each new test sample.
- Step 8: Check the right side ejector for four new test samples, with similar procedures from step 1 to step 7.

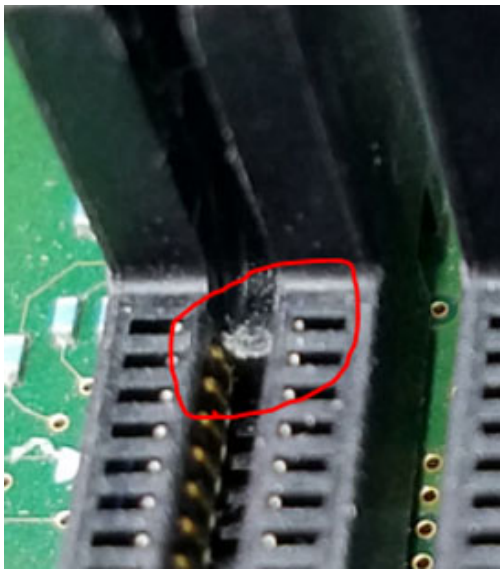


Figure F.2 ejector wear observed

TASK GROUP CONTRIBUTOR

AMPHENOL EAST ASIA LTD.
ARGOSY RESEARCH INC.
DELL INC.
FOXCONN INTERCONNECT TECHNOLOGY LTD
HEWLETT PACKARD ENTERPRISE COMPANY
HP INC.
IBM CORPORATION
INTEL CORPORATION
INVENTEC CORPORATION
LOTES CO. LTD.
LUXSHARE-ICT, INC.
MICRON TECHNOLOGY INC.
MOLEX LLC
SAMSUNG SEMICONDUCTOR
SHENZHEN DEREN ELECTRONIC CO. LTD.
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TE CONNECTIVITY
WLCO SHENZHEN CO. LTD.

CHANGE RECORD

IF THE CHANGE INVOLVES ANY WORDS ADDED OR DELETED (EXCLUDING DELETION OF ACCIDENTALLY REPEATED WORDS), THE CHANGE IS INCLUDEC. PUNCTUATION CHANGES MAY OR MAY NOT BE INCLUDEC.

INITIAL ISSUE: A	Date: DECEMBER 2020	JC11 Item Number: 11.14-203S

CHANGE RECORD HISTORY:

ISSUE: A.01	DATE: JULY 2021	ITEM NUMBER: 11.14-203S
LOCATION:	CHANGED FROM:	CHANGED TO:
Page 3		Add EIA-364-09
Page 9	EIA-364-99	EIA-364-09
Page 26	Apple	Apply

ISSUE: B	DATE: October 2022	ITEM NUMBER: 11.14-213
LOCATION:	CHANGED FROM:	CHANGED TO:
Page 14,15,16,17,18,19		Update table 8 • Extend maximum frequency from 10.0 GHz up to 20.0 GHz for 1:1 S/G S-parameter requirements. • Extend maximum frequency from 5.0 GHz to 10.0 GHz for 2:1 S/G S-parameter requirements. • Add limit plot.