CONNECTOR STANDARD FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS

PS-006
DDR5 262 Pin SODIMM Connector Performance Standard

(Double Data Rate 5)

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Date: September 2024 **Issue: B**
Item: 11.14-226

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DDR5 SODIMM CONNECTOR PERFORMANCE STANDARD

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(From JEDEC Board Ballot JCB-15-57, formulated under the cognizance of the JC-11.14 Subcommittee on Microelectronic Assemblies.)

1 SCOPE

This standard defines the form, fit and function of SODIMM DDR5 connectors for modules supporting channels with transfer rates 6.4 GT/S and beyond. It contains mechanical, electrical and reliability requirements for a one-piece connector mated to a module with nominal thickness of 1.20 mm. The intent of this document is to provide performance standards to enable connector, system designers and manufacturers to build, qualify and use the SODIMM DDR5 connectors in client and server platforms.

1.1 Connector Overview

The 262 pin, 0.50 mm pitch right angle connector is defined for applications where a 1.20 mm nominal thickness module card enters the connector on an angle and rotates parallel to the system board.

2 REFERENCES

The following references provide normative requirements as specified in the body of this standard:

JEDEC JEP95, MO-337: Microelectronic Outline - 262 pin, 0.5mm pitch

JEDEC JEP95, SO-024: Socket Outlines - 262 pin, 0.5mm pitch

EIA-364-1000, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Controlled Environment.

EIA-364-05, Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors

EIA-364-09, Durability Test Procedure for Electrical Connectors and Contacts

EIA-364-13, Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets

EIA 364-23, Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets

EIA-364-27, Shock Test Procedure for Electrical Connectors

EIA-364-28, Vibration Test Procedure for Electrical Connectors and Sockets

EIA-364-29, Contact Retention Test Procedure for Electrical Connectors

EIA-364-31, Humidity Test Procedure for Electrical Connectors and Sockets

EIA-364-32, Thermal Shock Test Procedure for Electrical Connectors and Sockets

EIA 364-70, Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets

JEDEC JESD22-B102, Solderability

JEDEC/ECA JS709A, Definition of “Low-Halogen” for Electronic Product

3 ACRONYMS, TERMS, AND DEFINITIONS

Table 3-1 Acronyms, terms, and definitions

Term	Description
BOL	Beginning of Life
dB	Given in dB-volts, i.e., 20log10(V2/V1)
DDR	Double Data Rate
DUT	Device under test
EIA	Electronics Industry Alliance
EOL	End of Life
Horizontal connector	A connector that accepts a module parallel to the system board
JEDEC	JEDEC Solid State Technology Association
System board	PCB on which the SODIMM DDR5 connector is mounted

4 PIN NUMBERING

This section describes pin numbers in SODIMM DDR5 connectors. The SODIMM DDR5 connector pin list is shown in Table 4-1.

Table 4-1 SODIMM DDR5 Number Sequence

Pin #			**Pin #**
1	Pin	Pin	2
3	Pin	Pin	4
5	Pin	Pin	6
7	Pin	Pin	8
9	Pin	Pin	10
11	Pin	Pin	12
13	Pin	Pin	14
15	Pin	Pin	16
17	Pin	Pin	18
19	Pin	Pin	20
21	Pin	Pin	22
23	Pin	Pin	24
25	Pin	Pin	26
27	Pin	Pin	28
29	Pin	Pin	30
31	Pin	Pin	32
33	Pin	Pin	34
35	Pin	Pin	36
37	Pin	Pin	38
39	Pin	Pin	40
41	Pin	Pin	42
43	Pin	Pin	44
45	Pin	Pin	46
47	Pin	Pin	48
49	Pin	Pin	50
51	Pin	Pin	52
53	Pin	Pin	54
55	Pin	Pin	56
57	Pin	Pin	58
59	Pin	Pin	60
61	Pin	Pin	62
63	Pin	Pin	64
65	Pin	Pin	66
67	Pin	Pin	68
69	Pin	Pin	70
71	Pin	Pin	72
221	Pin	Pin	222
223	Pin	Pin	224
225	Pin	Pin	226
227	Pin	Pin	228
229	Pin	Pin	230
231	Pin	Pin	232
233	Pin	Pin	234

Pin #			**Pin #**
73	Pin	Pin	74
75	Pin	Pin	76
77	Pin	Pin	78
79	Pin	Pin	80
81	Pin	Pin	82
83	Pin	Pin	84
85	Pin	Pin	86
87	Pin	Pin	88
89	Pin	Pin	90
91	Pin	Pin	92
93	Pin	Pin	94
105	Pin	Pin	106
107	Pin	Pin	108
109	Pin	Pin	110
111	Pin	Pin	112
113	Pin	Pin	114
115	Pin	Pin	116
117	Pin	Pin	118
119	Pin	Pin	120
121	Pin	Pin	122
123	Pin	Pin	124
125	Pin	Pin	126
Key			
Key			
Key			
Key			
127	Pin	Pin	128
129	Pin	Pin	130
131	Pin	Pin	132
133	Pin	Pin	134
135	Pin	Pin	136
137	Pin	Pin	138
139	Pin	Pin	140
141	Pin	Pin	142
143	Pin	Pin	144
145	Pin	Pin	146
235	Pin	Pin	236
237	Pin	Pin	238
239	Pin	Pin	240
241	Pin	Pin	242
243	Pin	Pin	244
245	Pin	Pin	246
247	Pin	Pin	248

Pin #			**Pin #**
147	Pin	Pin	148
149	Pin	Pin	150
151	Pin	Pin	152
153	Pin	Pin	154
155	Pin	Pin	156
157	Pin	Pin	158
159	Pin	Pin	160
161	Pin	Pin	162
163	Pin	Pin	164
165	Pin	Pin	166
169	Pin	Pin	170
171	Pin	Pin	172
173	Pin	Pin	174
175	Pin	Pin	176
177	Pin	Pin	178
179	Pin	Pin	180
181	Pin	Pin	182
183	Pin	Pin	184
185	Pin	Pin	186
187	Pin	Pin	188
189	Pin	Pin	190
191	Pin	Pin	192
193	Pin	Pin	194
195	Pin	Pin	196
197	Pin	Pin	198
199	Pin	Pin	200
201	Pin	Pin	202
203	Pin	Pin	204
205	Pin	Pin	206
207	Pin	Pin	208
209	Pin	Pin	210
211	Pin	Pin	212
213	Pin	Pin	214
215	Pin	Pin	216
217	Pin	Pin	218
219	Pin	Pin	220
249	Pin	Pin	250
251	Pin	Pin	252
253	Pin	Pin	254
255	Pin	Pin	262
257	Pin	Pin	258
259	Pin	Pin	260
261	Pin	Pin	262

5 CONNECTOR SOCKET OUTLINE

5.1 SODIMM DDR5 Connector Overview

A primary consideration for SODIMM DDR5 development objective was to scale the connector in an evolutionary manner and minimize the platform volumetric and cost constraints. The mounting technology is surface mount (SMT). SODIMM DDR5 connectors are uniquely keyed to prevent interchangeability with the previous connector generations. The keying capability supports module variations across all SODIMM form factors. The pin count increase to 262 pins is primarily due to 1:1 S:G ratio and GND referenced CA required by signaling performance scalability. The connector pin pitch and the module size are the same as DDR4.

5.2 Socket Outline

A general view of the SODIMM DDR5 DIMM connector with inserted module is shown in Figure 5-1. An example of the socket outlines is shown Figure 5-2.

For the detailed outline, refer to JEDEC JEP95, SO-024. All dimensions are in millimeters.

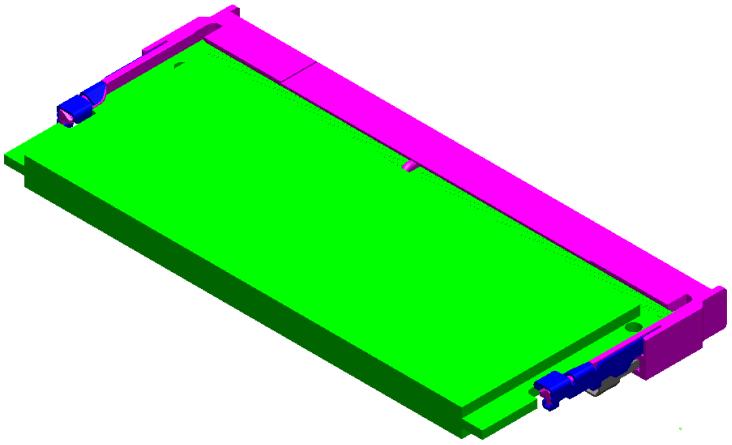


Figure 5-1 SODIMM DDR5 Module and Socket

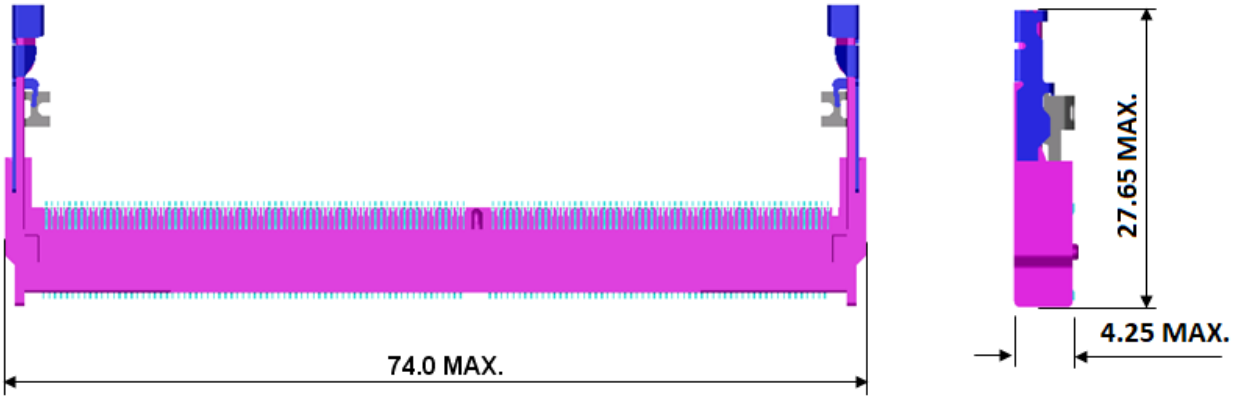


Figure 5-2 SODIMM DDR5 Surface Mount (SMT) Connector Socket Outline 4.0 mm height

5.3 Terminal dimensions

The lead dimensions are recommended in Figure 5-3.

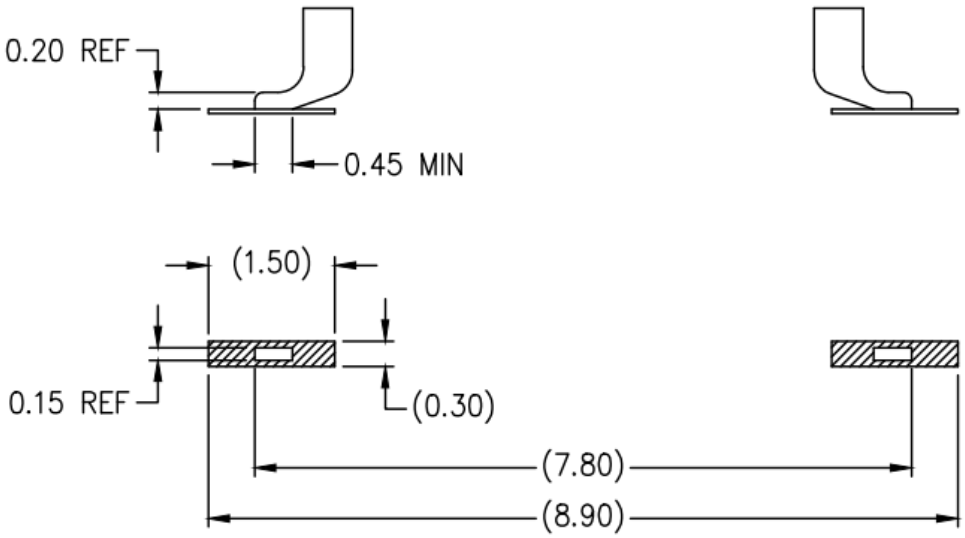


Figure 5-3 SODIMM DDR5 Surface Mount (SMT) Connector Socket Outline 4.0 mm height

6 MODULE OUTLINE

6.1 Module Mechanical Dimensions

SODIMM DDR5 modules are 2mm longer (69.60 mm) and 0.2 mm thicker (1.20 mm) than the SODIMM DDR3. Tightened tolerances on module slot and pad dimensions, in addition to smaller sized pads, are necessary for equivalent mating/shorting performance compared to SODIMM DDR3. The SODIMM DDR5 DIMM outline is shown in Figure 6-1.
For the detailed outline, refer to JEP95, MO-337. All dimensions are in millimeters

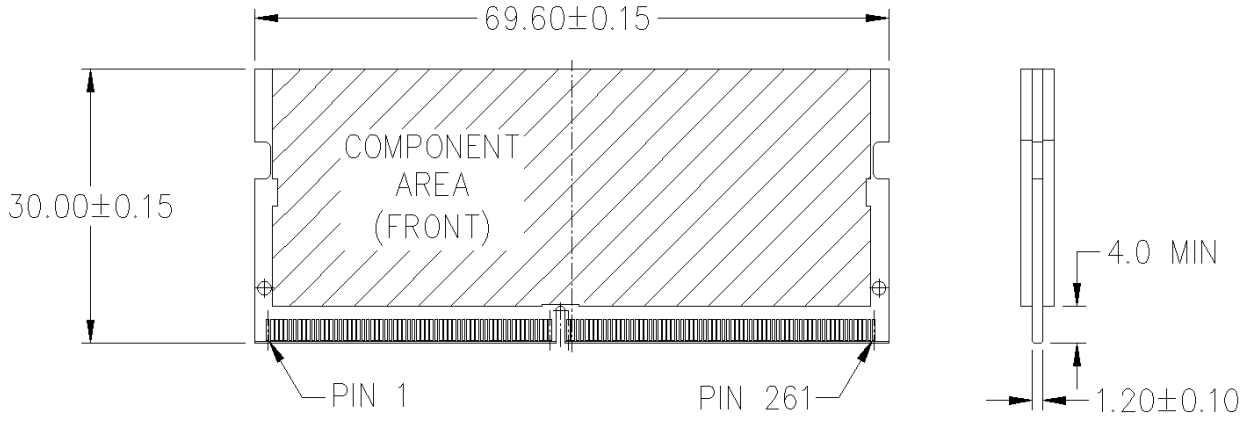


Figure 6-1 SODIMM DDR5 Module Outline

6.2 DIMM gold finger plating options

For the detailed gold finger and plating options, refer to JEDEC JEP95, MO-337.

7 Reliability Requirements

Reliability benchmark testing shall be performed per EIA 364-1000 test groups 1, 2, 3, and 4 for 3, 5, or 7 year lifecycle requirements. A minimum 5 samples are to be tested per subgroup.

7.1 Mechanical and Other Requirements

Table 7-1 Mechanical and Other Requirements

Mechanical Test Description	**Procedure**	**Requirement**
Visual and dimensional inspections	Meets product drawing	Gauge accuracy shall be 10 times more accurate than tolerance specified on drawing and be traceable to NIST
Insertion Force (Module to Connector)	EIA-364-13 Axial Tension/Compression machine such as an Instron Tensile Tester. Rate: 25.4 mm/min.	59.8 N Maximum (with 1.3 mm maximum PCB thickness)
Retention Force - Terminal	EIA 364-29	100 gf minimum per pin; maximum movement of contact of 0.38 mm
Durability (mating/unmating)	EIA 364-09 Perform 25 cycles plug and unplug cycles at a rate of 25.4 mm/minute	LLCR and no nickel plating exposed at contact interface
Additional Tests	**Procedure**	**Requirement**
Solderability - Lead Free	JESD22-B102; Condition C, 8 hours ± 15 minutes steam precondition.	95% coverage minimum
Lead Free Process ability	260 °C, 5 seconds.	No physical damage to connector per visual inspection at 24 inches. No magnification

7.2 Reliability Test Conditions

Table 7-2 Reliability Test Sequence

Test	Test Group			
	1	2	3	4
Low Level Contact Resistance	1,4,6	1,4,6,8	1,4,6	1,4,6,8,10
Reseating	5	7		9
Vibration			3	
Mechanical Shock			5	
Durability (preconditioning)	2	2	2	2
Temperature Life	3			
Temperature Life (preconditioning)				3
Thermal Shock		3		
Cyclic Temp and Humidity		5		
Mixed Flowing Gas				5
Thermal Disturbance				7

7.3 Reliability Test Conditions

Table 7-3 Reliability Test Conditions

Reliability Test Description	Procedure	Requirement
Durability (preconditioning)	EIA-364-09, perform 5 plug/unplug cycles	no evidence of physical damage
Temperature Life Temperature Life (preconditioning)	EIA-364-17, Method A (without electrical load) 60 °C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 8. 60°C field temperature. Test Temperature and Test Duration per EIA 364-1000 Table 9	electrical, mechanical and environmental criteria
Low Level Contact Resistance (LLCR)	EIA-364-23 (termination of connector to board carrier shall be included in the measurements)	Refer to Table 5.4.2
Shock Unpackaged	EIA-364 -27 Trapezoidal shock 50 g, ± 10% Duration 11 ms Velocity change 170 inches/sec, ± 10%	electrical, mechanical and environmental criteria
	Three drops in each of six directions are applied to each of the three samples	

	Detail in Annex C	
Vibration Unpackaged	EIA-364 -28 Random profile: 5 Hz @ 0.01 g2/Hz to 20 Hz @ 0.02 g2/Hz (slope up) 20 Hz to 500 Hz @ 0.02 g2/Hz (flat) Input acceleration is 3.13 g RMS 10 minutes per axis for all 3 axes on all samples Random control limit tolerance is ± 3 dB Detail in Annex C	no discontinuities of ≥ 1 microsecond electrical, mechanical and environmental criteria
Cyclic Temperature & Humidity	EIA-364-31B, Method III without conditioning, initial measurements, cold shock and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 24 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Shock	EIA-364-32, Method A, Table 2, Test Condition 1, -55 °C to 85 °C, perform 5 cycles in mated condition	electrical, mechanical and environmental criteria
Thermal Disturbance	EIA-364-1000, Cycle the connector between 15 °C ± 3 °C and 85 °C ± 3 °C, as measured on the part. Ramps should be a minimum of 2 °C/minute. Dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled; perform 10 cycles in mated condition.	electrical, mechanical and environmental criteria
Mixed Flowing Gas	EIA-364-65, class IIA, Option 4. Expose all specimens in the mated condition for the total mixed flowing gas exposure duration per EIA 364-1000, Table 4.1.	electrical, mechanical and environmental criteria
Reseating	Manually unplug/plug the connector. Perform 3 cycles	No evidence of physical damage

7.4 Environmental Requirements

Table 7-4 Connector Environmental Requirements

Environmental Requirements	Procedure	Requirement
Flammability	UL 94	V-0
Lead Free	RoHS compliant per IEC 62474	RoHS directive (2011/65/EU)
Low Halogen	1000 ppm max Cl when used in a flame retardant 1000 ppm max Br when used in a flame retardant Per JS-709A Standard (Clause 4)	Sample combustion followed by ion chromatography as specified in British Standard Methods BS EN 114582/2007, Characterization of waste – Halogen and sulfur content – Oxygen combustion in closed systems and determination methods OR US EPA-5050 (BOM Preparation Method for Solid Waste)

7.5 Electrical Requirements

Table 7-5 Connector Electrical Requirements

DC Electrical Requirements	Procedure	Requirement
LLCR (Contact resistance)	EIA364-23B Subject mated contacts assembled in housing to 20 mV maximum voltage at 100 mA maximum current	Post Stress: the resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading shall not exceed 20 mΩ
LLCR Contact resistance, Initial	EIA-364 -23	4.0H/5.2H connector: 40 mΩ Max 8.0H/9.2H connector: 55 mΩ Max
Withstanding Voltage	EIA-364-20, Condition I. 250 volts ac at sea level.	One minute hold with no breakdown or flashover.
Insulation resistance	EIA-364 -21	1 MΩ minimum
Current carrying capability at 30 °C temperature rise per contact	EIA-364 Test Procedure 70 Detail in Annex C	1.0 amp/pin De-rated

8 Signal Integrity Requirements

The electrical requirements are measured by the connector and its interfaces with baseboard and module as shown in Figure 8-1. The device under test (DUT) includes 0.635mm microstrip from SMT pad, SMT pad on baseboard, connector pin, gold finger and 0.635mm microstrip from gold finger edge. The detail of the DUT is shown in Figure 8-1 and the detail of the testboard is described in Annex D.

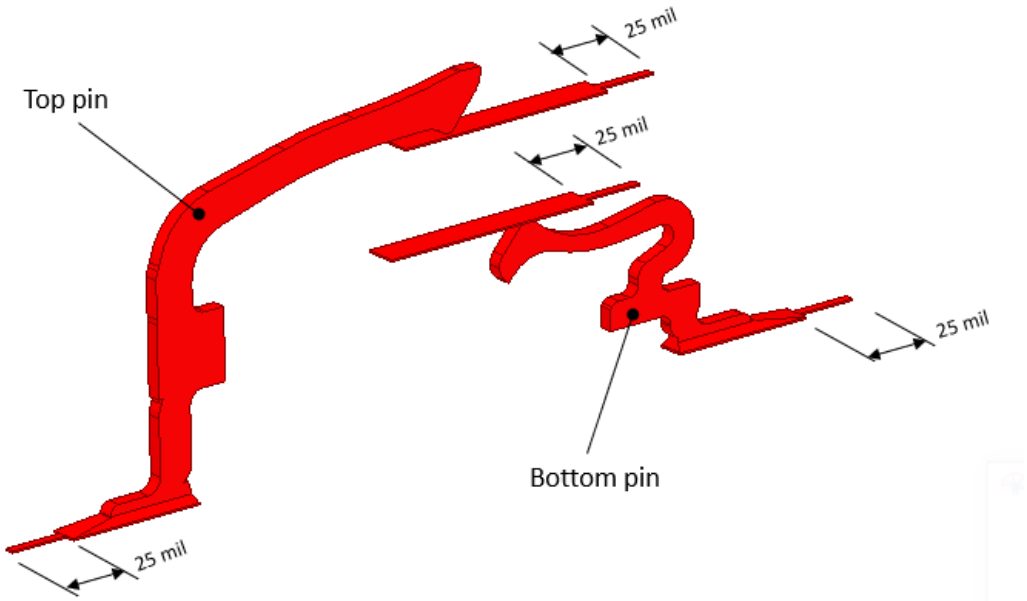


Figure 8-1 Top pin and bottom pin of DDR5 SODIMM connector.

8.1 Skew requirements

The propagation delay is the amount of time it takes for the signal to travel from point A (SMT pad edge) to point B (Gold finger edge). The illustration of the propagation delay of DDR5 SODIMM connector top pin and bottom pin is shown in Figure 8-2

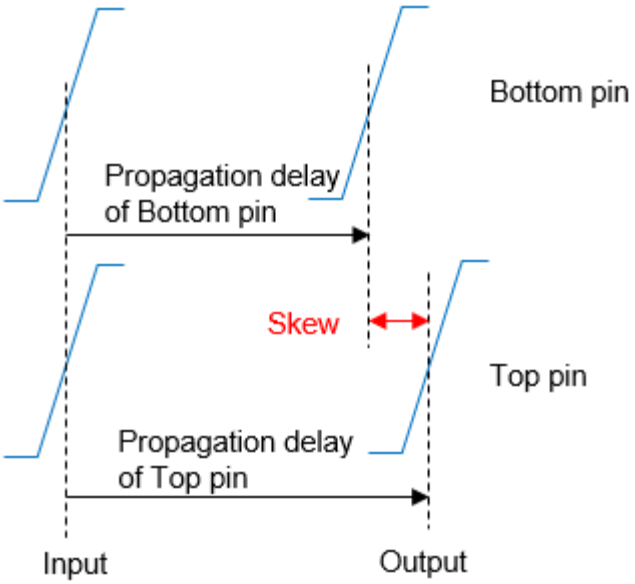


Figure 8-2 Device under test (DUT)

The Skew requirement for 262-pin DDR5 SODIMM connector is shown in Table 2-1

Notes:

- Effects of the baseboard SMT pad and module gold finger are included
- Apply to all DDR5 SODIMM connectors

Table 8-1 DDR5 SODIMM connector skew requirement

Specification	Procedure	Pass Criteria
Skew between top pin and bottom pin	Skew = TP_top – TP_bottom • TP_top: Propagation delay of top pin • TP_bottom: Propagation delay of bottom pin	20 ± 7 (ps)

8.2 Impedance requirements

The DDR5 262-pin connector impedance requirement is shown in

Table 8-2 and Table 8-3.

Notes:

- 4.0H and 5.2H DDR5 SO-DIMM connectors share the same requirement
- 8.0H and 9.2H DDR5 SO-DIMM connectors share the same requirement
- Effects of the baseboard SMT pad and module gold finger are included
- Reference impedance = 50 ohm
- Rise time = 80 ps (10% ~ 90%)
- TDR launch is from baseboard side and module side

Table 8-2 4.0H/5.2H DDR5 SO-DIMM connector impedance requirement

Specification	Pass Criteria (top pin)	Pass Criteria (bottom pin)
Impedance	46 Ω ~ 54 Ω	42 Ω ~ 52 Ω

Table 8-3 8.0H/9.2H DDR5 SO-DIMM connector impedance requirement

Specification	Pass Criteria (top pin)	Pass Criteria (bottom pin)
Impedance	46 Ω ~ 54 Ω	44 Ω ~ 52 Ω

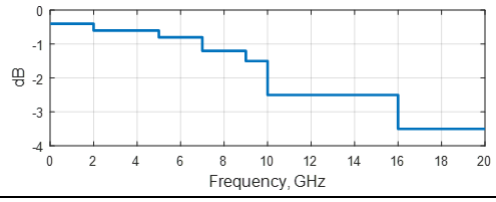
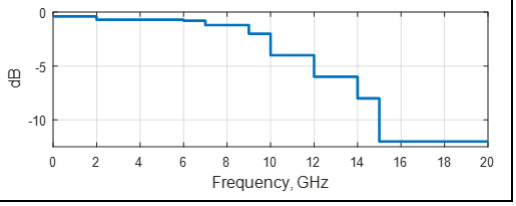
8.3 Frequency domain requirements

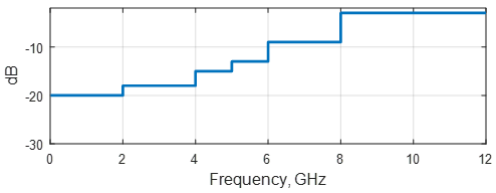
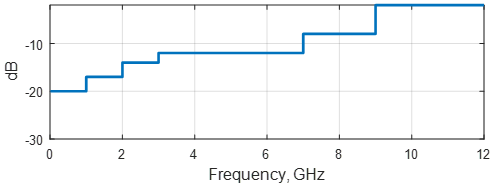
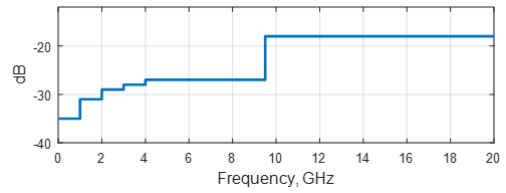
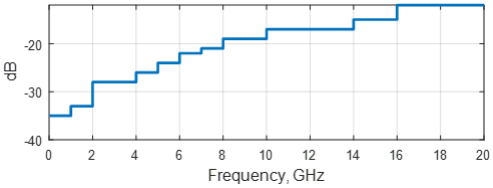
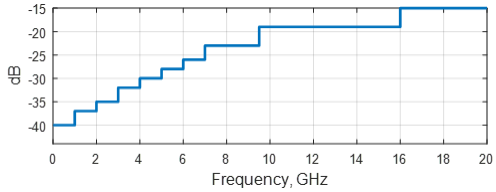
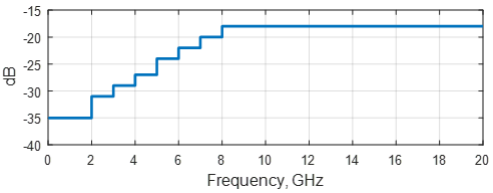
The S-parameter requirements for DDR5 262-pin SODIMM connector are shown from Table 8-4 to Table 8-5

Notes:

- Effects of the baseboard SMT pad and module gold finger are included
- Reference impedance = 50ohm

Table 8-4 4.0H/5.2H DDR5 SODIMM connector S-parameter requirements

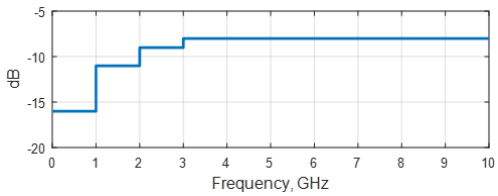
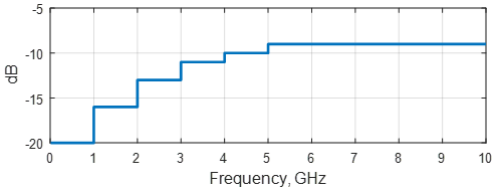
S-Parameter	Target Value (top pin)	Target Value (bottom pin)
Insertion Loss **Note:** Signals with 1:1 S/G	> -0.40 dB (f <= 2.0 GHz) > -0.60 dB (2.0 GHz < f <= 5.0 GHz) > -0.80 dB (5.0 GHz < f <= 7.0 GHz) > -1.20 dB (7.0 GHz < f <= 9.0 GHz) > -1.50 dB (9.0 GHz < f <= 10.0 GHz) > -2.50 dB (10.0 GHz < f <= 16.0 GHz) > -3.50 dB (16.0 GHz < f <= 20.0 GHz) 	> -0.40 dB (f <= 2.0 GHz) > -0.70 dB (2.0 GHz < f <= 6.0 GHz) > -0.80 dB (6.0 GHz < f <= 7.0 GHz) > -1.20 dB (7.0 GHz < f <= 9.0 GHz) > -2.0 dB (9.0 GHz < f <= 10.0 GHz) > -4.00 dB (10.0 GHz < f <= 12.0 GHz) > -6.00 dB (12.0 GHz < f <= 14.0 GHz) > -8.00 dB (14.0 GHz < f <= 15.0 GHz) > -12.00 dB (15.0 GHz < f <= 20.0 GHz) 

Return Loss **Note:** Signals with 1:1 S/G	< -20.0 dB (f <= 2.0 GHZ) < -18.0 dB (2.0 GHz < f <= 4.0 GHz) < -15.0 dB (4.0 GHz < f <= 5.0 GHz) < -13.0 dB (5.0 GHz < f <= 6.0 GHz) < -9.0 dB (6.0 GHz < f <= 8.0 GHz) < -3.0 dB (8.0 GHz < f <= 12.0 GHz) 	< -20.0 dB (f <= 1.0 GHZ) < -17.0 dB (1.0 GHz < f <= 2.0 GHz) < -14.0 dB (2.0 GHz < f <= 3.0 GHz) < -12.0 dB (3.0 GHz < f <= 7.0 GHz) < -8.0 dB (7.0 GHz < f <= 9.0 GHz) < -2.0 dB (9.0 GHz < f <= 12.0 GHz) 
1:1 S/G Same Side NEXT **Note:** Both the victim and the aggressor are located at the same side	< -35.0 dB (f <= 1.0 GHZ) < -31.0 dB (1.0 GHz < f <= 2.0 GHz) < -29.0 dB (2.0 GHz < f <= 3.0 GHz) < -28.0 dB (3.0 GHz < f <= 4.0 GHz) < -27.0 dB (4.0 GHz < f <= 9.5 GHz) < -18.0 dB (9.5 GHz < f <= 20.0 GHz) 	< -35.0 dB (f <= 1.0 GHZ) < -33.0 dB (1.0 GHz < f <= 2.0 GHz) < -28.0 dB (2.0 GHz < f <= 4.0 GHz) < -26.0 dB (4.0 GHz < f <= 5.0 GHz) < -24.0 dB (5.0 GHz < f <= 6.0 GHz) < -22.0 dB (6.0 GHz < f <= 7.0 GHz) < -21.0 dB (7.0 GHz < f <= 8.0 GHz) < -19.0 dB (8.0 GHz < f <= 10.0 GHz) < -16.0 dB (10GHz < f <= 14.0 GHz) < -15.0 dB (14.0 GHz < f <= 16.0 GHz) < -12.0 dB (16.0 GHz < f <= 20.0 GHz) 
1:1 S/G Same Side FEXT **Note:** Both the victim and the aggressor are located at the same side	< -40.0 dB (f <= 1.0 GHZ) < -37.0 dB (1.0 GHz < f <= 2.0 GHz) < -35.0 dB (2.0 GHz < f <= 3.0 GHz) < -32.0 dB (3.0 GHz < f <= 4.0 GHz) < -30.0 dB (4.0 GHz < f <= 5.0 GHz) < -28.0 dB (5.0 GHz < f <= 6.0 GHz) < -26.0 dB (6.0 GHz < f <= 7.0 GHz) < -23.0 dB (7.0 GHz < f <= 9.5 GHz) < -19.0 dB (9.5 GHz < f <= 16.0 GHz) < -15.0 dB (16.0 GHz < f <= 20.0 GHz) 	< -35.0 dB (f <= 2.0 GHZ) < -31.0 dB (2.0 GHz < f <= 3.0 GHz) < -29.0 dB (3.0 GHz < f <= 4.0 GHz) < -27.0 dB (4.0 GHz < f <= 5.0 GHz) < -24.0 dB (5.0 GHz < f <= 6.0 GHz) < -22.0 dB (6.0 GHz < f <= 7.0 GHz) < -20.0 dB (7.0 GHz < f <= 8.0 GHz) < -18.0 dB (8.0 GHz < f <= 20.0 GHz 

<table>
<tr>
<td>2:1 S/G Same Side NEXT

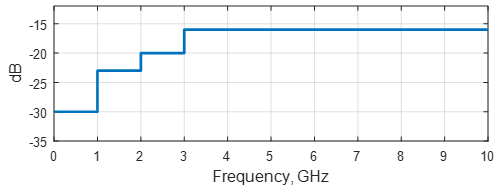
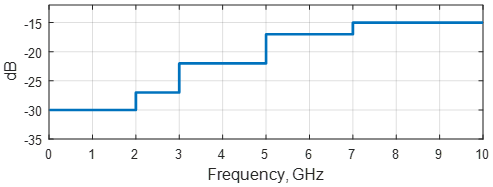
<u>Note:</u>

Both the victim and the aggressor are located at the same side</td>
<td>< -16.0 dB (f <= 1.0 GHZ)
< -11.0 dB (1.0 GHz < f <= 2.0 GHz)
< -9.0 dB (2.0 GHz < f <= 3.0 GHz)
< -8.0 dB (3.0 GHz < f <= 10.0 GHz)

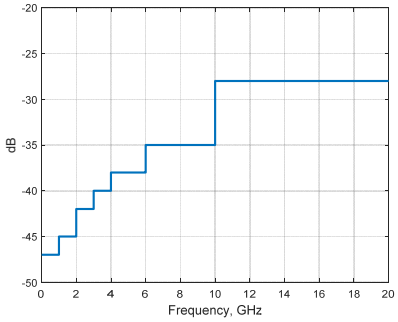
  </td>
<td>< -20.0 dB (f <= 1.0 GHZ)
< -16.0 dB (1.0 GHz < f <= 2.0 GHz)
< -13.0 dB (2.0 GHz < f <= 3.0 GHz)
< -11.0 dB (3.0 GHz < f <= 4.0 GHz)
< -10.0 dB (4.0 GHz < f <= 5.0 GHz)
< -9.0 dB (5.0 GHz < f <= 10.0GHz)
  </td>
</tr>
<tr>
<td>2:1 S/G Same Side FEXT

<u>Note:</u>

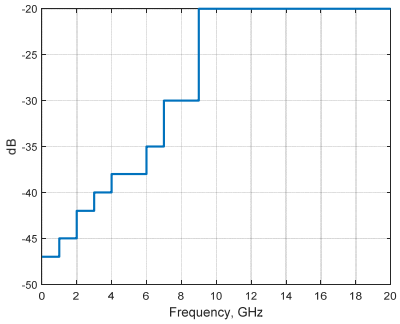
Both the victim and the aggressor are located at the same side</td>
<td>< -30.0 dB (f <= 1.0 GHZ)
< -23.0 dB (1.0 GHz < f <= 2.0 GHz)
< -20.0 dB (2.0 GHz < f <= 3.0 GHz)
< -16.0 dB (3.0 GHz < f <= 10.0 GHz)

  </td>
<td>< -30.0 dB (f <= 2.0 GHZ)
< -27.0 dB (2.0 GHz < f <= 3.0 GHz)
< -22.0 dB (3.0 GHz < f <= 5.0 GHz)
< -17.0 dB (5.0 GHz < f <= 7.0GHz)
< -15.0 dB (7.0 GHz < f <= 10.0GHz)
  </td>
</tr>
<tr>
<td>1:1 S/G Opposite Side NEXT

<u>Note:</u>

The victim and the aggressor are located at the opposite side, measured from SMT footprint side</td>
<td>< -47.0 dB (f <= 1.0 GHZ)
< -45.0 dB (1.0 GHz < f <= 2.0 GHz)
< -42.0 dB (2.0 GHz < f <= 3.0 GHz)
< -40.0 dB (3.0 GHz < f <= 4.0 GHz)
< -38.0 dB (4.0 GHz < f <= 6.0 GHz)
< -35.0 dB (6.0 GHz < f <= 10.0 GHz)
< -28.0 dB (10.0 GHz < f <= 20.0 GHz)</td>
<td>  </td>
</tr>
<tr>
<td>1:1 S/G Opposite Side NEXT

<u>Note:</u>

The victim and the aggressor are located at the opposite side, measured from gold finger side</td>
<td>< -47.0 dB (f <= 1.0 GHZ)
< -45.0 dB (1.0 GHz < f <= 2.0 GHz)
< -42.0 dB (2.0 GHz < f <= 3.0 GHz)
< -40.0 dB (3.0 GHz < f <= 4.0 GHz)
< -38.0 dB (4.0 GHz < f <= 6.0 GHz)
< -35.0 dB (6.0 GHz < f <= 7.0 GHz)
< -30.0 dB (7.0 GHz < f <= 9.0 GHz)
< -20.0 dB (9.0 GHz < f <= 20.0 GHz)</td>
<td>  </td>
</tr>
</table>

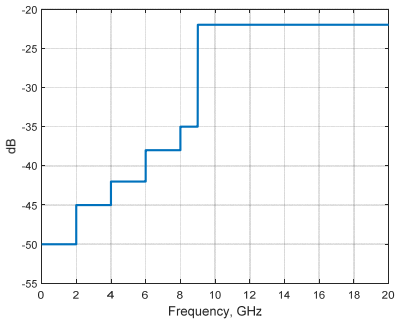
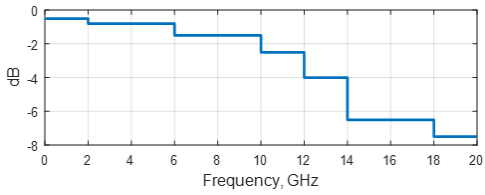
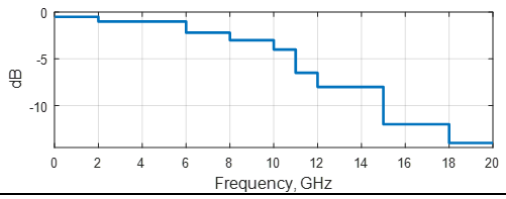
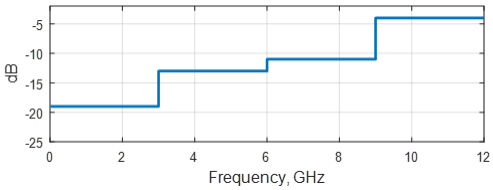
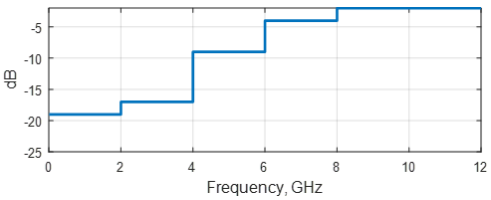
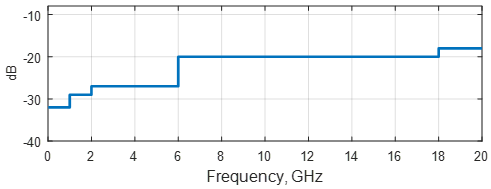
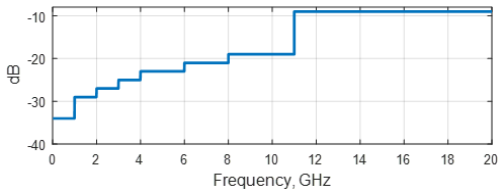
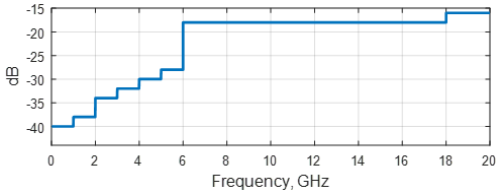
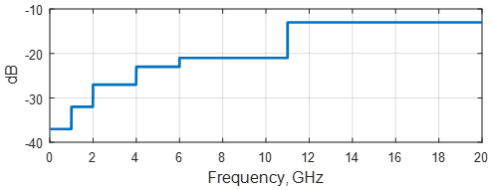
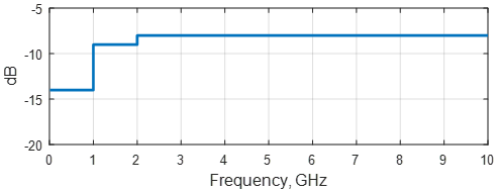
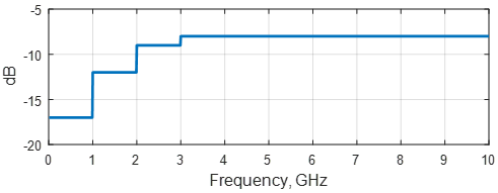
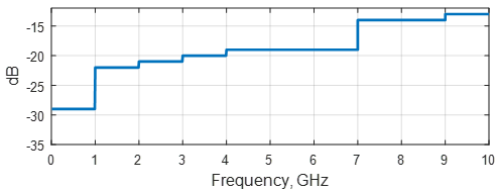
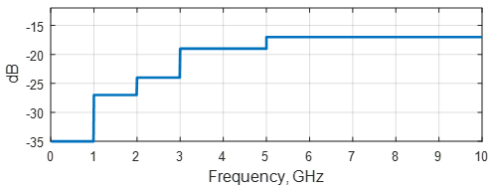
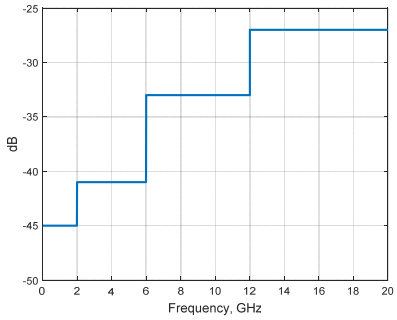
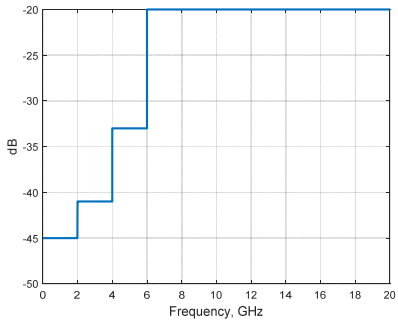
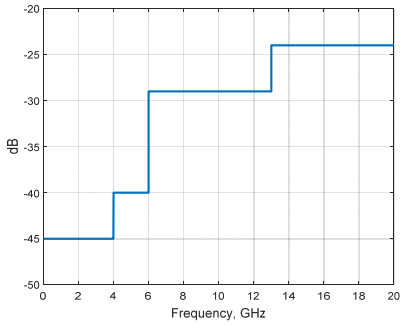
1:1 S/G Opposite Side FEXT **Note:** The victim and the aggressor are located at the opposite side.	< -50.0 dB (f <= 2.0 GHZ) < -45.0 dB (2.0 GHz < f <= 4.0 GHz) < -42.0 dB (4.0 GHz < f <= 6.0 GHz) < -38.0 dB (6.0 GHz < f <= 8.0 GHz) < -35.0 dB (8.0 GHz < f <= 9.0 GHz) < -22.0 dB (9.0 GHz < f <= 20.0 GHz)	

Table 8-5 8.0H/9.2H DDR5 SODIMM connector S-parameter requirements

S-Parameter	Target Value (top pin)	Target Value (bottom pin)
Insertion Loss **Note:** Signals with 1:1 S/G	> -0.50 dB (f <= 2.0 GHz) > -0.80 dB (2.0 GHz < f <= 6.0 GHz) > -1.50dB (6.0 GHz < f <= 10.0 GHz) > -2.50 dB (10.0 GHz < f <= 12.0 GHz) > -4.00 dB (12.0 GHz < f <= 14.0 GHz) > -6.50 dB (14.0 GHz < f <= 18.0 GHz) > -7.50 dB (18.0 GHz < f <= 20.0 GHz) 	> -0.50 dB (f <= 2.0 GHz) > -1.00 dB (2.0 GHz < f <= 6.0 GHz) > -2.20 dB (6.0 GHz < f <= 8.0 GHz) > -3.0 dB (8.0 GHz < f <= 10.0 GHz) > -4.0 dB (10.0 GHz < f <= 11.0 GHz) > -6.50 dB (11.0 GHz < f <= 12.0 GHz) > -8.0 dB (12.0 GHz < f <= 15.0 GHz) > -12.0 dB (15.0 GHz < f <= 18.0 GHz) > -14.0 dB (18.0 GHz < f <= 20.0 GHz) 
Return Loss **Note:** Signals with 1:1 S/G	< -19.0 dB (f <= 3.0 GHZ) < -13.0 dB (3.0 GHz < f <= 6.0 GHz) < -11.0 dB (6.0 GHz < f <= 9.0 GHz) < -4.0 dB (9.0 GHz < f <= 12.0 GHz) 	< -19.0 dB (f <= 2.0 GHZ) < -17.0 dB (2.0 GHz < f <= 4.0 GHz) < -9.0 dB (4.0 GHz < f <= 6.0 GHz) < -4.0 dB (6.0 GHz < f <= 8.0 GHz) < -2.0 dB (8.0 GHz < f <= 12.0 GHz) 

1:1 S/G Same Side NEXT **Note:** The victim and the aggressor are located at the same side	< -32.0 dB (f <= 1.0 GHZ) < -29.0 dB (1.0 GHz < f <= 2.0 GHz) < -27.0 dB (2.0 GHz < f <= 6.0 GHz) < -20.0 dB (6.0 GHz < f <= 18.0 GHz) < -18.0 dB (18.0 GHz < f <= 20.0 GHz) 	< -34.0 dB (f <= 1.0 GHZ) < -29.0 dB (1.0 GHz < f <= 2.0 GHz) < -27.0 dB (2.0 GHz < f <= 3.0 GHz) < -25.0 dB (3.0 GHz < f <= 4.0 GHz) < -23.0 dB (4.0 GHz < f <= 6.0 GHz) < -21.0 dB (6.0 GHz < f <= 8.0 GHz) < -19.0 dB (8.0 GHz < f <= 11.0 GHz) < -9.0 dB (11.0 GHz < f <= 20.0 GHz) 
1:1 S/G Same Side FEXT **Note:** Both the victim and the aggressor are located at the same side	< -40.0 dB (f <= 1.0 GHZ) < -38.0 dB (1.0 GHz < f <= 2.0 GHz) < -34.0 dB (2.0 GHz < f <= 3.0 GHz) < -32.0 dB (3.0 GHz < f <= 4.0 GHz) < -30.0 dB (4.0 GHz < f <= 5.0 GHz) < -28.0 dB (5.0 GHz < f <= 6.0 GHz) < -18.0 dB (6.0 GHz < f <= 18.0 GHz) < -16.0 dB (18.0 GHz < f <= 20.0 GHz) 	< -37.0 dB (f <= 1.0 GHZ) < -32.0 dB (1.0 GHz < f <= 2.0 GHz) < -27.0 dB (2.0 GHz < f <= 4.0 GHz) < -23.0 dB (4.0 GHz < f <= 6.0 GHz) < -21.0 dB (6.0 GHz < f <= 11.0 GHz) < -13.0 dB (11.0 GHz < f <= 20.0 GHz) 
2:1 S/G Same Side NEXT **Note:** Both the victim and the aggressor are located at the same side	< -14.0 dB (f <= 1.0 GHZ) < -9.0 dB (1.0 GHz < f <= 2.0 GHz) < -8 dB (2.0 GHz < f <= 10.0 GHz) 	< -17.0 dB (f <= 1.0 GHZ) < -12.0 dB (1.0 GHz < f <= 2.0 GHz) < -9.0 dB (2.0 GHz < f <= 3.0 GHz) < -8.0 dB (3.0 GHz < f <= 10.0 GHz) 

2:1 S/G Same Side FEXT **Note:** Both the victim and the aggressor are located at the same side	< -29.0 dB (f <= 1.0 GHZ) < -22.0 dB (1.0 GHz < f <= 2.0 GHz) < -21.0 dB (2.0 GHz < f <= 3.0 GHz) < -20.0 dB (3.0 GHz < f <= 4.0 GHz) < -19.0 dB (4.0 GHz < f <= 7.0 GHz) < -14.0 dB (7.0 GHz < f <= 9.0 GHz) < -13.0 dB (9.0 GHz < f <= 10.0 GHz) 	< -35.0 dB (f <= 1.0 GHZ) < -27.0 dB (1.0 GHz < f <= 2.0 GHz) < -24.0 dB (2.0 GHz < f <= 3.0 GHz) < -19.0 dB (3.0 GHz < f <= 5.0GHz) < -17.0 dB (5.0 GHz < f <= 10.0GHz) 
1:1 S/G Opposite Side NEXT **Note:** The victim and the aggressor are located at the opposite side, measured from SMT footprint side	< -45.0 dB (f <= 2.0 GHZ) < -41.0 dB (2.0 GHz < f <= 6.0 GHz) < -33.0 dB (6.0 GHz < f <= 12.0 GHz) < -27.0 dB (12.0 GHz < f <= 20.0 GHz)	
1:1 S/G Opposite Side NEXT **Note:** The victim and the aggressor are located at the opposite side, measured from gold finger side	< -45.0 dB (f <= 2.0 GHZ) < -41.0 dB (2.0 GHz < f <= 4.0 GHz) < -33.0 dB (4.0 GHz < f <= 6.0 GHz) < -20.0 dB (6.0 GHz < f <= 20.0 GHz)	
1:1 S/G Opposite Side FEXT **Note:** The victim and the aggressor are located at the opposite side	< -45.0 dB (f <= 4.0 GHZ) < -40.0 dB (4.0 GHz < f <= 6.0 GHz) < -29.0 dB (6.0 GHz < f <= 13.0 GHz) < -24.0 dB (13.0 GHz < f <= 20.0 GHz)	

Annex A LLCR Measurements

A.1 Reference Equipment

Micro-ohmmeter (such as Keithly 580; Agilent 4338B)

Cable with clamper or pogo pins

A.2 Test Fixture

Figure A1 and A2 illustrates LLCR measurement examples using 4-terminal technique.

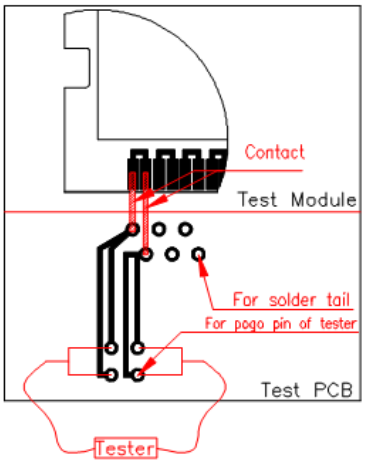


Figure A-1 4-wire connection example (two pins in series)

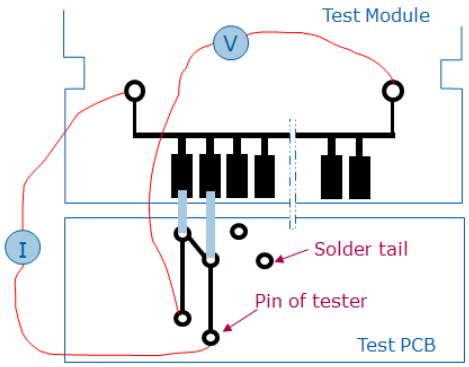


Figure A-2 4-wire connection example (two pins in parallel)

Annex B Current Carrying Capability Testing

B.1 Reference Equipment

T-Rise Method (Reference EIA 364-70 Method 2)

B.2 Test Procedure

The method summary as follows: Minimum of 5 connector samples.

- Ambient system temperature stabilized (testing to occur at ambient system temperature)
  - Current necessary to produce the specified temperature of 30 °C. (Do not exceed maximum connector temperature rating e.g., 105 °C)
  - Test multiple contacts in housing per wiring diagram, current through wire 1 and wire 2 for top pin measurement and current through wire 2 and wire 4 for bottom pin measurement.
- Report results per EIA 364-70 Table “test documentation Annex”.

B.3 Test Board Daisy Chain Connection

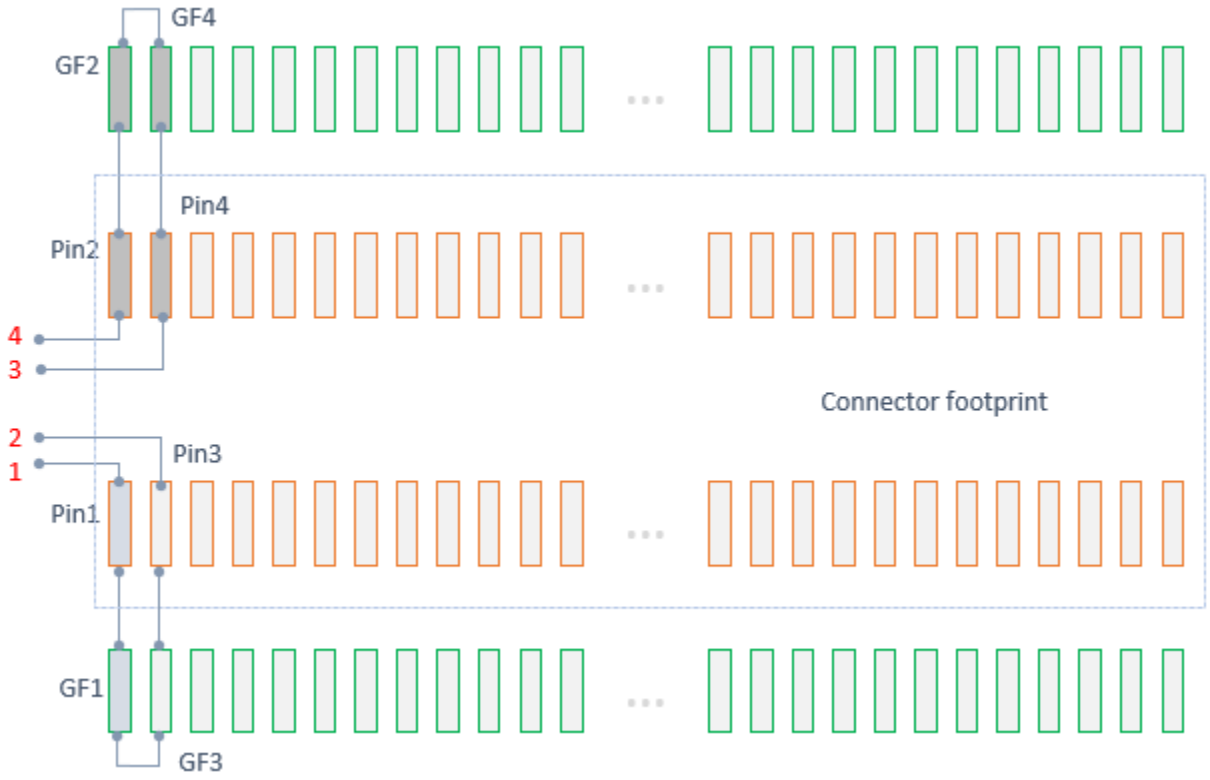


Figure B-1 Daisy chain connection

Annex C Shock and Vibration Test Board

C.1 Shock and Vibration

Shock and Vibration Test Board to be specified by OEM/ODM due to various system layouts

C.2 Test Module - Weight and Center of Gravity

Module weight 9.1 ± 1 grams. Center of Gravity (COG): 35 mm measured from Pin 1 corner of module, 17mm measured from gold finger edge.

Module thickness: 1.20 ± 0.1 mm

Module to check continuity

C.3 Shock Unpackaged

C.3.1 Purpose

To ensure the boards are sufficiently robust to withstand shocks when shipped in a system. Board Unpackaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.3.2 Quantity

Investigation: 1 Board

Validation: 3 Boards

C.3.2 Test Conditions

Trapezoidal shock 50 g, ± 10%

Velocity change 170 inches/sec, ± 10%

Three drops in each of six directions are applied to each of the three samples

C.4 Vibration Unpackaged

C.4.1 Purpose

To ensure the board is sufficiently robust to withstand vibration when mounted in a system, which is being shipped. Board unpackaged testing does not pre-qualify a board for shipping as an un-mounted unit inside a shipping container.

C.4.2 Quantity

Investigation: 1 Board

Validation: 3 Boards

C.3.2 Test Conditions

Random profile:

5 Hz @ 0.01 g2/Hz to 20 Hz @ 0.02 g2/Hz (slope up)

20 Hz to 500 Hz @ 0.02 g2/Hz (flat)

Input acceleration is 3.13 g RMS

10 minutes per axis for all 3 axes on all samples

Random control limit tolerance is ± 3 dB

Annex D (informative) Signal integrity test board

D.1 Reference Equipment

Vector Network Analyzer (VNA) System

2X through calibration capability required.

Connectors: Molex 2.92mm connector (# 0732520090) or equivalent connector

Two 50 Ω high frequency, low loss phase-matched cables. Recommended cables are offered by Micro Coax (part number UFB197C) or equivalence. The cables are used to connect the 2.92mm connector to the measurement ports on the VNA.

D.2 Test board

The testboard includes base board and module card. 2X through calibration traces are included on the base board to save PCB space.

D.2.1 Test board stackup

Figure D.1 describe details of the 4-layer DUT board and DUT module PCB stackup to be used. The DUT board and DUT module impedance are defined as 50 (± 5%) ohms, recommended trace width for the testboard is 6.5mil.

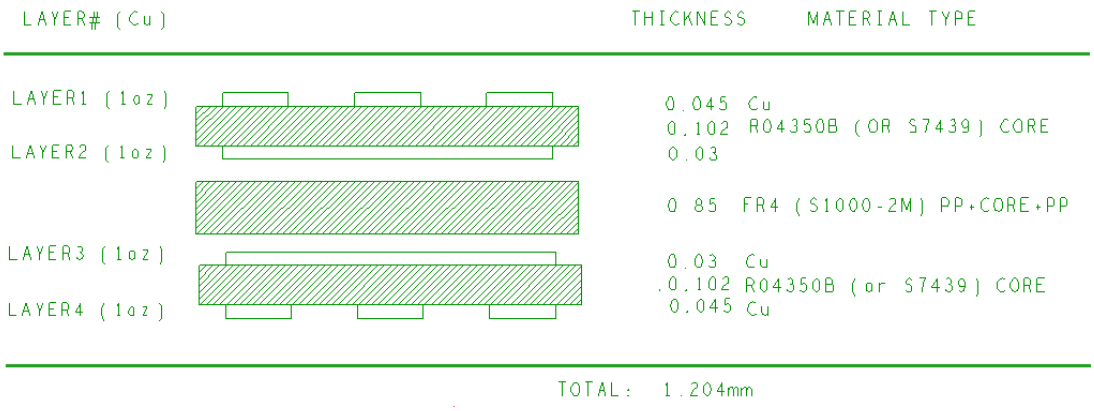


Figure D.1 Stackup of DDR5 SODIMM connector testboard

D.2.2 Baseboard

The reference plane for de-embedded is set to be 0.635mm from SMT pad edge on the baseboard. The trace length from reference plane to 2.92mm connector is 32.25mm. There is a cut out on L2 ground layer underneath for each signal pad, the size of the cut out is the same as the SMT pad.

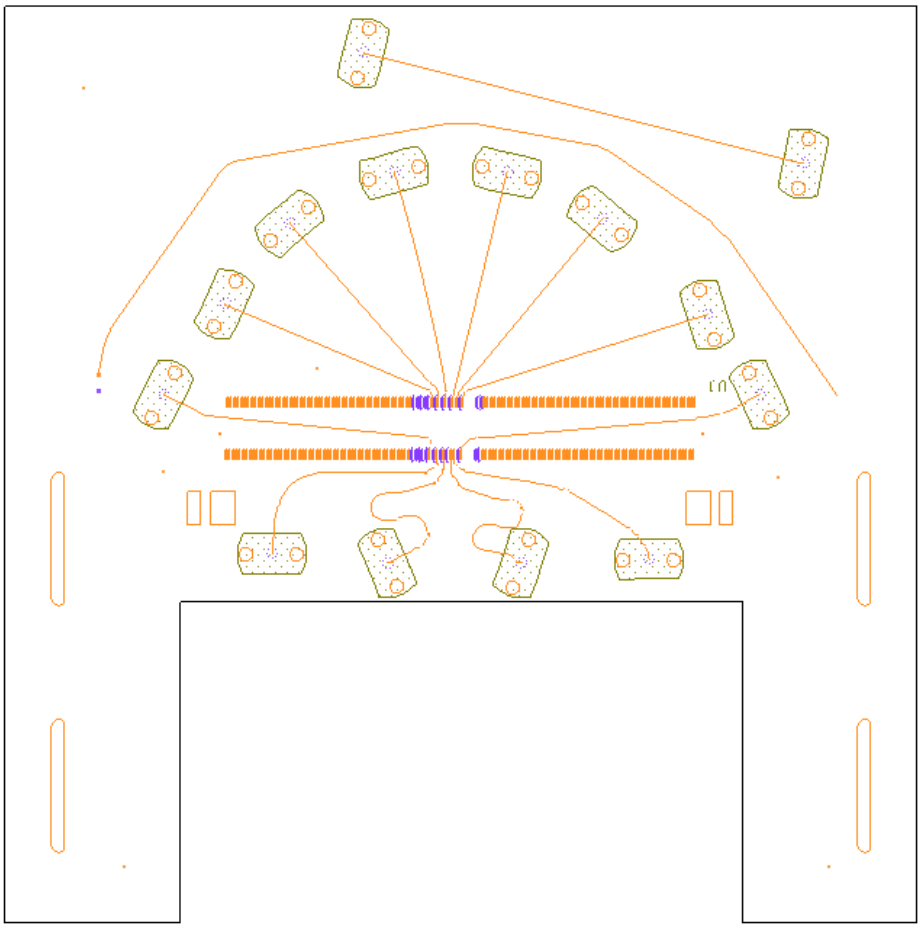


Figure D.2 DDR5 base board

D.2.3 Module card

The reference plane for de-embedded is set to be 0.635mm from gold finger pad edge on the module card. The trace length from reference plane to 2.92mm connector is 32.25mm. The L2/L3 ground layer was cut up to the gold finger inside edge.

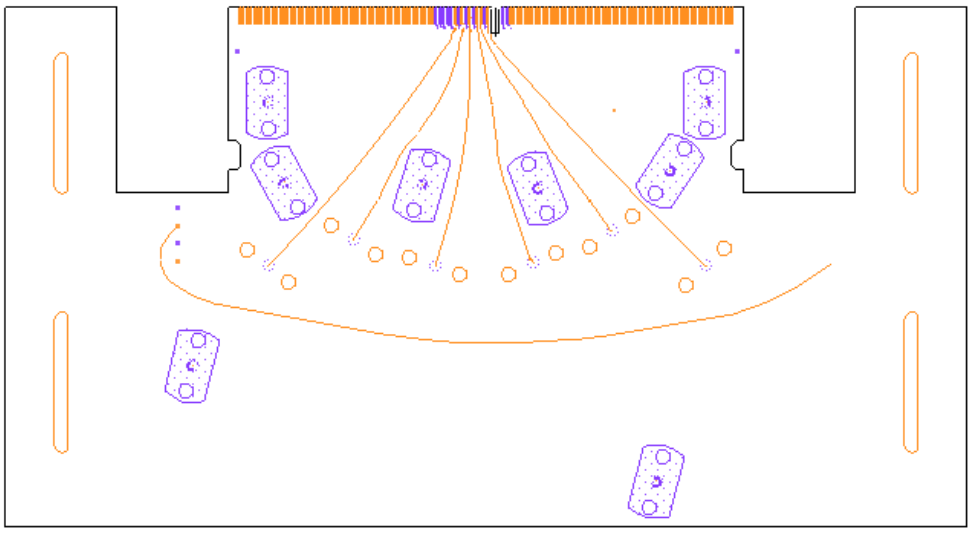
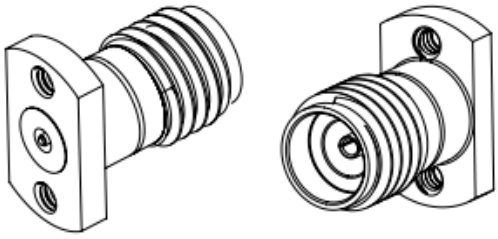


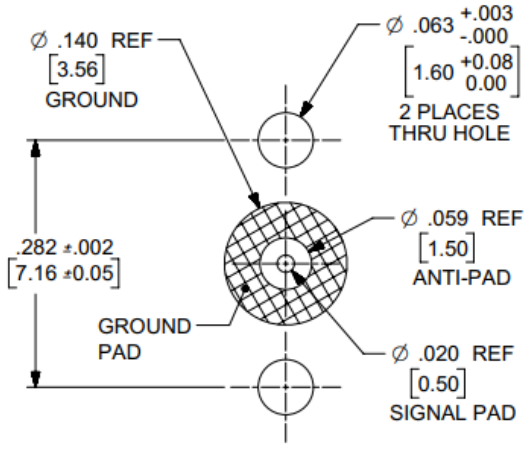
Figure D.3 DDR5 module card

D.2.4 2.92mm connector

Molex 2.92mm connector (# 0732520090) or equivalence is recommended to use, as shown in Figure D.4. The 2.92mm connector will be screw mounted on the PCB for cable vertical access.



(a)



(b)

Figure D.4 (a) 2.92mm connector (b) Recommended footprint of the 2.92mm connector

D. 3 Testing

Any 2.92mm connectors not connected to VNA for testing should be terminated with 50-ohm load.

TASK GROUP CONTRIBUTOR

AMPHENOL EAST ASIA LTD.
ARGOSY RESEARCH INC.
DELL INC.
FOXCONN INTERCONNECT TECHNOLOGY LTD
HP INC.
INTEL CORPORATION
INVENTEC CORPORATION
LOTES CO. LTD.
LUXSHARE-ICT, INC.
MICRON TECHNOLOGY INC.
MOLEX LLC
SAMSUNG SEMICONDUCTOR
SHENZHEN DEREN ELECTRONIC CO. LTD.
SK HYNIX INC.
TE CONNECTIVITY
WLCO SHENZHEN CO. LTD.

CHANGE RECORD

IF THE CHANGE INVOLVES ANY WORDS ADDED OR DELETED (EXCLUDING DELETION OF ACCIDENTALLY REPEATED WORDS), THE CHANGE IS INCLUDEC. PUNCTUATION CHANGES MAY OR MAY NOT BE INCLUDEC.

INITIAL ISSUE: A	DATE: October 2022	ITEM NUMBER: 11.14-214

CHANGE RECORD HISTORY:

ISSUE: B	DATE: September	ITEM NUMBER: 11.14-226
LOCATION:	CHANGED FROM:	CHANGED TO:
Table 7-5	0.5 amp/pin	1.0 amp/pin