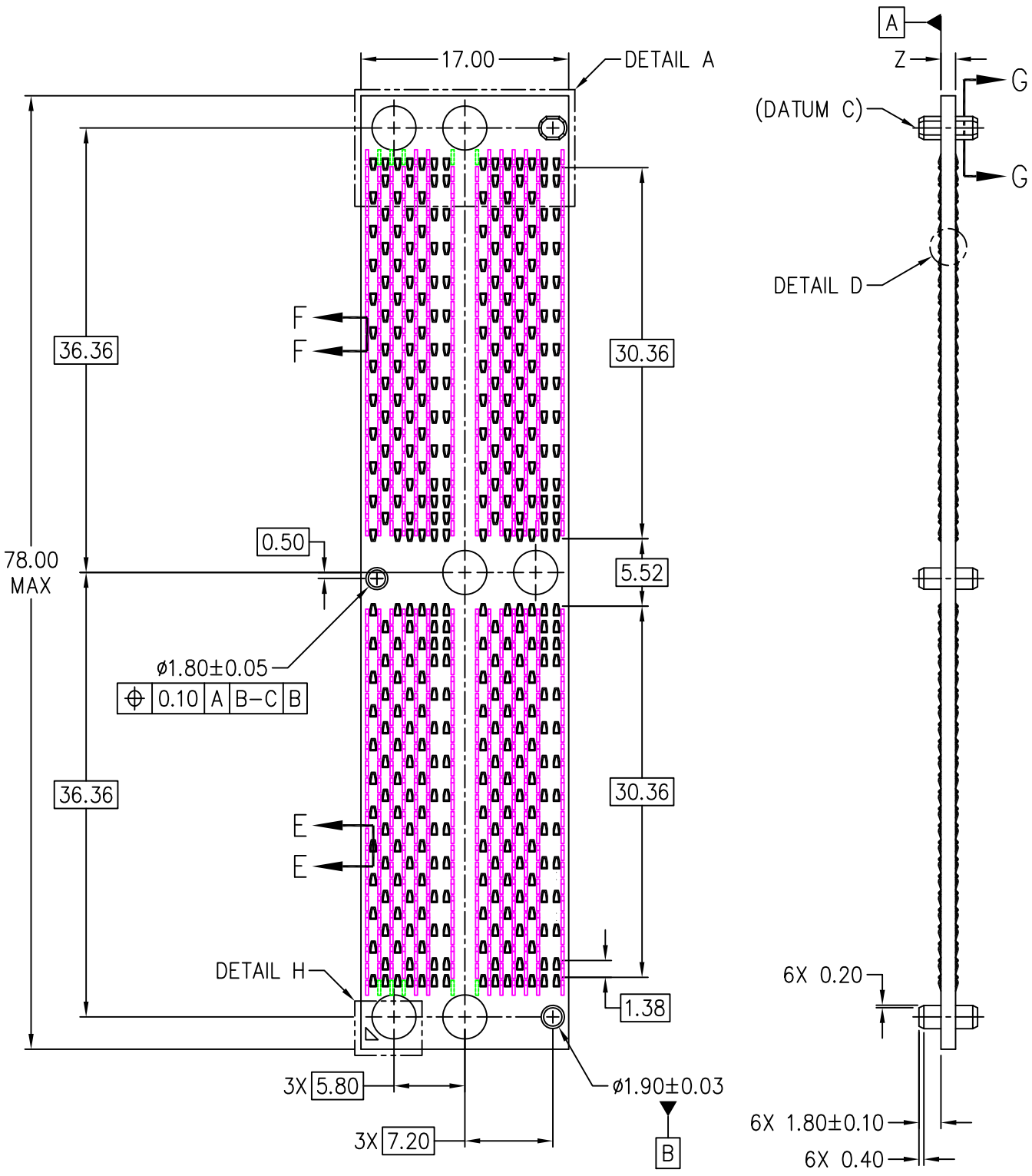
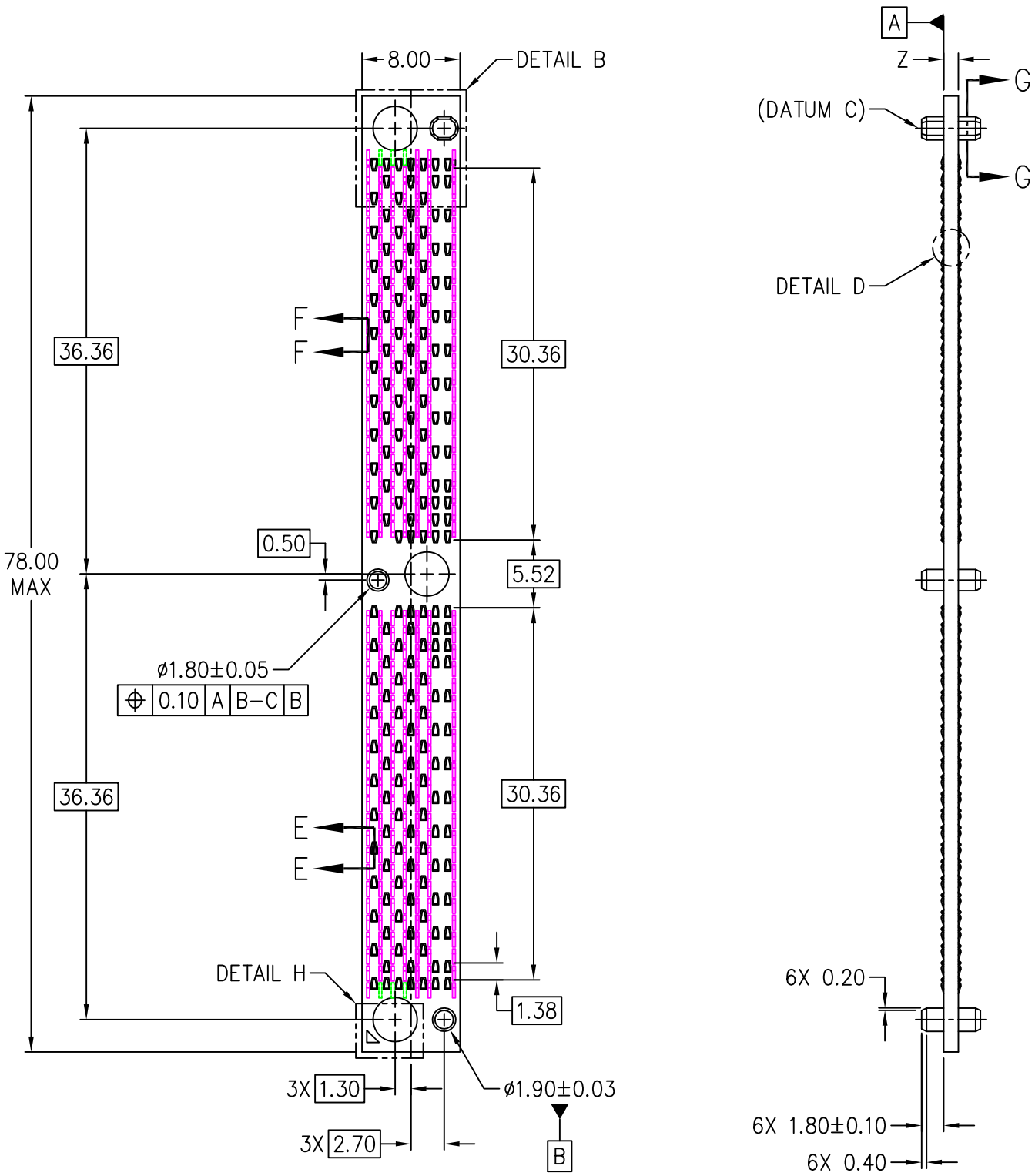


VARIATION: Axxx

8 PATENT CLAIMS

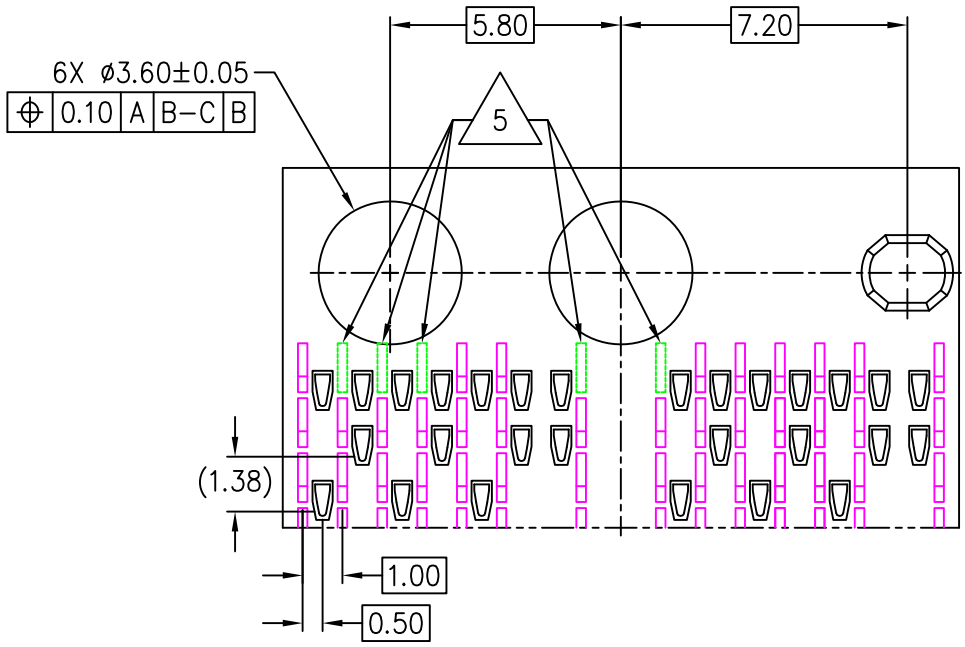
JEDEC SOLID STATE PRODUCT OUTLINE 	THIS *REGISTERED OUTLINE* HAS BEEN PREPARED BY THE JEDEC JC-11 COMMITTEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR.

TITLE	PACKAGE DESIGNATOR	NUMBER	ISSUE	DATE	SHEET
PLASTIC DUAL UPPER TO BOTTOM, 1.38 MM X1.00 MM PITCH CONNECTOR (CMT)	PDUtBXC-H...	SO-032	C	JUN 2024	1 OF 21

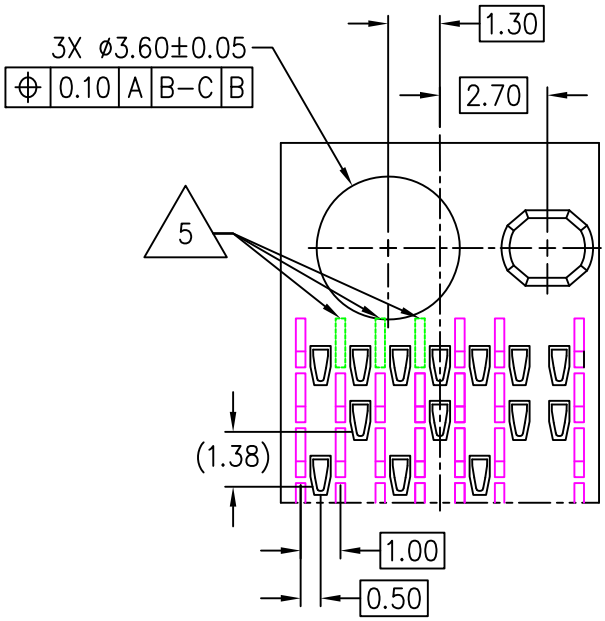


VARIATION: Bxxx

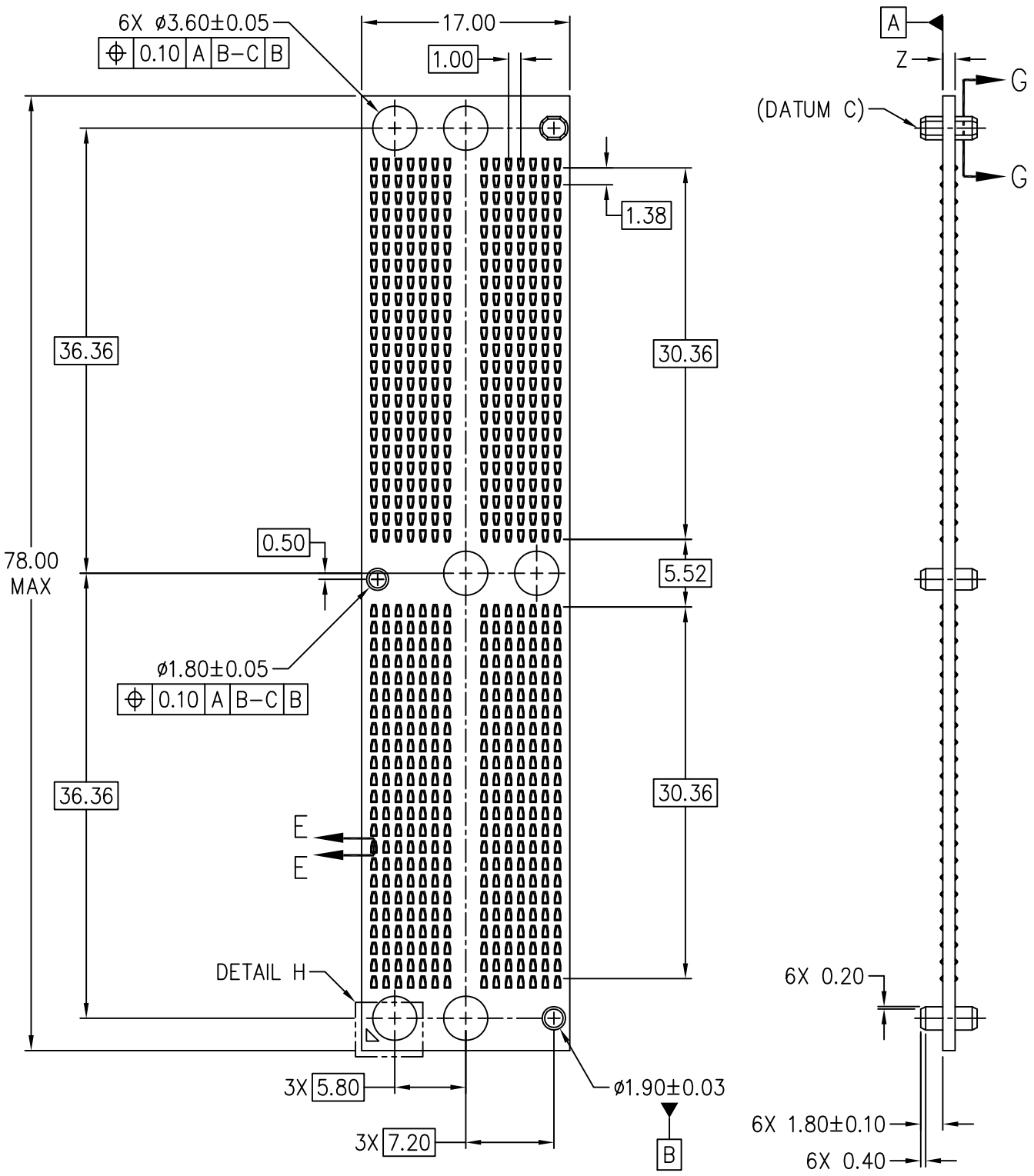
JEDEC SOLID STATE PRODUCT OUTLINE	TITLE	NUMBER	ISSUE	DATE	SHEET
	PLASTIC DUAL UPPER TO BOTTOM, 1.38 MM X1.00 MM PITCH CONNECTOR (CMT)	SO-032	C	JUN 2024	2 OF 21



DETAIL A

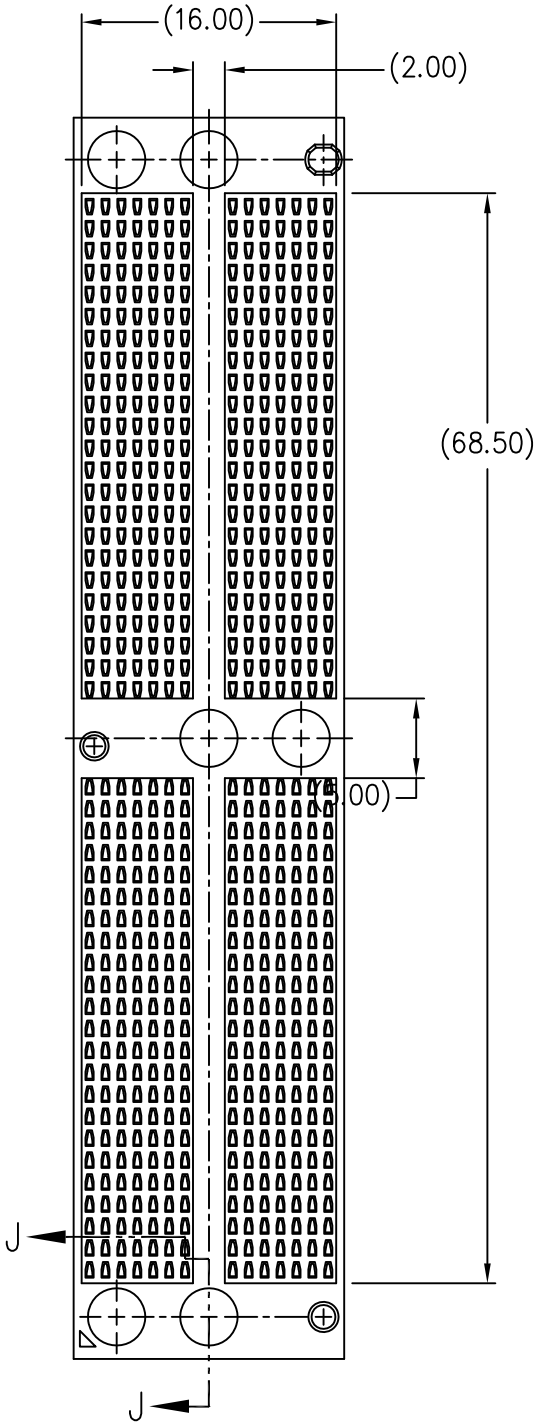


DETAIL B



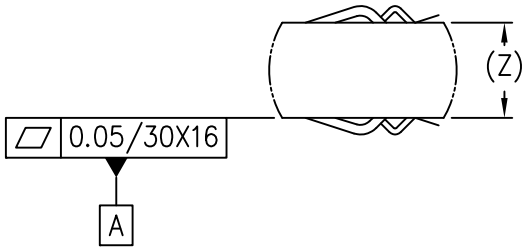
VARIATION: Cxxx

JEDEC SOLID STATE PRODUCT OUTLINE	TITLE	NUMBER	ISSUE	DATE	SHEET
	PLASTIC DUAL UPPER TO BOTTOM, 1.38 MM X1.00 MM PITCH CONNECTOR (CMT)	SO-032	C	JUN 2024	4 OF 21

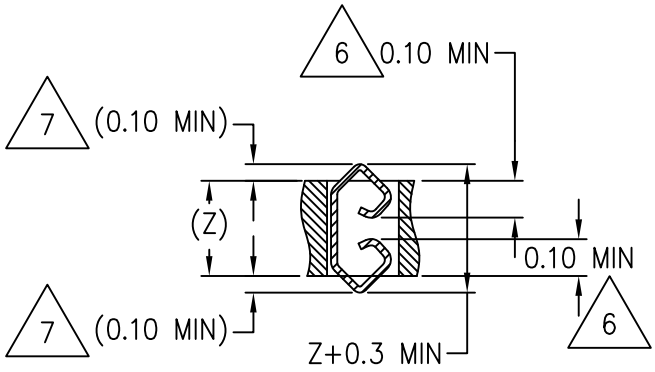


VARIATION: Cxxx WITH RECOMMENDED
RECESSED CONTACT AREA (OPTIONAL)

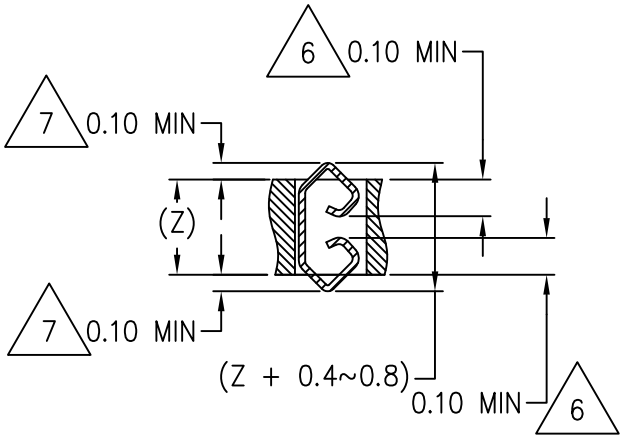
JEDEC SOLID STATE PRODUCT OUTLINE	TITLE PLASTIC DUAL UPPER TO BOTTOM, 1.38 MM X1.00 MM PITCH CONNECTOR (CMT)	NUMBER	ISSUE	DATE	SHEET
		SO-032	C	JUN 2024	5 OF 21



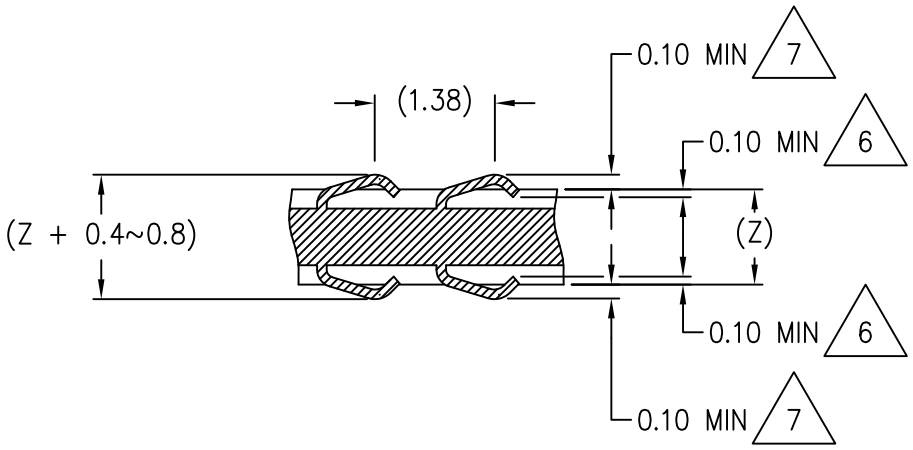
DETAIL D
ROTATE 90 DEGREE CCW



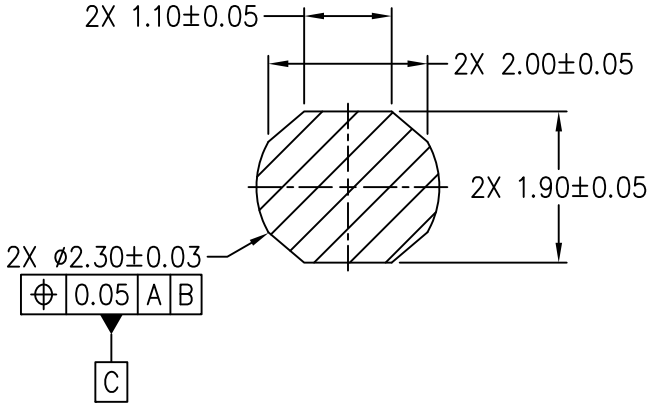
SECTION E – E
FLOATING PIN SHAPE A
ROTATE 90 DEGREE CW



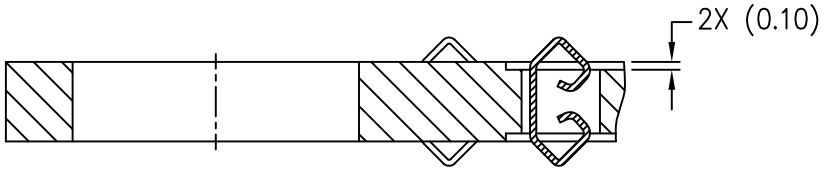
SECTION E – E
LOCKED PIN SHAPE A
ROTATE 90 DEGREE CW



SECTION F – F
PIN SHAPE B
ROTATE 90 DEGREE CCW

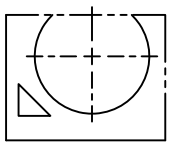


SECTION G – G

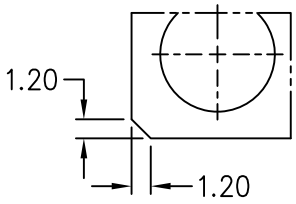


SECTION J – J
ROTATE 90 DEGREE CW
(OPTIONAL)

JEDEC SOLID STATE PRODUCT OUTLINE Copyright © 2024 JEDEC	TITLE PLASTIC DUAL UPPER TO BOTTOM, 1.38 MM X1.00 MM PITCH CONNECTOR (CMT)	NUMBER	ISSUE	DATE	SHEET
		SO-032	C	JUN 2024	7 OF 21



OPTION A



OPTION B

DETAIL H

TABLE 1

HEIGHT					
VARIATION ▶		xAxx	xBxx	xCxx	xDxx
SYMBOL ▼					
Z	MIN	0.95	1.80	2.80	7.45
	NOM	1.00	1.85	2.85	7.50
	MAX	1.05	1.90	2.90	7.55
NOTES		–			
REF		14–215, 14–222			
ISSUE		B			

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5–2009.

2. ALL DIMENSIONS ARE IN MILLIMETERS, TOLERANCES ON ALL DIMENSIONS ±0.15 UNLESS OTHERWISE SPECIFIED.

3. REFER TO CAMM REGISTERED OUTLINE MO–357 FOR LP5 CAMM2 MODULE DIMENSIONS.
REFER TO CAMM REGISTERED OUTLINE MO–358 FOR LPDDR5 CAMM2 MODULE DIMENSIONS.

4. REFER TO JEDEC PS–007, DDR5/LPDDR5 CAMM CONNECTOR PERFORMANCE STANDARD.

△5 THESE CONTACTS NEAR THE MOUNTING HOLES ARE ALLOWED TO BE REMOVED DUE TO MANUFACTURING CONCERN.

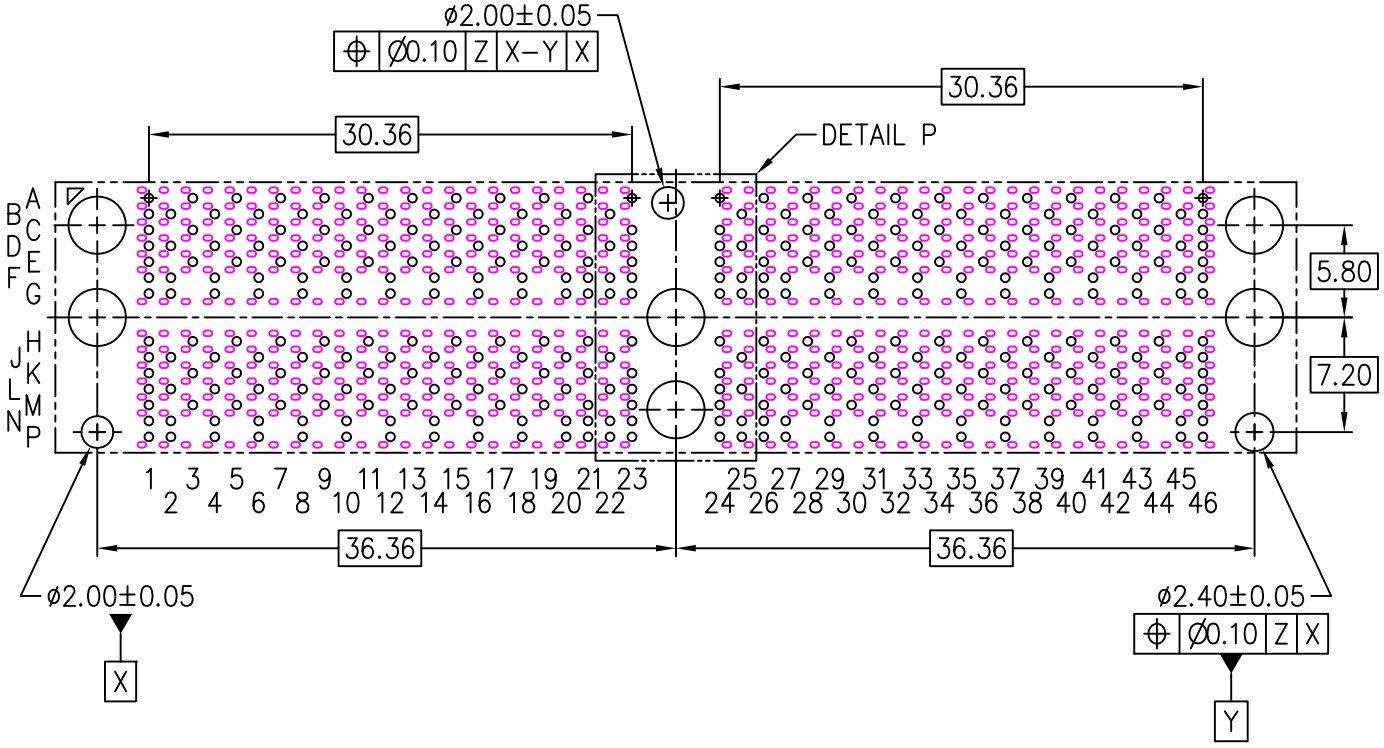
△6 THE PIN TIPS ARE BURIED IN THE HOUSING FOR BOTH SIDES.

△7 THE PIN CONTACT SURFACE ARE EXPOSED OUT OF THE HOUSING FOR BOTH SIDES.

△8 VARIOUS COMPANIES HAVE ISSUED PATENTS AND RELATED PATENT APPLICATIONS THAT MAY APPLY TO THIS REGISTRATION. IF THE CURRENT ISSUE PATENTS OR LATER PATENTS RESULTING FROM RELATED APPLICATIONS DO APPLY, THESE COMPANIES INTEND TO COMPLY WITH THE JEDEC PATENT POLICY AND LICENSE UNDER REASONABLE TERMS AND CONDITIONS THAT ARE DEMONSTRABLY FREE OF ANY UNFAIR DISCRIMINATION. REFERENCED PATENTS ARE AS FOLLOWS.

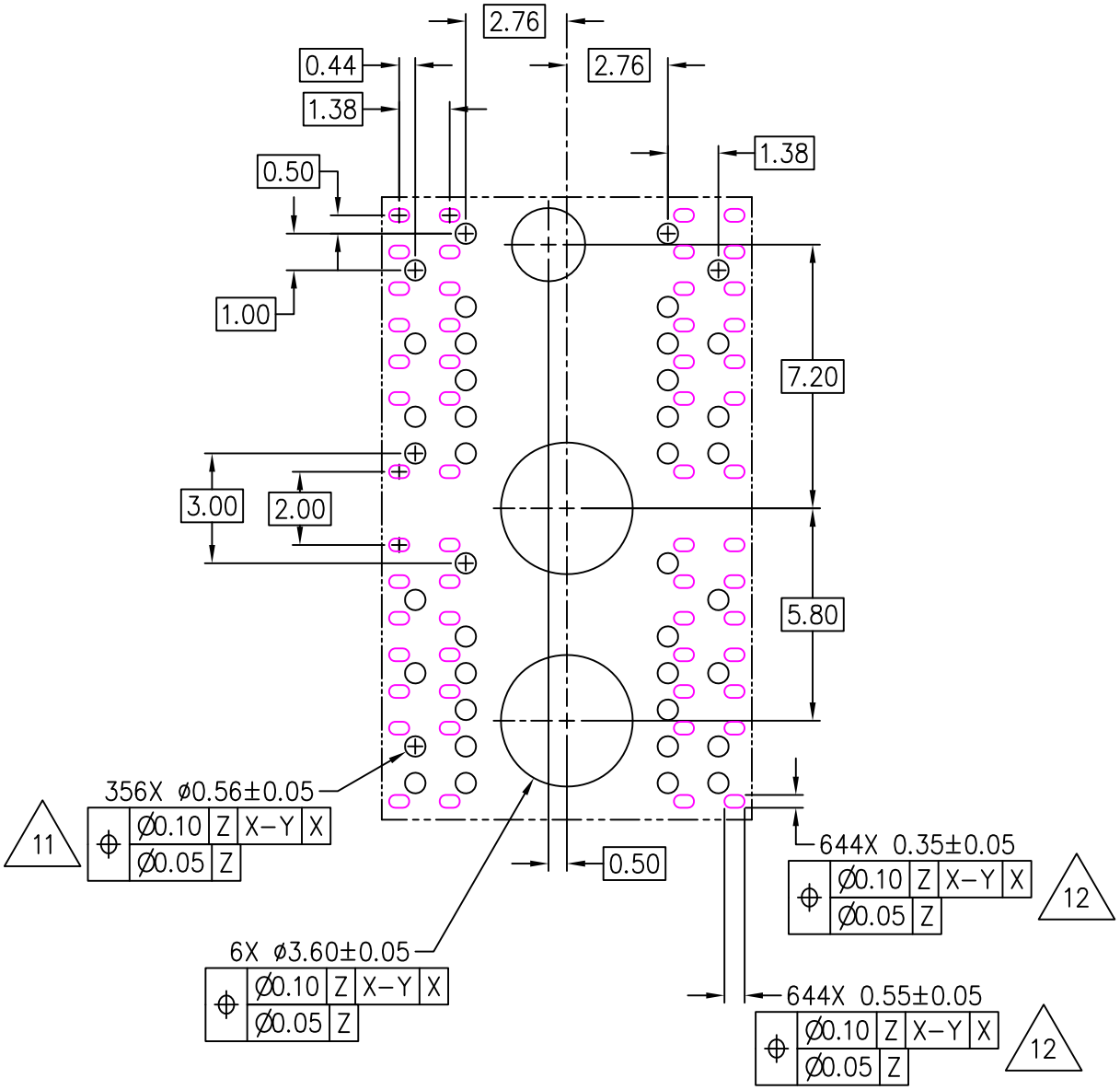
AMPHENOL	PATENT NO.: 9,425,525

9. REFERENCE PCB FOOTPRINT (APPLY TO VARIATION: Axxx ONLY). CONNECTOR PINS SHALL LAND ON THE PAD BEFORE AND AFTER DEFLECTION DURING THE ASSEMBLY.



JEDEC SOLID STATE PRODUCT OUTLINE	TITLE	NUMBER	ISSUE	DATE	SHEET
	PLASTIC DUAL UPPER TO BOTTOM, 1.38 MM X1.00 MM PITCH CONNECTOR (CMT)	SO-032	C	JUN 2024	9 OF 21

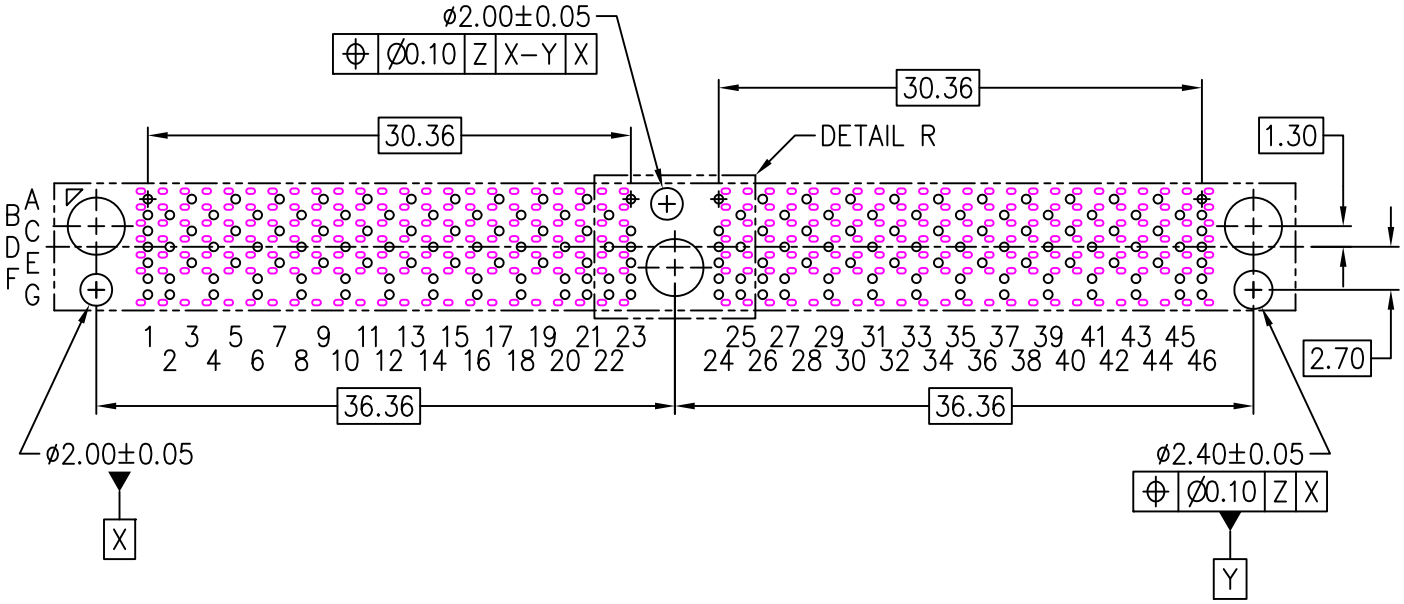
NOTES CONTINUED:

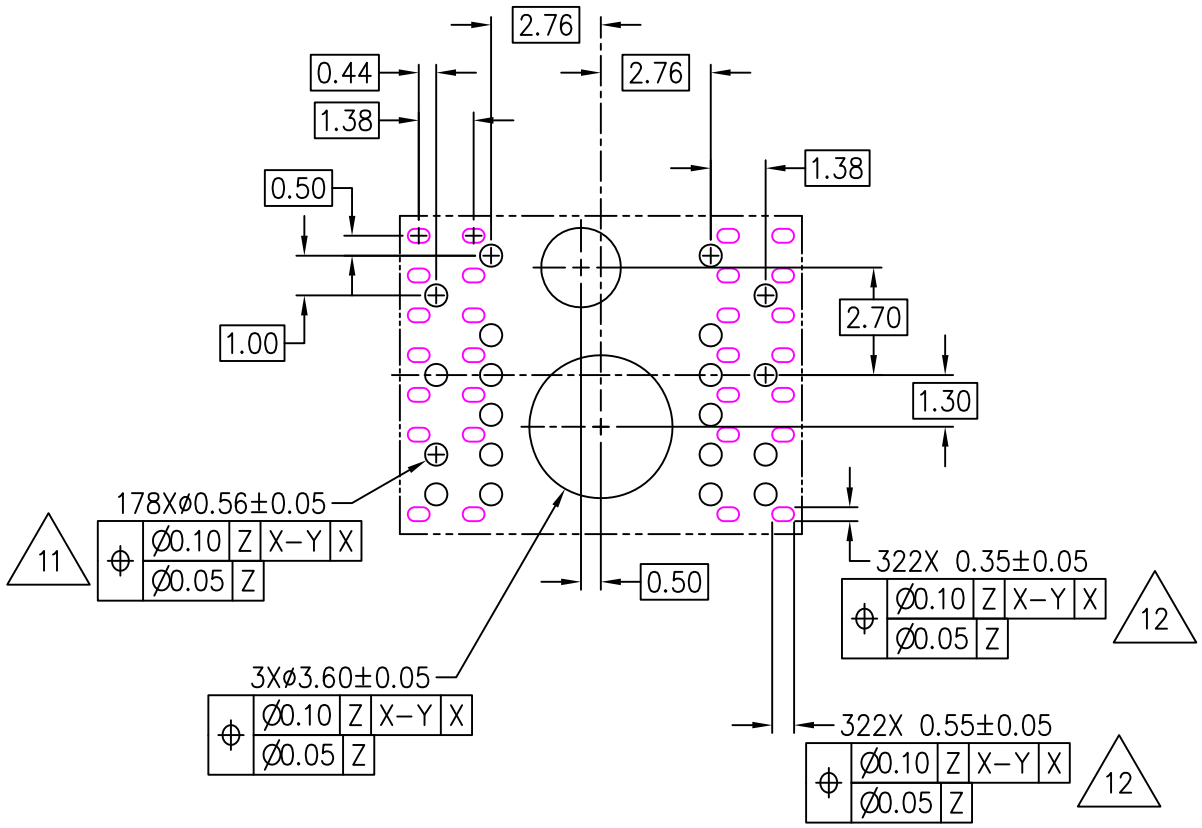


DETAIL P
DATUM Z: PCB SURFACE

NOTES CONTINUED:

10. REFERENCE PCB FOOTPRINT (APPLY TO VARIATION: Bxxx ONLY). CONNECTOR PIN SHALL LAND ON THE PAD BEFORE AND AFTER DEFLECTION DURING THE ASSEMBLY.





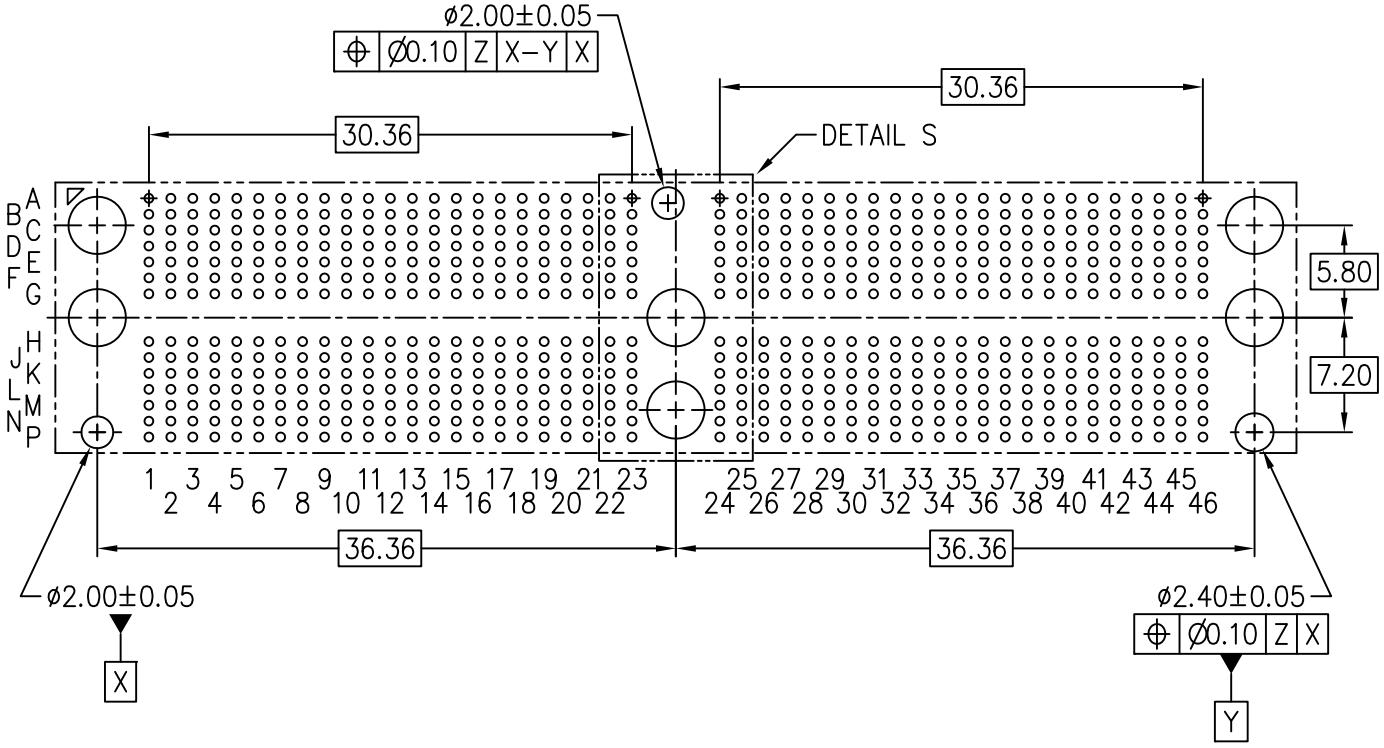
DETAIL R
DATUM Z: PCB SURFACE

NOTES CONTINUED:

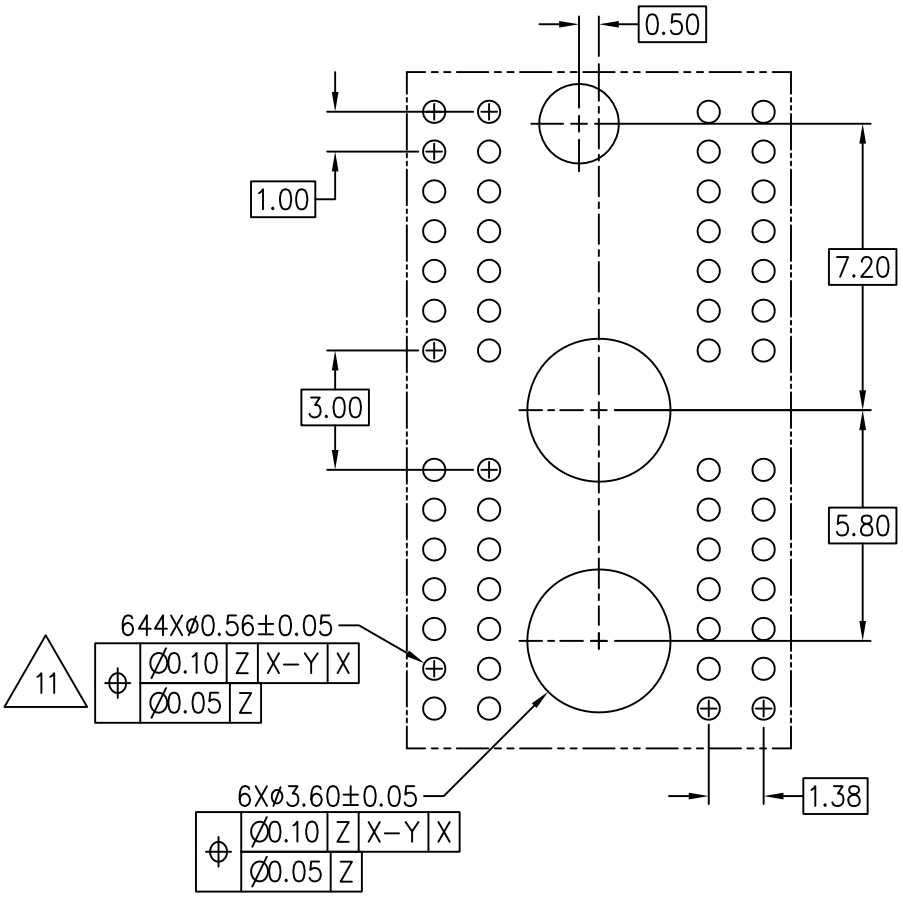
11 PCB CONTACT PAD FOR CONNECTOR PIN SHAPE A.

12 PCB CONTACT PAD FOR CONNECTOR PIN SHAPE B.

13. REFERENCE PCB FOOTPRINT (APPLY TO VARIATION: Cxxx ONLY). CONNECTOR PINS SHALL LAND ON THE PAD BEFORE AND AFTER DEFLECTION DURING THE ASSEMBLY.



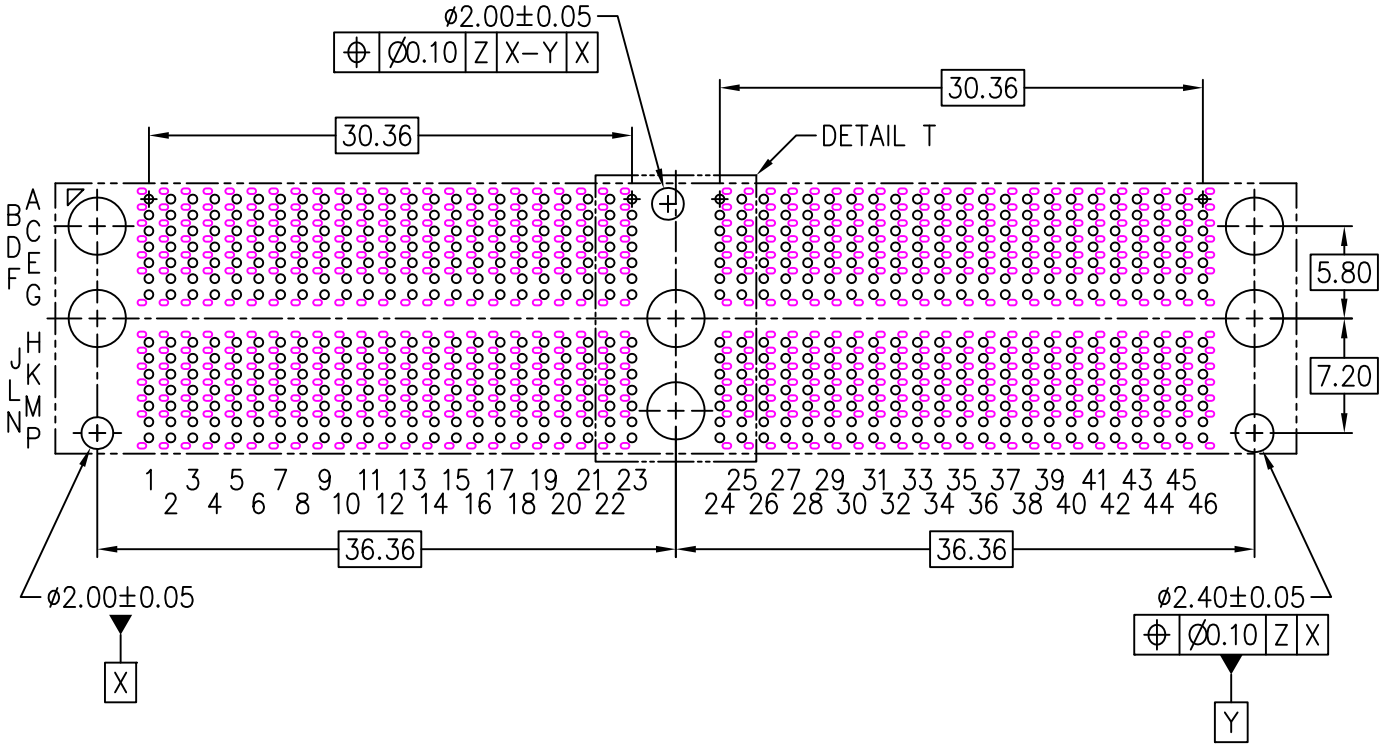
NOTES CONTINUED:



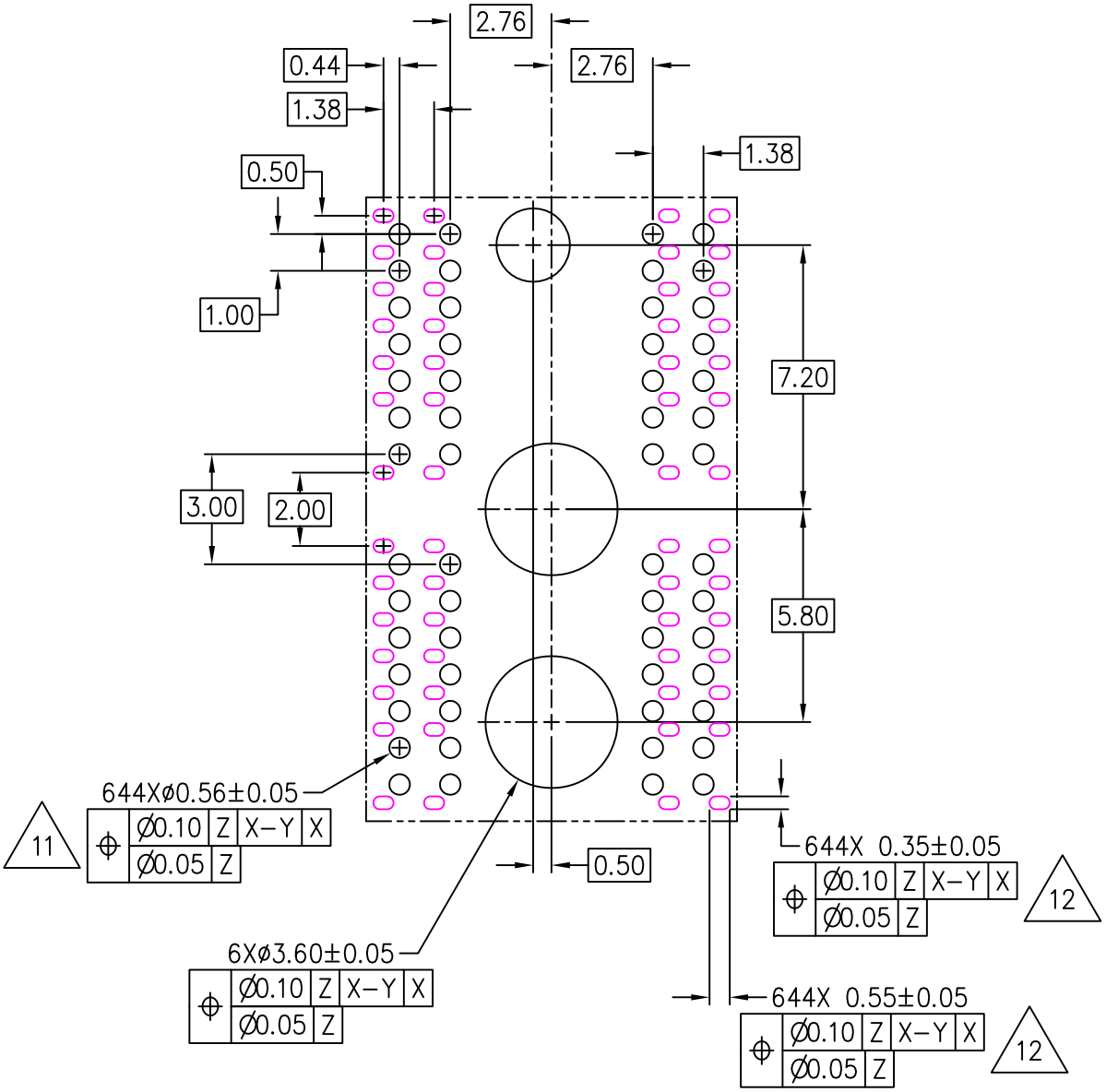
DETAIL S
DATUM Z: PCB SURFACE

NOTES CONTINUED:

14. REFERENCE PCB FOOTPRINT (APPLY TO VARIATION: Axxx AND Cxxx). CONNECTOR PINS SHALL LAND ON THE PAD BEFORE AND AFTER DEFLECTION DURING THE ASSEMBLY.



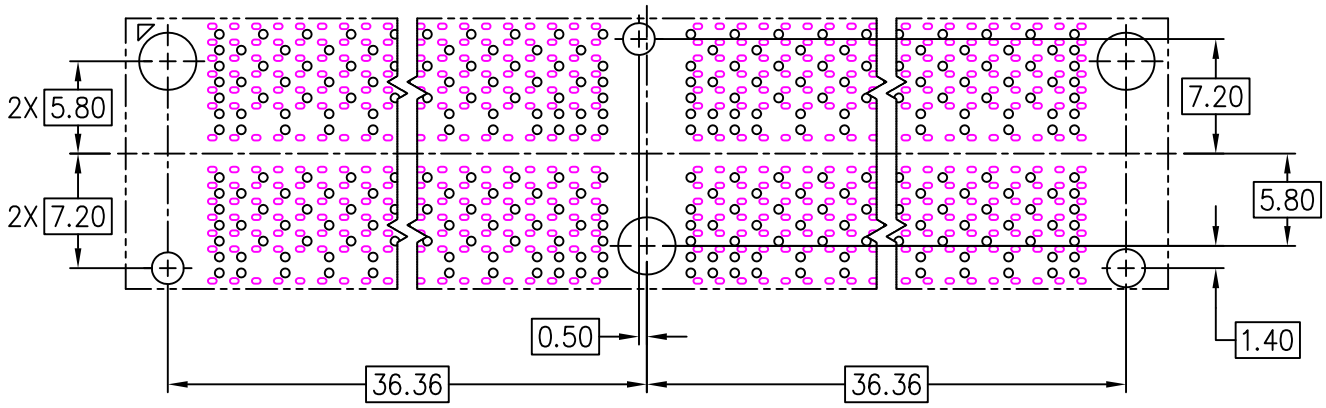
NOTES CONTINUED:



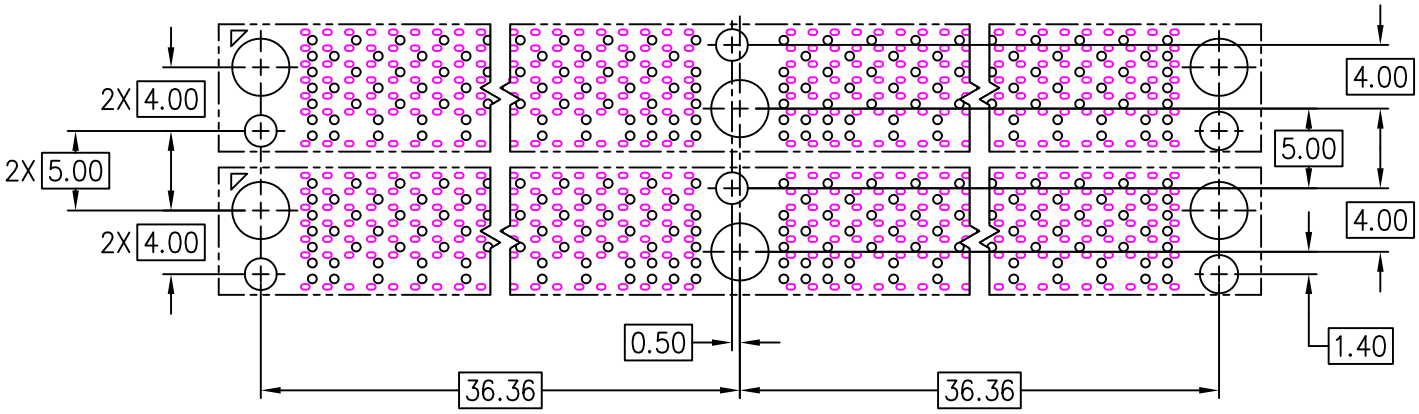
DETAIL T
DATUM Z: PCB SURFACE

APPLICATION NOTES:

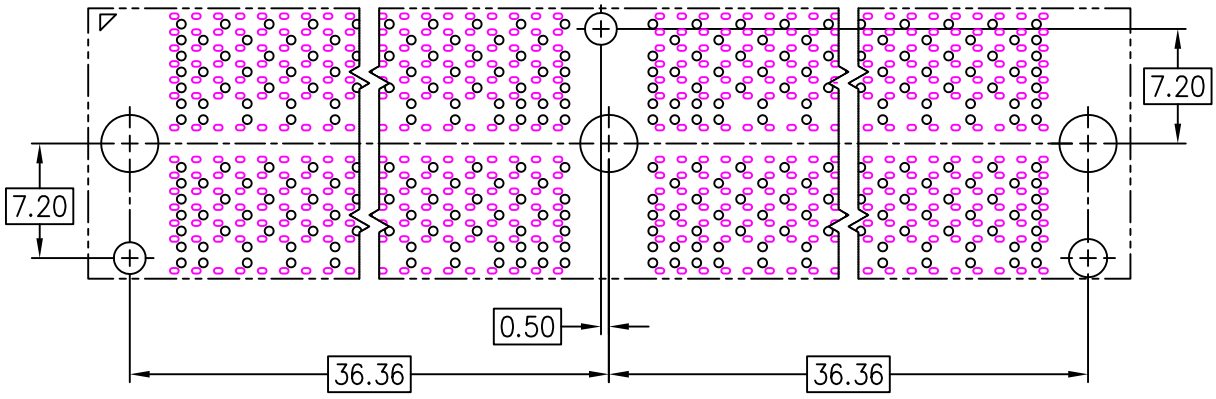
15. REFERENCE PCB LAYOUT (VARIATION Axxx ONLY AND DDR5 APPLICATION).



16. REFERENCE PCB LAYOUT (VARIATION BXXX ONLY AND DDR5 APPLICATION).

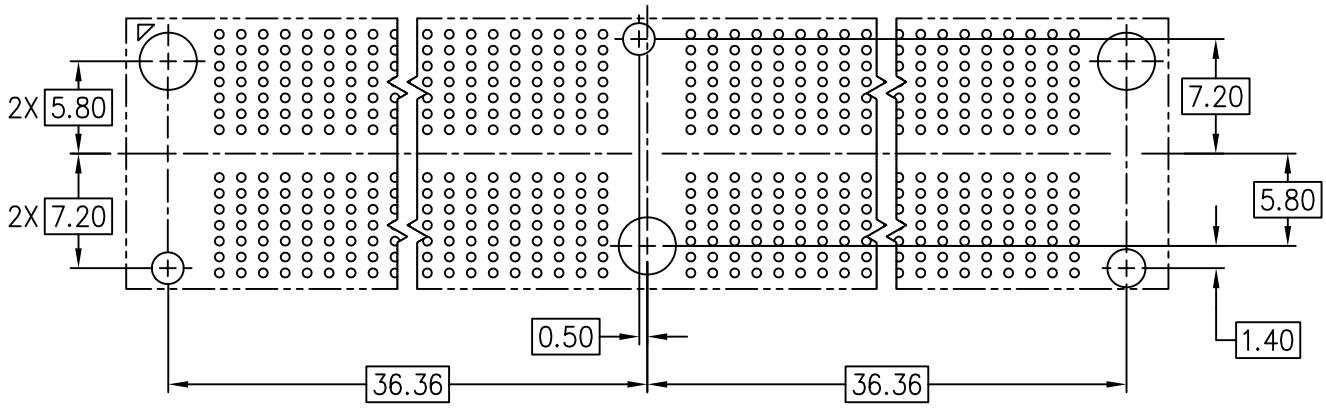


17. REFERENCE PCB LAYOUT (VARIATION AXXX ONLY AND LPDDR5 APPLICATION).

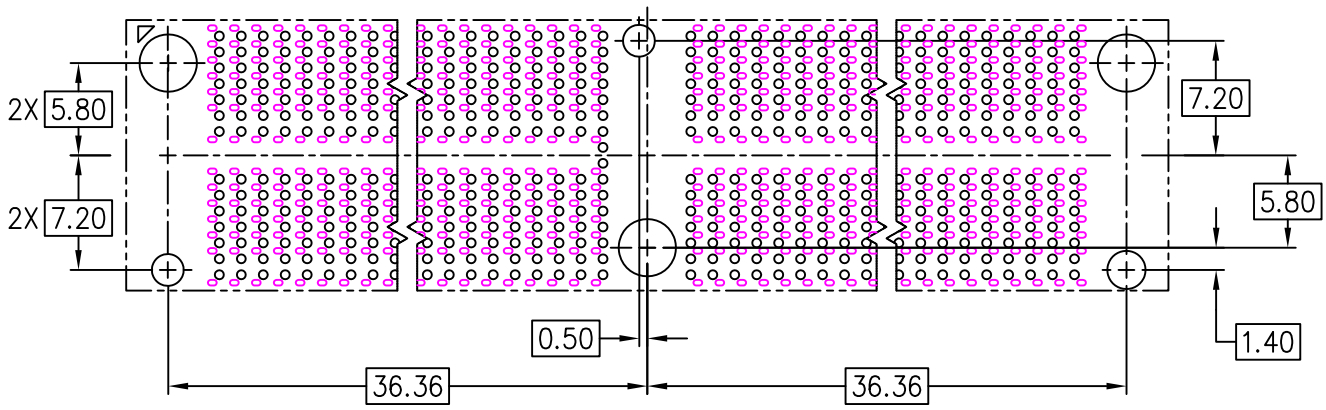


APPLICATION NOTES CONTINUED:

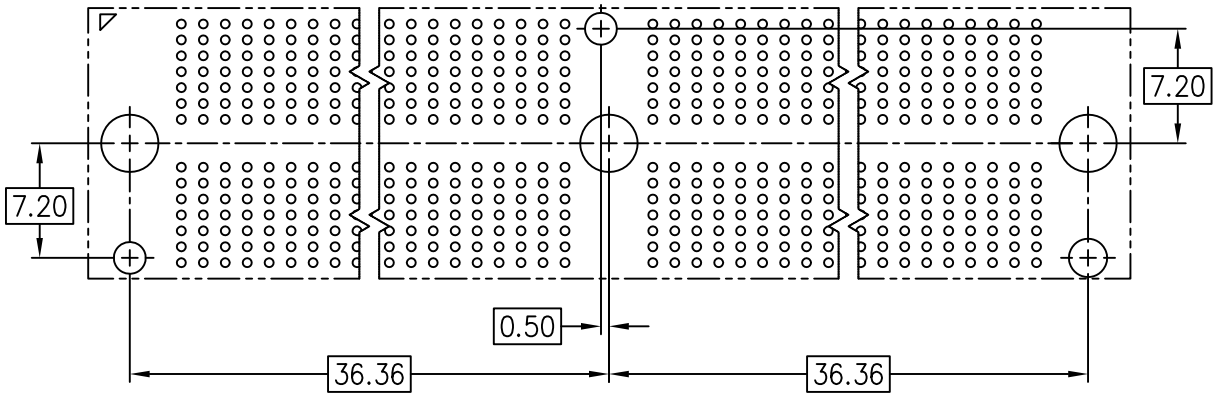
18. REFERENCE PCB LAYOUT (VARIATION Cxxx ONLY; DDR5 APPLICATION).



19. REFERENCE PCB LAYOUT (COMBINATION OF VARIATION AXXX AND VARIATION CXXX; DDR5 APPLICATION).

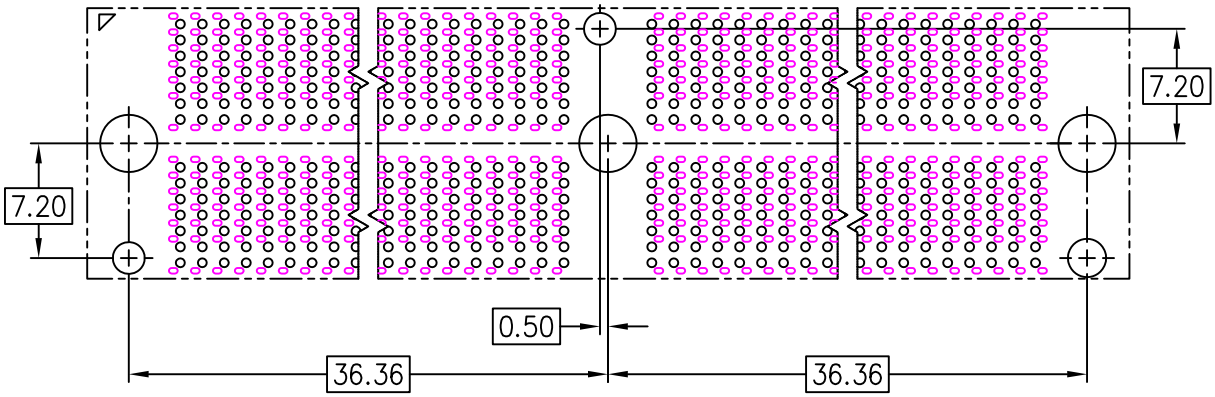


20. REFERENCE PCB LAYOUT (VARIATION CXXX ONLY; LPDDR5 APPLICATION).

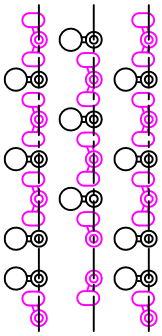


APPLICATION NOTES CONTINUED:

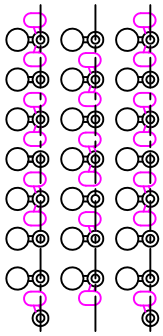
21. REFERENCE PCB LAYOUT (COMBINATION OF VARIATION Axxx AND VARIATION Cxxx; LPDDR5 APPLICATION).



22. REFERENCE NON-HDI PCB ROUTING AND VIA PLACEMENT.



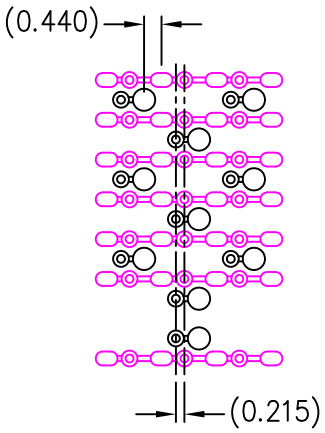
VARIATION:
Axxx OR Bxxx



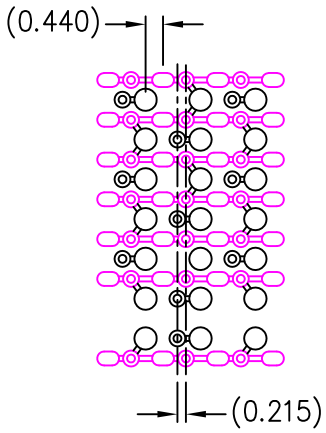
VARIATION:
Axxx AND Cxxx

OPTION 1
1:1 S/G VIA PATTERN
FOR MORE ROUTING SPACE

APPLICATION NOTES CONTINUED:

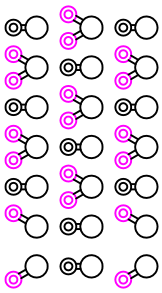


VARIATION:
Axxx OR Bxxx



VARIATION:
Axxx AND Cxxx

OPTION 2
1:2 S/G VIA PATTERN
FOR BETTER SIGNAL INTEGRITY



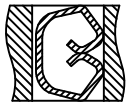
VARIATION: Cxxx

OPTION 3
2:1 S/G VIA PATTERN FOR MORE ROUTING SPACE
AND BETTER SIGNAL INTEGRITY

APPLICATION NOTES CONTINUED:

23. THE CONNECTOR STAMPED TERMINALS MAY NEED TO BE SHUNTED UNDER THE DEFLECTED CONDITION TO MEET THE ELECTRICAL REQUIREMENTS. EITHER TOP OR BOTTOM PLATE MAY BE REQUIRED TO ENSURE RELIABLE RETENTION FOR SYSTEM APPLICATION.

UNDEFLECTED

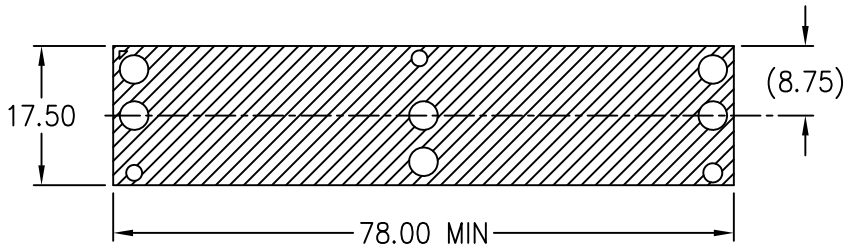


DEFLECTED

24. THE CONNECTORS MAY BE PACKED IN A TRAY. FOR DETAILS REFER TO JEDEC CO-040.

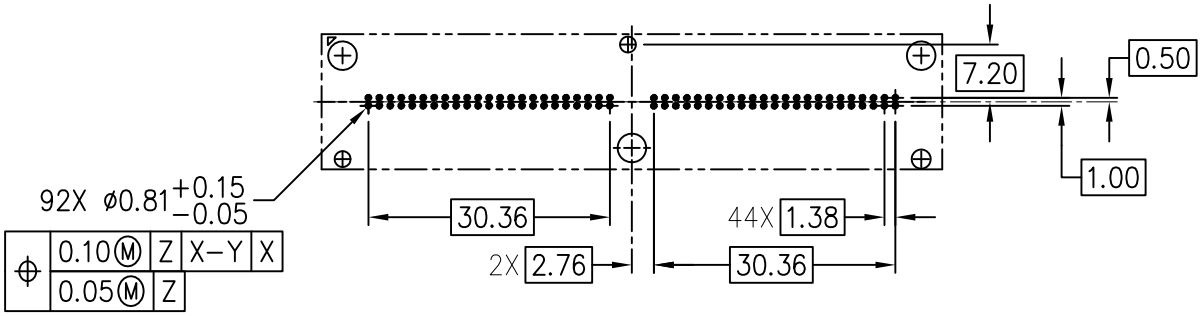
25. THE DIMENSIONS ENCLOSED IN PARENTHESES ARE FOR REFERENCE ONLY.

26. SOLDER MASK IS RECOMMENDED TO BE REMOVED IN THIS AREA ON THE TOP LAYER OF SYSTEM BOARD, WHERE THE CONNECTOR IS TO BE MOUNTED.

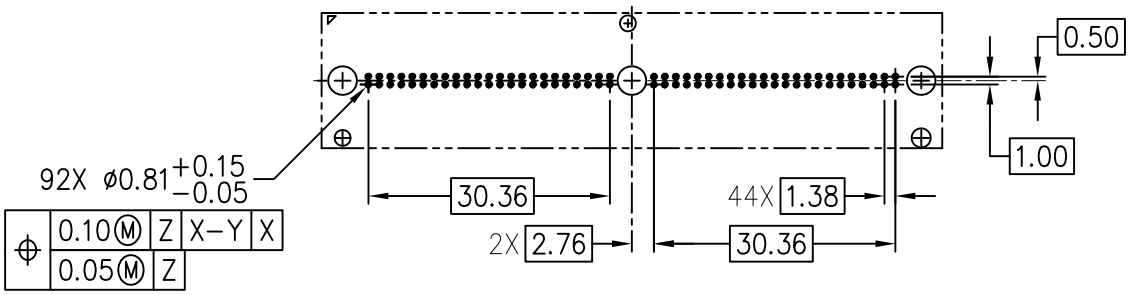


APPLICATION NOTES CONTINUED:

27. VOID METAL WITHIN AREA OF ø0.81 CIRCLES ON THE BOTTOM LAYER WHERE CONNECTOR TERMINALS COULD BE PRESENT.



VARIATION Axxx



VARIATION Cxxx

STP (3D) FILE RECORD

3D FILE NAMES MAY EXCEED LENGTH REQUIREMENTS FOR SOME SOFTWARE TOOLS.

STP FILE NAME	DATE	ITEM NUMBER
SO-032A_PDUtBXC-H500_l0p5-R8p15x78p0Z2p9	JUL 2023	14-215
SO-032A_PDUtBXC-H500_l0p5-R8p15x78p0Z6p90	JUL 2023	14-215
SO-032A_PDUtBXC-H1000_l0p5-R17p15x78p0Z1p90	JUL 2023	14-215
SO-032A_PDUtBXC-H1000_l0p5-R17p15x78p0Z2p90	JUL 2023	14-215
SO-032B_PDUtBXC-H644_l1p0-R17p15x78p0Z1p05	NOV 2023	14-222

TASK GROUP CONTRIBUTORS

ALIBABA(CHINA) CO. LTD
AMPHENOL CORPORATION
ARGOSY RESEARCH INC.
CHANGXIN MEMORY TECHNOLOGIES INC (CXMT)
DELL INC.
FOXCONN INTERCONNECT TECHNOLOGY
HEWLETT PACKARD ENTERPRISE
HP INC.
INTEL CORPORATION
LENOVO
LOTES CO., LTD
LUXSHARE–ICT, INC.
MICRON TECHNOLOGY INC.
MOLEX LLC
NEOCONIX, INC.
SAMSUNG SEMICONDUCTOR
SMART MODULAR TECHNOLOGIES INC.
TE CONNECTIVITY
WLCO SHENZHEN CO., LTD.

CHANGE RECORD

IF THE CHANGE INVOLVES ANY WORDS ADDED OR DELETED (EXCLUDING DELETION OF ACCIDENTALLY REPEATED WORDS), THE CHANGE IS TO BE INCLUDED BELOW. PUNCTUATION CHANGES MAY OR MAY NOT BE INCLUDED.

INITIAL ISSUE: A	DATE: JULY 2023	ITEM NUMBER: 14–215

CHANGE RECORD HISTORY:

INITIAL ISSUE: B	DATE: NOVEMBER 2023	ITEM NUMBER: 14–222

LOCATION	CHANGED FROM:	CHANGED TO:
SHEETS 1, 2 & 4		ADD DETAIL H
SHEET 5		NEW SHEET, ADDED OPTIONAL RECESSED CONTACT AREA
SHEET 7		ADDAED SECTION J–J
SHEET 8		ADDED DETAIL H
SHEET 8, TABLE 1	xDxx FROM: 6.80, 6.85, 6.90	xDxx TO: 7.45, 7.50, 7.55
SHEET 18, NOTE 20	DDR5	LPDDR5

ISSUE: C	DATE: JUNE 2024	ITEM NUMBER: 14–227

LOCATION	CHANGED FROM:	CHANGED TO:
SHEET 11, 12 & 16	5.52 BASIC	REMOVE DIMENSION: BASIC 5.52
		ADD DIMENSION: BASIC 2.76
SHEET 20		ADD NOTE 26
SHEET 21		ADD NOTE 27