JEDEC STANDARD

Standard for Description of 3877: 2.5 V, Dual 5-Bit, 2-Port, DDR FET Switch

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Standard for description of 3877: 2.5 V, Dual 5-bit, 2-port, DDR FET switch

(From Board Ballot JCB-01-62, formulated under the cognizance of the JC-40.2 Subcommittee on Bus Switch Logic Products.)

1 Scope

This standard covers the specification for the 3877, 2.5 V, FET transmission-gate bus switch device with 2.5 V LVTTL compatible control inputs. Not included in this document are device specific parameters and performance levels that the vendor must also supply for the full device description.

The purpose of this standard is to provide a set of uniform data sheet parameters for the description of the 3877, 2.5 V, DDR FET switch device. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of the 3877, 2.5 V, DDR FET switch device.

NOTE The designation '3877' refers to the numerical portion of the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Definitions for the purpose of this document

switch device: A semiconductor logic device designed to connect or disconnect busses or control signals without active drivers in the connection path.

connect: A state in a switch device is characterized by a minimum series impedance through the designated electrical path.

disconnect: A state in a switch device is characterized by the high series impedance of the designated electrical path.

3 Standard specification

3.1 Device description

This 10-bit, two-port bus switch is designed for 2.3 V to 2.7 V, V_{DD} operation.

All inputs are compatible with the JEDEC standard for 2.5 V, CMOS.

The 3877 device is organized into two banks of 5-bit, transmission-gate bus switches. Each bank is enabled through an associated Bus Enable ($\overline{BE}$), which is driven low to enable the switches and connect the A-port to the B-port. Driving $\overline{BE}$ high will disable the switches and disconnect the A-port from the B-port with a high impedance state. The 3877, is intended to be used with X4 SDRAM memory. The fifth transmission gate in each provides a path for overhead data.

The bus enable $\overline{BE}$ pins do not have an internal pull-up resistor.

The output pins on the B-side of the device are pulled down to ground reference through a weak resistor structure to provide termination to the transmission gate switch channels.

Package options for this device include thin small-outline package (MO-153 AD).

3.2 Logic block diagram and device pin configuration

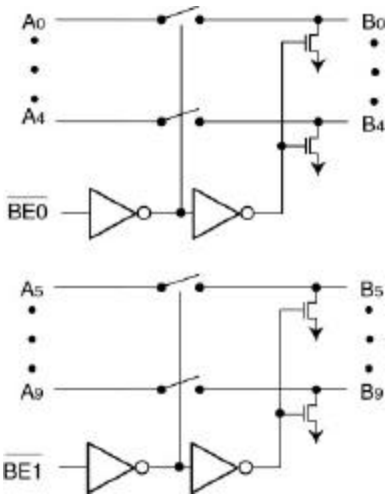


Figure 1 — Logic block diagram

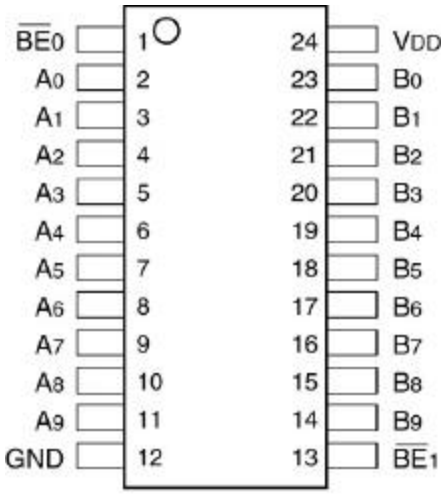


Figure 2 — Device pin configuration

3 Standard specification (cont'd)

3.3 Product pin description and truth table

Table 1 — Device pin description

Pin Name	Description
$\overline{BE0}$, $\overline{BE1}$	Bus Enable Input (Active LOW)
A0–9	A-port
B0–9	B-port
GND	Ground
V_{DD}	Power

Table 2 — Logic Truth Table

Function	**$\overline{BE0}$**	**A0–A4**	**B0–B4**
Disconnect	H	Hi-Z	L
Connect	L	B0–B4	A0–A4
Function	**$\overline{BE1}$**	**A5–A9**	**B5–B9**
Disconnect	H	Hi-Z	L
Connect	L	B5–B9	A5–A9
H = High Voltage Level L = Low Voltage Level Hi-Z = High Impedance			

3.4 Absolute maximum ratings

Table 3 — Absolute maximum ratings over operating free-air temperature range (see Note)

Supply voltage range, V_{DD}	–0.5 V to +3.6 V
DC input voltage	–0.5 V to +3.6 V
Bus I/O Voltage to Ground Potential	–0.5 V to +3.6 V
DC channel current	±128 mA
Storage temperature	65 °C to 150 °C

NOTE Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3 Standard specification (cont'd)

3.5 Recommended operating conditions

Table 4 — Recommended operating conditions (see Note)

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	2.3	2.7	V
T_A	Operating Free-Air temperature	0	+70	°C

NOTE Unused device control inputs must be held at V_{DD} or GND to ensure proper device operation.

3.6 DC electrical specifications

Table 5 — Electrical characteristics over recommended operating free-air temperature range

Parameter	Description	Test Conditions*	Min	Typ.†	Max.	Units
V_{IH}	High –Level input voltage	Guaranteed Logic level High	1.6		V_{DD} +0.3	V
V_{IL}	Low-level input voltage	Guaranteed Logic level Low	–0.3		0.9	V
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., I_{IN} = –18 mA			–1.2	V
I_{OZH}	High Impedance Output Current	$\overline{BE}$ = H B-Port I/O level = 2.5V			250	µA
R_{ON}	Switch ON Resistance‡	V_{DD} = Min., V_{IN} = 0.9 V, I_{ON} = 20 mA		17	33	Ω
		V_{DD} = Min., V_{IN} = 1.6 V, I_{ON} = 15 mA		22	30	Ω

* For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.

† Typical values are at V_{DD} = 2.5 V, T_A = 25 °C ambient and maximum loading.

‡ Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.

3.6 DC electrical specifications (cont'd)

Table 6 — Capacitance

Parameter *	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	3.0	pF
C_{OFF}	A Capacitance, Switch OFF	V_{IN} = 0 V	3.0	pF
C_{ON} (A/B)	A/B Capacitance, Switch ON	V_{IN} = 0 V	7.0	pF
* These parameters are determined by device characterization; not production tested.				

Table 7 — Power Supply Characteristics

Parameter	Description	Test Conditions*‡	Min.	Typ. †	Max.	Units
I_{DD}	Quiescent power supply current	V_{DD} = max	--	--	10	uA

* For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.

† Typical values are at V_{DD} = 2.5 V, +25 °C ambient.

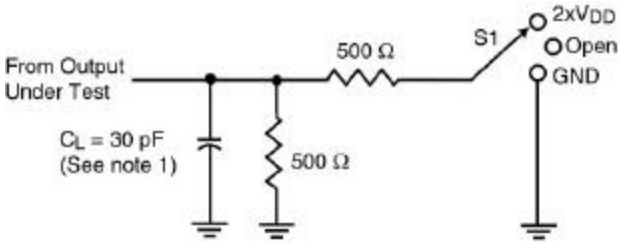
‡ Pins of A-port and B-port do not contribute to I_{DD}.

3.7 AC Specifications

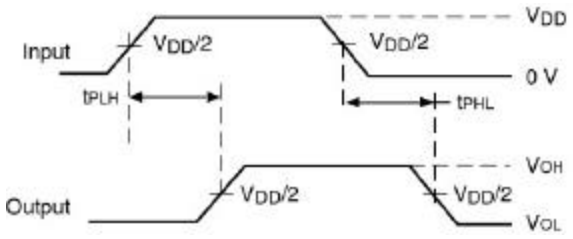
Table 8 — Switching characteristics over recommended operating free-air temperature range (see Figure 2)

Parameter	Description	Test Conditions	Comm.		Units
			Min.	Max.	
t_{PZH}	Bus Enable Time $\overline{BE}$ to Ax or Bx = High	CL = 30 pF, RL = 500 Ω	1	3	ns
t_{PZL}	Bus Enable Time $\overline{BE}$ to Ax or Bx = Low		1	3.5	
t_{PHZ}	Bus Disable Time $\overline{BE}$ to Ax or Bx =High		1	3	
t_{PLZ}	Bus Disable Time $\overline{BE}$ to Ax or Bx =Low		1	3.8	

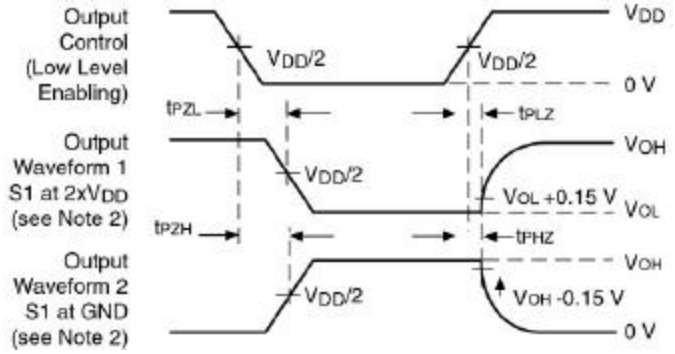
4 Parameter measurements



Load Circuit



Voltage waveforms
propagation delay times



Voltage waveforms
Enable and disable times

TEST	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	$2xV_{DD}$
t_{PHZ}/t_{PZH}	GND

Figure 3 — Parameter measurements

NOTE 1 C_L includes probe and jig capacitance.

NOTE 2 Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

NOTE 3 All input pulses are supplied by generators having the following characteristics: PRR<10 MHz, Z_O = 50 Ω, $t_R \leq 2$ ns, $t_F \leq 2$ ns.

NOTE 4 The outputs are measured one at a time with one transition per measurement.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