JEDEC STANDARD

Application Thermal Derating Methodologies

JEP149.01

(Editorial Revision of JEP149, November 2004, Reaffirmed September 2019)

JANUARY 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2021
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

or refer to www.jedec.org under Standards-Documents/Copyright Information.

APPLICATION THERMAL DERATING METHODOLOGIES

Introduction

Derating refers to the method of setting a value within the manufacturer's specifications for environmental or operational maximum use conditions. This practice has been used to provide greater functionality margin within the manufacturer's specifications, and, with the assistance of the manufacturer, potentially extend useful life or increase reliability. The process presented here is not a casual analysis, but is intended to be a part of a more sophisticated application analysis process performed by highly informed engineering staff working closely with the respective experts from the component manufacturer(s).

Derating can be used as a mitigation response to various uncertainties surrounding:

- the specification limit given by the component manufacturer,
- the actual use environmental conditions,
- the approximate nature of mathematical models normally employed.

Traditionally, users of electronic components have employed various methods for derating. They include assigning a maximum percentage of the manufacturer specification limit, setting absolute limits, or absolute margin value from the manufacturer specification limit.

While design margin is desirable, stacking of multiple sources of margin can result in high costs, lost opportunities and, potentially, increased failures (i.e. some failure mechanisms are inversely dependent on temperature). Sources of margin include:

- conservative estimates of the operational characteristics of the application,
- component manufacturer specification limit margin,
- application derating methods.

The practice of derating requires a good understanding of the manufacturer’s absolute maximum ratings, specification limits, and the consequences of approaching them. These ratings should have their foundation in the physical failure mechanisms and performance limitations associated with the component or technology in question. Also needed is a good understanding of the application use conditions and how the appropriate stress conditions can be derived from them for comparison to the manufacturers specification limits. This illustrates the need for close communication with the component manufacturer. Manufacturer’s specification limits are typically derived from a combination of technology capability, design, margin and marketing objectives. It should be noted that many of these limits are interrelated with other specifications, such as the junction temperature relationship with ambient air or case temperature through the thermal resistance of the various mechanical interfaces between them. Where such interrelationships exist, prudent derating of selected operational, performance or environmental conditions may make it possible to extend other specification limits such that the application required performance and reliability meet requirements. In these cases, the parameter or physical element most closely connected with the associated failure mechanism or required functional performance takes precedence. For example, if electromigration is a concern and it is affected by junction temperature, then junction temperature should be managed. Adjustments can occur with other related elements so long as the junction temperature is within the desired limits. These elements may include ambient air temperature or thermal resistance through thermal planes or heat sinks, power dissipation through clock speed, operational voltage, output drive (fan-out) or others.

APPLICATION THERMAL DERATING METHODOLOGIES

(From JEDEC Board Ballot JCB-20-30, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

1 Scope

This publication applies to the application of integrated circuits and their associated packages in end use designs. It summarizes the methodology of thermal derating and the suitability of such methodologies.

NOTE This publication advocates the use of derating, but leaves the amount of derating up to the user. This should vary depending on many application requirements including reliability, criticality, functional performance needs, etc. Also note that mechanical related mechanisms (such as vibration, shock, etc.) may not be suitable for derating per the methodology described here.

2 References

JEP122*, Failure Mechanisms and Models for Semiconductor Devices*

JEP143*, Solid State Reliability Assessment and Qualification Methodologies*

JESD47*, Stress Test Driven Qualification of Integrated Circuits*

JESD51*, Methodology for the Thermal Measurement of Component Packages*

JESD69*, Information Requirements for the Qualification of Silicon Devices*

JESD85*, Methods for Calculating Failure Rates in Units of FITs*

JESD94*, Application Specific Qualification Using Knowledge Based Test Methodology*

JESD51-12.01*, Guidelines for Reporting and Using Electronic Package Thermal Information JC15 document*

3 Terms and definitions

For the purposes of this standard, the following definitions apply.

Derating: The practice of using an electronic device in a narrower environmental and/or operating envelope than its manufacturer designated limits.

Application Use Conditions: The full environmental and/or operating range that the application is specified to function within.

Typical Use Conditions: The normal environmental and/or operating range that the application is known to function within. This is a subset of the Application Use Conditions.

Maximum Use Condition: This is the upper limit of an Application Use Condition.

4 Derating process

Simplistically, derating is a two step process. A “rated” stress value for the device is determined from the manufacturer’s specification, and then a reduced value is assigned for the application stress maximum.

As stated in the introduction, derating can be employed to achieve various goals. The method of derating may need to be adjusted depending on the goal as well. Since reliability is determined primarily from the use conditions the device encounters most of the time, derating for this purpose may be best achieved through a large margin from manufacturer’s specification limits, compared to typical use conditions. Conversely, if assurance of functional performance, not related to reliability (i.e., for short, unusual use conditions), is the goal, a smaller margin from the manufacturer’s specification limits, compared to maximum use conditions, may be appropriate.

In other cases, the difference between the typical and maximum use condition may be small such that these goals should be treated as the same. Here functionality and reliability should be evaluated at the maximum use condition and a margin set dependent on the customer needs and criticality of the application.

NOTE 1 With modern CMOS circuits, it may be relatively straightforward to derate for speed, but not typically so for functionality. In these cases, the published functionality limits should be used, independent from derating.

NOTE 2 When applying derating to new technologies and packages, an equipment manufacturer needs to address many issues. This typically involves user qualification tests and analyses of the technology as assembled in a typical use configuration. These tests and analyses should show a level of robustness and margin above the actual expected use conditions. The user application qualification process is out of the scope of this document, however the results of such testing and analysis can be used as a data point from which to derate from, with assistance from the component manufacturer.

4.1 Derating for reliability

Operating conditions such as temperature, power consumption, operating voltage, and output current or fanout all have an impact on reliability. Most of these impact reliability through failure mechanisms related to higher interconnect current densities, gate oxide field strength, or chip temperature. There are also package related concerns that are accelerated by temperature, such as the degradation of Au/Al intermetallic causing bond failures in plastic encapsulated devices containing certain flame retardant. Bromated epoxies release bromide when heated, which has the effect of accelerating intermetallic formation between the gold bond wires and the aluminum die bond pads[1]. Consideration is needed for the glass transition temperature of the encapsulant as well.

[1] “Reliability Implications of Derating Leading Edge High Complexity Microcircuits”, S. Richard Biddle, Texas Instruments Inc., January 26, 2000.

4.1 Derating for reliability (cont'd)

Methodologies for evaluation of semiconductor reliability can be found in JEP143 "Solid State Reliability Assessment and Qualification Methodologies". These can be factored to use conditions from acceleration factors listed in the documents referenced within JEP143 and with assistance from the manufacturer. Items to be considered include both FIT rate versus temperature and lifetime versus temperature. Figure 1 shows an example of FIT rate versus temperature. Consultation with the manufacturer is necessary for this information[2]. All of this should be factored with respect to the use operating conditions of the application. Since many of the failure mechanisms are related to operating temperature, this is used here as an example (also see Annex A for more guidance on thermal derating). In this respect, reliability is impacted by the time loading at various operating temperatures or time at temperature. In some cases, the highest known operating temperature is assumed to be constant resulting in a very conservative reliability estimate. More realistic estimates can be achieved through the use of a probability plot of time versus temperature. A conservative estimate can still be calculated using a temperature figure that contains significantly larger than 50% of the total time at temperature under this curve. For example, Figure 1 shows a mean use condition junction temperature of 55 °C, and a standard deviation of 15 °C. If the temperature 1 sigma from the mean is used in a reliability calculation, 84.1% of the total time at use condition is below that temperature. Assuming this use temperature of 70 °C as a constant temperature could be one way of providing more realistic, yet conservative, reliability estimations, while providing a large margin below the manufacturer's maximum specification limit of 120 °C.

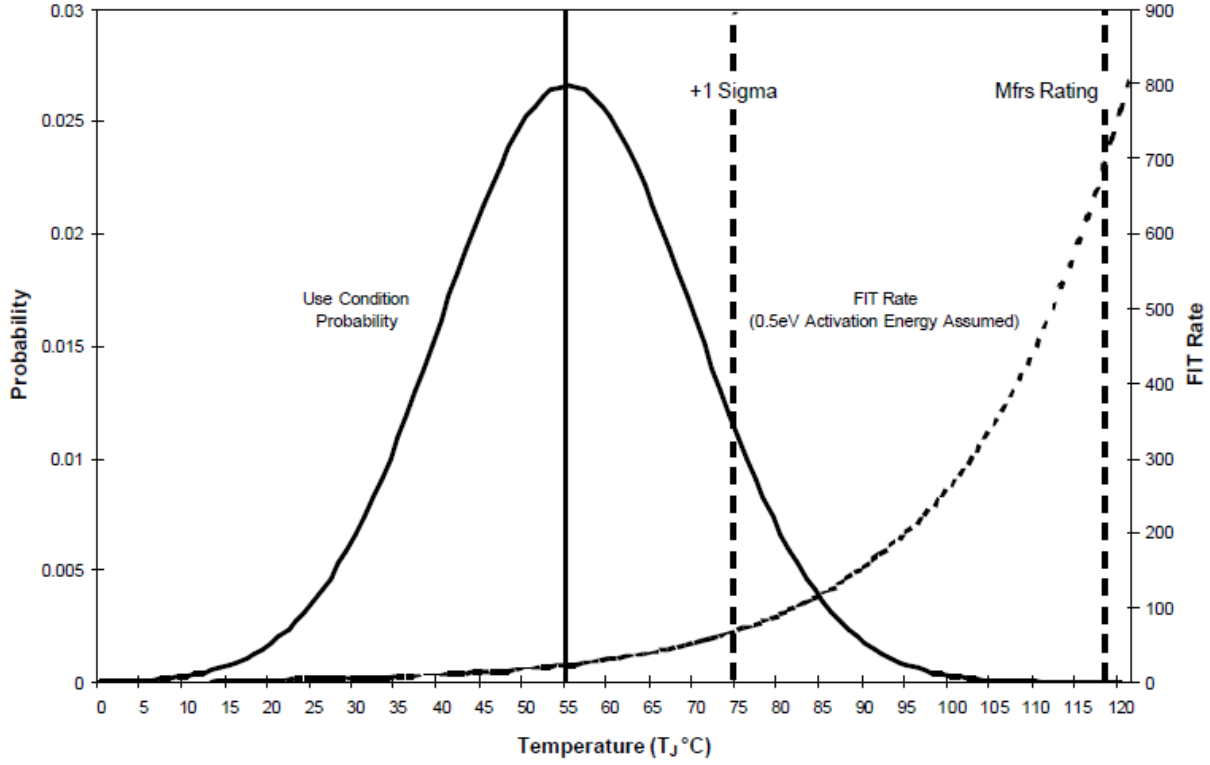

Figure 1 — Application thermal environment and FIT rate plot

[2] Manufacturers may communicate reliability and life information to customers in the form of a Quality Assurance Agreement (QAA), or similar document. Guidance from the manufacturer is necessary to extend the reliability or life data, provided in this documentation, through derating.

4.1 Derating for reliability (cont'd)

Another example of a method for determining a mathematically appropriate derating margin involves using the RMS (square root of the sum of squares) result of the quantifiable condition (electrical, environmental, etc.) as the derated value. Derating to a RMS value can be appropriate and practical; especially when there are cumulative variances or other use condition data available.

Significant operating time spent at higher temperatures will impact wearout mechanisms in semiconductor devices. JEDEC publication, JEP122 addresses many of these wearout failure mechanisms and provides general models for estimating life for various conditions.

4.2 Derating for functionality

Applications often have a relatively narrow range of "normal" operating conditions as compared to the maximum use conditions that may compose a very small percentage of the total application life. These maximum conditions are typically due to specific events like breakdown of the local area cooling system or influence of unusual weather conditions. Thus, reliability may not be significantly impacted by these maximum conditions. In such cases, the functionality of a device is required, but can be evaluated independently from reliability. The major difference is that the margin under the manufacturer rated maximum conditions can be smaller than that used for derating for reliability.

Microcircuits generally slow down at higher temperatures. Derating the application circuit to account for these slower speeds involves adding some margin to the circuit timing design and analysis.

In the example in Figure 2, functionality is assured by the manufacturer up to a junction temperature of 120 °C. The margin below this temperature should be set, taking into account the uncertainties mentioned in the Introduction and mission requirements of the application. In the example of Figure 2, statistically, 99.87% of all use time is below the 3 sigma point. For example: If the operating conditions are known with certainty, a statistical approach can be useful in setting this margin closer to the manufacturer's specification limit. If the mission requirements are less critical, the margin can also be set closer. If not, a larger margin may be necessary

4.2 Derating for functionality (cont'd)

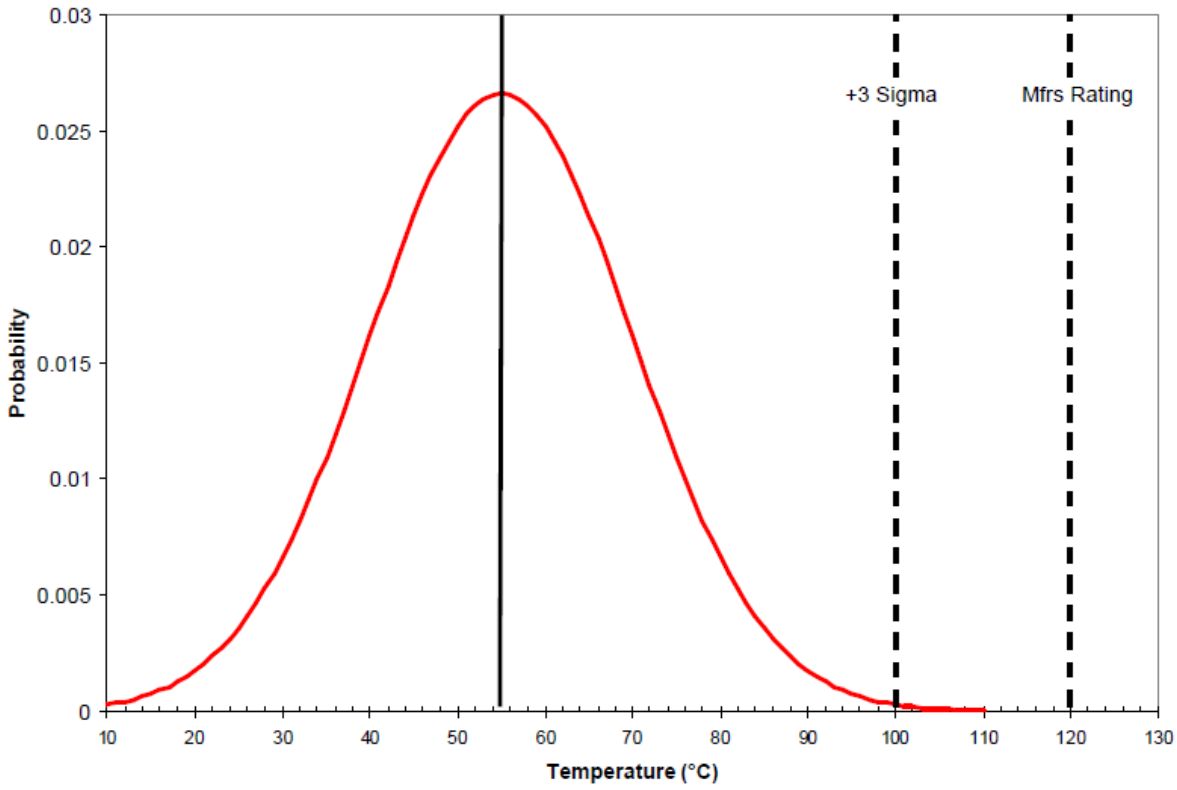

Figure 2 — Application Thermal Environment Derating

Annex A (informative) Thermal derating

The derating process essentially consists of managing the junction temperature through lower power dissipation or lower thermal resistance. The example thermal analysis at the end of this Annex shows an example of derating that could be used throughout the process of this clause.

Power dissipation can be lower in an application than the maximum specified by the manufacturer through various operating choices. These include operating at a lower frequency, lower duty cycle, lower voltage, reducing the fan-out, etc. A chart showing power dissipation derating is shown in Figure A.1. In this example, assuming the maximum rated TJ is reached at maximum rated power at 85 °C, the device could operate at 110 °C ambient if the power dissipation in the application was 60% or less of the rated maximum, thus assuring the maximum rated junction temperature is not exceeded.

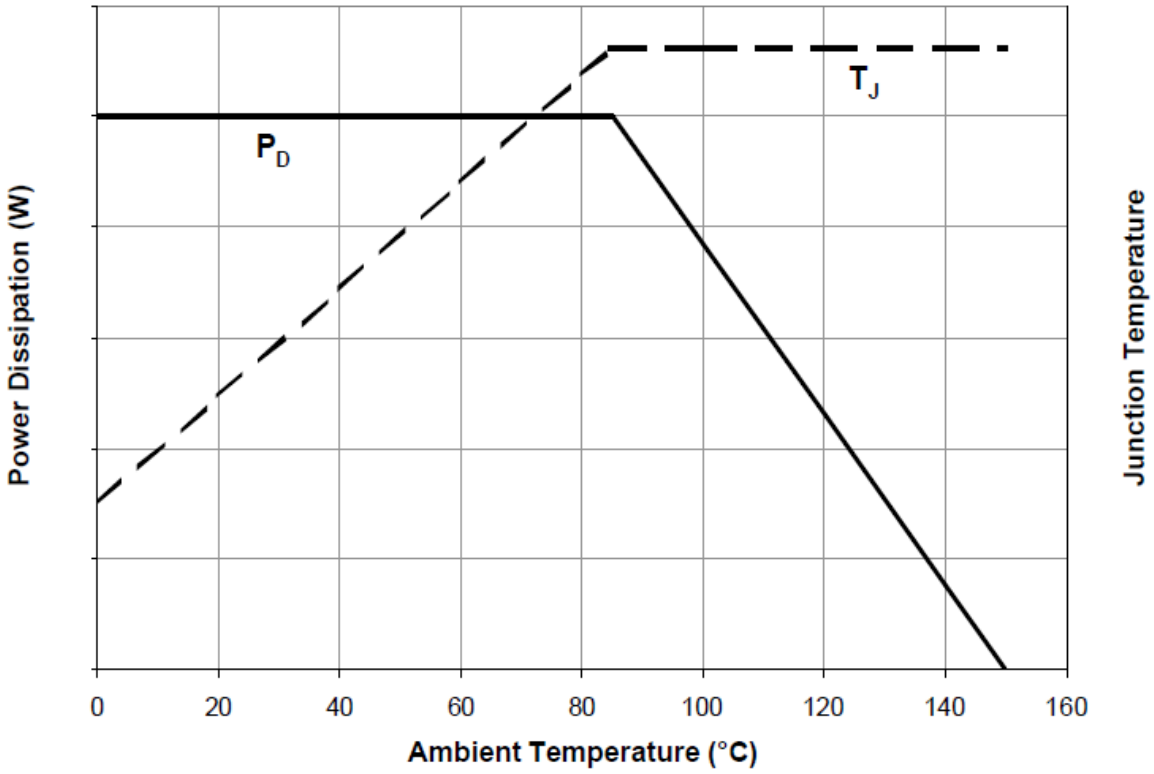

Figure A.1 — Junction Temperature versus Power Dissipation

Thermal resistance can be lowered through the addition of thermal planes in the printed wiring board, thermal pads under the part, heat sinks, etc. This has the affect of lowering the junction temperature without altering the ambient temperature or power dissipation.

Be advised that nominal operating conditions near the maximum ratings will affect reliability. Reliability is a function of how much time is spent at a particular condition. Be aware that in some new technologies, there may be an increase in power dissipation at elevated temperatures, which would mean junction temperature would not increase linearly with application temperature.

Annex A (informative) Thermal derating (cont'd)

Conversely, attempting to extend the reliability of a component beyond the published FIT rate, by reducing the power dissipation of the part (through reduction of operating frequency or other means) may have some limitations. For example: this practice may reduce electromigration effects but may not significantly affect gate-oxide wear-out. Gate-oxide wear-out is primarily related to the gate-oxide thickness and field across the oxide.

A.1 Characterize the Application Use Environment

The use environment can take many forms. If we take the example of the temperature use conditions, the application typically has a range of operating temperatures that it experiences. This range can be expressed in terms of a maximum and minimum required operating temperature or in the form of a probability density versus temperature plot. This plot can be constructed from actual application data, if available, estimated use conditions or design objectives. Optionally, it can be assumed that the device is always exposed to the worst case use temperature; however this will result in a very pessimistic reliability estimation for the application (see 3.1 for examples of determining a conservative use condition for reliability derating).

This plot will provide needed data to estimate reliability of the device and to determine probabilities of exposing the device to extreme temperatures.

A.2 Collect Thermal Information for Semiconductor Device

The process of selecting components for use in this known operating environment involves the collection and review of various component specifications. These include thermal resistance and conditions, maximum specification limits, package considerations, parametric/functional performance limits, etc. Care should be given to select components that are specified over the application operating environment. Component manufacturers will not guarantee, nor are they liable, for use outside of the published specifications.

JESD69 defines the requirements for the component qualification package, which the supplier provides on request. JESD86 describes test methods for assessing electrical parameter distributions of components, with the intent to assess their capability to function within the specification parameters over time and the application environment. JESD51, and associated parts, provide the basis for thermal measurements on component packages containing single chip semiconductors and are also the basis for determining published thermal resistance specifications.

A.3 Analyze Application to Determine Junction Temperature

Determine best thermal resistance specification to use, based on airflow, ability to direct heat away from component (i.e., thermal planes or heat sinks), and other sources of thermal heat flow. JESD51, and associated parts, is used to determine standardized thermal resistance specifications. It should be noted that these are standardized specifications and may not be equivalent to the application conditions. However, these can be used as a part of the initial thermal analysis of the application, pending actual hardware test results outlined in A.5.

A.3.1 Determine Application Power Dissipation

Determine power dissipation in component as used in the application. This power dissipation is to be used in clauses A.3.2 and A.3.3.

A.3.2 Calculate Nominal TJ for Device Application Reliability

Calculate junction temperature for nominal conditions for reliability. Adjust published FIT rate information from manufacturer to application junction temperature using appropriate acceleration factor. JESD85 is used by semiconductor manufacturers to determine FIT rates based on accelerated test results. These results can be factored to application use conditions using this standard and acceleration models from JEP122.

A.3.3 Calculate Worst Case Device T_J for Functionality

Calculate junction temperature for reasonable worst case conditions for assurance of functional performance. Compare to maximum rating for junction temperature or other specifications as appropriate to determine functionality.

A.3.4 Compare to Derating Criteria

Apply appropriate margin to achieve derating objectives. This involves assigning some value under the maximum junction temperature or percentage of junction temperature, in addition to the margin built into the manufacturer's specification limit. This value can vary depending on the needs of the application or market served.

A.4 Consult Manufacturer

If there are remaining capability questions regarding reliability or functional performance, or these cannot be determined from published information, the device manufacturer should be consulted for additional detail and guidance.

Traditionally, component capability has been demonstrated through qualification test, such as those outlined in JESD47, for basic ability to withstand certain standardized stress conditions. FIT rate versus temperature can be demonstrated using JESD85 and JEP122. Other standards for assessment of component capabilities are outlined in JEP143. Optionally, a customized qualification of the component based on application conditions may be conducted as outlined in JESD94. Manufacturers vary in their approach to these tests and analyses; thus the manufacturer should be consulted as to which methods they employ and in the appropriate interpretation and use of the resultant data.

A.5 Validation of Conclusions

Junction temperature estimations can be validated through application design test of hardware. Typically this consists of applying thermocouples to the case of various devices in question and applying case to junction thermal resistance specifications to determine junction temperature. It is recommended that the selection of locations for thermocouples be optimized based on the analysis performed in the derating process of clause 4 and by initial non-contact infrared measurements. In this way, coverage of the parts running at the highest temperature can be assured.

Annex A (informative) Thermal derating (cont'd)

Example Thermal Analysis

Step A.1 – Use Environment

Power dissipation..... 2.5 W
Case temperature maximum .....80 °C
Case temperature nominal ..... 60 °C

Step A.2 – Collect Component Specification Information

Junction temperature maximum..... 100 °C
Thermal impedance θ_{JC}..... 4.8 °C/W

Step A.3 – Application Thermal Analysis

A.3.1 – Application Power Dissipation

2.5 watts

A.3.2 – Calculate T_J for Reliability

$T_{NOM} + \theta_{JC} \bullet P_D = T_J$
60 °C + 4.8 °C/W • 2.5W = 72 °C

A.3.3 – Calculate TJ for Functionality

$T_{MAX} + \theta_{JC} \bullet P_D = T_J$
80 °C + 4.8 °C/W • 2.5W = 92 °C

A.3.4 – Compare to Derating Criteria

For reliability, this may be factored into the example FIT rate versus temperature curve in Figure 1. For 72 °C T_J, the FIT rate is approximately 80 ppb hours. This figure should be used in the overall reliability prediction for the application. (This example shows a simple calculation involving a nominal use temperature. If the use environment envelope is known with confidence [such as that shown in Figure 1] and a FIT rate versus temperature is obtained from the manufacturer, these functions can be integrated into an aggregate failure rate for reliability.)

For lifetime, wearout curves were obtained from the manufacturer that indicate a lifetime of 30 years, given a T_J nominal of 72 °C, at which point the failure rate will exceed 100 ppm. This failure level should also be factored into the application reliability prediction and lifetime compared to the application useful life requirements.

For functionality, assume that the user defines a derating criterion of 90% of maximum value for functionality. For this component, the derating level for TJ (90 °C) is not met. Further thermal mitigation actions are needed in the application design or a different component needs to be chosen.

Annex B (informative) Differences between revisions

This annex briefly describes changes made to entries that appear in this document, JEP149.01, compared to its predecessors.

A.1 Differences between JEP149.01 and JEP149 (November 2004)

Clause	Description of change
2	Added reference for JESD51-12.01

Standard Improvement Form JEDEC _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC®