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Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)

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PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)

(From JEDEC Board Ballot JCB-03-43, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This procedure is intended for VNA (Vector Network Analyzer) based measurement of pin input capacitance for devices with SSTL (Stub Series Terminated Logic) interface . This procedure does not mandate a specific method for measuring input capacitance. It has only to be considered mandatory if it is explicitly refered to by a component specification in conjunction with a value of an input capacitance defined in such a specification.

The procedure outlined below

- … was written having DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) devices in mind.
- … is expected to yield an accuracy of 10% (or 100 fF, whichever is greater) and a accuracy of 10% (or 50 fF, whichever is greater) for measuring capacitance differences (Cdelta).
- … ignores (in its simplified version) the error introduced by the inductance of the test fixture.
- … ignores the inductance of the input pin.
- … is intended for application frequencies < 200 MHz; pin inductance < 7 nH and input capacitance Cin > 1 pF.
- … allows S-parameter based de-embedding of the test fixture, if those parameters are known.
- … may be applied to interfaces other than SSTL.

2 Equipment requirements and preparation

2.1 Required hardware

- Vector Network Analyzer (e.g. Agilent 8753ES or equivalent) with minimum bandwidth of 3 GHz.
- Microwave probes (DC to 40 GHz, (G,S) or (S,G) footprint, 3.5 mm connector compatible, low-loss coaxial technique). Probe needs to support SOL (Short, Open, Load) calibration.

2 Equipment requirements and preparation (cont'd)

2.1 Required hardware (cont'd)

- Test cable, 120 cm, 20 GHz with 3.5 mm or SMA connectors, with low phase variation (phase change on bending < 4° @ radius of 58 mm)
- appropriate torque wrenches
- test fixture requirements :
  - accept components
  - allow the use of coplanar probes and add minimum parasitics *(Cfix < 0.5 pF; Lfix < 0.5 nH;* this will generally allow the simple capacitance calculation outlined in section 3.3*)*
- Probing station for fixing the probe to test fixture
- APC 7 mm to male 3.5 mm or SMA connector adapter
- Two DC power supplies
- Impedance Standard Substrate, supports SOL calibration, wide pitch range, suitable for microwave probes from DC to 40 GHz, allowing probe (G,S) or (S,G) footprint, in combination with CalKit software for VNA.

2 Equipment requirements and preparation (cont'd)

2.2 Measurement setup

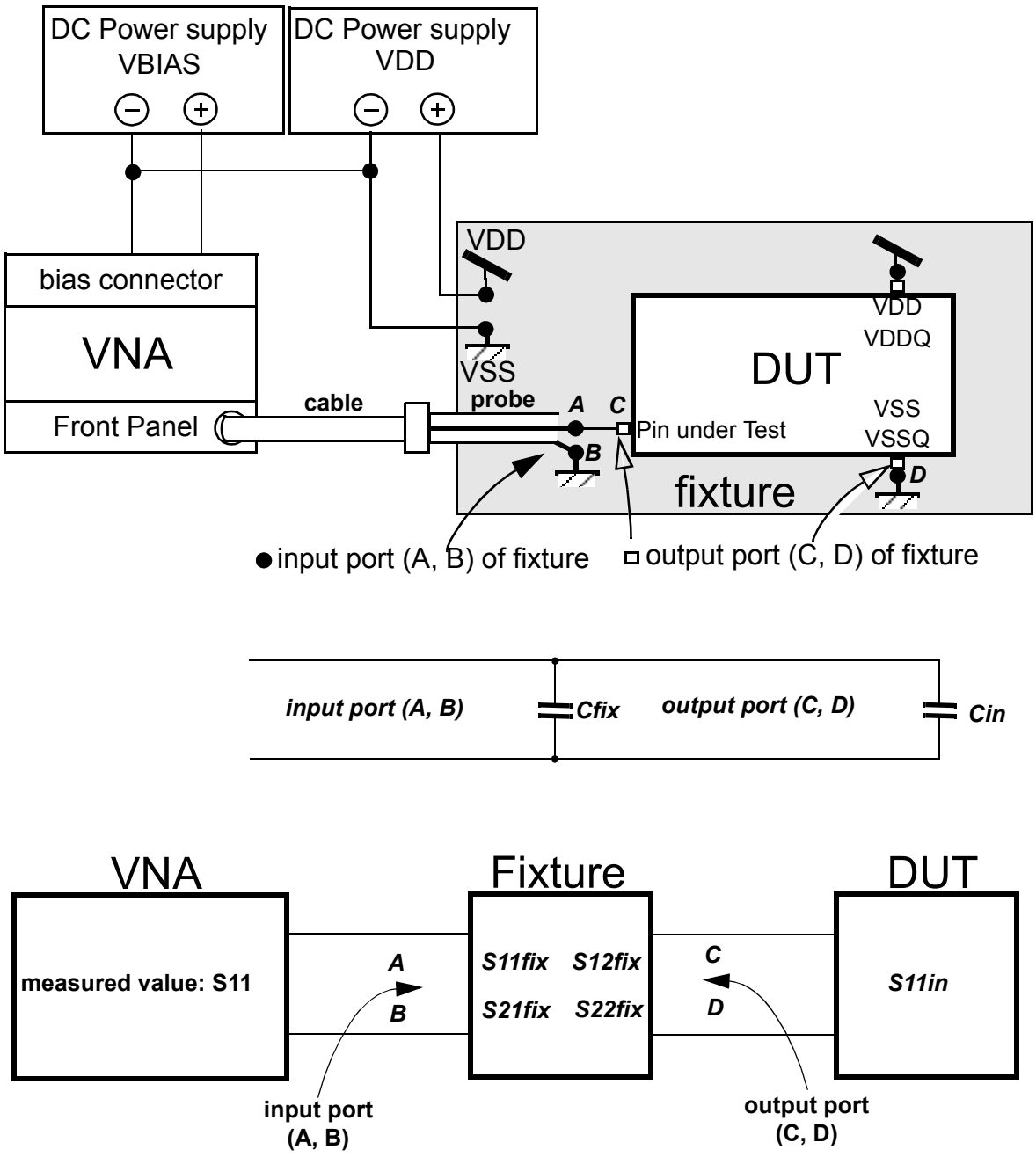

Figure 1 — Measurement setup, simple equivalent circuit and S-parameter representation

2 Equipment requirements and preparation (cont'd)

2.3 Settings

- measurement is performed at 25 ^{o}C
- start frequency: 6.25 MHz
- stop frequency: 2.5 GHz
- number of points: 400
- sweep type: linear
- sweep time: Auto
- input power: -16 dBm, DC level = VBIAS
- set current limit on VBIAS
- IF bandwidth: 30 Hz
- VDD = VDDQ = 2.5 V (for SSTL_2); VDD = VDDQ = 1.8 V (for SSTL_18)
- VBIAS = 1.25 V (for SSTL_2); VBIAS = 0.9 V (for SSTL_18)

NOTE 1 frequency sweep is recommended but not required

NOTE 2 If the nominal voltage VDDQ of the device is not VDD, then this nominal voltage should be applied.

NOTE 3 Pins for interfaces other than SSTL may be measured using the same procedure. The values specific for these interfaces need to explicitly be specified in these cases along with a reference to this procedure.

NOTE 4 "Input power" refers to the setting of the VNA and does not imply a certain power actually being driven into the pin during test.

2.4 Calibration

- SOL (50 Ω)

3 Measurement procedure

3.1 Test fixture measurement

1) Place the test fixture into the probing station.
2) Place the probe on the pins of interest, and measure S11 of the test fixture only
3) Calculate the impedance Zfix (@ f = 100 MHz):

$$Zfix = 50\Omega \times \frac{1+S11}{1-S11}$$

4) Calculate test fixture capacitance Cfix:

$$Cfix = \frac{-1}{2 \cdot \pi \cdot 100MHz \cdot Im(Zfix)}$$

3.2 Component measurement

1) Place the component with test fixture into the probing station
2) set VDD and VBIAS to the above values
3) connect other pins (not under test) to the specified voltage levels as outlined in the device specification (see section 4). Preferably all pins (other than supply pins) are left floating; this allows to measure all pins of interest without change of wiring.
4) place the probe on the pin of interest and measure S11

3.3 Capacitance calculation

1) Calculate the impedance Zterm:

$$Zterm = 50\Omega \times \frac{1+S11}{1-S11}$$

2) Calculate the total measured capacitance:

$$Ctotal = \frac{-1}{2 \cdot \pi \cdot 100MHz \cdot Im(Zterm)}$$

3) the parasitic capacitance introduced by the test fixture must be subtracted from Ctotal:

$$Cin = Ctotal - Cfix$$

3 Measurement procedure (cont'd)

3.4 S-parameter based de-embedding of fixture

If the S-parameters *Sfix* of the fixtures are known (by independent measurement or modelling), a more accurate calculation using those parameters maybe applied:

$$S11in = \frac{S11 - S11fix}{S12fix \cdot S21fix + S11 \cdot S22fix - S11fix \cdot S22fix}$$

$$Zin = 50\Omega \times \frac{1 + S11in}{1 - S11in}$$

$$Cin = \frac{-1}{2 \cdot \pi \cdot 100MHz \cdot Im(Zin)}$$

The above equations may also be used to evaluate whether the simple calculation (3.3) is a reasonable approximation.

Generally if the error introduced by the fixture is less than the greater of 3% or 60 fF, the calculation according to section 3.3 seems sufficient.

4 Example device specification

Reference to this procedure must be accompanied by language (in the device specification) determining the state (mode of operation) in which the device should be in. Below in an example for a DDR SDRAM (JESD79) (for reference only):

"Input capacitance is measured according to JEP147 with VSS, VSSQ, VDD , VDDQ applied and all other pins (except the pin under test) floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level."

5 References

General Introduction to the use of S-parameters, Agilent Technologies: Application Note AN 154

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JEDEC JEP147

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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