# JEDEC PUBLICATION

## GDDR5 Measurement Procedures

## JEP171

**AUGUST 2014**

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# GDDR5 MEASUREMENT PROCEDURES

(From JEDEC Board Ballot JCB-13-55, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

## 1 Scope

This publication is to inform all industry participants of a unified procedure to enable consistent measurement across the industry. This document contains the measurement procedures for testing GDDR5.

This document provides the test methodology details on:

1. CK and WCK Timings: tCK, tWCK, tCH/tCL, tWCKH/tWCKL, CK TJ/RJrms, CK and WCK Jitter
2. CK and WCK Input Operating Conditions: VIXCK, VIXWCK, VIDCK(ac), VIDWCK(ac), VIDCK(dc), VIDWCK(dc), CKslew, and WCKslew
3. Data Input Timings: tDIVW, tDIPW

NOTE The procedures described in this document are intended to provide information about the tests that will be used in JEDEC GDDR5 recommended measurement parameter. This testing is not a replacement for an exhaustive test validation plan.

## 2 CK and WCK Timings

### 2.1 Test Setup

1. Probe differential at the {W}CK and {W}CK_c to the oscilloscope input channels. Connect one channel ve+ to {W}CK and ve- to {W}CK_c.

NOTE Specs are defined “at the pin”; however this is difficult when implemented in a design and require probing at vias or probe points at some distance from the pin. An analysis needs to be done to determine best probe distance from the pin. It is recommended that probe points, termination and so forth be noted with the measurement results.

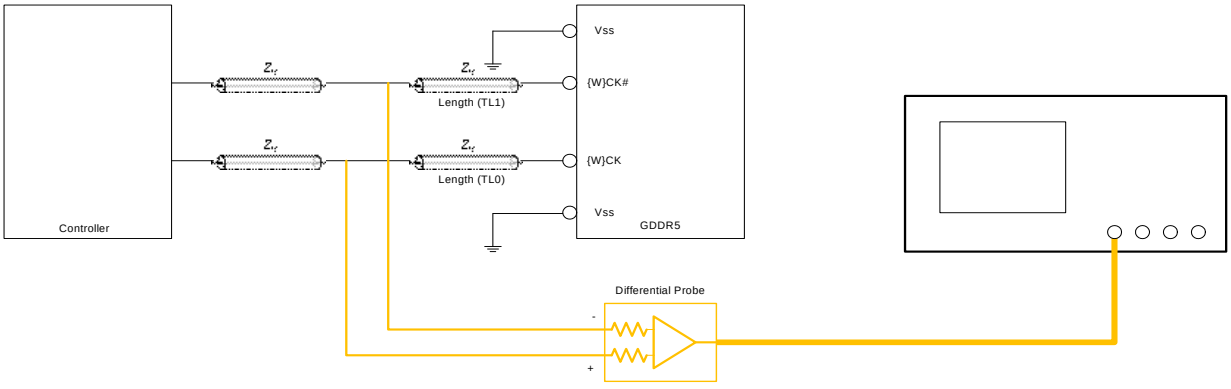


**Figure 1 — CK and WCK Timings Measurement Setup – differential**

### 2.2 tCK and tWCK Measurement Procedure

tCK and tWCK are calculated as the average clock period across any consecutive $N_{top}$ cycle window, where each clock period is calculated from rising edge to rising edge.

NOTE A single cycle can be less than t{W}CK(avg)min. spec. and greater than t{W}CK(avg)max. spec. Allowable jitter is a partner to these specifications.

$$t\{W\}CK = \left(\sum_{j=1}^{N} t\{W\}CK_j\right) / N$$
$$where\ N = N_{top}$$

#### 2.2.1 Test Procedure t{W}CK

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect one channel to {W}CK and {W}CK_c.
3. Power up device under ‘nominal’ condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the ‘nominal’ power up condition of the device.
4. Using the signals provided by the device at ‘nominal’ condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). he following is an example of steps taken:
   a. Recall factory setup on the scope.
   b. Set sample rate.
   c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.
5. Measure from rising edge at 0V to next rising edge at 0V across $N_{top}$ cycles.

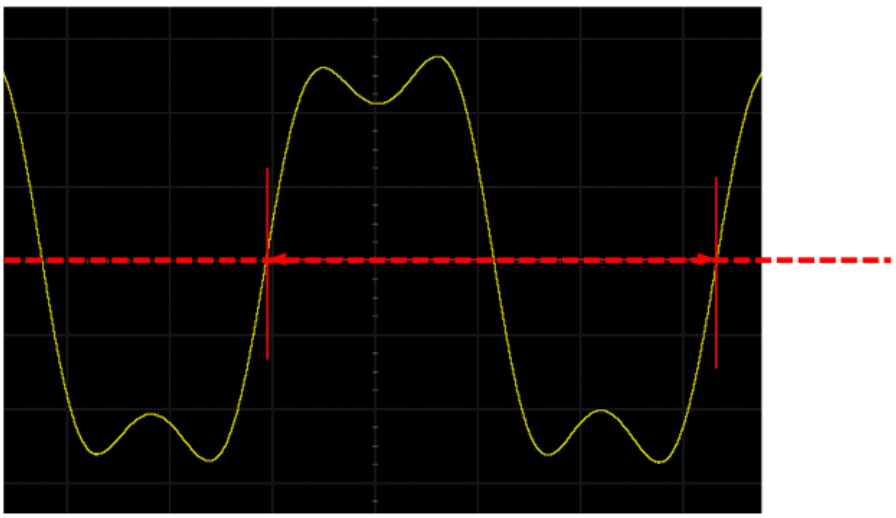

**Figure 2 — t{W}CK Measurement Example**

### 2.2.1 Test Procedure t{W}CK (cont'd)

6. Calculate t{W}CK.

$$t\{W\}CK = \left(\sum_{j=1}^{N} t\{W\}CK_j\right) / N$$
$$where\ N = N_{top}$$

7. Record values and conditions and compare against specification.

| Vdd/Vddq[1] | Temperature[2] | Probe point TL0/TL1[3] | Termination ODT enable, disable, or external[4] | Termination value[5] | ZQ | Measured value[6] |
|---|---|---|---|---|---|---|
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement.

**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement.

**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for {W}CK_c.

**NOTE 4** **Termination – ODT enable, disable, or external** – Designate the type of termination used.

**NOTE 5** **Termination value –** termination resistance.

**NOTE 6** **Measured Value –** Value measured as per procedure.

### 2.3 tCH/tCL and tWCKH/tWCKL Measurement Procedure

tCH and tWCKH are defined as the average high pulse width, as calculated across any consecutive $N_{top}$ high pulses. tCL and tWCKL are defined as the average low pulse width, as calculated across any consecutive $N_{top}$ low pulse.

$$tCH = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tCH_j\right) / (N*tCK(avg)) \qquad tWCKH = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tWCKH_j\right) / (N*tCK(avg))$$

$$tCL = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tCL_j\right) / (N*tCK(avg)) \qquad tWCKL = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tWCKL_j\right) / (N*tCK(avg))$$

#### 2.3.1 Test Procedure tCK/tCL and tWCKH/tWCKL

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect one channel to {W}CK and another to {W}CK_c.
3. Power up device under ‘nominal’ condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the ‘nominal’ power up condition of the device.
4. Using the signals provided by the device at ‘nominal’ condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). he following is an example of steps taken:
    a. Recall factory setup on the scope.
    b. Set sample rate.
    c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.
5. Measure from rising edge to falling edge at 0V for tCH and from falling edge to rising edge at 0V for tCL across $N_{top}$ cycles.

### 2.3.1 Test Procedure tCK/tCL and tWCKH/tWCKL (cont'd)

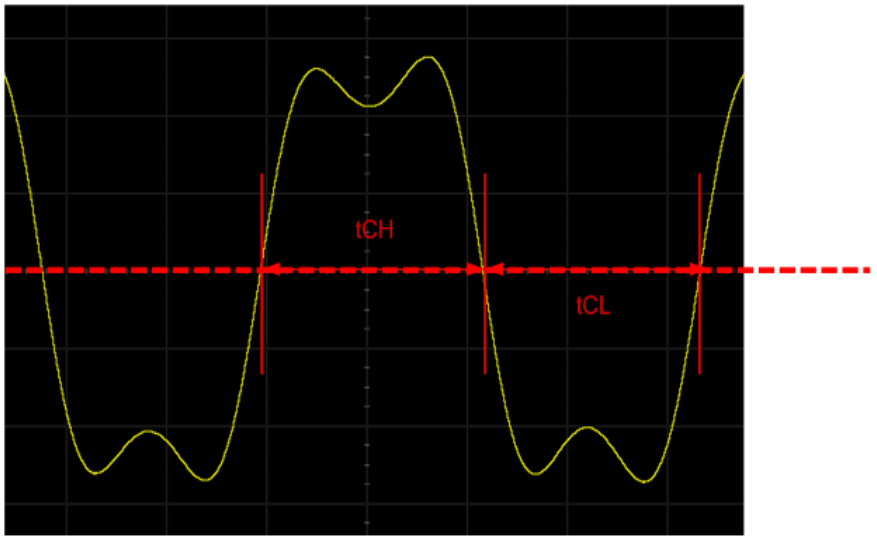


**Figure 3 — tCH/tCL Measurement Example**

6. Calculate tCH/tWCKH and tCL/tWCKL.

$$tCH = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tCH_j\right) / (N*tCK(avg)) \qquad tWCKH = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tWCKH_j\right) / (N*tCK(avg))$$

$$tCL = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tCL_j\right) / (N*tCK(avg)) \qquad tWCKL = \left(\sum_{\substack{j=1 \\ where\ N=N_{top}}}^{N} tWCKL_j\right) / (N*tCK(avg))$$

7. Record values and compare to specification.

| Vdd/Vddq[1] | Temperature[2] | Probe point TL0/TL1[3] | Termination ODT enable, disable, or external[4] | Termination value[5] | ZQ | Measured Value[6] |
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement.
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement.
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for {W}CK_c.
**NOTE 4** **Termination – ODT enable, disable, or external** – Designate the type of termination used.
**NOTE 5** **Termination value –** termination resistance.
**NOTE 6** **Measured Value –** Value measured as per procedure.

### 2.4 CK and WCK Jitter Measurement Procedure

Jitter for WCK and CK clocks are defined for N-cycle half-period jitter. TIE is measured across Mjtr half-cycles. TJN and RJN(rms) are calculated for each N-cycle half-period up to Ntop at the tested Bit Error Ratio (BER).

**Table 1 — Key Jitter Characterization Parameter**

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Number of half periods per Jitter Measurement | $M_{jtr}$ | $1e^{+6}$ | | | 1 |
| Number of half periods across which Cumulative Error is Measured with PLL Off | $N_{top\text{-}off}$ | 50 | | | |
| Number of half periods across which Cumulative Error is Measured with PLL On | $N_{top\text{-}on}$ | | | | 2 |
| Bit Error Ratio | BER | | | | 3,4 |

1. A half period, in this context, is one half of one clock cycle.
2. Vendor specified value.
3. Vendor specified Bit Error Ratio.
4. Bit Error Ratio is the probability for a single bit to be received in error. It is recommended that this value not be less than 1e-12

For CK and WCK clocks, the maximum allowable jitter information can be measured and reported for N-cycle Half Period jitter as shown in Table 2. Refer to vendor specified values for application speed and PLL on or off case. The conditions involving temperature, VDD, and VDDQ are all recommended to be determined and reported along with the jitter results.

**Table 2 — Maximum Allowable Clock Input Jitter for N-Cycle Half Period Jitter tCK/tWCK = tbd Ghz Temp = tbd, VDD = tbd, VDDQ = tbd**

| N | $RJ^N$ RMS | $TJ^N$ |
|---|---|---|
| 1 | | |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| ... | | |
| Ntop | | |

#### 2.4.1 Test Procedure {W}CK Jitter

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect one channel to {W}CK and {W}CK_c.
3. Power up device under ‘nominal’ condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the ‘nominal’ power up condition of the device.
4. Using the signals provided by the device at ‘nominal’ condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
    a. Recall factory setup on the scope.
    b. Set sample rate.
    c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.

### 2.4.1 Test Procedure {W}CK Jitter (cont'd)

5. Measure at 0V crossing point from actual edge vs ideal for each 0 to Mjtr half-cycles. Ideal half-period is defined as a measured average creating a TIE mean of zero. $F_k = t_k - t_{refk}$, k = 0,...,Mjtr.

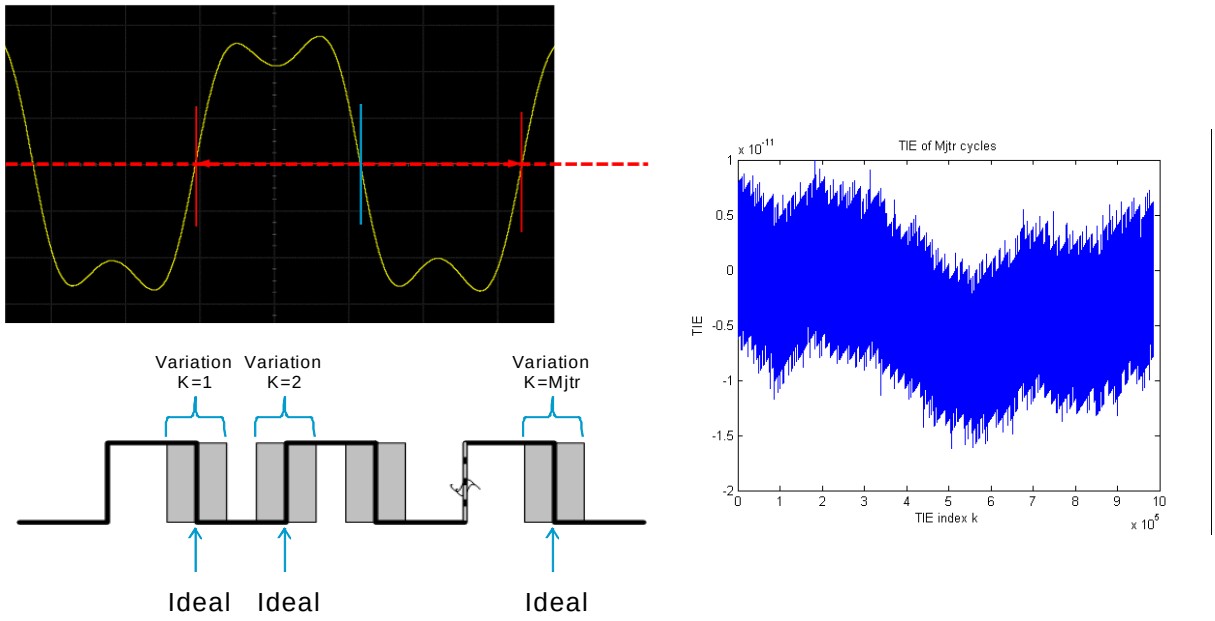
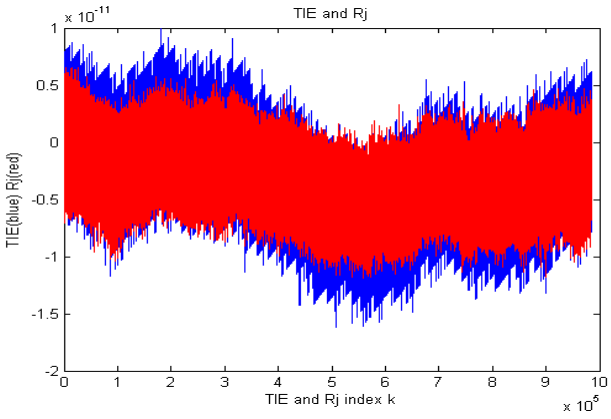



**Figure 4 — Measure WCK and CK from Ideal**

6. Separate TIE sequence F into DJ and RJ sequences. After separation, each point in TIE can be represented as: $F_k = DJ_k + RJ_k$, k=0,...,Mjtr, see Figure 5.

NOTE There are several methods to separate RJ and DJ. Any method to separate RJ and DJ in to their index values is an acceptable method.)




TIE – blue
Rj – red

**Figure 5 — Calculate Rj for each index k**

7. Calculate differences for $F^N$ for TIE F and $RJ^N$ for RJ for each N half-cycle. $F^N_k = F_k - F_{k-N}$ and $RJ^N_k = RJ_k - RJ_{k-N}$ where k=N,..,Mjtr; N=1,...,Ntop

### 2.4.1 Test Procedure {W}CK Jitter (cont'd)

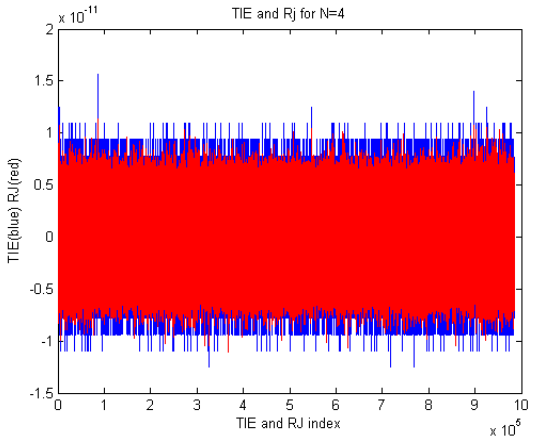



**Figure 6 — Calculate $F^N$ and $RJ^N$**

8. Calculate the standard deviation for RJ for each N from step 7 to get $RJ^N$(rms).
9. Calculate $DJ_{dd}{}^N$ (for each N = 1..Ntop) using max $F^N$ and min $F^N$ from step 7 and $RJ^N$(rms) from step 9. Djdd = max($F^N$) - min($F^N$) - 2*Q(1/Mjtr)*s($RJ^N$) where Q(x) = sqrt(2)*erfc$^{-1}$(2x)
10. Calculate TJN (for each N = 1..Ntop). $TJ^N = DJ_{dd}{}^N + 2*Q(BER)*s(RJ^N)$.
11. Record values and compare to specification.

| N | Vdd/Vddq[1] | Temerature[2] | Probe point TL0/TL1[3] | BER[4] | tck/tWCK[5] | TJN[6] | RJN(rms)[7] |
|---|---|---|---|---|---|---|---|
| 1 | | | | | | | |
| 2 | | | | | | | |
| 3 | | | | | | | |
| 4 | | | | | | | |
| 5 | | | | | | | |
| 6 | | | | | | | |
| 7 | | | | | | | |
| 8 | | | | | | | |
| ... | | | | | | | |
| N top | | | | | | | |

**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement.
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement.
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for {W}CK_c.
**NOTE 4** **BER** – Tested bit error ratio.
**NOTE 5** **tCK/tWCK –** CK ir WCK cycle time tested.
**NOTE 6** **TJN –** Total jitter from step 10 for each N half-cycle.
**NOTE 7** **RJN(rms) –** RMS Random Jitter from step 8 for each N half-cylce.

# 3 CK and WCK Input Operating Conditions

## 3.1 Test Setup

1. Probe dual single ended at the {W}CK and {W}CK_c to the oscilloscope input channels. Connect one channel to {W}CK and Vss and another to {W}CK_c and Vss. Vid is measured on a differential signal. Vid can be connected the same and then a math function to measure a differential signal or connected as shown in figure 8. [Note: Specs are defined “at the pin”; however this is difficult when implemented in a design and require probing at vias or probe points at some distance from the pin. An analysis needs to be done to determine best probe distance from the pin. There are variable termination possibilities – ODT, external termination, or no termination. There are also variable loading possibilities and sharing between die. It is recommended that probe points, termination and so forth be noted with the measurement results.]

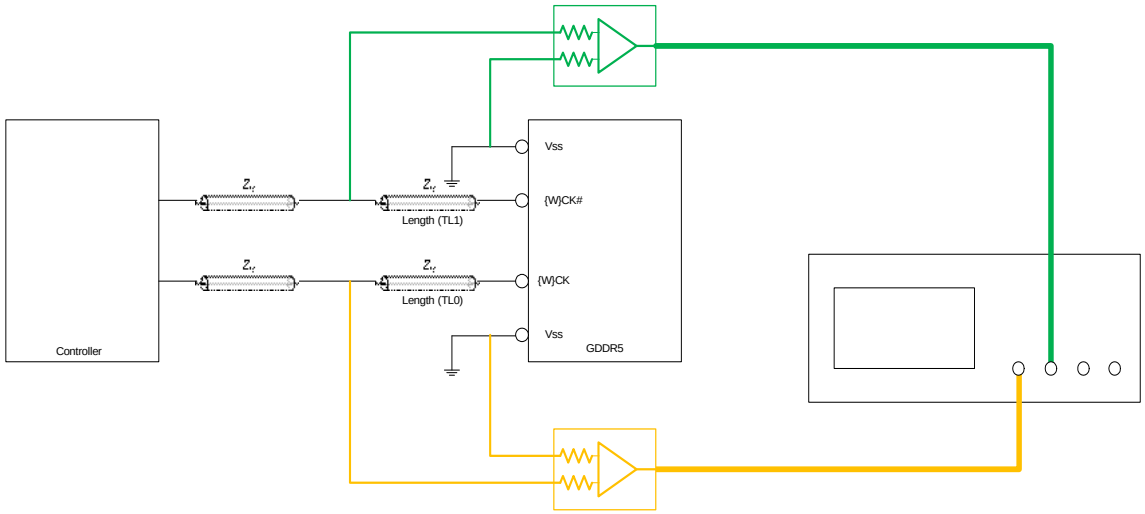



**Figure 7 — CK and WCK Input Operating Conditions Measurement Setup - Dual Singled Ended**

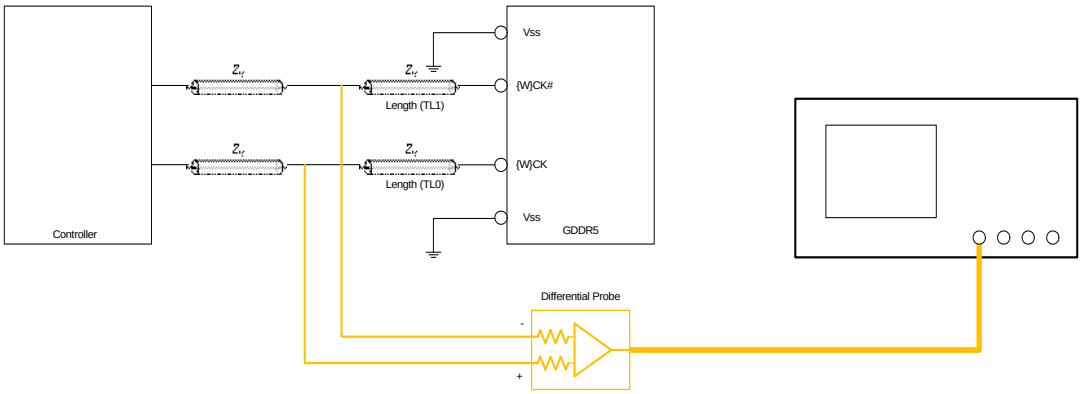



**Figure 8 — Alternative for Vid Measurements – differential**

### 3.2 VIXCK(ac) and VIXWCK(ac) Measurement Procedure

VIX{W}CK is the clock input crossing point voltage. For CK/CK_c, the crossing point must be within +/- 0.12V of VREFC. For WCK/WCK_c, the crossing point must be within +/- 0.10V of VREFD.

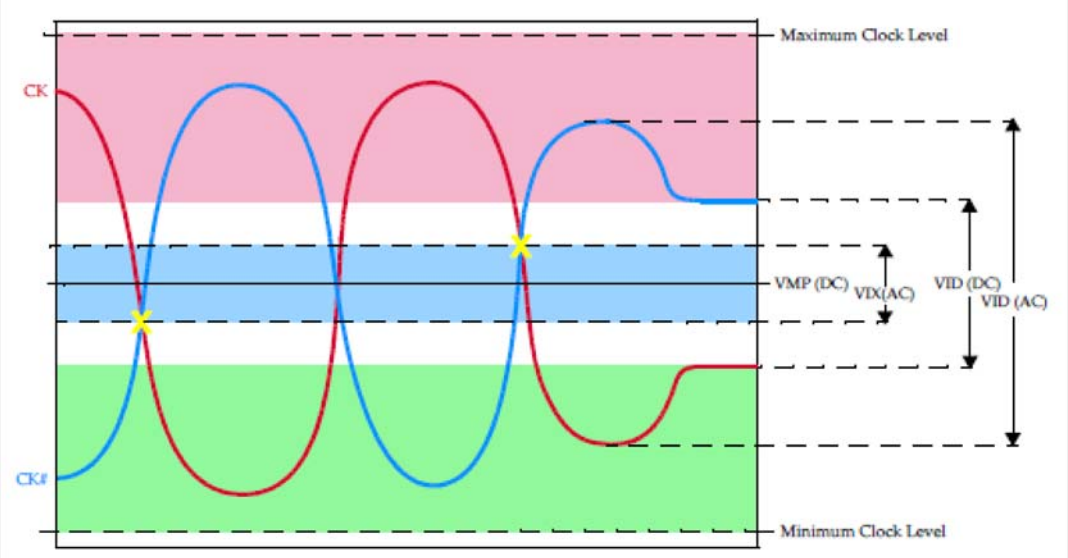



**Figure 9 — Definition for VIX(ac)**
References: [1] GDDR5 SGRAM specification (rev G) – Figure 82

#### 3.2.1 Test Procedure

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect two active probes to oscilloscope channels.
3. Connect one channel to {W}CK and another to {W}CK_c.
4. Power up device under ‘nominal’ condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the ‘nominal’ power up condition of the device.
5. Using the signals provided by the device at ‘nominal’ condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
    a. Recall factory setup on the scope.
    b. Set sample rate.
    c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.
6. Turn on sin(x)/x interpolation.
7. For CK, measure the “mean” voltage of VREFC and for WCK, measure the “mean” voltage of VREFD across 200 CK or WCK cycles. There are various methods to measure the “mean” voltage of VREF(C/D) depending on preference and measurement equipment. Any tool that measures and calculates the mean value is an acceptable method. Examples include a scope’s histogram or statistical software that measures and calculates the mean voltage. The following is an example using a vertical histogram to measure the mean of VREFC across the 200 clock cycles for slew measurement. (Note: If VREFD is internal, it is up to the user to define what the effective vref level is based on internal vrefd optimization that was done for any particular system).

### 3.2.1 Test Procedure (cont'd)

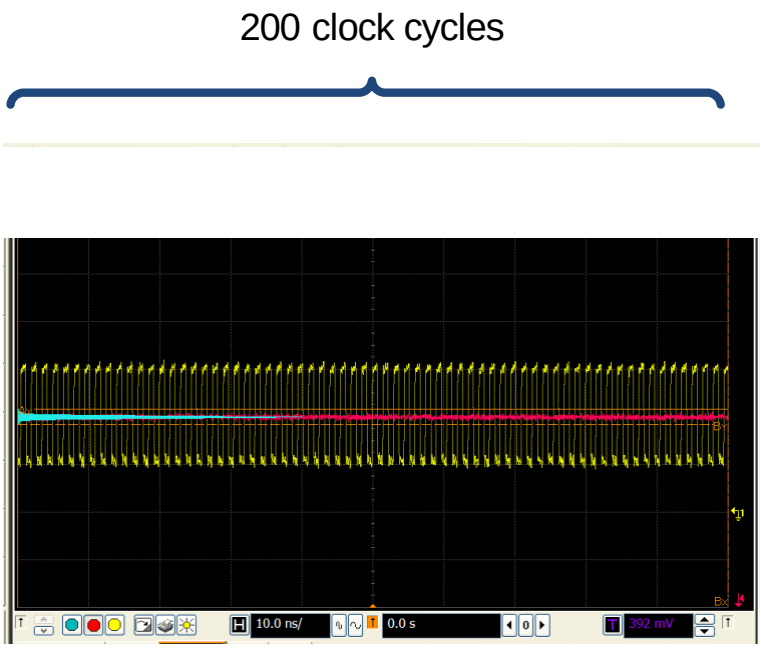



**Figure 10 — Set measurement across 200 cycles**

8. Measure the crossing points of {W}CK and {W}CK_c. There are various methods to measure the crossing point depending on preference and measurement equipment. Examples include marker placement at crossing points or scopes embedded software that finds and measures the crossing points. The following is an example using a marker placement to measure the {W}CK and {W}CK_c crossing points.

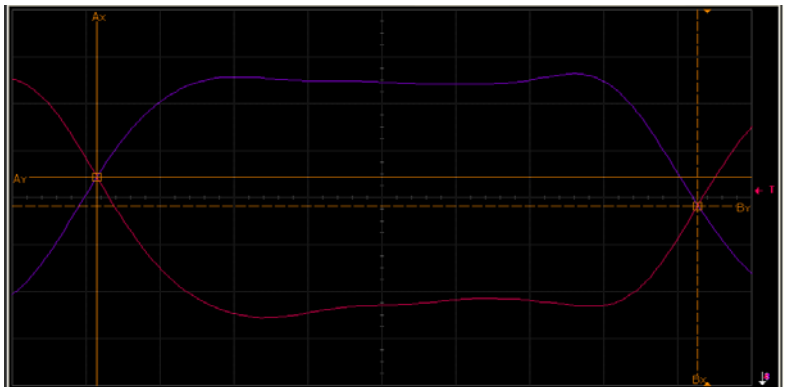


**Figure 11 — Markers are placed at the crossing points to make voltage measurements**

### 3.2.1 Test Procedure (cont'd)

9. Record the voltage level of the crossing points (Vcrossing). Reference values as a difference from VREF(C/D) and record value of maximum difference from VREF(C/D) for both the positive and negative Vix values. Value = Vcrossing – Vref. This number will be negative for values crossing below the Vref and positive for crossing above Vref.

10. Repeat across 200 cycles.

11. Record the most positive value in the positive Vix column and the most negative value in the negative Vix column. Record measurement conditions.

| Vdd/Vddq[1] | Temerature[2] | Probe point TL0/TL1[3] | Termination ODT enable, disable, or external[4] | Termination value[5] | ZQ | Measured Value Positive Vix[6] | Measured Value Negative Vix[7] |
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement.
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement.
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for Vref(c/d).
**NOTE 4** **Termination – ODT enable, disable, or external** – Designate the type of termination used.
**NOTE 5** **Termination value –** termination resistance.
**NOTE 6** **Measured Value Positive Vix –** Positive measured value as per procedure (Vcrossing – Vref).
**NOTE 7** **Measured Value Negative Vix –** Negative measured value as per procedure (Vcrossing – Vref).

### 3.3 VIDCK(ac) and VIDWCK(ac) Measurement Procedure

VIDCK is the magnitude of the difference between the input level in CK and the input level on CK_c. The input reference level for signals other than CK and CK_c is VREFC. VIDWCK is the magnitude of the difference between the input level in WCK and the input level on WCK_c. The input reference level for signals other than WCK and WCK_c is either VREFD, VREFD2 or the internal VREFD. The CK and CK_c input reference level (for timing referenced to CK and CK_c) is the point at which CK and CK_c cross. The WCK and WCK_c input reference level (for timing referenced to WCK and WCK_c) is the point at which WCK and WCK_c cross.

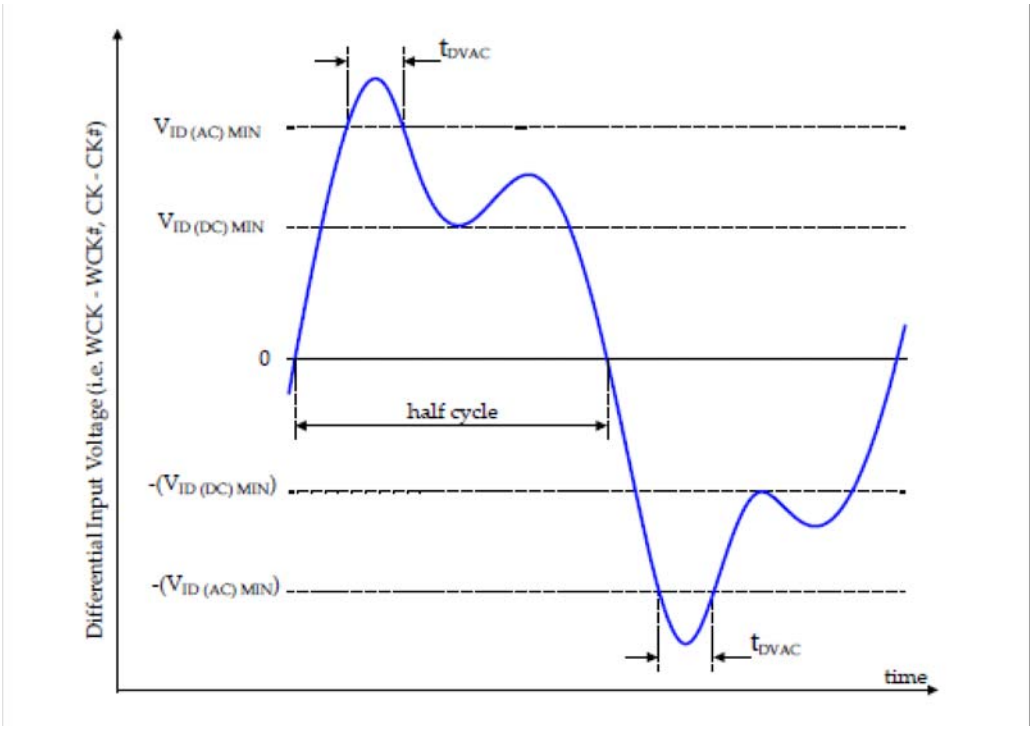


**Figure 12 — Definition of differential ac-swing and "time above ac-level" tDVAC**
References: [1] GDDR5 SGRAM specification (rev G) – Figure 83

#### 3.3.1 Test Procedure

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect two active probes to two oscilloscope channels.
3. Connect one channel to {W}CK and {W}CK_c.
4. Power up device under 'nominal' condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the 'nominal' power up condition of the device.
5. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
    a. Recall factory setup on the scope.
    b. Set sample rate.
    c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.

### 3.3.1 Test Procedure (cont'd)

6. Determine measurement window. The beginning of the window (t0) starts when the signal crosses Vid(ac) spec value (400mV). The end of the window (t2) is tDVAC from t0. The beginning of the measurement window (t1) is the first peak of the signal after it crosses Vid(ac). [Note: this is used as the beginning of the measurement window to measure a real Vid(ac) value and margin. Using t0 as the beginning, would always measure a value of Vid(ac) or less.] If tDVAC is 0 – t2=t1=t0.

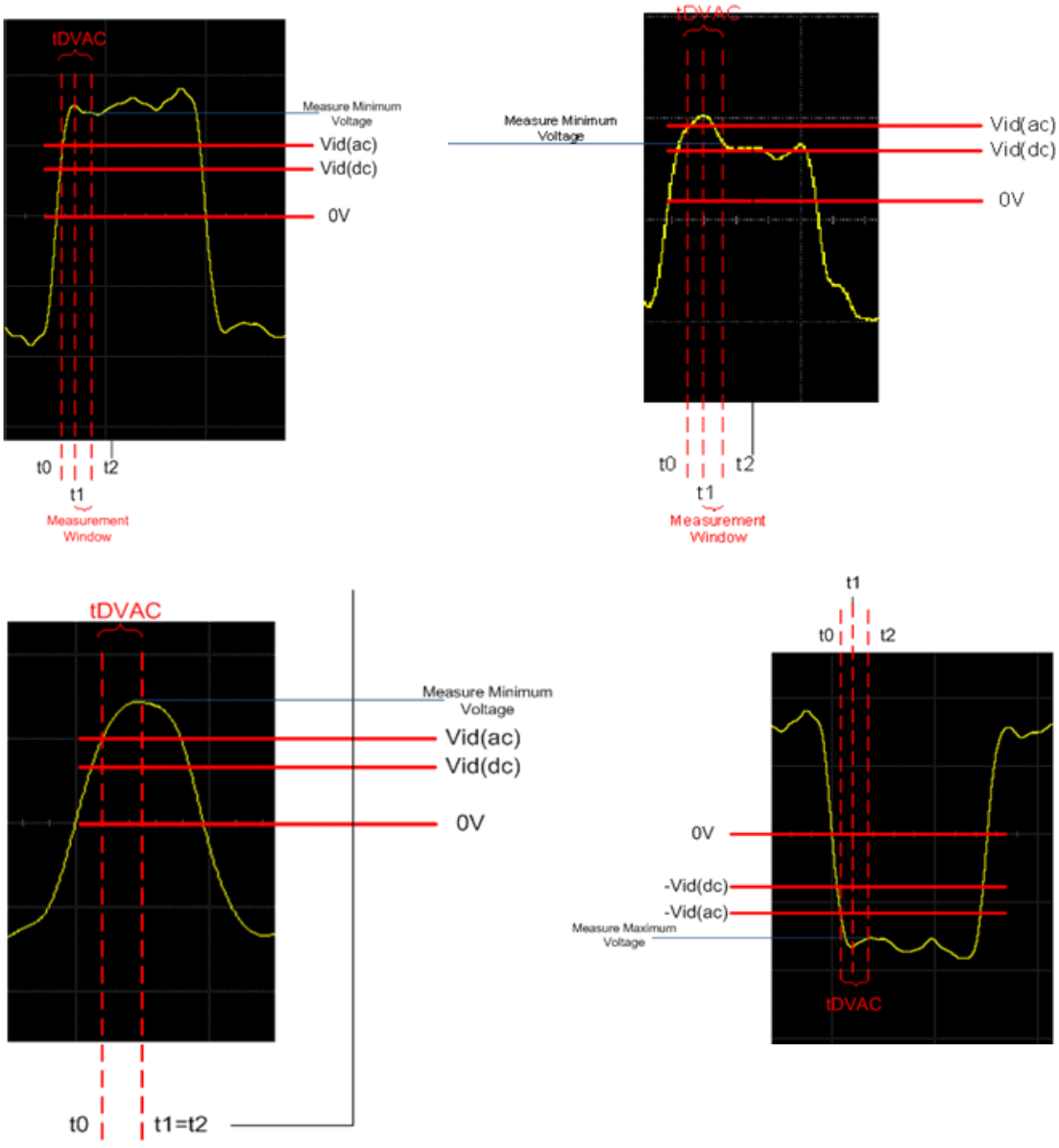


**Figure 13 — Measurement Window Examples**

### 3.3.1 Test Procedure (cont'd)

7. VID(ac) is the min voltage value within the valid window time for the high signal and the max voltage value within the valid window time for the low signal. There are various methods to measure the "min" voltage within the defined measurement window depending on preference and measurement equipment. Any tool that measures the min value is an acceptable method. Examples include a scope's histogram or statistical software that measures the voltage. The following is an example using a vertical histogram to measure the min voltage value within the measurement window.

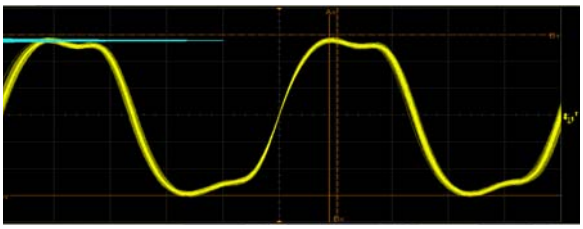

**Figure 14 — Histogram measurement for VID(ac)**

8. Repeat measurements across 200 cycles. Record min value for high clock and max value for low clock and compare against Vid{W}CK(ac).

9. Record values and conditions.

| Vdd/Vddq[1] | Temerature[2] | Probe point TL0/TL1[3] | Termination ODT enable, disable, or external[4] | Termination value[5] | ZQ | Measured Value [6] |
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement.
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement.
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for {W}CK_c.
**NOTE 4** **Termination – ODT enable, disable, or external** – Designate the type of termination used.
**NOTE 5** **Termination value –** termination resistance.
**NOTE 6** **Measured Value –** Value measured as per procedure.

### 3.4 VIDCK(dc) and VIDWCK(dc) Measurement Procedure

VIDCK is the magnitude of the difference between the input level in CK and the input level on CK_c. The input reference level for signals other than CK and CK_c is VREFC. VIDWCK is the magnitude of the difference between the input level in WCK and the input level on WCK_c. The input reference level for signals other than WCK and WCK_c is either VREFD, VREFD2 or the internal VREFD. The CK and CK_c input reference level (for timing referenced to CK and CK_c) is the point at which CK and CK_c cross. The WCK and WCK_c input reference level (for timing referenced to WCK and WCK_c) is the point at which WCK and WCK_c cross. [See figure 5]

There is no specific spec when CK or WCK can cross Vid(dc). Two specs that have to be met are tCH/tCL and slew rate. These two specs help indicate when it is valid for the signal to cross Vid(dc) [See Figure 2] .

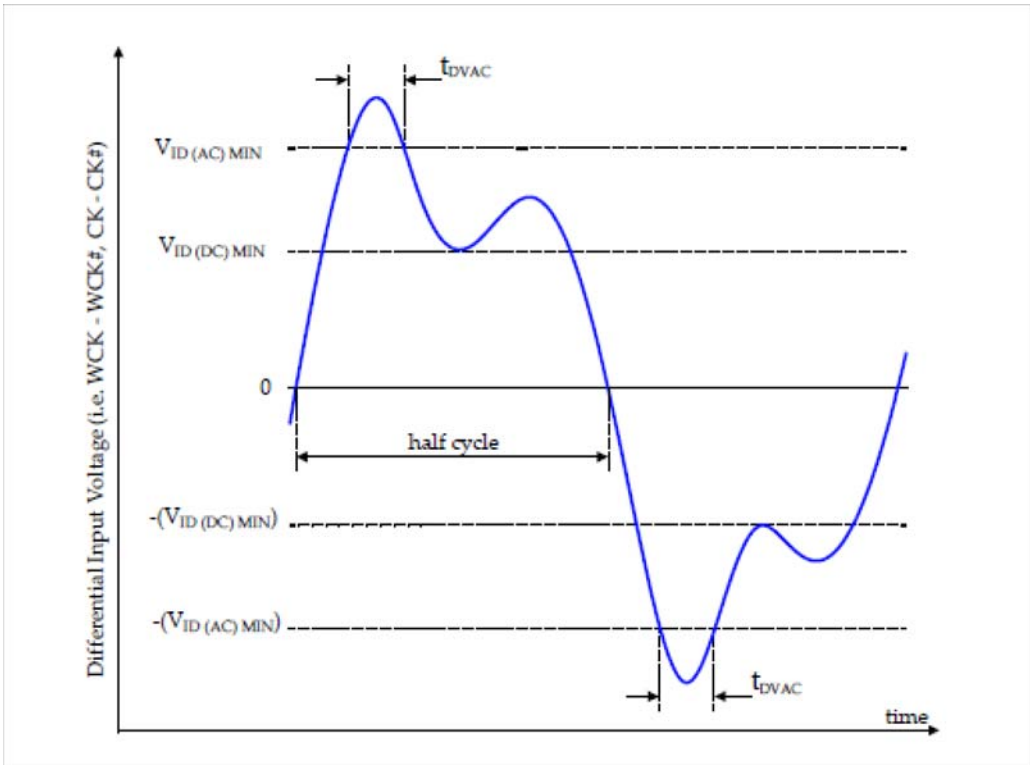


**Figure 15 — Definition of differential ac-swing and "time above ac-level" tDVAC**

References: [1] GDDR5 SGRAM specification (rev G) – Figure 83

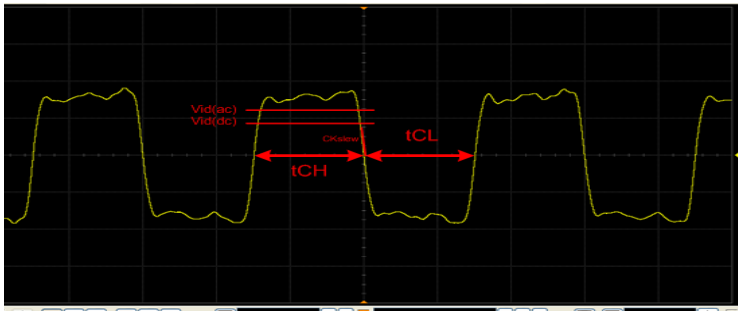


**Figure 16 — The signal is valid to cross Vid(dc) when both tCH and min slew rate are met**

### 3.4 IDCK(dc) and VIDWCK(dc) Measurement Procedure (cont'd)

#### 3.4.1 Test Procedure

1. Perform scope and probe calibration as required by the equipment manufacturer.

2. Connect two active probes to two oscilloscope channels.

3. Connect one channel to {W}CK and another to {W}CK_c.

4. Power up device under 'nominal' condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the 'nominal' power up condition of the device.

5. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:

   a. Recall factory setup on the scope.
   b. Set sample rate.
   c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.

6. Determine measurement window. The beginning of the measurement window (t1) is the first peak after the signal crosses Vid(ac)

   NOTE The point at which the signal shall not cross Vid(dc) until the end of the pulse). The end of the measurement window (t2) is t@0V + tCH – 1/[6V/ns/Vid(dc))].

   The end of the window is defined by when the signal can legally cross below the dc value – meeting both tCH and the minimum slew rate of 6V/ns.

### 3.4 IDCK(dc) and VIDWCK(dc) Measurement Procedure (cont'd)

#### 3.4.1 Test Procedure (cont'd)

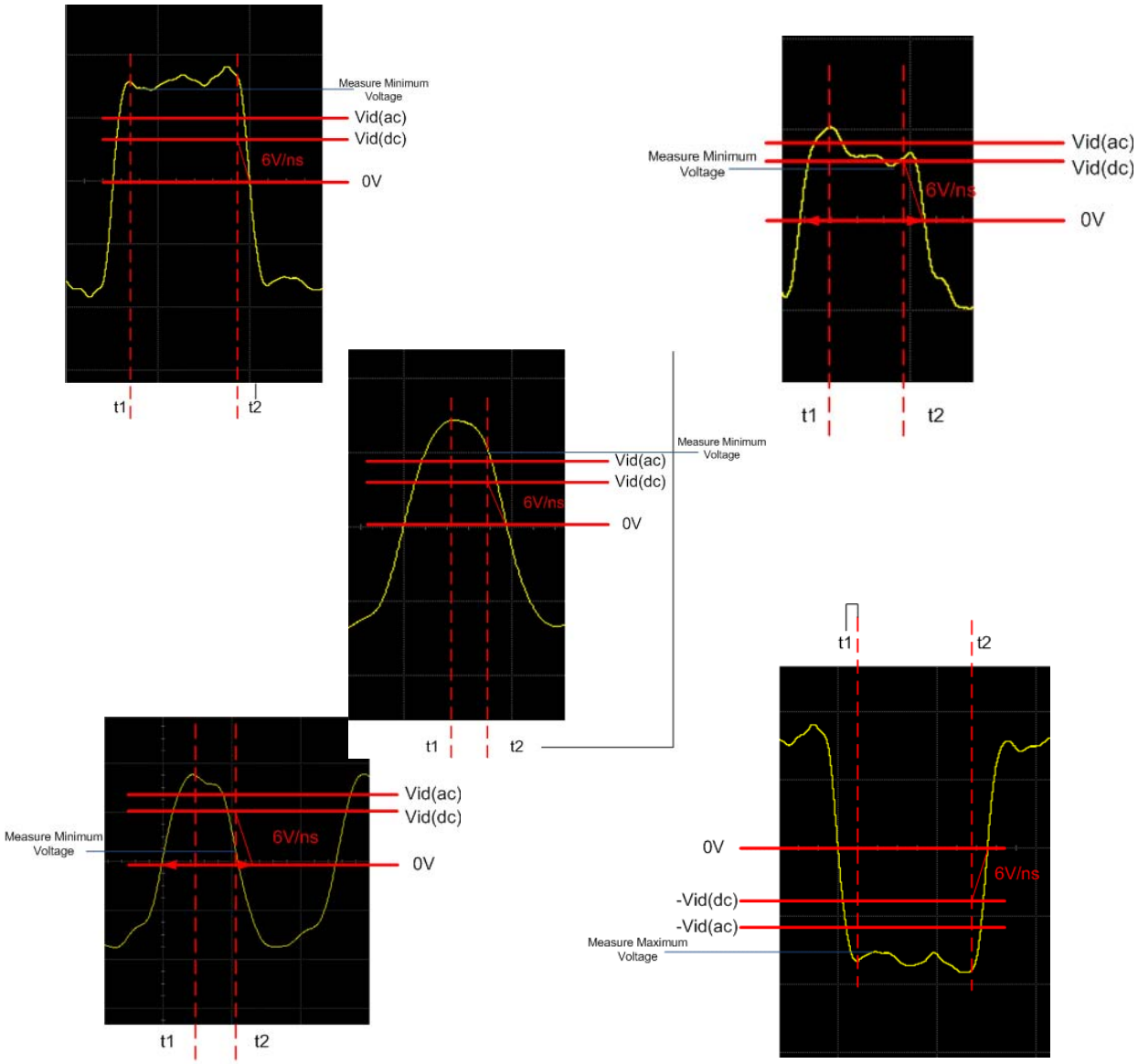


**Figure 17 — Measurement Window Examples**

7. VID(dc) is the min voltage value within the valid window time for the high signal and the max voltage value within the valid window time for the low signal. There are various methods to measure the "min" voltage within the defined measurement window depending on preference and measurement equipment. Any tool that measures the min value is an acceptable method. Examples include a scope's histogram or statistical software that measures the voltage. The following is an example using a vertical histogram to measure the min voltage value within the measurement window.

### 3.4 IDCK(dc) and VIDWCK(dc) Measurement Procedure (cont'd)

#### 3.4.1 Test Procedure (cont'd)

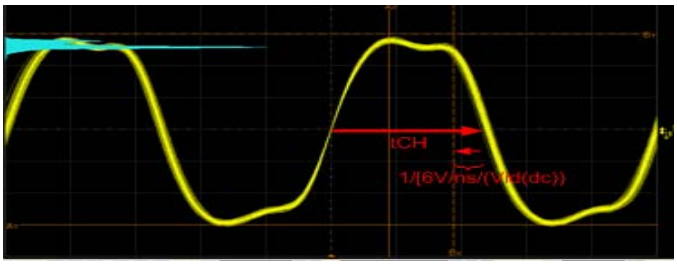


**Figure 18 — Histogram measurement for VID(ac)**

8. Repeat measurements across 200 cycles. Record min value for high clock and max value for low clock and compare against Vid{W}CK(dc).

9. Record values and conditions.

| Vdd/Vddq[1] | Temerature[2] | Probe point TL0/TL1[3] | Termination ODT enable, disable, or external[4] | Termination value[5] | ZQ | Measured Value [6] |
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement.
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement.
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for {W}CK_c.
**NOTE 4** **Termination – ODT enable, disable, or external** – Designate the type of termination used.
**NOTE 5** **Termination value –** termination resistance.
**NOTE 6** **Measured Value –** Value measured as per procedure.

### 3.5 CKslew and WCKslew Measurement Procedure

CKslew and WCKslew are the single ended slew rate measurements for their respective clock. CKslew is measured from VREFC crossing and VIXCK(ac). WCKslew is measured from VREFD crossing and VIXWCK(ac).

#### 3.5.1 Test Procedure

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect two active probes to oscilloscope channels.
3. Connect one channel to {W}CK and another to VREFC(for CK) or VREFD(for WCK).
4. Power up device under 'nominal' condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the 'nominal' power up condition of the device.
5. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
    a. Recall factory setup on the scope.
    b. Set sample rate.
    c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.
6. Turn on sin(x)/x interpolation.
7. For CK, measure the "mean" voltage of VREFC and for WCK, measure the "mean" voltage of VREFD across 200 CK or WCK cycles. There are various methods to measure the "mean" voltage of VREF(C/D) depending on preference and measurement equipment. Any tool that measures and calculates the mean value is an acceptable method. Examples include a scope's histogram or statistical software that measures and calculates the mean voltage. The following is an example using a vertical histogram to measure the mean of VREFC across the 200 clock cycles for slew measurement. (Note: If VREFD is internal, it is up to the user to define what the effective vref level is based on internal vrefd optimization that was done for any particular system. 200 cycles is the recommended minimum number of cycles. It is up to the user to define the effective number of cycles based on low frequency noise, SSC, and so forth.)

### 3.5 CKslew and WCKslew Measurement Procedure (cont'd)

#### 3.5.1 Test Procedure (cont'd)

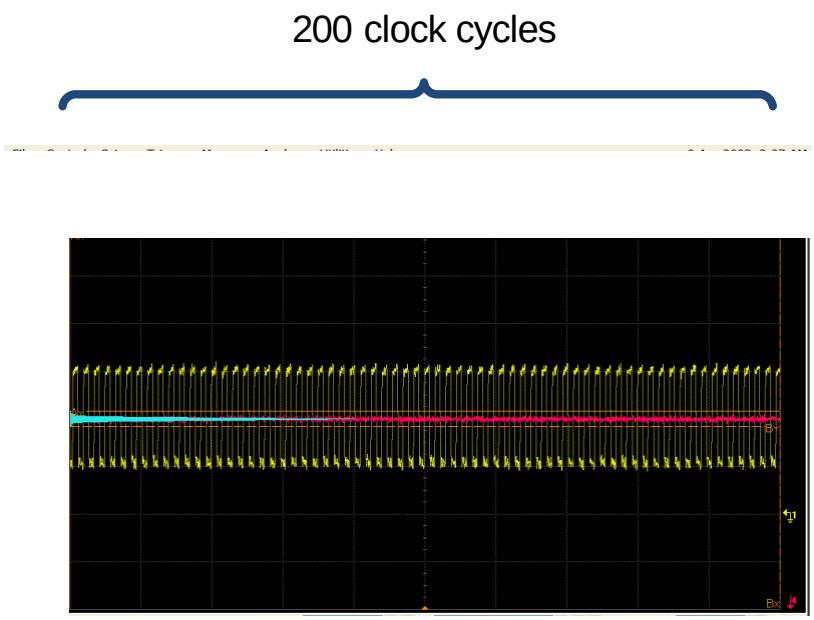


**Figure 19 — Set measurement across 200 cycles**

8. Using Vix(ac) specification, measure CKslew or WCKslew from VREF(avg) to Vix(ac). Vix(ac) is +/- 0.12V for CK and +/-0.10V for WCK. Vref(avg) to positive Vix(ac) for rising and Vref(avg) to negative Vix(ac) for falling. Continue across 200 cycles. Record worst case rising and falling measurements.

   NOTE 200 cycles is the recommended minimum number of cycles. It is up to the user to define the effective number of cycles based on low frequency noise, SSC, and so forth.

## 3.5 CKslew and WCKslew Measurement Procedure (cont'd)

### 3.5.1 Test Procedure (cont'd)

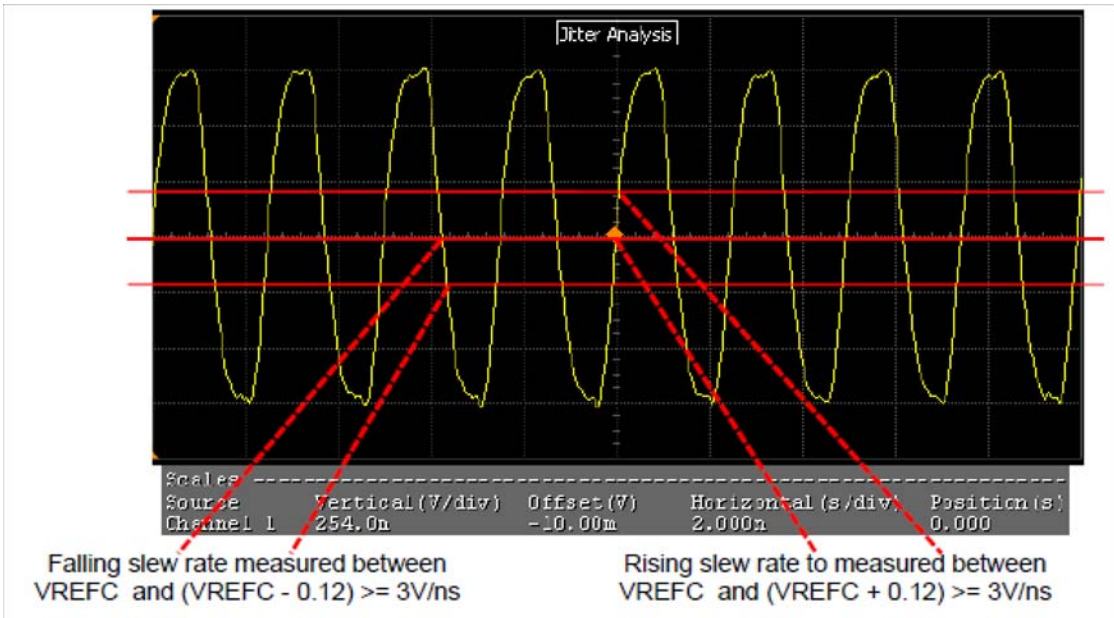


**Figure 20 — Measurement of slew from VREF to Vix(ac)**

9. Repeat step 3 - step 8 for compliment clock – CK_c and WCK_c.

10. Record values and conditions.

| Vdd/Vddq[1] | Temerature[2] | Probe point TL0/TL1[3] | Termination ODT enable, disable, or external[4] | Termination value[5] | ZQ | Measured Value | Number of Cycles[7] |
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for Vref(c/d)
**NOTE 4** **Termination – ODT enable, disable, or external** – Designate the type of termination used.
**NOTE 5** **Termination value –** termination resistance
**NOTE 6** **Measured value –** Value measured as per procedure.
**NOTE 7** **Number of cycles –** Number of cycles used in measurement.

# 4 Data Input Timings

## 4.1 Test Setup

1. Probe the DQ by connecting the probe ve+ to DQ and ve- to GND. Probe any other channels required to identify write bursts.

NOTE Specification defined “at the pin”; however this is difficult when implemented in a design and require probing at vias or probe points at some distance from the pin. An analysis needs to be done to determine best probe distance from the pin. It is recommended that probe points, termination and so forth be noted with the measurement results.

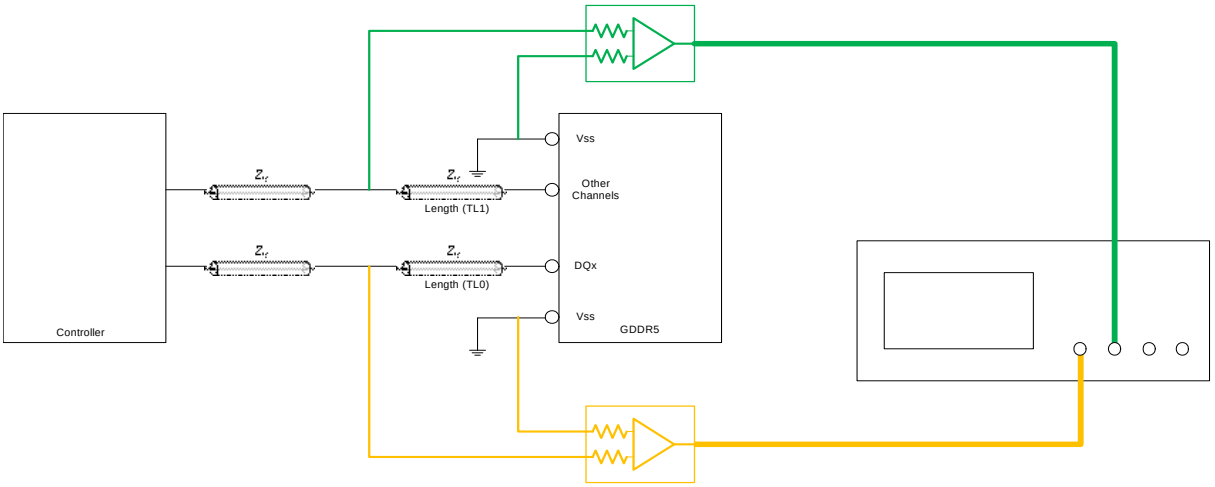


**Figure 21 — tDIVW Measurement Setup**

## 4.2 tDIVW Measurement Procedure

The data input valid window, tDIVW, defines the time region when input data must be valid for reliable data capture at the receiver for any one worst?case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (i.e. within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL/DLL mode and bandwidth. tDIVW is measured at the pins. tDIVW is defined for the PLL/DLL off and on mode separately. In the case of PLL on, tDIVW must be specified for each supported bandwidth. In general tDIVW is smaller than tDIPW.

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### 4.2.1 Test Procedure tDIVW

1. Perform scope and probe calibration as required by the equipment manufacturer.

2. Connect one channel to DQx and GND. Connect other channels as needed to identify write data from read data.

3. Power up device under ‘nominal’ condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the ‘nominal’ power up condition of the device.

## 4.2 tDIVW Measurement Procedure (cont'd)

### 4.2.1 Test Procedure tDIVW (cont'd)

4. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:

   a. Recall factory setup on the scope.

   b. Set sample rate.

   c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.

5. Determine tWCK2DQI and center align WCK with corresponding data bit. Note: exact eye center is not necessary. This will define the correct clock reference to measure DQ to WCK jitter.

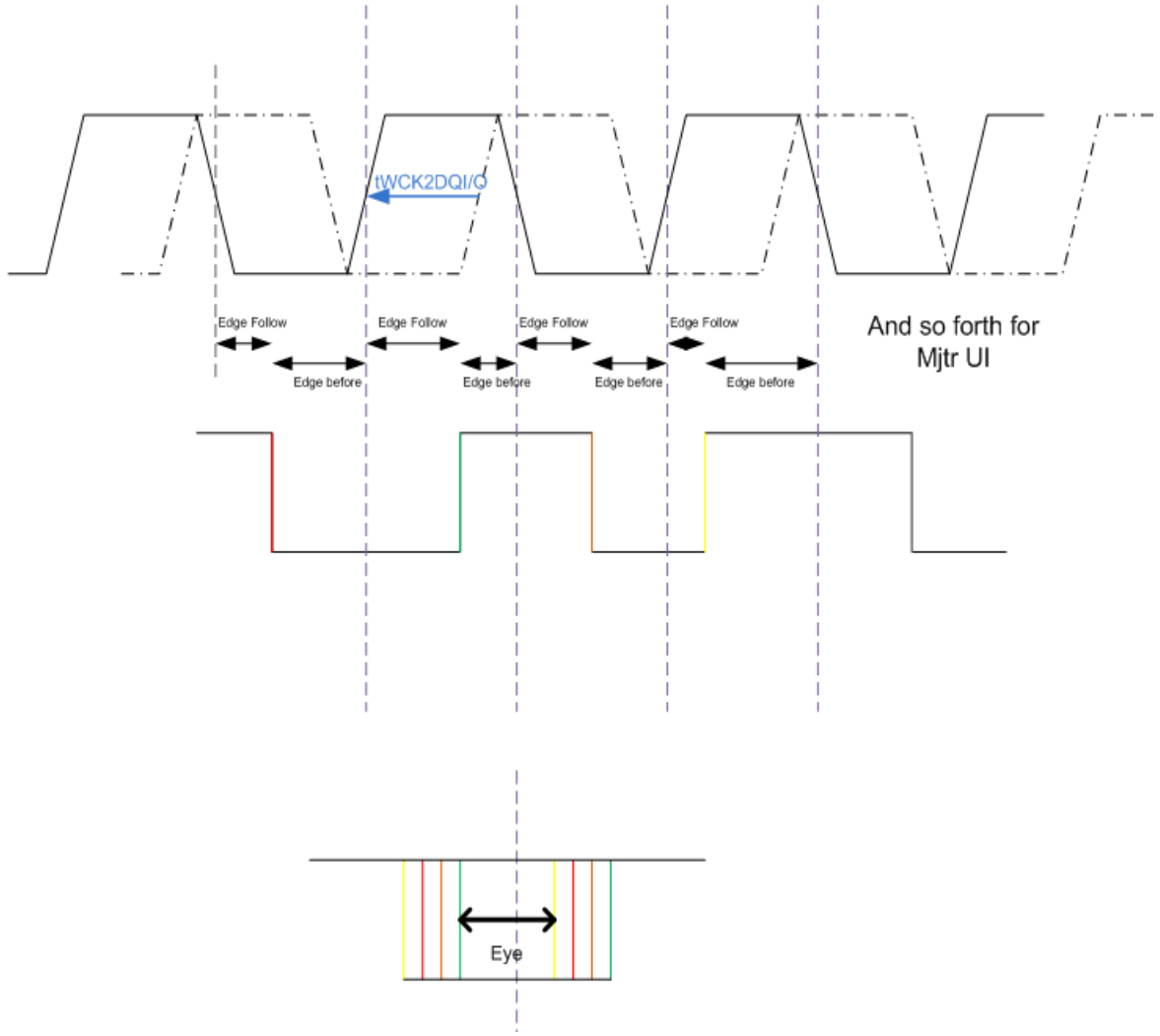


**Figure 22 — Determine tWCK2DQI and shift clock to align with correct data bit**

## 4.2 tDIVW Measurement Procedure (cont'd)

### 4.2.1 Test Procedure tDIVW (cont'd)

6. For Mjtr UI, at Vref measure Time Interval Error (TIE) for all data edges preceding WCK edge (TIE left). Measure TIE for all data edges following WCK transition (TIE right). Since the measurement is to characterize the data at the input of the part, this measurement is done the same way for both PLL on and PLL off cases. A PLL clock recovery algorithm can be used to debug and gain insight into the effects of jitter for the PLL on case, but not to compare against specification. [Note: While a specific data pattern is not required, it is recommended that the following data patterns exist within Mjtr measurements. Some variation from measurement to measurement is expected since a consistant data pattern is not in use. 00010001, 11101110, 10101010, 01010101, 00110011, 11001100]

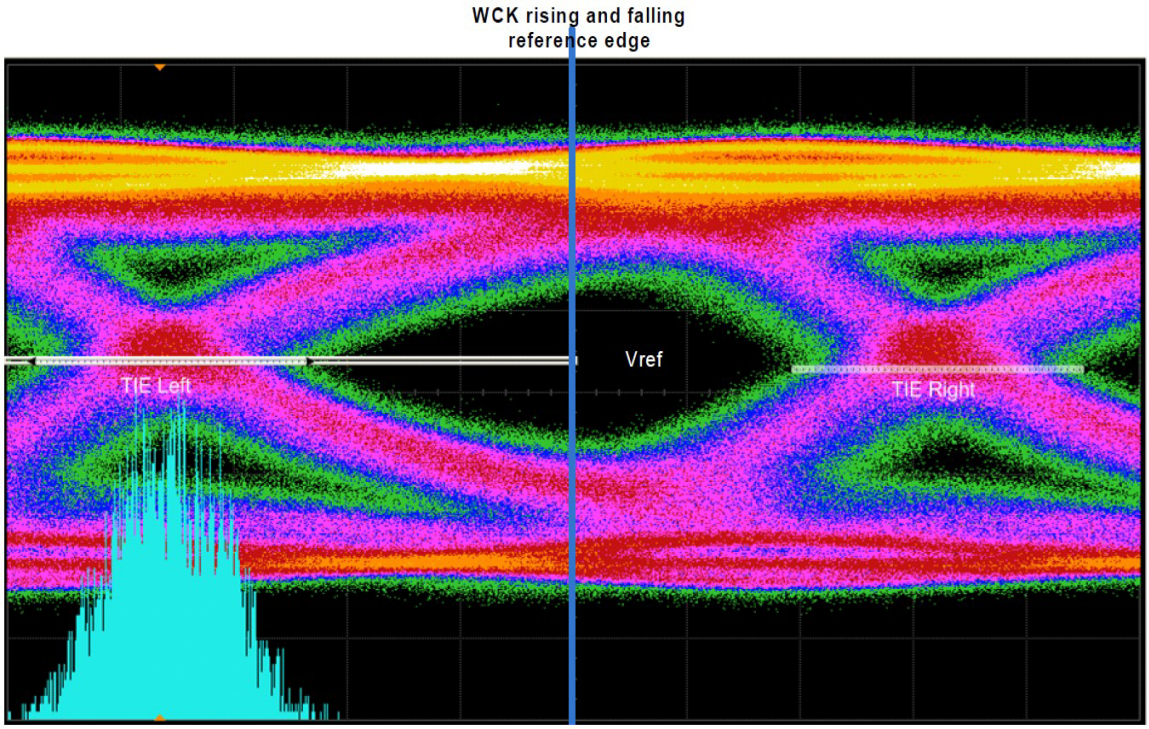


**Figure 23 — TIE Measurement**

7. Determine Tj for TIE left and TIE right, for the given Bit Error Rate (BER). An example measurement for figure 3 would be a TjLeft of 170.04ps and a TjRight of 171.4ps.

### 4.2 tDIVW Measurement Procedure (cont'd)

#### 4.2.1 Test Procedure tDIVW (cont'd)

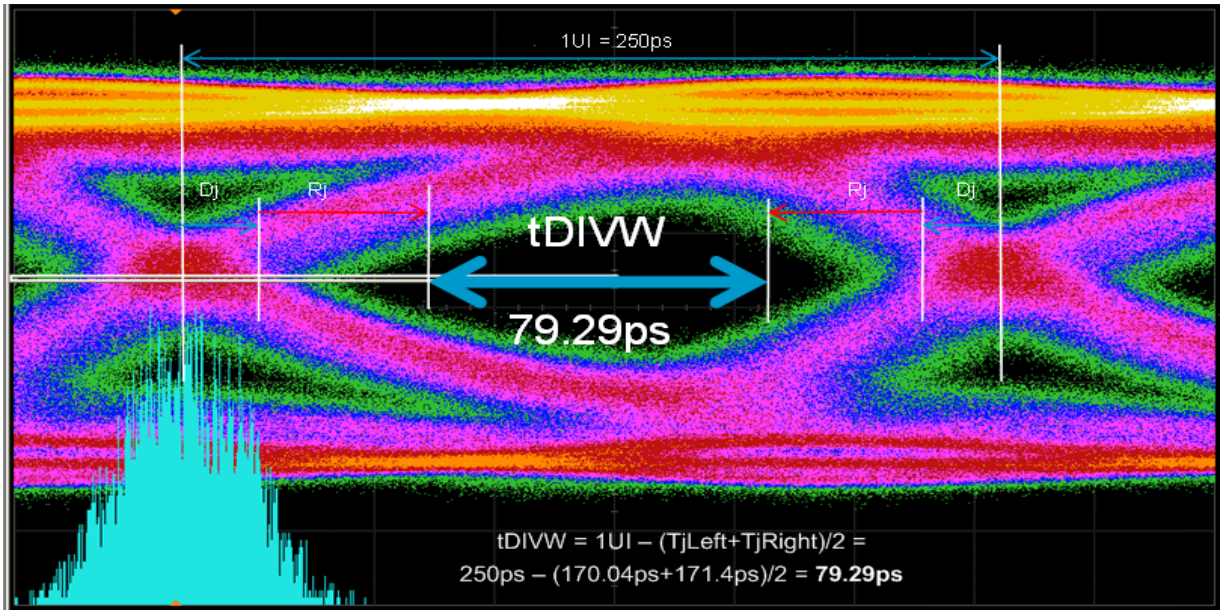


**Figure 24 — Example of tDIVW measurement calculation**

8. tDIVW is equal to 1UI-(TjLeft+TjRight)/2. Record value in table.

| Vdd/Vddq[1] | Temerature[2] | Probe point TL0/ TL1[3] | tDIVW[4] |
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for {W}CK_c.
**NOTE 4** **tDIVW –** Measured Data Input Valid Window.

### 4.3 tDIPW Measurement Procedure

The data input pulse width, tDIPW, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. tDIPW is measured at the pins. tDIPW is independent of the PLL/DLL mode. In general tDIPW is larger than tDIVW.

#### 4.3.1 Test Procedure tDIPW

1. Perform scope and probe calibration as required by the equipment manufacturer.
2. Connect one channel to DQx and GND. Connect other channels as needed to identify write data from read data.
3. Power up device under 'nominal' condition (room temperature, VDD(nom)). Before making the actual measurement, the scope is first conditioned (set sample rate, memory depth and vertical settings) for measurement using the clock signals provided by the 'nominal' power up condition of the device.
4. Using the signals provided by the device at 'nominal' condition, the scope is readied for measurement (e.g., required setup for voltage settings, time capture, etc). The following is an example of steps taken:
   a. Recall factory setup on the scope.
   b. Set sample rate.
   c. Adjust the vertical settings so the signals will fill the scope screen but avoid clipping. This maximizes the vertical resolution of the scope for measurement.
5. Measure each write data pulse from where the edge crosses Vref to the next edge to cross Vref. Recommend to measure at least 1000 edges to garuntee a good statistical population of pulses and data patterns.

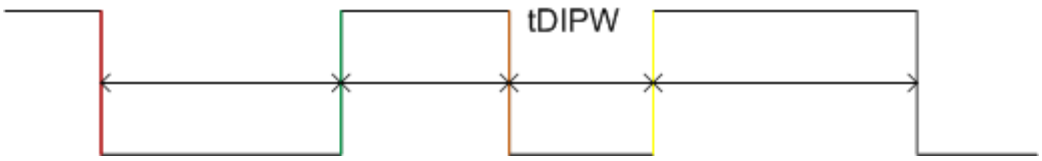


**Figure 25 — Measure DQx at Vref**

## 4.3 tDIPW Measurement Procedure (cont'd)

### 4.3.1 Test Procedure tDIPW (cont'd)

6. Record values in table.

| Vdd/Vddq[1] | Temerature[2] | Probe point TL0/ TL1[3] | tDIPW[4] |
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**NOTE 1** **Vdd/Vddq** – Supply voltage used in measurement.
**NOTE 2** **Temperature** – Ambient, or set temperature used in measurement.
**NOTE 3** **Probe point TL0/TL1** – TL0 Trace length/location and characteristics of trace for {W}CK, TL1 Trace length/ location and characteristics of trace for {W}CK_c.
**NOTE 4** **tDIVW –** Measured Data Input Pulse Width.

## Standard Improvement Form JEDEC _____

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

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3. Other suggestions for document improvement:

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Submitted by

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Company: _____ E-mail: _____

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City/State/Zip: _____ Date: _____


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