JEDEC STANDARD

Definition of Skew Specifications for Standard Logic Devices

JESD65B

(Revision of JESD65-A)

SEPTEMBER 2003

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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DEFINITIONS OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES

(From JEDEC Board Ballots JCB-02-67, JCB-02-112, JCB-02-113, and JCB-02-114, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines skew specifications and skew testing for standard logic devices.

The purpose is to provide a standard for specifications to achieve uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

2 Terms and definitions

These definitions are provided for the purpose of this document. For general definitions of skew time, see the latest revision of JEDEC Standard No. 99 *Terms, Definitions, and Letter Symbols for Microelectronic Devices*.

2.1 Device terms and definitions

PLL device: A logic device that includes a phase-locked loop and may also include other logic functions, such as counters, registers, and buffers.

2.2 Parameter terms and definitions

skew (time): The magnitude of the time difference between two events that ideally would occur simultaneously.

controlled edge: The output signal edge that is locked to the PLL trigger reference.

jitter: The time deviation of a PLL-generated controlled edge from its nominal position.

threshold crossing: The point at which a logic signal transitions from one logic state to another.

primary threshold crossing: The threshold crossing of a clock signal indicating the start of a new cycle and the end of the previous cycle.

secondary threshold crossing: The threshold crossing of a clock signal indicating the second part of the clock cycle.

3 Standard specifications

All skew parameters are specified over the guaranteed temperature and supply operating ranges. If more than one temperature or supply operating range is used, the range(s) for the skew specification(s) must be identified. PLL logic devices must be supplied with a stable input reference clock within the operating frequency range of the component.

Table 1 — Symbols for skew and other specifications

Symbol	Parameter	Units	Notes
$t_{sk(o)}$	output skew	ps, ns	1
$t_{sk(LH)}$	output skew for low-to-high transitions	ps, ns	
$t_{sk(HL)}$	output skew for high-to-low transitions	ps, ns	
$t_{sk(pr)}$	process skew	ps, ns	
$t_{sk(pp)}$	part-to-part skew	ps, ns	
$t_{sk(b)}$	bank skew	ps, ns	1
$t_{sk(p)}$	pulse skew	ps, ns	
$t_{sk(inv)}$	inverting skew	ps, ns	1, 4
$t_{sk(\omega)}$	multiple-frequency skew	ps, ns	
$t_{(\phi)}$	static phase offset	ps, ns	
$t_{(\phi)dyn}$	dynamic phase offset	ps, ns	
$t_{(\phi)tot}$	total phase offset	ps, ns	
$t_{jit(cc)}$	cycle-to-cycle period jitter	ps, ns	2, 5
$t_{jit(per)}$	period jitter	ps, ns	2, 5
$t_{jit(hper)}$	half-period jitter	ps, ns	
$t_{jit(duty)}$	duty cycle jitter	ps, ns	
$t_{jit(\phi)}$	phase jitter	ps, ns	1, 3, 5
lock (f)	frequency locked		
lock (ϕ)	phase locked		
t_L	power-up PLL lock time	ns, ms	
$t_{L(\omega)}$	PLL lock time after frequency change	ns, ms	
$t_{recL(\phi)}$	PLL recovery after phase change	ns, ms	
n_L	cycles to acquire PLL lock	cycles	
ODC	PLL output duty cycle	%	

NOTE 1 This parameter is not production tested.

NOTE 2 The sample size shall be greater than or equal to 1000.

NOTE 3 The sample size shall be greater than or equal to 2000.

NOTE 4 The test load for this parameter may be a nonstandard load identified in the data sheet.

Table 2 — Example of suggested jitter specifications

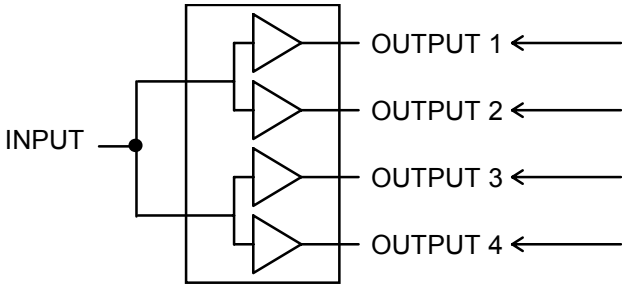
Symbol	Parameter	Sample size	Typ	Max	Unit	Notes
$t_{jit(cc)}$	cycle-to-cycle period jitter	1,000 cycles	x	x	ps	5, 6
$t_{jit(per)}$	period jitter	10,000 cycles	x	x	ps	5, 6
$t_{jit(\phi)}$	phase jitter	2,000 cycles	x	x	ps	5, 6

NOTE 5 Test Loads and Conditions are shown in Clause 4 “Standard test circuits for skew testing” for the designated voltage range.

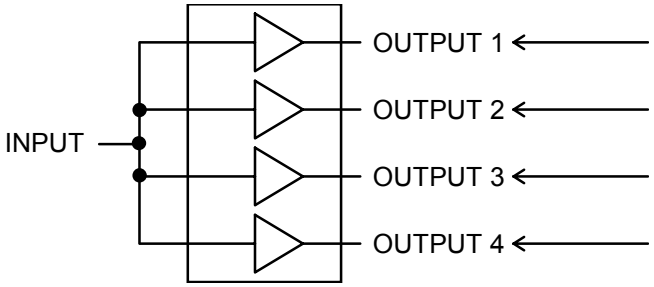
NOTE 6 Operating frequency range is 10 MHz to 100 MHz.

3 Standard specifications (cont'd)

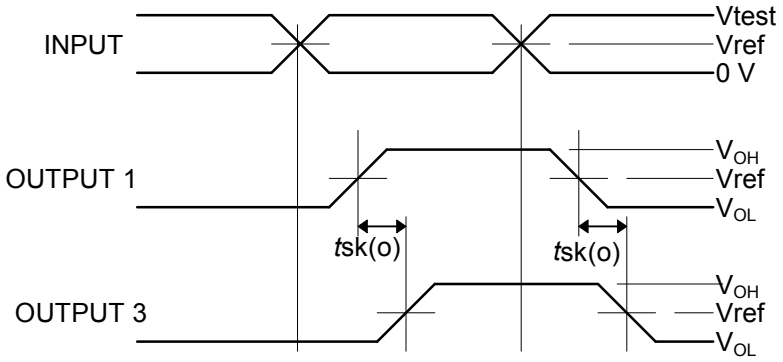
output skew ($t_{sk(o)}$): The skew between specified outputs of a single logic device with all driving inputs switching simultaneously and the outputs driving identical specified loads.



An example of a multiple bank logic device



An example of a logic device without banks

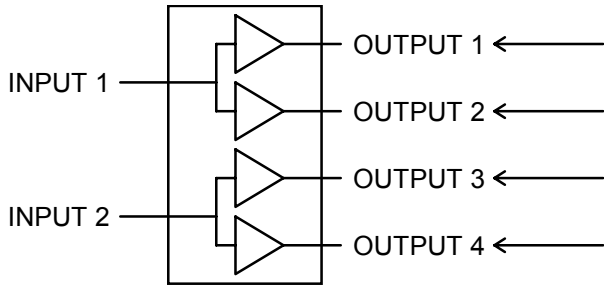


An example of output waveforms

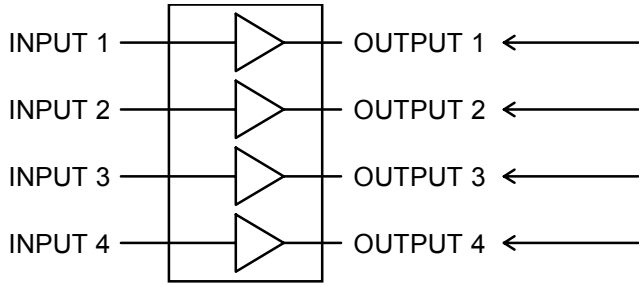
3 Standard specifications (cont'd)

output skew ($t_{sk(LH)}$, $t_{sk(HL)}$): The skew between specified outputs of a single logic device when the outputs have identical specified loads and are switching in the same direction.

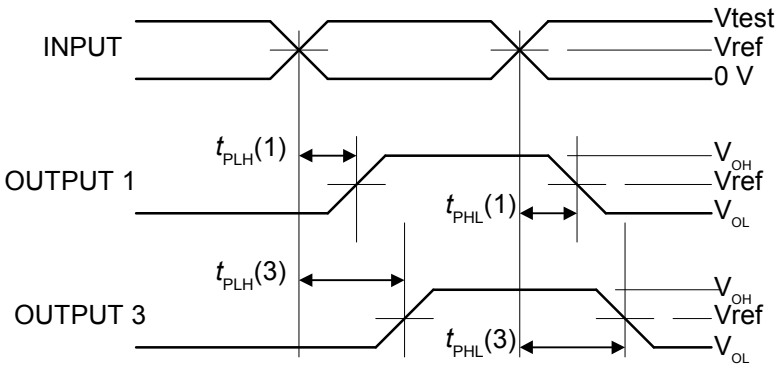
NOTE Each input-to-output delay time is tested individually, and the difference is the skew.



An example of a multiple bank logic device



An example of a logic device without banks



$$tsk(LH) = \left| t_{PLH}(1) - t_{PLH}(3) \right|$$

$$tsk(HL) = \left| t_{PHL}(1) - t_{PHL}(3) \right|$$

An example of output waveforms

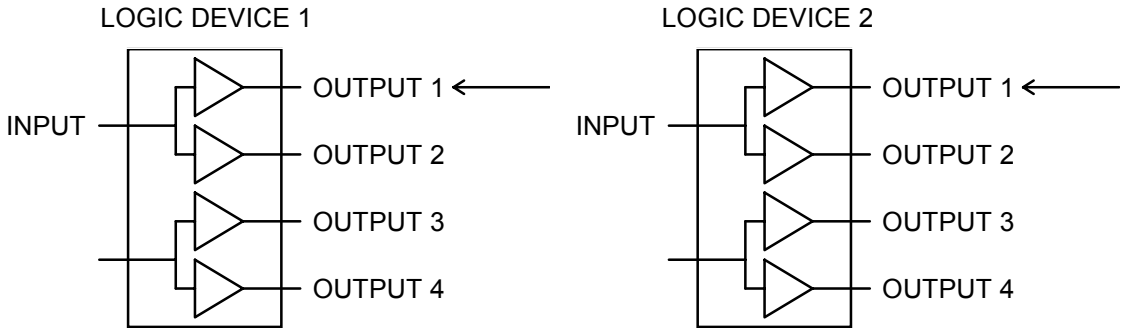
3 Standard specifications (cont'd)

process skew ($t_{sk(pr)}$): The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages, operate at the same temperature, and have identical package styles, identical specified loads, identical internal logic functions, and the same manufacturer.

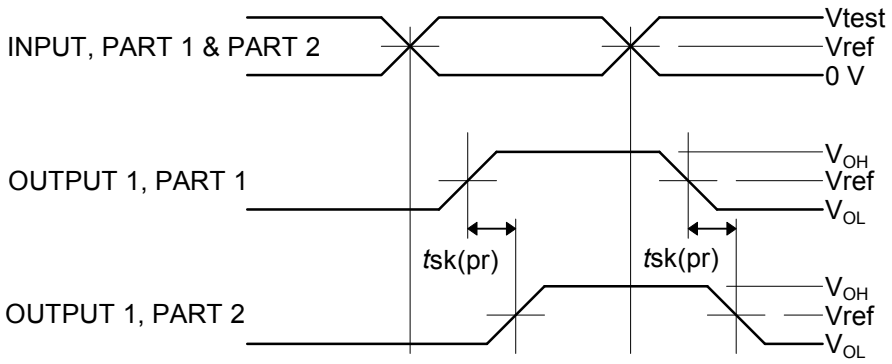
NOTE To calculate any other skew parameter between two logic devices, the process skew should be added to the selected skew parameter for a single logic device.

EXAMPLE 1 Output skew between two logic devices = $t_{sk(pr)} + t_{sk(o)}$.

EXAMPLE 2 Inverting skew between two logic devices = $t_{sk(pr)} + t_{sk(inv)}$.



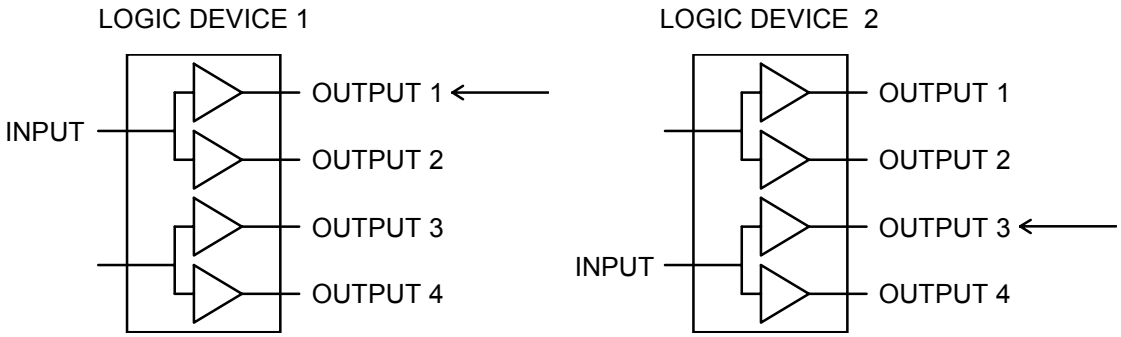
An example of two logic devices



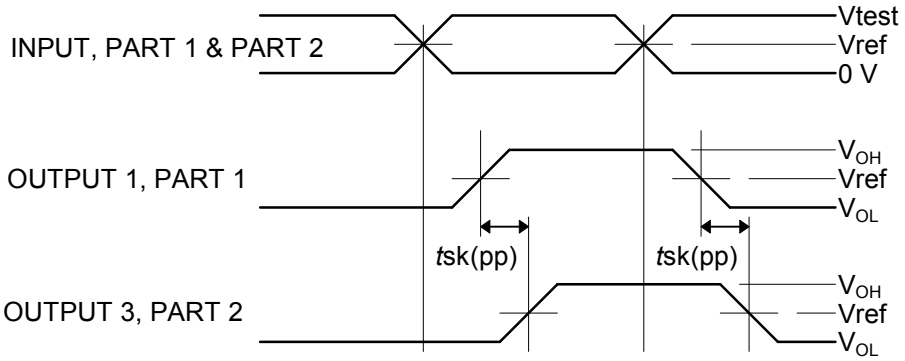
An example of output waveforms

3 Standard specifications (cont'd)

part-to-part skew ($t_{sk(pp)}$): The magnitude of the difference in propagation delay times between any specified terminals of two logic devices when both logic devices operate with the same supply voltages, operate at the same temperature, and have identical package styles, identical specified loads, and identical internal logic functions.



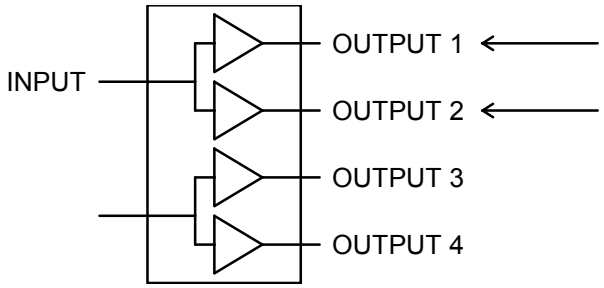
An example of two parts



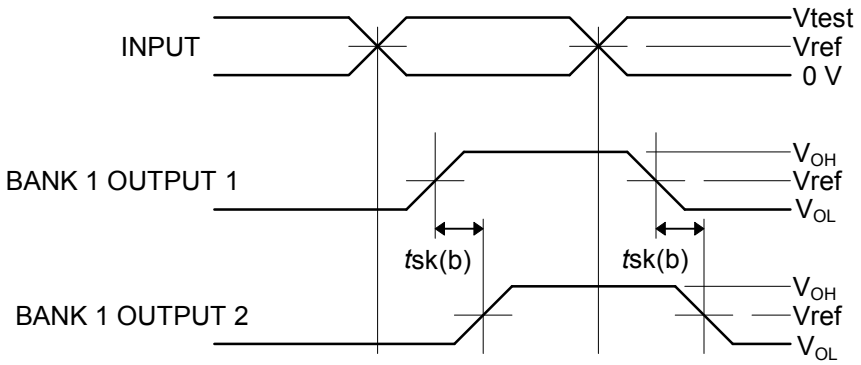
An example of output waveforms

3 Standard specifications (cont'd)

bank skew ($t_{sk(b)}$): The output skew between outputs with a single driving input terminal.



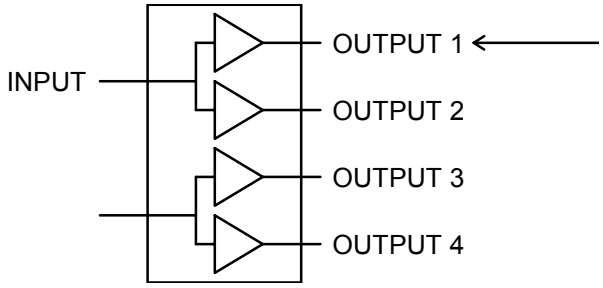
An example of a logic device with banks



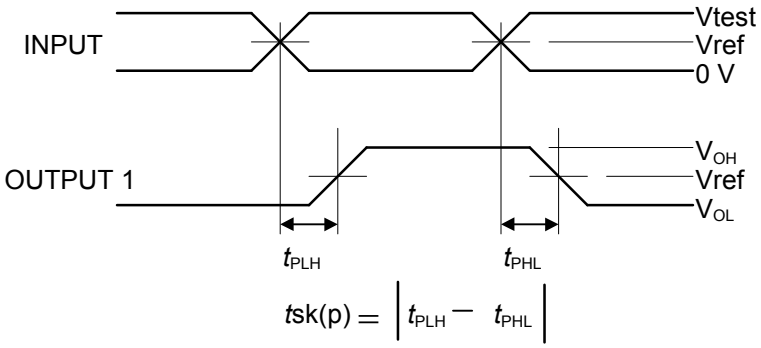
An example of output waveforms

3 Standard specifications (cont'd)

pulse skew ($t_{sk(p)}$): The magnitude of the time difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch.



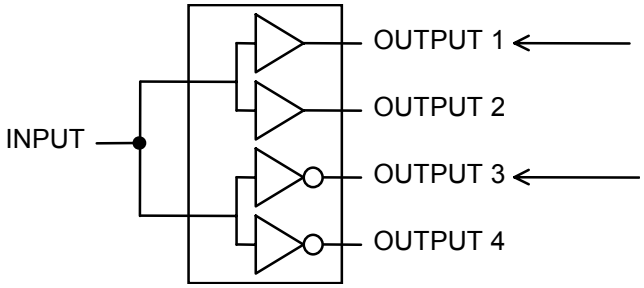
An example of a logic device



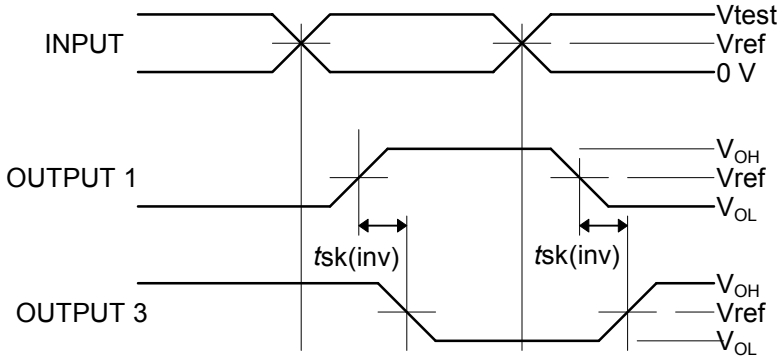
An example of an output waveform and $t_{sk(p)}$ measurement

3 Standard specifications (cont'd)

inverting skew ($t_{sk(inv)}$): The skew between specified outputs of a single logic device with all driving inputs connected together and the outputs switching in opposite directions while driving identical specified loads.



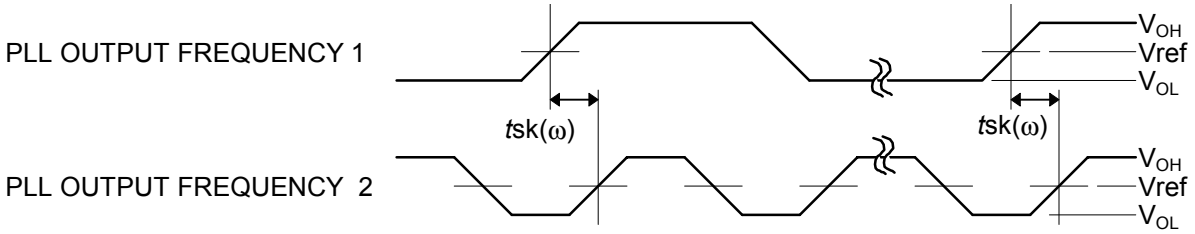
An example of a package with both inverting and non-inverting outputs



An example of output waveforms

multiple-frequency skew ($t_{sk(\omega)}$): The skew between the controlled-edge position of two different output frequencies on a PLL or counting device that has more than one output frequency, when both signals are rising or both signals are falling.

NOTE If the multiple frequency skew specification includes combined rising and falling edges, this may be identified in a footnote.



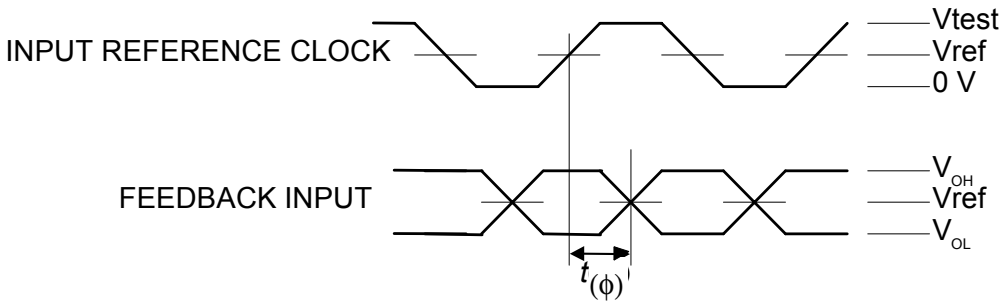
An example of an output waveform

3 Standard specifications (cont'd)

static phase offset ($t_{(\phi)}$): The time interval between similar points on the waveforms of the averaged input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 1 PLL jitter may cause excursions of $t_{(\phi)}$ beyond the specified maximum.

NOTE 2 The term "PLL reference zero delay" has been used for this concept but its use is deprecated.

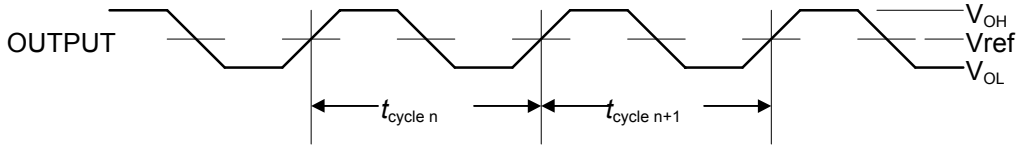


An example of input waveforms

dynamic phase offset ($t_{(\phi)dyn}$): The incremental phase offset between the input reference clock and the feedback input signal of a PLL resulting from modulation of the input reference clock.

total phase offset ($t_{(\phi)TOT}$): The sum of static phase offset, dynamic phase offset, and phase jitter.

cycle-to-cycle period jitter ($t_{jit(cc)}$): The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.



$t_{jit(cc)} = | t_{cycle\ n} - t_{cycle\ n+1} |$ where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges.

$t_{jit(cc+)} = t_{cycle\ n+1} - t_{cycle\ n}$ where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges, and the period of $t_{cycle\ n+1}$ is longer than or equal to the period of $t_{cycle\ n}$.

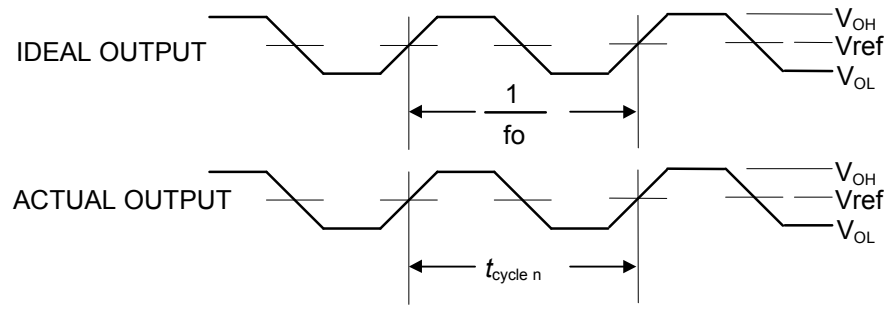
$t_{jit(cc-)} = t_{cycle\ n} - t_{cycle\ n+1}$ where $t_{cycle\ n}$ and $t_{cycle\ n+1}$ are any two adjacent cycles measured on controlled edges, and the period of $t_{cycle\ n}$ is longer than or equal to the period of $t_{cycle\ n+1}$.

Examples of an output waveform and cycle-to-cycle period jitter measurements

NOTE In all these examples, the minimum value would be tcycle n = tcycle n+1, which is zero. Negative values are not possible.

3 Standard specifications (cont'd)

period jitter ($t_{jit(per)}$): The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles.

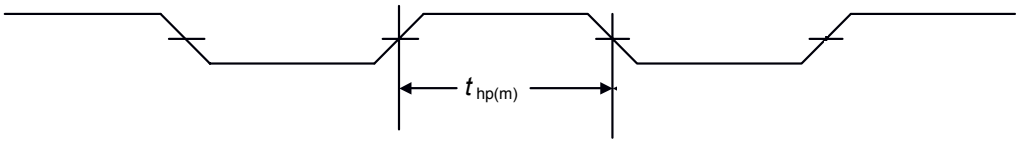


$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{fo}$$

where fo is the nominal output frequency and $t_{cycle\ n}$ is any cycle within the sample measured on controlled edges

An example of an output waveform and jitter measurement

half-period jitter ($t_{jit(hper)}$): The magnitude of the deviation in time duration between half cycle threshold crossings of a single over a random sample of half cycles.



$$t_{jit(hper)} = t_{hp(m)} - \frac{1}{2 \cdot f_o}$$

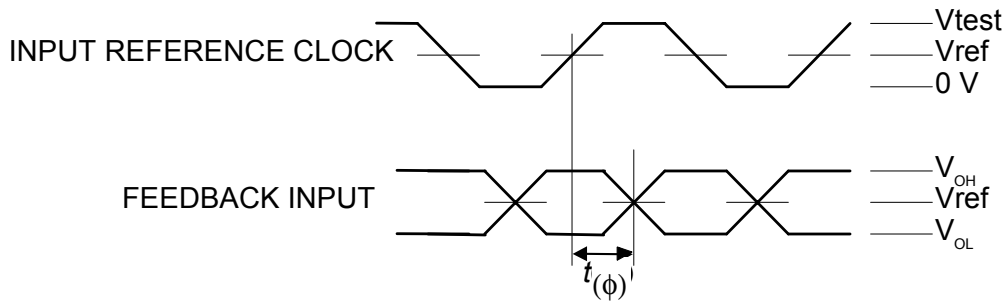
where $t_{hp(m)}$ is the duration of any half cycle within the sample

An example of half-period jitter

duty cycle jitter ($t_{jit(duty)}$): The magnitude of the deviation in time duration between the primary threshold crossing and the secondary threshold crossing in a cycle over a random sample of cycles.

3 Standard specifications (cont'd)

phase jitter ($t_{jit(\phi)}$): The deviation in static phase offset $t_{(\phi)}$ for a controlled edge with respect to the mean value of $t_{(\phi)}$ in a random sample of cycles.



$t_{jit(\phi)} = t_{(\phi)} - t_{(\phi)mean}$ Where $t_{(\phi)}$ is any random sample and $t_{(\phi)mean}$ is the average of the sampled cycles measured on controlled edges.

An example of an output waveform and jitter measurement

frequency locked [lock (f)]: The condition of a PLL device where the frequency of the feedback input is equal to the averaged reference input frequency within a designated tolerance.

NOTE This definition is useful in defining lock under conditions where the reference input is undergoing jitter or is skipping cycles.

phase locked [lock (ϕ)]: The condition of a PLL device where the reference input and the feedback input remain within the designated static phase offset.

NOTE This definition requires the reference input to remain stable within a designated tolerance.

power-up PLL lock time (t_L): During PLL power up, the time required for the PLL to lock after achieving the minimum specified operating voltage.

PLL lock time after frequency change ($t_{L(\omega)}$): The time required for a PLL to lock after the input reference clock frequency changes.

NOTE The PLL lock time after frequency change is measured from the time the new input reference clock frequency is stable, to the time the PLL locks.

PLL recovery time ($t_{recL(\phi)}$): The time interval required for a PLL to recover phase lock after the input reference clock changes phase.

cycles to acquire PLL lock (n_L): The number of input clock cycles required for a PLL to lock when operating in the guaranteed operating range with a stable input reference clock frequency.

PLL output duty cycle (ODC): The ratio of (1) the time interval from the PLL-controlled edge to the noncontrolled edge to (2) the time interval between PLL-controlled edges, expressed as a percentage (%).

4 Standard circuits for skew testing

4.1 Except for PLL components, the skew testing frequency shall be 1 MHz or as specified by the manufacturer in the component data sheet.

4.2 The skew testing frequency for PLL components shall be within the recommended operating range of the PLL component and specified by the manufacturer in the component data sheet.

4.3 The test load shall be the industry standard test load for the particular logic family being tested or as specified by the manufacturer in the component data sheet.

4.4 For standardization of testing, a suggested additional test load of 15 pF and 500 Ω may also be used.

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Standard Improvement Form

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1. I recommend changes to the following:

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

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