JEDEC STANDARD

Standard for Description of 3.3 V NFET Bus Switch Devices with Integrated Charge Pumps

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STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS

(From Board Ballot JCB-00-99, formulated under the cognizance of the JC-40 Committee on Digal Logic.)

1 Scope

This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices with integrated charge pumps. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description.

The purpose of this standard is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

2 Definitions for the purpose of this document

switch device: A semiconductor logic device designed to connect or disconnect busses or control signals without active drivers in the connection path.

connect: A state in a switch device characterized by a minimum series impedance through the designated electrical path.

disconnect: A state in a switch device characterized by the high series impedance of the designated electrical path.

3 Standard specifications

3.1 Absolute maximum continuous ratings [1,2]

Symbol	Parameter	Rating	Units
V_{DD}	Supply voltage	-0.5 to 4.6	V
V_I	dc input voltage, control terminals(3)	-0.5 to 5.5	V
V_{SW}	dc switch voltage(3)	-0.5 to 5.5	V
I_{IK}	dc input clamp	-50	mA
I_{OK}	dc clamp current, switch terminals	-50	mA
I_{SW}	dc continuous channel current	120	mA
T_{STG}	Storage temperature	-65 to 150	°C

NOTE 1 Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

NOTE 2 Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

NOTE 3 The dc negative voltage ratings may be exceeded if the dc input clamp current ratings are observed.

3.2 Recommended operating conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
V_{IN}	Control input voltage	0	5.5	V
V_{SW}	Switch terminal voltage	0	5.5	V
T_A	Operating free-air temperature	-40	85	°C

3.3 Capacitance(1)

Symbol	Parameter	Condition	Typ.	Unit
C_{IN}	Control input capacitance			pF
C_{SW}	Switch terminal capacitance	Switch disconnected		pF

NOTE 1 Capacitance is characterized but not tested

3 Standard specifications (cont'd)

3.4 Power supply characteristics

Symbol	Description	Test Conditions	Max	Unit
I_{DD}	Quiescent power supply current	V_{DD} = 3.6 V V_{SW} = GND or V_{DD}		mA
ΔI_{DD}	Quiescent power supply current TTL control inputs high(1)	V_{DD} = 3.6 V V_{IN} = 2.0 V V_{SW} = GND		µA
Q_D	Dynamic power supply current(2)	V_{SW} = GND Control pin toggling at 10 MHz and 50% duty cycle		µA/ MHz

NOTE 1 Per TTL driven control input

NOTE 2 All switch inputs grounded. One control pin toggling. All other control pins at V_{DD} or GND.

3.5 Switching characteristics over operating range

Symbol	Description	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Data path propagation delay(1,2)	—			ns
t_{PZH} t_{PZL}	Switch connect delay(1)	—			ns
t_{PHZ} t_{PLZ}	Switch disconnect delay(1)	—			ns
f_{CNTL}	Control frequency(3)	—			MHz

NOTE 1 Path must be specified.

NOTE 2 This parameter is not tested.

NOTE 3 The maximum frequency at which the enable/select input can be continuously toggled without discharging the integrated charge pump. The channel frequency has no influence on the charge pump.

3 Standard specifications (cont'd)

3.6 DC specifications

Symbol	Parameter	Test Conditions		Min	Max	Unit
V_{IH}	High-level input voltage			2.0	—	V
V_{IL}	Low-level input voltage			—	0.8	V
V_{PASS}	Pass voltage (V_O)	V_{SW} = 5.0 V V_{DD} =3.3 V Iout = -30 mA		4.5		V
R_{ON}	Switch connect resistance[2,3]	V_{SW} = 0 V	I_{SW} = (1)	—		Ω
		V_{SW} =2.4 V	I_{SW} = (1)	—		Ω
I_{OS}	Short circuit current[2,4]	V_{SW} = V_{DD} V_{OUT} = GND			—	mA
I_{DD}	Quiescent power supply current	V_{DD} = Max., V_{IN} = V_{DD} or GND		—		µA
V_{IK}	Clamp diode voltage	Switch Terminals I_{SW} = -18 mA		—		V
		Control Terminals, I_{IN} = -18 mA		—		V
I_{OZ}	Current during switch disconnect[6]	V_{DD} = Max. V_{SW} = GND to 5.5 V V_{OUT} = GND		—		µA
I_{IL} I_{IH}	Control input current	V_{DD} = Max.	V_I = GND V_I = V_{DD}	—		µA
I_{OFF}	Switch terminal leakage[5]	V_{DD} = 0 V V_{SW} = 5.5 V		—		µA

NOTE 1 See the manufacturer's data sheet.

NOTE 2 The connect path must be specified.

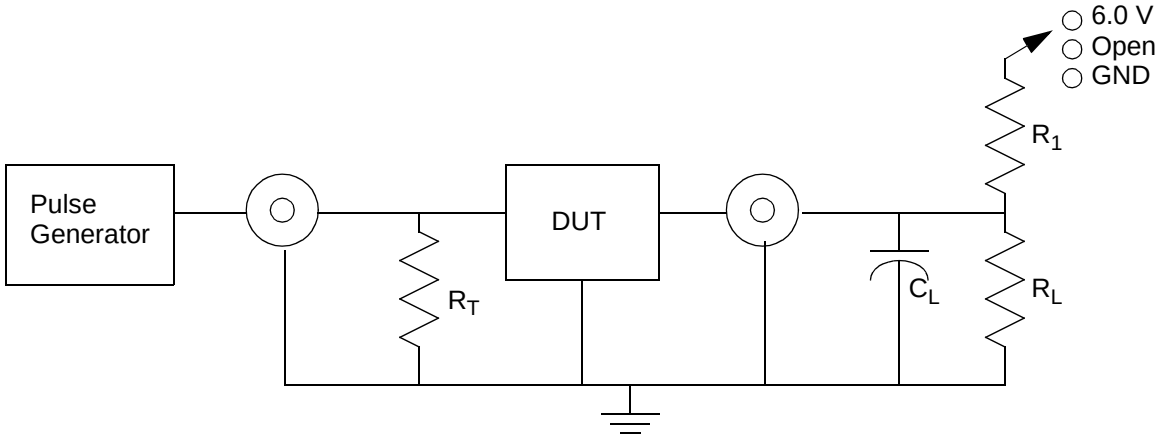
NOTE 3 Resistance is measured as $\Delta V/\Delta I$. For V_{SW} = 0 V, the resistance is measured while V_{OUT} is pulled higher to the designated current level. For V_{SW} = 2.4 V, the resistance is measured while V_{OUT} is pulled lower to the designated current level.

NOTE 4 Not more than one output should be tested at a time. Duration of the test must not exceed one second. This is an optional parameter.

NOTE 5 This is an optional parameter.

NOTE 6 I_{OZ} is guaranteed with V_{SW} between GND and 5.5V, but is tested at V_{SW} = V_{DD}.

4 Test circuits and switching waveforms



C_L = 50 pF or equivalent (includes test setup and probe capacitance).

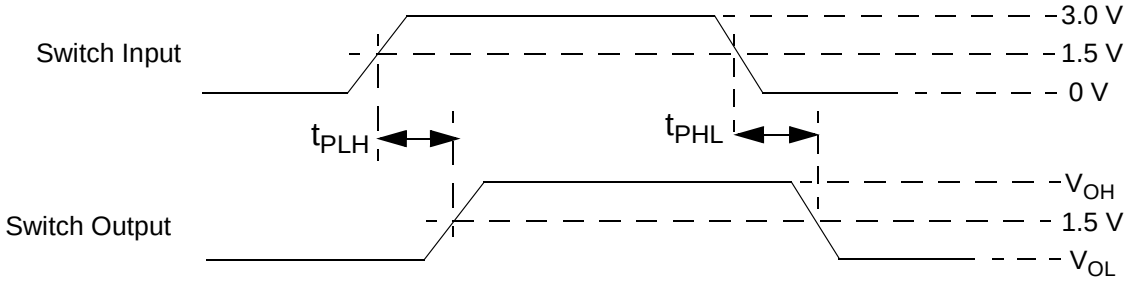
$R_L = R_1$ = 500 Ω or equivalent

R_T = Pulse generator termination resistance

Pulse generator has the following characteristics: $t_r \leq 2.5$ ns, $t_f = \leq 2.5$ ns, PRR ≤ 10 MHz

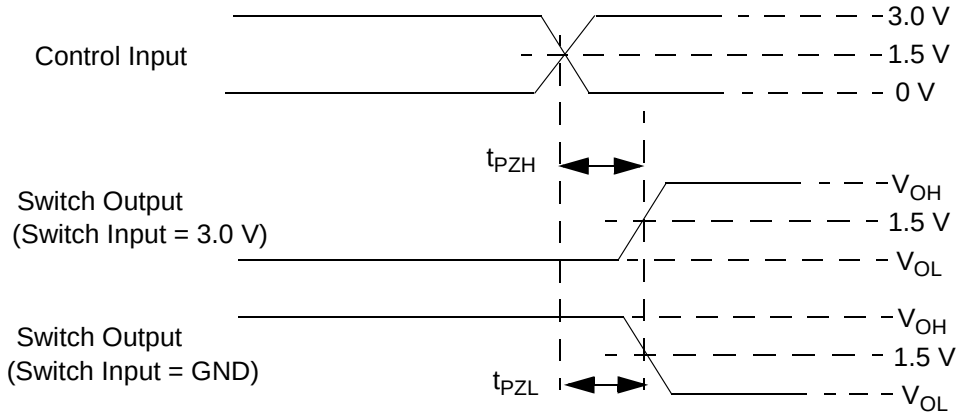
Test	Switch S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	6.0 V
t_{PHZ}	Open
t_{PLZ}	6.0 V

4.1 Propagation delay measurement

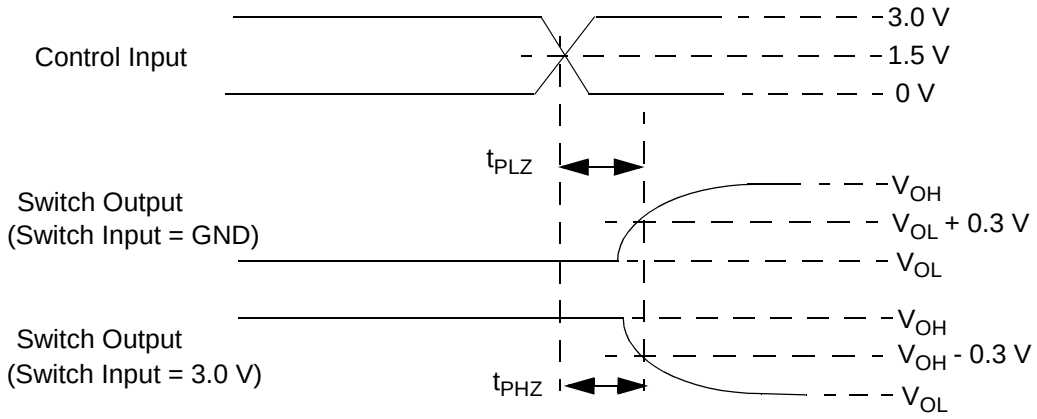


4 Test circuits and switching waveforms (cont'd)

4.2 Connect delay measurement



4.2 Disconnect delay measurement



NOTE Reference to Other Applicable JEDEC Standards and Publications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