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Addendum No. 3 to JESD79-3: 3D Stacked SDRAM

JESD79-3-3

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(From JEDEC BoD ballot JCB-12-12, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1 Scope

This addendum to JESD79-3 defines the 3DS DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for compliant 8Gbit through 64Gbit x4 and x8 3DS DDR3 SDRAM devices. This document was created based on the E revision of the DDR standard (JESD79). Each aspect of the changes for 3DS DDR3 SDRAM operation was considered.

The requirement for 3DS devices compliant to this spec addendum is to have a single electrical load for the stacked devices no matter if the stack is comprised of 2, 4 or 8 devices. The I/O buffer circuitry can be built into the base SDRAM of the stack or into a separate logic buffer device. In either case (built in native DRAM circuitry or separate logic die), the assumption is that the I/O buffers are located at the bottom of the stack closest to the package substrate. All pictures and diagrams in the spec depict a master die at the bottom of the stack.

1.1 Definition of Terms

3DS: 3D Stacked SDRAM devices with a single electrical load. In the remainder of this document both the long form as well as the abbreviation are used interchangeably.

Logical Rank: 3DS devices are divided into 2, 4 or 8 logical ranks. Devices with 2 or 4 logical ranks use 2 or 4 chip select pins to select the logical ranks. Devices with 8 logical ranks use 4 chip select pins and a single ID pin to select the logical ranks. There is not necessarily a 1-to-1 relationship between a physical die and a logical rank.

Package Rank: A package rank on a 3D stacked module consists of all 3DS packages that together span the whole data width of the module. For example with a 72-bit ECC module using x4 3DS devices, a package rank consists of 18 packages.

Master Logical Rank: The master logical rank in the 3DS device is the device in the stack that buffers external signals between the controller and the SDRAM stack. Other logical ranks in the stack only communicate to the master logical rank and are not visible as loads on the DDR bus to the controller. By convention, the master logical rank is controlled by CS0_n.

2 3DS SDRAM Package Pinout and Addressing

2.1 Overview

These ballouts have been derived from JEDEC DDR3 Standard JESD79-3. The ballout comprehends x4 and x8 data widths, where x4 is a subset of the x8 ballout. Address mirroring option for existing A[15:0] is preserved without change, e.g. as allowed by DDR3 UDIMM and LRDIMM specifications.

2.2 3D Stacked / DDR3 SDRAM x4 Ballout using MO-207

Ball locations highlighted in red in Figure 1, "3D Stacked DDR3 SDRAM x4 Ballout" indicate deviations from JESD 79-3 Quad-stacked/Quad-die SDRAM x4 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				NU	VSS	VDD	NC
G		VSS	VSSQ	DQ0				DM	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	NC	DQS_n				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ	
L		NC	VSS	RAS_n				CK_t	VSS	CID, NC[1]	
M		ODT	VDD	CAS_n				CK_c	VDD	CKE	
N		CS1_n	CS0_n	WE_n				A10/AP	ZQ	NC	
P		VSS	BA0	BA2				A15, NC[2]	VREFCA	VSS	
R		CS2_n, NC[3]	A3	A0				A12/Bacon	BA1	VDD	
T		CS3_n, NC[3]	A5	A2				A1	A4	VSS	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET_n	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC

1. Not used for 3DS devices with two or four logical ranks
2. Not used for 3DS devices with 2Gb logical rank densities
3. Not used for 3DS devices with two logical ranks

Figure 1 — 3D Stacked DDR3 SDRAM x4 Ballout

2.3 3D Stacked / DDR3 SDRAM x8 Ballout using MO-207

Ball locations highlighted in red in Figure 2, "3D Stacked DDR3 SDRAM x8 Ballout" indicate deviations from JESD 79-3 Quad-stacked/Quad-die SDRAM x8 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC		NC				NC		NC	NC
B											
C	NC	NC		NC				NC		NC	NC
D											
E											
F	NC	VSS	VDD	NC				TDQS_n	VSS	VDD	NC
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	
J		VSSQ	DQ6	DQS_n				VDD	VSS	VSSQ	
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	
L		NC	VSS	RAS_n				CK_t	VSS	CID, NC[1]	
M		ODT	VDD	CAS_n				CK_c	VDD	CKE	
N		CS1_n	CS0_n	WE_n				A10/AP	ZQ	NC	
P		VSS	BA0	BA2				A15, NC[2]	VREFCA	VSS	
R		CS2_n, NC[3]	A3	A0				A12/BC_n	BA1	VDD	
T		CS3_n, NC[3]	A5	A2				A1	A4	VSS	
U		VDD	A7	A9				A11	A6	VDD	
V	NC	VSS	RESET_n	A13				A14	A8	VSS	NC
W											
Y											
AA	NC	NC		NC				NC		NC	NC
AB											
AC	NC	NC		NC				NC		NC	NC

1. Not used for 3DS devices with two or four logical ranks
2. Not used for 3DS devices with 2Gb logical rank densities
3. Not used for 3DS devices with two logical ranks

Figure 2 — 3D Stacked DDR3 SDRAM x8 Ballout

2.4 Logical Rank Addressing

The 3DS package is organized into two, four or eight logical ranks.

For 3DS devices with 2 and 4 logical ranks, the logical ranks are selected by dedicated CS_n inputs. For 3DS devices with eight logical ranks, an additional select input CID (Chip ID) is used together with the four CS_n inputs to decode eight internal select signals. Figure 5, “8-4-1-1 Device (8H)” and Table 4, “DDR3 Address table: 8H Stacked SDRAM” define the behavior of the CID input.

The functional behavior of logical rank(s) should not deviate from DDR3 JEDEC standard SDRAMs, except when noted in this document. Each logical rank may be implemented as a single slice but the DDR3 3DS specification doesn’t require this to be the case. For example a 3DS device with four logical ranks may be implemented as eight slices, i.e. two 4Gb slices with 1 KB page size may be combined into an 8Gb logical rank with 2KB page size. Such an implementation has the advantage of not requiring a CID pin, making it more compatible with existing hosts and module support chips than regular 8H 3DS devices with eight 4Gb logical ranks (with 1KB page size).

2.5 3D Stack Organizations

Table 1, “Supported 3D Stack Organizations,” indicates valid configurations supported by the 3DS specification.

Table 1 — Supported 3D Stack Organizations

# of Logical Ranks	# of CS_n	# of CKE	# of ODT
2	2	1	1
4	4	1	1
8	4	1	1

Figure 3, Figure 4, and Figure 5 show one architectural diagram per row of Table 1. For the names of the these figures the standard *3DS configuration notation* LR-CS-CKE-ODT is used where LR indicates the number of logical ranks, CS_n indicates the number of chip select inputs, CKE indicates the number of CKE inputs and ODT indicates the number of ODT inputs. Since there is only one valid configuration for each number of logical ranks, this document will typical use the abbreviations 2H, 4H and 8H to describe 3DS devices with two, four or eight logical ranks. Table 1 shows all valid CKE and ODT configurations.

2.6 3DS SDRAM System Addressing

3DS addressing scheme for 3DS devices is explained in section 2.7. This document comprehends using these 3DS devices in RDIMM and LRDIMM applications with x4 or x8 3DS SDRAMs.

2.7 DDR3 3DS Stack Addressing Table

3DS devices with two and four logical ranks use dedicated CS_n inputs to select these logical ranks. 3DS SDRAMs with eight logical ranks require the additional address input CID (Chip ID) to select logical ranks 4 to 7. Figure 5 and Table 4 define the behavior of the CID pin.

Table 2, Table 3, and Table 4 indicate the address and select pins that are used for different configurations of 3DS stacks.

The 3DS DDR3 devices may be derived from monolithic DDR3 devices. Therefore the address signals used within a logical rank are identical to the address signals used by a monolithic DRAM of the same density.

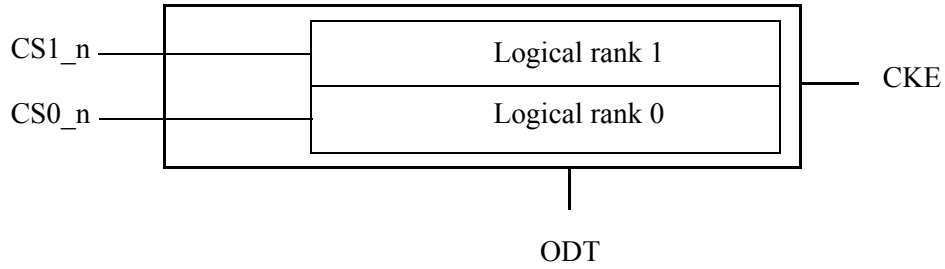


Figure 3 — 2-2-1-1 Device (2H)

Table 2 — DDR3 Address table: 2H Stacked SDRAM

DDR3 3DS address table : 2H 3D Stacked SDRAM								
3DS Logical Rank Organization					3DS Package Organization			
Density	Page Size	MSB Address			Capacity	Page Size	Logical Rank	Logical Rank selected by
		Row	Col					
			x4 Die	x8 Die				
2Gb	1KB	A14	A11	A9	4Gb	1KB	0	CS0_n
							1	CS1_n
4Gb	1KB	A15	A11	A9	8Gb	1KB	0	CS0_n
							1	CS1_n
8Gb	2KB	A15	A13	A11	16Gb	2KB	0	CS0_n
							1	CS1_n

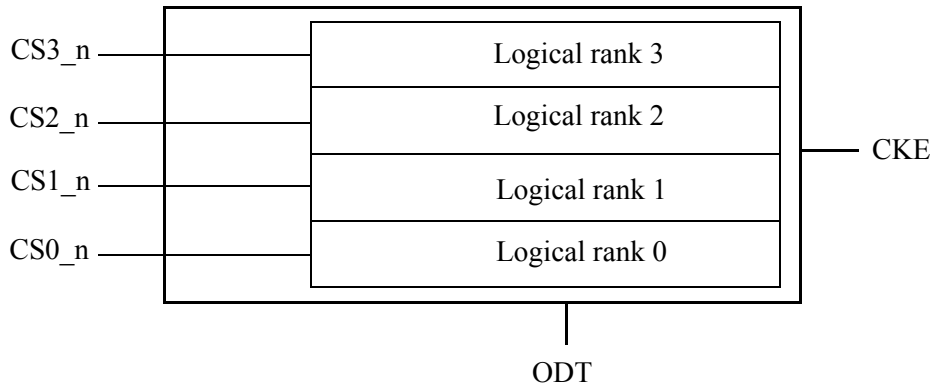


Figure 4 — 4-4-1-1 Device (4H)

Table 3 — DDR3 Address table: 4H Stacked SDRAM

DDR3 3DS address table : 4H Stacked SDRAM								
3DS Logical Rank Organization					3DS Package Organization			
Density	Page Size	MSB Address			Capacity	Page Size	Logical Rank	Logical Rank selected by
		Row	Col					
			x4 Die	x8 Die				
2Gb	1KB	A14	A11	A9	8Gb	1KB	0	CS0_n
							1	CS1_n
							2	CS2_n
							3	CS3_n
4Gb	1KB	A15	A11	A9	16Gb	1KB	0	CS0_n
							1	CS1_n
							2	CS2_n
							3	CS3_n
8Gb	2KB	A15	A13	A11	32Gb	2KB	0	CS0_n
							1	CS1_n
							2	CS2_n
							3	CS3_n

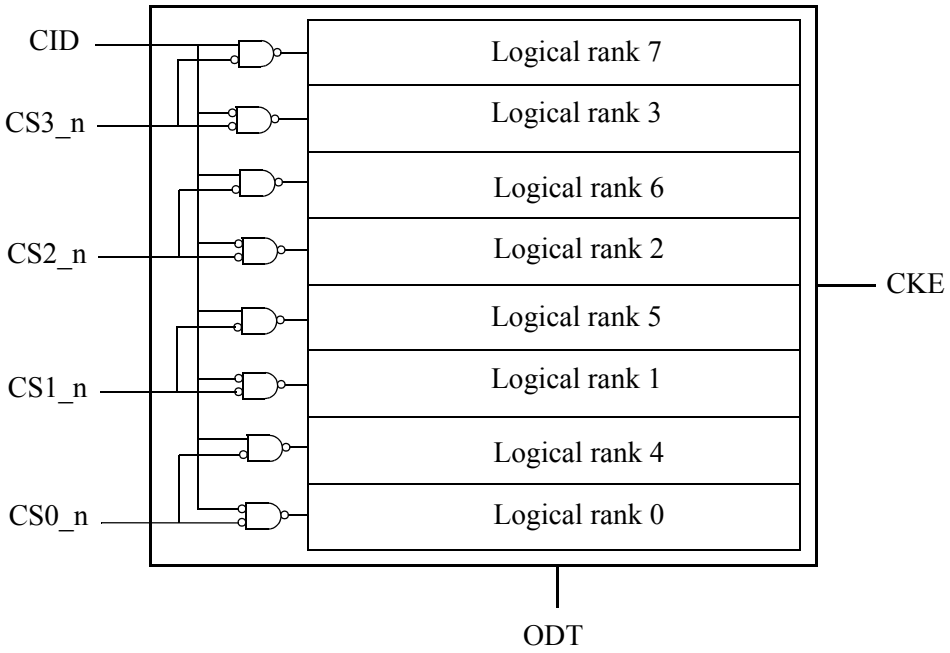


Figure 5 — 8-4-1-1 Device (8H)

Table 4 — DDR3 Address table: 8H Stacked SDRAM

DDR3 3DS address table : 8H Stacked SDRAM									
3DS Logical Rank Organization					3DS Package Organization				
Density	Page Size	MSB Address			Capacity	Page Size	Logical Rank	Logical Rank selected by	
		Row	Col						
			x4 Die	x8 Die					
2Gb	1KB	A14	A11	A9	16Gb	1KB	0	CS0_n	CID=L
							1	CS1_n	CID=L
							2	CS2_n	CID=L
							3	CS3_n	CID=L
							4	CS0_n	CID=H
							5	CS1_n	CID=H
							6	CS2_n	CID=H
							7	CS3_n	CID=H
4Gb	1KB	A15	A11	A9	32Gb	1KB	0	CS0_n	CID=L
							1	CS1_n	CID=L
							2	CS2_n	CID=L
							3	CS3_n	CID=L
							4	CS0_n	CID=H
							5	CS1_n	CID=H
							6	CS2_n	CID=H
							7	CS3_n	CID=H
8Gb	2KB	A15	A13	A11	64Gb	2KB	0	CS0_n	CID=L
							1	CS1_n	CID=L
							2	CS2_n	CID=L
							3	CS3_n	CID=L
							4	CS0_n	CID=H
							5	CS1_n	CID=H
							6	CS2_n	CID=H
							7	CS3_n	CID=H

Note that these diagrams show only the logical organizations of these devices. No 1:1 relationship to physical organizations is implied.

2.8 Bank Selection

3DS devices can accommodate up to 64 independent banks. Figure 6, “Bank Selection” shows how these banks are selected.

									CS3_n	CS2_n	CS1_n	CS0_n	CID
Logical Rank 7	Bank 63	Bank 62	Bank 61	Bank 60	Bank 59	Bank 58	Bank 57	Bank 56	0	1	1	1	1
Logical Rank 6	Bank 55	Bank 54	Bank 53	Bank 52	Bank 51	Bank 50	Bank 49	Bank 48	1	0	1	1	1
Logical Rank 5	Bank 47	Bank 46	Bank 45	Bank 44	Bank 43	Bank 42	Bank 41	Bank 40	1	1	0	1	1
Logical Rank 4	Bank 39	Bank 38	Bank 37	Bank 36	Bank 35	Bank 34	Bank 33	Bank 32	1	1	1	0	1
Logical Rank 3	Bank 31	Bank 30	Bank 29	Bank 28	Bank 27	Bank 26	Bank 25	Bank 24	0	1	1	1	0
Logical Rank 2	Bank 23	Bank 22	Bank 21	Bank 20	Bank 19	Bank 18	Bank 17	Bank 16	1	0	1	1	0
Logical Rank 1	Bank 15	Bank 14	Bank 13	Bank 12	Bank 11	Bank 10	Bank 9	Bank 8	1	1	0	1	0
Logical Rank 0	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0	1	1	1	0	0
Addressed by BA[2:0] =													
	111	110	101	100	011	010	001	000					

Figure 6 — Bank Selection

3 Functional Description

3.1 Simplified State Diagram

DDR3 3D Stacked SDRAMs use the same simplified state diagram documented in JESD79-3. Situations involving more than one bank, and multiple logical ranks are not reflected in the simple state diagram.

3.2 Basic Functionality

The 3DS DDR3 SDRAM is a 2H, 4H or 8H stacked high-speed dynamic random-access memory with each logical rank configured as an eight-logical bank SDRAM. The 3DS SDRAM has 16, 32 or 64 physical banks available internally, depending on the number of logical ranks. The 3DS DDR3 SDRAM retains the use of an 8n pre-fetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the 3DS DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal SDRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

3.3 Reset Signal and Initialization Procedure

Prior to normal operation, the 3DS DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

A single reset pin with a single load is available per 3DS device. It is expected that the entire stack of SDRAMs within the package reset as per DDR3 specification. After RESET_n is de-asserted, the SDRAM will start internal state initialization; this will be done independently of external clocks. All steps in the JESD79-3 initialization sequence must be followed. No additional steps are required for 3DS DDR3 devices but the unique nature of 3DS devices (which have a single external I/O structure shared by all logical ranks of the entire device) has to be considered when programing the SDRAM mode register bits (see next section for details).

3.4 Mode Register Definition

Like planar DDR3 SDRAMs, DDR3 3D Stacked SDRAMs have four Mode Registers. One set of registers controls the entire stack regardless if the 3DS stack has two, four or eight logical ranks, and they must be programmed via a Mode Register Set (MRS) command.

For 3DS DDR3 stacks configured as n logical ranks, the single set of MRS registers is addressed by CS0_n as shown in Table 5.

Table 5 — Simplified Truth Table for MRS Command

DRAM Command	CS0_n	CS1_n	CS2_n	CS3_n	CID	Logical rank 0	Logical rank 1	Logical rank 2	Logical rank 3	Logical rank 4	Logical rank 5	Logical rank 6	Logical rank 7	Notes
Mode Register Set	L	V	V	V	V	MRS	MRS	MRS	MRS	MRS	MRS	MRS	MRS	1 2
Mode Register Set	H	V	V	V	V	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	DES or NOP	2
Any Command	H	H	H	H	V	DES	DES	DES	DES	DES	DES	DES	DES	2

1. Mode Register Set to all logical ranks
2. "V" means H or L (but a defined logic level)

Programming the register fields for a stacked device has some special considerations. Waiting for the timing parameter tMRD is required between two MRS commands issued to any logical rank in a stacked device. After an MRS command is given, waiting for tMOD is required before a non-MRS command can be given to any logical rank in the stack.

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. Due to the additional latency caused by stacking multiple memory dies, one additional CAS Latency setting (CL-15), which was not used in the JESD79-3 base specification, has been added to the MR0 bits A[6:4], as shown in Figure 7.

BA2	BA1	BA0	A15 ~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
																	Address Field

0^1	0	0	0^1	PPD	WR	DLL	TM	CL	RBT	CL	BL	
												Mode Register 0

A6	A5	A4	A2	CL
0	0	0	0	Reserved
0	0	1	0	Reserved for CL5 of non-3D device
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14
0	1	1	1	15
1	0	0	1	Reserved
1	0	1	1	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

1. Must be programmed to 0

Figure 7 — Mode Register 0 Definition

In MR1, Additive Latency (AL) of CL-3 is supported for the case that tAA is larger than tRCD (optional if tAA=tRCD), as shown in Figure 8.

BA2	BA1	BA0	A15 ~ A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
																	Address Field

0^1	0	1	0^1	Qoff	TDQS	0^1	Rtt_Nom	0^1	Level	Rtt_Nom	D.I.C.	AL	Rtt_Nom	D.I.C.	DLL	
																Mode Register 1

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	CL-3[2]

1. Must be programmed to 0
2. For devices supporting the DDR3-1066F-3DS1B, DDR3-1333H-3DS1B, DDR3-1600K-3DS1B and DDR3-1866M-3DS1B speed bins, support for AL=CL-3 is optional

Figure 8 — Mode Register 1 Definition

Mode registers 2 to 3 are identical to the equivalent mode registers in planar DDR3 SDRAMs.

As the default values of the Mode Registers (MR#) are not defined, the contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

4 SDRAM Command Description and Operation

4.1 Write Leveling

The host initiates write leveling mode to all SDRAMs by setting bit 7 of MR1 to 1. Upon entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode.

Since a 3DS SDRAM configured as n logical ranks only has one physical set of output devices in the master die, the host only performs write leveling to one of the logical ranks in the package rank and doesn't need to perform write leveling to the other logical ranks. Therefore the host write levels one package rank at a time, and the outputs of other package ranks must be disabled by setting MR1 bit A12 to 1 in all other package ranks (which could be comprised of 3D Stacked devices or planar devices) on the same channel, which requires the host to be aware of what ranks in the channel are associated with individual package ranks.

4.2 ACTIVE Command

In a 3D Stacked DDR3 SDRAM the four chip select pins and the CID pin select the logical rank. No more than one logical rank ACTIVE command can be initiated simultaneously to DDR3 3DS devices, i.e. no more than a single chip select can be active when a ACTIVE command is send to a 3DS device, as shown in Table 6.

The minimum time interval between successive ACTIVE commands to the same bank of a DDR3 SDRAM is defined by tRC. The minimum time interval between successive ACTIVE commands to different banks of a DDR3 SDRAM is defined by tRRD.

For a 3DS device, the timing parameter that applies to successive ACTIVE commands to different banks in the same logical rank is defined as tRRD_slr (MIN). The timing parameter that applies to successive ACTIVE commands to different logical ranks is defined as tRRD_dlr (MIN).

No more than four bank ACTIVE commands may be issued in a given tFAW_slr (MIN) period to the same logical rank. For all logical ranks in a 3DS device, the tFAW_dlr timing constraint applies, i.e. no more than four bank ACTIVE commands to the whole 3DS SDRAM may be issued in a given tFAW_dlr (MIN) period.

The timing restrictions covering ACTIVE commands are documented in "Electrical Characteristics and AC Timings" on page 63.

Table 6 — Truth Table for ACTIVE Command

DRAM Command	CS0_n	CS1_n	CS2_n	CS3_n	CID	Logical rank 0	Logical rank 1	Logical rank 2	Logical rank 3	Logical rank 4	Logical rank 5	Logical rank 6	Logical rank 7	Notes
Active (ACT)	L	H	H	H	L	**ACT**	DES	DES	DES	DES	DES	DES	DES	
Active (ACT)	H	L	H	H	L	DES	**ACT**	DES	DES	DES	DES	DES	DES	
Active (ACT)	H	H	L	H	L	DES	DES	**ACT**	DES	DES	DES	DES	DES	
Active (ACT)	H	H	H	L	L	DES	DES	DES	**ACT**	DES	DES	DES	DES	
Active (ACT)	L	H	H	H	H	DES	DES	DES	DES	**ACT**	DES	DES	DES	
Active (ACT)	H	L	H	H	H	DES	DES	DES	DES	DES	**ACT**	DES	DES	
Active (ACT)	H	H	L	H	H	DES	DES	DES	DES	DES	DES	**ACT**	DES	
Active (ACT)	H	H	H	L	H	DES	DES	DES	DES	DES	DES	DES	**ACT**	
Active (ACT)	V	V	L	L	V	illegal								1
Active (ACT)	V	L	V	L	V	illegal								1
Active (ACT)	L	V	V	L	V	illegal								1
Active (ACT)	V	L	L	V	V	illegal								1
Active (ACT)	L	V	L	V	V	illegal								1
Active (ACT)	L	L	V	V	V	illegal								1
Any Command	H	H	H	H	V	DES	DES	DES	DES	DES	DES	DES	DES	1

1. "V" means H or L (but a defined logic level)

4.3 Precharge and Precharge All Commands

The Single Bank Precharge (PRE) and Precharge All Banks (PREA) commands apply only to selected logical ranks of a 3D Stacked SDRAM. It means that these commands are allowed to be issued to multiple ranks (four logical ranks maximum) at the same time (broadcast command). And it is illegal to issue PREA commands to multiple logical ranks simultaneously if they have more than 8 open rows in total.

The bank(s) will be available for a subsequent row activation a specified time (tRP) after the Precharge command is issued, except in the case of concurrent auto precharge, where a Read or Write command to a different rank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters **in a logical rank**.

PRE commands (or PRE commands to each open bank) have to be issued to all logical ranks with open banks before the device can enter Self Refresh mode.

A Precharge command is allowed if there is no open row in that bank (idle state) of **the selected logical rank(s)** or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last Precharge command issued to the bank of **the selected logical rank(s)**.

Each logical rank of 3D Stacked SDRAMs has the same values for tRP, tRTP, tRAS and tDAL as planar DDR3 SDRAMs of the same frequency.

Table 7 and Table 8 show the truth tables for Precharge and Precharge All commands.

Table 7 — Truth Table for Precharge Command

DRAM Command	CS0_n	CS1_n	CS2_n	CS3_n	CID	Logical rank 0	Logical rank 1	Logical rank 2	Logical rank 3	Logical rank 4	Logical rank 5	Logical rank 6	Logical rank 7	Notes
Precharge (PRE)	L	L	L	L	L	**PRE**	**PRE**	**PRE**	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	L	L	L	H	L	**PRE**	**PRE**	**PRE**	DES	DES	DES	DES	DES	1 2
Precharge (PRE)	L	L	H	L	L	**PRE**	**PRE**	DES	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	L	L	H	H	L	**PRE**	**PRE**	DES	DES	DES	DES	DES	DES	1 2
Precharge (PRE)	L	H	L	L	L	**PRE**	DES	**PRE**	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	L	H	L	H	L	**PRE**	DES	**PRE**	DES	DES	DES	DES	DES	1 2
Precharge (PRE)	L	H	H	L	L	**PRE**	DES	DES	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	L	H	H	H	L	**PRE**	DES	DES	DES	DES	DES	DES	DES	1 2
Precharge (PRE)	H	L	L	L	L	DES	**PRE**	**PRE**	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	H	L	L	H	L	DES	**PRE**	**PRE**	DES	DES	DES	DES	DES	1 2
Precharge (PRE)	H	L	H	L	L	DES	**PRE**	DES	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	H	L	H	H	L	DES	**PRE**	DES	DES	DES	DES	DES	DES	1 2
Precharge (PRE)	H	H	L	L	L	DES	DES	**PRE**	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	H	H	L	H	L	DES	DES	**PRE**	DES	DES	DES	DES	DES	1 2
Precharge (PRE)	H	H	H	L	L	DES	DES	DES	**PRE**	DES	DES	DES	DES	1 2
Precharge (PRE)	L	L	L	L	H	DES	DES	DES	DES	**PRE**	**PRE**	**PRE**	**PRE**	1 2
Precharge (PRE)	L	L	L	H	H	DES	DES	DES	DES	**PRE**	**PRE**	**PRE**	DES	1 2
Precharge (PRE)	L	L	H	L	H	DES	DES	DES	DES	**PRE**	**PRE**	DES	**PRE**	1 2
Precharge (PRE)	L	L	H	H	H	DES	DES	DES	DES	**PRE**	**PRE**	DES	DES	1 2
Precharge (PRE)	L	H	L	L	H	DES	DES	DES	DES	**PRE**	DES	**PRE**	**PRE**	1 2
Precharge (PRE)	L	H	L	H	H	DES	DES	DES	DES	**PRE**	DES	**PRE**	DES	1 2
Precharge (PRE)	L	H	H	L	H	DES	DES	DES	DES	**PRE**	DES	DES	**PRE**	1 2
Precharge (PRE)	L	H	H	H	H	DES	DES	DES	DES	**PRE**	DES	DES	DES	1 2
Precharge (PRE)	H	L	L	L	H	DES	DES	DES	DES	DES	**PRE**	**PRE**	**PRE**	1 2
Precharge (PRE)	H	L	L	H	H	DES	DES	DES	DES	DES	**PRE**	**PRE**	DES	1 2
Precharge (PRE)	H	L	H	L	H	DES	DES	DES	DES	DES	**PRE**	DES	**PRE**	1 2
Precharge (PRE)	H	L	H	H	H	DES	DES	DES	DES	DES	**PRE**	DES	DES	1 2
Precharge (PRE)	H	H	L	L	H	DES	DES	DES	DES	DES	DES	**PRE**	**PRE**	1 2
Precharge (PRE)	H	H	L	H	H	DES	DES	DES	DES	DES	DES	**PRE**	DES	1 2
Precharge (PRE)	H	H	H	L	H	DES	DES	DES	DES	DES	DES	DES	**PRE**	1 2
Any Command	H	H	H	H	V	DES	DES	DES	DES	DES	DES	DES	DES	3

1. Precharge only to the same selected bank within selected logical rank(s)
2. A10=L
3. “V” means H or L (but a defined logic level)

Table 8 — Truth Table for Precharge All Command

DRAM Command	CS0_n	CS1_n	CS2_n	CS3_n	CID	Logical rank 0	Logical rank 1	Logical rank 2	Logical rank 3	Logical rank 4	Logical rank 5	Logical rank 6	Logical rank 7	Notes
Precharge (PREA)	L	L	L	L	L	**PREA**	**PREA**	**PREA**	**PREA**	DES	DES	DES	DES	1 2 3
Precharge (PREA)	L	L	L	H	L	**PREA**	**PREA**	**PREA**	DES	DES	DES	DES	DES	1 2 3
Precharge (PREA)	L	L	H	L	L	**PREA**	**PREA**	DES	**PREA**	DES	DES	DES	DES	1 2 3
Precharge (PREA)	L	L	H	H	L	**PREA**	**PREA**	DES	DES	DES	DES	DES	DES	1 2 3
Precharge (PREA)	L	H	L	L	L	**PREA**	DES	**PREA**	**PREA**	DES	DES	DES	DES	1 2 3
Precharge (PREA)	L	H	L	H	L	**PREA**	DES	**PREA**	DES	DES	DES	DES	DES	1 2 3
Precharge (PREA)	L	H	H	L	L	**PREA**	DES	DES	**PREA**	DES	DES	DES	DES	1 2 3
Precharge (PREA)	L	H	H	H	L	**PREA**	DES	DES	DES	DES	DES	DES	DES	1 3
Precharge (PREA)	H	L	L	L	L	DES	**PREA**	**PREA**	**PREA**	DES	DES	DES	DES	1 2 3
Precharge (PREA)	H	L	L	H	L	DES	**PREA**	**PREA**	DES	DES	DES	DES	DES	1 2 3
Precharge (PREA)	H	L	H	L	L	DES	**PREA**	DES	**PREA**	DES	DES	DES	DES	1 2 3
Precharge (PREA)	H	L	H	H	L	DES	**PREA**	DES	DES	DES	DES	DES	DES	1 3
Precharge (PREA)	H	H	L	L	L	DES	DES	**PREA**	**PREA**	DES	DES	DES	DES	1 2 3
Precharge (PREA)	H	H	L	H	L	DES	DES	**PREA**	DES	DES	DES	DES	DES	1 3
Precharge (PREA)	H	H	H	L	L	DES	DES	DES	**PREA**	DES	DES	DES	DES	1 3
Precharge (PREA)	L	L	L	L	H	DES	DES	DES	DES	**PREA**	**PREA**	**PREA**	**PREA**	1 2 3
Precharge (PREA)	L	L	L	H	H	DES	DES	DES	DES	**PREA**	**PREA**	**PREA**	DES	1 2 3
Precharge (PREA)	L	L	H	L	H	DES	DES	DES	DES	**PREA**	**PREA**	DES	**PREA**	1 2 3
Precharge (PREA)	L	L	H	H	H	DES	DES	DES	DES	**PREA**	**PREA**	DES	DES	1 2 3
Precharge (PREA)	L	H	L	L	H	DES	DES	DES	DES	**PREA**	DES	**PREA**	**PREA**	1 2 3
Precharge (PREA)	L	H	L	H	H	DES	DES	DES	DES	**PREA**	DES	**PREA**	DES	1 2 3
Precharge (PREA)	L	H	H	L	H	DES	DES	DES	DES	**PREA**	DES	DES	**PREA**	1 2 3
Precharge (PREA)	L	H	H	H	H	DES	DES	DES	DES	**PREA**	DES	DES	DES	1 3
Precharge (PREA)	H	L	L	L	H	DES	DES	DES	DES	DES	**PREA**	**PREA**	**PREA**	1 2 3
Precharge (PREA)	H	L	L	H	H	DES	DES	DES	DES	DES	**PREA**	**PREA**	DES	1 2 3
Precharge (PREA)	H	L	H	L	H	DES	DES	DES	DES	DES	**PREA**	DES	**PREA**	1 2 3
Precharge (PREA)	H	L	H	H	H	DES	DES	DES	DES	DES	**PREA**	DES	DES	1 3
Precharge (PREA)	H	H	L	L	H	DES	DES	DES	DES	DES	DES	**PREA**	**PREA**	1 2 3
Precharge (PREA)	H	H	L	H	H	DES	DES	DES	DES	DES	DES	**PREA**	DES	1 3
Precharge (PREA)	H	H	H	L	H	DES	DES	DES	DES	DES	DES	DES	**PREA**	1 3
Any Command	H	H	H	H	V	DES	DES	DES	DES	DES	DES	DES	DES	4

1. Precharge to all banks only in selected logical rank(s)
2. It is illegal to issue PREA commands to multiple logical ranks if they have more than 8 open rows in total
3. A10=H
4. “V” means H or L (but a defined logic level)

4.4 Read and Write Commands

In a 3D Stacked DDR3 SDRAM the four chip select pins and the CID pin select the logical rank. No more than one logical rank ACTIVE command can be initiated simultaneously to DDR3 3DS devices, i.e. no more than a single chip select can be active when a ACTIVE command is send to a 3DS device.

For 3DS devices the minimum time from issuing successive read-to-read or write-to-write commands to different logical ranks is tCCD even to different logical ranks. No additional latency needs to be added for logical rank to logical rank turnaround time.

For back-to-back read-to-write or write-to-read commands issued to different logical ranks, turnaround times are completely identical as to same logical rank.

The 3DS command to command timings are shown in Table 9.

Table 9 — Logical Rank to Logical Rank CMD-to-CMD Timings

Timing Parameter	Equation	Notes
Minimum Read after Read	tCCD	1
Minimum Write after Write	tCCD	
Minimum Write after Read	RL + BL(on the fly)/2 + 2 - WL	2
Minimum Read after Write	CWL + BL(fixed)/2 + tWTR	3

1. These timings require extended calibrations times tZQinit and tZQCS (values TBD)
2. BL(on the fly) = 8 for MR0(A1,A0) = 00b. BL(on the fly) = 4 for MR0(A1,A0) = 10b. BL(on the fly) = 4 for MR0(A1,A0) = 01b if A12/BC_n = LOW. BL(on the fly) = 8 for MR0(A1,A0) = 01b if A12/BC_n = HIGH.
3. BL(fixed) = 8 for MR0(A1,A0) = 00b or 01b. BL(fixed) = 4 for MR0(A1,A0) = 10b.

4.5 Refresh Command

No more than one logical rank Refresh Command can be initiated simultaneously to DDR3 3D Stacked SDRAMs, i.e. no more than a single chip select can be active when a Refresh command is send to a 3D stacked device, as shown in Table 10.

The minimum refresh cycle time to a single logical rank (=tRFC_slr) has the same value as tRFC for a planar DDR3 SDRAM of the same density as the logical rank.

The minimum time between issuing refresh commands to different logical ranks is specified as tRFC_dlr. After a Refresh command to a logical rank, other valid commands can be issued before tRFC_dlr to the other logical ranks that are not the target of the refresh.

Table 10 — Truth Table for Refresh Command

DRAM Command	CS0_n	CS1_n	CS2_n	CS3_n	CID	Logical rank 0	Logical rank 1	Logical rank 2	Logical rank 3	Logical rank 4	Logical rank 5	Logical rank 6	Logical rank 7	Notes
Refresh (REF)	L	H	H	H	L	**REF**	DES	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	H	L	H	H	L	DES	**REF**	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	H	H	L	H	L	DES	DES	**REF**	DES	DES	DES	DES	DES	1
Refresh (REF)	H	H	H	L	L	DES	DES	DES	**REF**	DES	DES	DES	DES	1
Refresh (REF)	L	H	H	H	H	DES	DES	DES	DES	**REF**	DES	DES	DES	1
Refresh (REF)	H	L	H	H	H	DES	DES	DES	DES	DES	**REF**	DES	DES	1
Refresh (REF)	H	H	L	H	H	DES	DES	DES	DES	DES	DES	**REF**	DES	1
Refresh (REF)	H	H	H	L	H	DES	DES	DES	DES	DES	DES	DES	**REF**	1
Refresh (REF)	V	V	L	L	V	illegal								1 2
Refresh (REF)	V	L	V	L	V	illegal								1 2
Refresh (REF)	L	V	V	L	V	illegal								1 2
Refresh (REF)	V	L	L	V	V	illegal								1 2
Refresh (REF)	L	V	L	V	V	illegal								1 2
Refresh (REF)	L	L	V	V	V	illegal								1 2
Any Command	H	H	H	H	V	DES	DES	DES	DES	DES	DES	DES	DES	1 2

1. CKE=H
2. "V" means H or L but a defined logic level)

In general, a Refresh command needs to be issued to each logical rank in 3D Stacked DDR3 SDRAM regularly every tREFI_slr interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands per logical rank can be postponed during operation of the 3D stacked DDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed per logical rank. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI_slr. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in") per logical rank, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI_slr. At any given time, a maximum of 16 REF commands per logical rank can be issued within 2 x tREFI_slr. Self-Refresh Mode may be entered with a maximum of eight Refresh commands per logical rank being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight per logical rank. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

4.6 Self-Refresh Operation and Power-Down Modes

The CKE functionality should adhere to the DDR3 specification for planar DDR3 SDRAMs in JESD79-3.

Since there is only one CKE pin per 3DS device, all logical ranks enter self refresh and power down together, as shown in Table 11.

Table 11 — Truth Table for SRE and PDE

DRAM Command	CS0_n	CS1_n	CS2_n	CS3_n	CID	Logical rank 0	Logical rank 1	Logical rank 2	Logical rank 3	Logical rank 4	Logical rank 5	Logical rank 6	Logical rank 7	Notes
Refresh (REF)	L	V	V	V	V	SRE	SRE	SRE	SRE	SRE	SRE	SRE	SRE	1 2
Refresh (REF)	H	V	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1 2
NOP	V	V	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1 2
Any Command	H	H	H	H	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1 2

1. "V" means H or L (but a defined logic level)
2. with CKE-->L

Self-Refresh exit (SRX) and power-down exit (PDX) apply to all logical ranks in a 3D Stacked device and is caused by the Low-to-High transition of the single CKE pin.

Either a No Operation command to any logical rank(s) of the device or a Deselect command can be used for SRX.

Either a No Operation command to any logical rank(s) of the device or a Deselect command can be used for PDX.

3D Stacked SDRAMs have the same values of all parameters for Self Refresh Timings and Power Down Timings as planar DDR3 SDRAMs of the same frequency. Specification of tXS 3D Stacked DDR3 has been modified with Refresh Parameter by Logical Rank Density.

Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress.The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the 3D stacked DDR3 SDRAM requires a minimum of one extra refresh command to all logical Ranks (each refresh period of tRFC_slr), before it is put back into Self-Refresh Mode.

4.7 ZQ Calibration Commands

Each 3DS package will have a single ZQ calibration pin, independent of the number of logical ranks in the stack. The lowest numbered chip select (CS0_n) of each package should be associated with the master logical rank. Since there is only one I/O per device, the ZQ0 pin should be associated with master logical rank, and other ZQ pins are tied to VSS

The calibration procedure and the result for 3DS devices adheres to the JESD79-3 DDR3 component specification. The host may issue ZQ calibration command to each logical rank. The SDRAM can choose to ignore the ZQ commands to the non-master logical rank or execute the calibration of the I/O attached to the master logical rank.

5 On Die Termination

No changes from JESD79-3.

Each 3D Stacked SDRAM has a single ODT input and wrt ODT functionality behaves like a mono DDR3 SDRAM.

6 Absolute Maximum Ratings

The ratings in Table 12 guarantee 1.5V voltage tolerance for DDR3 3D Stacked SDRAMs.

Table 12 — Absolute Maximum DC Ratings

Symbol	Parameter/Condition	Rating	Units	Notes
Vdd	Voltage on VDD pin relative to Vss	-0.4V ~ 1.70V	V	1 2
VddQ	Voltage on VDD Qpin relative to Vss	-0.4V ~ 1.70V	V	1 2
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4V ~ 1.70V	V	1
TSTG	Storage Temperature	-55 to +100	^{o}C	1 3

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD and VDDQ must be within 300 mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.
3. Storage Temperature is the case temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

7 AC & DC Operating Conditions

Operating at 1.5V or 1.25V is not a requirement for DDR3 3D Stacked SDRAMs.

Table 13 — Recommended DC Operating Conditions

Symbol	Parameter/Condition	Min	Typ	Max	Units	Notes
Vdd	Supply voltage	1.283	1.35	1.45	V	1
VddQ	Supply voltage for Output	1.283	1.35	1.45	V	1

1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g., 1 sec).

8 AC & DC Input Measurement Levels

No changes from the DDR3L, Addendum No. 1 to JESD79-3 (JESD79-3-1).

9 AC & DC Output Measurement Levels

No changes from the DDR3L, Addendum No. 1 to JESD79-3 (JESD79-3-1).

10 IDD Current Specification

10.1 IDD and IDDQ Measurement Conditions

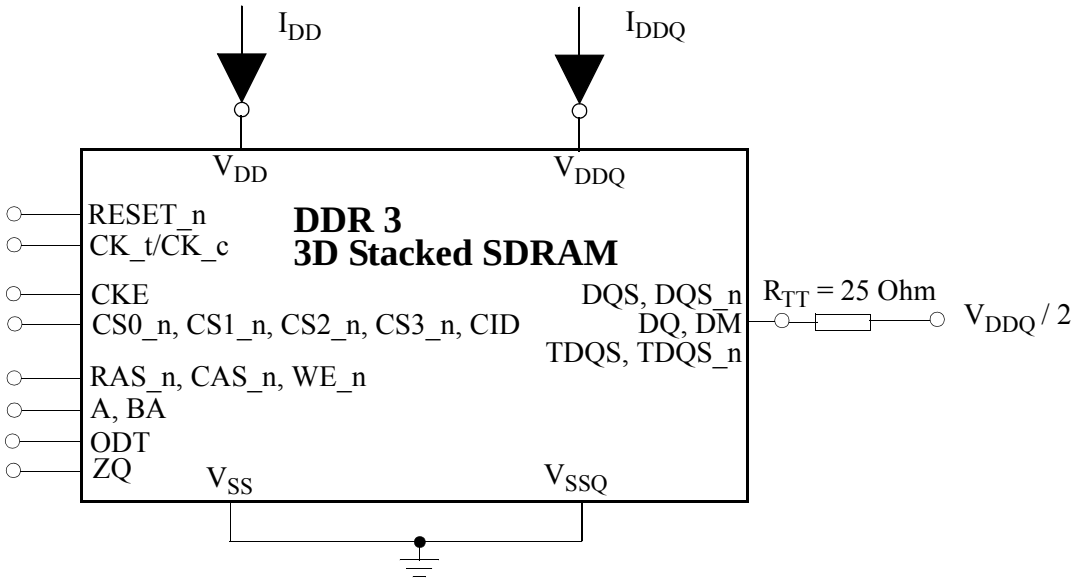
In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 9 shows the setup and test load for IDD and IDDQ measurements.

IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B1, IDD5B2, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.

IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 10. In SDRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN <= VILAC(max).
- "1" and "HIGH" is defined as VIN >= VIHAC(min).
- "MID-LEVEL" is defined as inputs are VREF = VDD / 2.
- Timings used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 14, "Timings used for IDD and IDDQ measurements loop patterns".
- Basic IDD and IDDQ Measurement Conditions are described in Table 15, "Basic IDD and IDDQ Measurement Conditions".
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- **Attention:** The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS0_n, CS1_n, CS2_n, CS3_n, CID, RAS_n, CAS_n, WE_n } := {HIGH, **H**IGH, HIGH, HIGH, LOW, LOW, LOW, LOW}
- Define D# = {CS0_n, CS1_n, CS2_n, CS3_n, CID, RAS_n, CAS_n, WE_n } := {HIGH, HIGH, HIGH, HIGH, HIGH, HIGH, HIGH, HIGH}



Note: DIMM level Output test load condition may be different from above.

Figure 9 — Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements

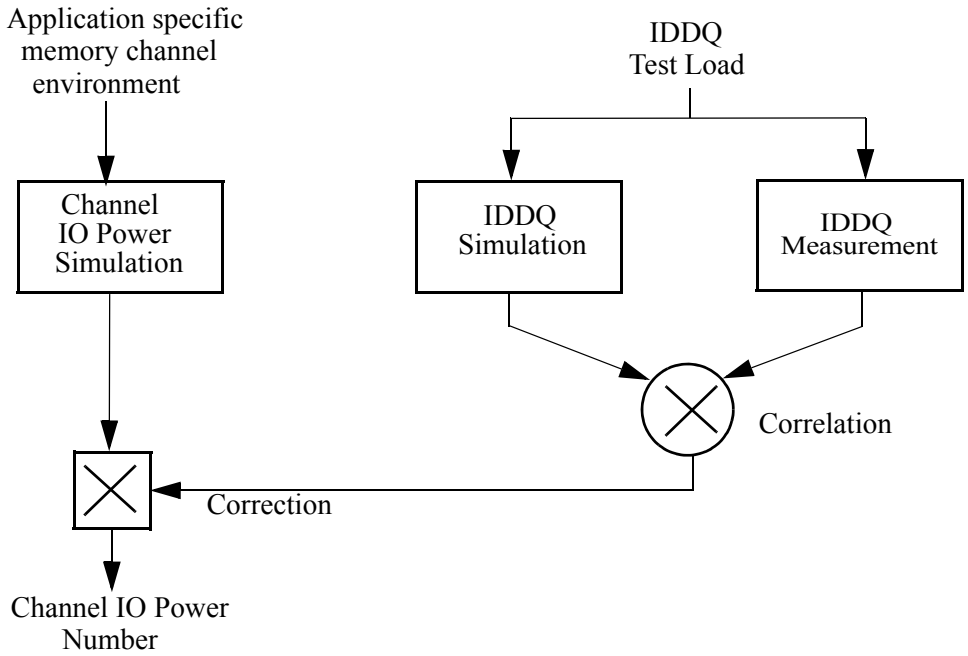


Figure 10 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 14 — Timings used for IDD and IDDQ measurements loop patterns

Symbol		DDR3-800	DDR3-1066					DDR3-1333				Unit
		7-6-6	8-7-7	8-8-7	9-7-7	9-8-8	10-8-8	10-9-9	10-10-9	11-9-9	11-10-10	
tCK		2.5	1.875					1.5				ns
CL		7	8	8	9	9	10	10	10	11	11	nCK
nRCD		6	7	8	7	8	8	9	10	9	10	nCK
nRC		21	27	27	27	28	28	34	33	34	35	nCK
nRAS		15	20					25				nCK
nRP		6	7	7	7	8	8	9	9	9	10	nCK
nFAW_slr	1KB page size	16	20					20				nCK
	2KB page size	20	27					30				nCK
nRRD_slr	1KB page size	4	4					4				nCK
	2KB page size	4	6					5				nCK
nRFC_slr 2 Gb		64	86					107				nCK
nRFC_slr 4 Gb		120	139					174				nCK
nRFC_slr 8 Gb		140	187					234				nCK
nRFC_dlr 2 Gb		24	32					40				nCK
nRFC_dlr 4 Gb		36	48					60				nCK
nRFC_dlr 8 Gb		48	64					80				nCK

Table 14 — Timings used for IDD and IDDQ measurements loop patterns (Continued)

Symbol		DDR3-1600			DDR3-1866		Unit
		12-11-11	12-12-11	13-11-11	14-14-13	15-13-13	
tCK		1.25			1.07		ns
CL		12	12	13	14	15	nCK
nRCD		11	12	11	14	13	nCK
nRC		39	39	39	45	45	nCK
nRAS		28			32		nCK
nRP		11	11	11	13	13	nCK
nFAW_slr	1KB page size	24			26		nCK
	2KB page size	32			33		nCK
nRRD_slr	1KB page size	5			5		nCK
	2KB page size	6			6		nCK
nRFC_slr 2 Gb		128			150		nCK
nRFC_slr 4 Gb		208			243		nCK
nRFC_slr 8 Gb		280			328		nCK
nRFC_dlr 2 Gb		48			56		nCK
nRFC_dlr 4 Gb		72			84		nCK
nRFC_dlr 8 Gb		96			112		nCK

Table 15 defines 3DS IDD Definition Per 3DS Package

Table 15 — Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 14; BL: 8[1]; AL: 0; CS[3:0]_n: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 16; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,… (see Table 16); Logical Rank Activity: Cycling with one rank active at a time; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: see Table 16.** **Non-activated logical rank is in Precharge Standby state.**
IDD1	**Operating One Bank Active-Read-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling according to **Table 17**; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see **Table 17**); **Logical Rank Activity: Cycling with one rank active at a time; Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see **Table 17** **Non-activated logical rank is in Precharge Standby state.**
IDD2N	**Precharge Standby Current, all pages closed** **CKE**: High; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 18**; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see **Table 18**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 19**; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to **Table 19**; **Pattern Details:** see **Table 19**
IDDQ2NT (optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current.
IDD2P0	**Precharge Power-Down Current Slow Exit** **CKE:** Low; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Slow Exit[3]
IDD2P1	**Precharge Power-Down Current Fast Exit** **CKE:** Low; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Fast Exit[3]

Table 15 — Basic IDD and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current, all pages open** **CKE**: High; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 18**; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks **of all logical ranks** open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see **Table 18**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1,7]; **AL:** 0; **CS[3:0]_n**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 20**; **Data IO:** seamless read data burst with different data between one burst and the next one according to **Table 20**; **DM**:stable at 0; **Bank Activity:** all banks **of all logical ranks** open, RD commands cycling through banks: 0,0,1,1,2,2,... (see **Table 20**) **and through logical ranks**; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see **Table 20** **Non-Read logical rank is in Active Standby state.**
IDDQ4R (optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 21**; **Data IO:** seamless write data burst with different data between one burst and the next one according to **Table 21**; **DM:** stable at 0; **Bank Activity:** all banks **of all logical ranks** open, WR commands cycling through banks: 0,0,1,1,2,2,... (see **Table 21**) **and through logical ranks**; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see **Table 21** **Non-Write logical rank is in Active Standby state.**
IDD5B1	**Burst Refresh Current** **CKE:** High; **External clock:** On; **tCK, CL, nRFC_slr**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: High between REF; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 22**; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** REF command every **nRFC_dlr** (see **Table 22**); **Logical Rank Activity: REF command staggered nRFC_dlr between REF command to REF command for different logical rank; Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see **Table 22** Non-Refresh logical rank is in Precharge Standby State.

Table 15 — Basic IDD and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDD5B2	**Burst Refresh Current** **CKE:** High; **External clock:** On; **tCK, CL, nRFC_slr**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n**: High between REF; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 23**; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** REF command every **nRFC_slr** (see **Table 23**); **Logical Rank Activity: REF command staggered nRFC_slr between REF command to REF command for different logical rank; Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see **Table 23** Non-Refresh logical rank is in Precharge Standby State.
IDD6	**Self Refresh Current: Normal Temperature Range** ***T*CASE:** 0 - 85°C; **Auto Self-Refresh (ASR)**: Disabled[4]; **Self-Refresh Temperature Range (SRT):** Normal[5]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n, Command, Address, Bank Address, Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IDD6ET	**Self-Refresh Current: Extended Temperature Range (optional)[6]** ***T*CASE:** 0 - 95°C; **Auto Self-Refresh (ASR)**: Disabled[6]**; Self-Refresh Temperature Range (SRT):** Extended[5]**; CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see **Table 14**; **BL:** 8[1]**; AL:** 0; **CS[3:0]_n, Command, Address, Bank Address, Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]**; ODT Signal:** MID-LEVEL
IDD6TC	**Auto Self-Refresh Current (optional)[6]** ***T*CASE:** 0 - 95°C; **Auto Self-Refresh (ASR)**: Enabled[6]; **Self-Refresh Temperature Range (SRT):** Normal[5]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see **Table 14**; **BL:** 8[1]; **AL:** 0; **CS[3:0]_n, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IDD7	**Operating One Logical Rank Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD_slr, nFAW_slr, CL**: see **Table 14**; **BL:** 8[1,7]; **AL: (TBD CL-1 or CL-3 or CL-4)**; **CS[3:0]_n**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling according to **Table 24**; **Data IO:** read data bursts with different data between one burst and the next one according to **Table 24**; **DM**:stable at 0; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see **Table 24**; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see **Table 24** **Non-activated logical rank is in Precharge Standby state.**
IDD8 (Optional)	**RESET Low Current** **RESET:** LOW; **External clock:** Off; **CK_t and CK_c:** LOW; **CKE:** FLOATING; **CS[3:0]_n**, **Command, Address, Bank Address, Data IO:** FLOATING; **ODT Signal:** FLOATING RESET Low current reading is valid once power is stable and RESET has been LOW for at least 1ms.

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
3. Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
5. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range

6. Refer to SDRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device
7. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

Table 16 — IDD0 measurement - Loop pattern[1], 4H Stacking as Example

CK_t,	CKE	Sub-Loop	Rank--Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	0	ACT	111	0	1	1	0	0	00	0	0	0	0	-
				1, 2	D, D	111 1	0	0	0	0	0	00	0	0	0	0	-
				3, 4	D#, D#	111 1	1	1	1	0	0	00	0	0	0	0	-
				...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
				nRAS	PRE	111 0	0	1	0	0	0	00	0	0	0	0	-
				...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
				1*nRC + 0	ACT	111 0	0	1	1	0	0	00	0	0	F	0	-
				1*nRC + 1, 2	D, D	111 1	0	0	0	0	0	00	0	0	F	0	-
				1*nRC + 3, 4	D#, D#	111 1	1	1	1	0	0	00	0	0	F	0	-
				...	repeat pattern nRC + 1,...,4 until 1*nRC + nRAS - 1, truncate if necessary												
				1*nRC + nRAS	PRE	111 0	0	1	0	0	0	00	0	0	F	0	-
				...	repeat nRC + 1,...,4 until 2*nRC - 1, truncate if necessary												
			1	2*nRC	repeat Rank-Loop 0, use **CS[3:0]_n = 1101** instead for ACT and PRE command												
			2	4*nRC	repeat Rank-Loop 0, use **CS[3:0]_n = 1011** instead for ACT and PRE command												
			3	6*nRC	repeat Rank-Loop 0, use **CS[3:0]_n = 0111** instead for ACT and PRE command												
		1		8*nRC	repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2		16*nRC	repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3		24*nRC	repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4		32*nRC	repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5		40*nRC	repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6		48*nRC	repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7		56*nRC	repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

1. DM must be driven LOW all the time. DQS, DQS_n are MID-LEVEL
2. DQ signals are MD-LEVEL

2H and 8H stacking IDD0 measurement loop pattern will be similar to the 4H stacking measurement loop pattern in Table 16, but with the logical rank select signal setting CS[3:0] and CID to be consistent with 3DS spec definition.

Table 17 — IDD1 measurement - Loop pattern[1], 4H Stacking as Example

CK_t,	CKE	Sub-	Rank-Loop	Cycle Number	Command	CS[3:0]	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	0	**ACT**	1110	0	1	1	0	**0**	00	0	0	**0**	0	-
				1, 2	D, D	1111	0	0	0	0	**0**	00	0	0	**0**	0	-
				3,4	D#, D#	1111	1	1	1	0	**0**	00	0	0	**0**	0	-
				...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
				nRCD	**RD**	1110	1	0	1	0	**0**	00	0	0	**0**	0	00000000
				...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
				nRAS	**PRE**	1110	0	1	0	0	0	00	0	0	**0**	0	-
				...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
				1*nRC + 0	**ACT**	1110	0	1	1	0	**0**	00	0	0	**F**	0	-
				1*nRC + 1, 2	D, D	1111	0	0	0	0	**0**	00	0	0	**F**	0	-
				1*nRC + 3, 4	D#, D#	1111	1	1	1	0	**0**	00	0	0	**F**	0	-
				...	repeat pattern nRC + 1,..., 4 until nRC + nRCD - 1, truncate if necessary												
				1*nRC + nRCD	**RD**	1110	1	0	1	0	**0**	00	0	0	**F**	0	00110011
				...	repeat pattern nRC + 1,..., 4 until nRC +nRAS - 1, truncate if necessary												
				1*nRC + nRAS	**PRE**	1110	0	1	0	0	0	00	0	0	**F**	0	-
				...	repeat pattern nRC + 1,..., 4 until 2 * nRC - 1, truncate if necessary												
			1	2*nRC	repeat Rank-Loop 0, use **CS[3:0]_n = 1101** instead for ACT and PRE command												
			2	4*nRC	repeat Rank-Loop 0, use **CS[3:0]_n= 1011** instead for ACT and PRE command												
			3	6*nRC	repeat Rank-Loop 0, use **CS[3:0]_n = 0111** instead for ACT and PRE command												
		1		8*nRC	repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2		16*nRC	repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3		24*nRC	repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4		32*nRC	repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5		40*nRC	repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6		48*nRC	repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7		56*nRC	repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

1. DM must be driven LOW all the time. DQS, DQS_n are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

2H and 8H stacking IDD1 measurement loop pattern will be similar to the 4H stacking measurement loop pattern in Table 17, but with the logical rank select signal setting CS[3:0] and CID to be consistent with 3DS spec definition.

Table 18 — IDD2N and IDD3N measurement - Loop pattern[1]

CK_t,	CKE	Sub-	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	D	1111	0	0	0	0	**0**	0	0	0	**0**	0	-
			1	D	1111	0	0	0	0	**0**	0	0	0	**0**	0	-
			2	D#	1111	1	1	1	0	**0**	0	0	0	**F**	0	-
			3	D#	1111	1	1	1	0	**0**	0	0	0	**F**	0	-
		1	4-7	repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2	8-11	repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3	12-15	repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4	16-19	repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5	20-23	repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6	24-27	repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7	27-31	repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

1. DM must be driven LOW all the time. DQS, DQS_n are MID-LEVEL
2. DQ signals are MID-LEVEL.

Table 19 — IDD2N and IDDQ2NT measurement-Loop pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	D	1111	0	0	0	**0**	**0**	0	0	0	**0**	0	-
			1	D	1111	0	0	0	**0**	**0**	0	0	0	**0**	0	-
			2	D#	1111	1	1	1	**0**	**0**	0	0	0	**F**	0	-
			3	D#	1111	1	1	1	**0**	**0**	0	0	0	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but **ODT = 0** and **BA[2:0] = 1**												
		2	8-11	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 2**												
		3	12-15	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 3**												
		4	16-19	repeat Sub-Loop 0, but **ODT = 0** and **BA[2:0] = 4**												
		5	20-23	repeat Sub-Loop 0, but **ODT = 0** and **BA[2:0] = 5**												
		6	24-27	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 6**												
		7	28-31	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 7**												

1. DM must be driven LOW all the time. DQS, DQS_n are MID-LEVEL.
2. DQ signals are MID-LEVEL.

Table 20 — IDD4R and IDDQ4R measurement-Loop pattern[1], 4H Stacking as Example

CK_t, CK_c	CKE	Sub-Loop	Rank-Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	0	RD	1110	1	0	1	0	0	00	0	0	0	0	00000000
				1	D	1111	0	0	0	0	0	00	0	0	0	0	-
				2, 3	D#,D#	1111	1	1	1	0	0	00	0	0	0	0	-
				4	RD	1110	1	0	1	0	0	00	0	0	F	0	00110011
				5	D	1111	0	0	0	0	0	00	0	0	F	0	-
				6, 7	D#,D#	1111	1	1	1	0	0	00	0	0	F	0	-
			1	8-15	repeat Rank-Loop 0, use **CS[3:0]_n = 1101** instead for RD command												
			2	16-23	repeat Rank-Loop 0, use **CS[3:0]_n = 1011** instead for RD command												
			3	24-31	repeat Rank-Loop 0, use **CS[3:0]_n = 0111** instead for RD command												
		1		32-63	repeat Sub-Loop 0, but **BA[2:0] = 1**												
		2		64-95	repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3		96-127	repeat Sub-Loop 0, but **BA[2:0] = 3**												
		4		128-159	repeat Sub-Loop 0, but **BA[2:0] = 4**												
		5		160-191	repeat Sub-Loop 0, but **BA[2:0] = 5**												
		6		192-223	repeat Sub-Loop 0, but **BA[2:0] = 6**												
		7		224-255	repeat Sub-Loop 0, but **BA[2:0] = 7**												

1. DM must be driven LOW all the time. DQS, DQS_n are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

2H and 8H stacking IDD4R measurement loop pattern will be similar to the 4H stacking measurement loop pattern in Table 20, but with the logical rank select signal setting CS[3:0] and CID to be consistent with 3DS spec definition.

Table 21 — IDD4W measurement-Loop pattern[1], 4H Stacking as Example

CK_t, CK_c	CKE	Sub-Loop	Rank-Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	0	WR	1110	1	0	0	1	0	00	0	0	0	0	00000000
				1	D	1111	0	0	0	1	0	00	0	0	0	0	-
				2, 3	D#, D#	1111	1	1	1	1	0	00	0	0	0	0	-
				4	WR	1110	1	0	0	1	0	00	0	0	F	0	00110011
				5	D	1111	0	0	0	1	0	00	0	0	F	0	-
				6, 7	D#, D#	1111	1	1	1	1	0	00	0	0	F	0	-
			1	8-15	repeat Rank-Loop 0, use **CS[3:0]_n = 1101** instead for WR command												
			2	16-23	repeat Rank-Loop 0, use **CS[3:0]_n = 1011** instead for WR command												
			3	24-31	repeat Rank-Loop 0, use **CS[3:0]_n = 0111** instead for WR command												
		1		8-15	repeat Sub-Loop 0, but **BA[2:0] = 1**												
		2		16-23	repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3		24-31	repeat Sub-Loop 0, but **BA[2:0] = 3**												
		4		32-39	repeat Sub-Loop 0, but **BA[2:0] = 4**												
		5		40-47	repeat Sub-Loop 0, but **BA[2:0] = 5**												
		6		48-55	repeat Sub-Loop 0, but **BA[2:0] = 6**												
		7		56-63	repeat Sub-Loop 0, but **BA[2:0] = 7**												

1. DM must be driven LOW all the time. DQS, DQS_n are used according to WR Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

2H and 8H stacking IDD4W measurement loop pattern will be similar to the 4H stacking measurement loop pattern in Table 21, but with the logical rank select signal setting CS[3:0] and CID to be consistent with 3DS spec definition.

Table 22 — IDD5B1 measurement-Loop pattern[1], 4H Stacking as Example

CK_t, CK_c	CKE	Rank-Loop	Sub-Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data [2]
toggling	Static High	0	0	0	**REF**	1110	0	0	1	0	**0**	0	0	0	**0**	0	-
			1	1, 2	D, D	1111	0	0	0	0	0	00	0	0	0	0	-
				3, 4	D#, D#	1111	1	1	1	0	0	00	0	0	F	0	-
				5...8	repeat cycles 1...4, but **BA[2:0] = 1**												
				9...12	repeat cycles 1...4, but **BA[2:0] = 2**												
				13...16	repeat cycles 1...4, but **BA[2:0] = 3**												
				17...20	repeat cycles 1...4, but **BA[2:0] = 4**												
				21...24	repeat cycles 1...4, but **BA[2:0] = 5**												
				25...28	repeat cycles 1...4, but **BA[2:0] = 6**												
				29...32	repeat cycles 1...4, but **BA[2:0] = 7**												
			2	33 ...	**Repeat Sub-Loop 1, until n**RFC_dlr - 1. Truncate, if necessary.												
		1		nRFC_dlr … 2*nRFC_dlr - 1	**Repeat Rank-Loop 0, use CS[3:0]_n = 1101 instead for REF command**												
		2		2*nRFC_dlr … 3*nRFC_dlr- 1	**Repeat Rank-Loop 0, use CS[3:0]_n = 1011 instead for REF command**												
		3		3*nRFC_dlr… 4*nRFC_dlr - 1	**Repeat Rank-Loop 0, use CS[3:0]_n = 0111 instead for REF command**												

1. DM must be driven Low all the time. DQS, DQS_n are MID-LEVEL.
2. DQ signals are MID-LEVEL.

2H and 8H stacking IDD5B1 measurement loop pattern will be similar to the 4H stacking measurement loop pattern in Table 22, but with the logical rank select signal setting CS[3:0] and CID to be consistent with 3DS spec definition.

Table 23 — IDD5B2 measurement-Loop pattern[1], 4H Stacking as Example

CK_t, CK_c	CKE	Rank-Loop	Sub-Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	0	**REF**	1110	0	0	1	0	**0**	0	0	0	**0**	0	-
			1	1, 2	D, D	1111	0	0	0	0	0	00	0	0	0	0	-
				3, 4	D#, D#	1111	1	1	1	0	0	00	0	0	F	0	-
				5...8	repeat cycles 1...4, but **BA[2:0] = 1**												
				9...12	repeat cycles 1...4, but **BA[2:0] = 2**												
				13...16	repeat cycles 1...4, but **BA[2:0] = 3**												
				17...20	repeat cycles 1...4, but **BA[2:0] = 4**												
				21...24	repeat cycles 1...4, but **BA[2:0] = 5**												
				25...28	repeat cycles 1...4, but **BA[2:0] = 6**												
				29...32	repeat cycles 1...4, but **BA[2:0] = 7**												
			2	33 ... nRFC_slr - 1	**Repeat Sub-Loop 1, until n**RFC_slr- 1. Truncate, if necessary.												
		1		nRFC_slr … 2*nRFC_slr - 1	**Repeat Rank-Loop 0, use CS[3:0]_n = 1101 instead for REF command**												
		2		2*nRFC_slr … 3*nRFC_slr- 1	**Repeat Rank-Loop 0, use CS[3:0]_n = 1011 instead for REF command**												
		3		3*nRFC_slr… 4*nRFC_slr - 1	**Repeat Rank-Loop 0, use CS[3:0]_n = 0111 instead for REF command**												

1. DM must be driven Low all the time. DQS, DQS_n are MID-LEVEL.
2. DQ signals are MID-LEVEL.

2H and 8H stacking IDD5B2 measurement loop pattern will be similar to the 4H stacking measurement loop pattern in Table 23, but with the logical rank select signal setting CS[3:0] and CID to be consistent with 3DS spec definition.

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9.

Table 24 — IDD7 measurement – Loop pattern

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[1]
toggling	Static High	0	0	ACT	1110	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	1110	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1111	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD_slr - 1												
		1	nRRD_slr	ACT	1110	0	1	1	0	1	00	0	0	F	0	-
			nRRD_slr + 1	RDA	1110	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD_slr + 2	D	1111	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2 * nRRD_slr -1												
		2	2 * nRRD_slr	repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3	3 * nRRD_slr	repeat Sub-Loop 1, but **BA[2:0] = 3**												
		4	4 * nRRD_slr	D	1111	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW_slr - 1, if necessary												
		5	nFAW_slr	repeat Sub-Loop 0, but **BA[2:0] = 4**												
		6	nFAW_slr+nRRD_slr	repeat Sub-Loop 1, but **BA[2:0] = 5**												
		7	nFAW_slr+2*nRRD_slr	repeat Sub-Loop 0, but **BA[2:0] = 6**												
		8	nFAW_slr+3*nRRD_slr	repeat Sub-Loop 1, but **BA[2:0] = 7**												
		9	nFAW_slr+4*nRRD_slr	D	1111	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2 * nFAW_slr - 1, if necessary												
		10	2*nFAW_slr+0	ACT	1110	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW_slr+1	RDA	1110	1	0	1	0	0	00	1	0	F	0	00110011
			2*nFAW_slr+2	D	1111	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2 * nFAW_slr + nRRD_slr - 1												

Table 24 — IDD7 measurement – Loop pattern (Continued)

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS[3:0]_n	RAS_n	CAS_n	WE_n	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[1]
toggling	Static High	11	2*nFAW_slr +nRRD_slr	ACT	1110	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW_slr +nRRD_slr+1	RDA	1110	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW_slr +nRRD_slr+2	D	1111	0	0	0	0	1	00	0	0	0	0	-
				repeat above D Command until 2 * nFAW_slr + 2 * nRRD_slr -1												
		12	2*nFAW_slr +2*nRRD_slr	repeat Sub-Loop 10, but **BA[2:0] = 2**												
		13	2*nFAW_slr +3*nRRD_slr	repeat Sub-Loop 11, but **BA[2:0] = 3**												
		14	2*nFAW_slr +4*nRRD_slr	D	1111	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3 * nFAW_slr - 1, if necessary												
		15	3*nFAW_slr	repeat Sub-Loop 10, but **BA[2:0] = 4**												
		16	3*nFAW_slr +nRRD_slr	repeat Sub-Loop 11, but **BA[2:0] = 5**												
		17	3*nFAW_slr +2*nRRD_slr	repeat Sub-Loop 10, but **BA[2:0] = 6**												
		18	3*nFAW_slr +3*nRRD_slr	repeat Sub-Loop 11, but **BA[2:0] = 7**												
		19	3*nFAW_slr +4*nRRD_slr	D	1111	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4 * nFAW - 1, if necessary												

1. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

10.2 IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

Table 25 — Specification Example 4Gbit DDR3-3DS

Speed Grade Bin	DDR3 - 800 7-6-6	DDR3 - 1066 9-7-7	DDR3 - 1333 11-9-9	DDR3 - 1600 13-11-11	DDR3 - 1866 15-13-13	Unit	Notes
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}						mA	x4/x8
I_{DD1}						mA	x4/x8
I_{DD2P} (0) slow exit						mA	x4/x8
I_{DD2P} (1) fast exit						mA	x4/x8
I_{DD2N}						mA	x4/x8
I_{DD2NT}						mA	x4/x8
I_{DDQ2NT} (Optional)						mA	x4/x8
I_{DD2Q}						mA	x4/x8
I_{DD3P} (fast exit)						mA	x4/x8
I_{DD3N}						mA	x4/x8
I_{DD4R}						mA	x4
						mA	x8
I_{DDQ4R} (Optional)						mA	x4
						mA	x8
I_{DD4W}						mA	x4
						mA	x8
I_{DD5B1}						mA	x4/x8
I_{DD5B2}						mA	x4/x8
I_{DD6}						mA	Refer to Table 26
I_{DD6ET}[1]						mA	
I_{DD6TC1}						mA	
I_{DD7}						mA	x4/x8

1. Users should refer to the SDRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 3D Stacked SDRAM devices support the following options or requirements referred to in this material.

Table 26 — I_{DD6} Specification[1] [2]

Symbol	Temperature Range	Value	Unit	Notes
I_{DD6}	0 - 85 °C		mA	3 4
I_{DD6ET}	0 - 95 °C		mA	5 6
I_{DD6TC}	0 °C ~ T_a		mA	6 7 8
	T_b ~ T_y		mA	6 7 8
	T_z ~ $T_{OPERmax}$		mA	6 7 8

1. Some I_{DD} currents are higher for x16 organization due to larger page-size architecture.
2. Max. values for I_{DD} currents considering worst case conditions of process, temperature and voltage.
3. Applicable for MR2 settings A6=0 and A7=0.
4. Supplier data sheets include a max value for I_{DD6}.
5. Applicable for MR2 settings A6=0 and A7=1. I_{DD6ET} is only specified for devices which support the Extended Temperature Range feature.
6. Refer to the supplier data sheet for the value specification method (e.g. max, typical) for I_{DD6ET} and I_{DD6TC}
7. Applicable for MR2 settings A6=1 and A7=0. I_{DD6TC} is only specified for devices which support the Auto Self Refresh feature.
8. The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of T_{OPER}. Refer to supplier data sheet for more information.

11 Input/Output Capacitance

No changes from JESD79-3.

12 Electrical Characteristics & AC Timings for DDR3-3DS-800 to DDR-3DS-1866

12.1 Clock Specification

No changes from JESD79-3.

12.2 Refresh parameters by logical rank density

Table 27 — Refresh parameters by logical rank density

Parameter	Symbol		Logical Rank Density			Units	Note
			2Gb	4Gb	8Gb		
REF command to ACT or REF command time to same logical rank	tRFC_slr		160	260	350	ns	
REF command to REF command to different logical rank	tRFC_dlr		60	90	120	ns	
Average periodic refresh interval in same logical rank	tREFI_slr	$0\ ^oC \leq T_{CASE} \leq 85\ ^oC$	7.8	7.8	7.8	us	
		$85\ ^oC < T_{CASE} \leq 95\ ^oC$	3.9	3.9	3.9	us	1

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

12.3 Standard 3DS Speed Bins

DDR3 3D Stacked SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

Table 28 — DDR3-800 3D Stacked Speed Bins and Operating Conditions

For specific Notes See “Speed Bin Table Notes” on page 61.						
Speed Bin			**DDR3-800E-3DS1A**		**Unit**	**Notes**
CL - nRCD - nRP			**7-6-6**			
Parameter		**Symbol**	**min**	**max**		
Internal read command to first data		t_{AA}	17.5	26.4	ns	
ACT to internal read or write delay time		t_{RCD}	15.0	—	ns	
PRE command period		t_{RP}	15.0	—	ns	
ACT to ACT or REF command period		t_{RC}	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9*tREFI_slr	ns	
CL= 6, nRCD=5, nRP=5 (667Mbps function)	CWL= 5	$t_{CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 10
CL=7, nRCD=6, nRP=6 (DDR3-800E-3DS1A)	CWL= 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 12
Supported CL Settings			6, 7		n_{CK}	
Supported nRCD Timings minimum			5		n_{CK}	16
Supported nRP Timings minimum			5		n_{CK}	17
Supported CWL Settings			5		n_{CK}	

Table 29 — DDR3-1066 3D Stacked Speed Bins and Operating Conditions

For specific Notes See "Speed Bin Table Notes" on page 61.													
Speed Bin			**DDR3-1066F-3DS1A (Optional)**		**DDR3-1066F-3DS1B (Optional)**		**DDR3-1066F-3DS2A**		**DDR3-1066G-3DS1A (Optional)**		**Unit**	**Notes**
CL - nRCD - nRP			**8-7-7**		**8-8-7**		**9-7-7**		**9-8-8**			
Parameter		**Symbol**	**min**	**max**	**min**	**max**	**min**	**max**	**min**	**max**		
Internal read command to first data		t_{AA}	15	26.4	15	26.4	16.875	26.4	16.875	26.4	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	—	15	—	13.125	—	15	—	ns	
PRE command period		t_{RP}	13.125	—	13.125	—	13.125	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	50.625	—	50.625	—	50.625	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9*tREFI_slr	37.5	9*tREFI_slr	37.5	9*tREFI_slr	37.5	9*tREFI_slr	ns	
CL= 6, nRCD=5, nRP=5 (667Mbps function)	CWL= 5	$t_{CK(AVG)}$	3.0	3.3	Reserved		Reserved		3.0	3.3	ns	1, 2, 3, 4 6, 10
CL= 7, nRCD=6, nRP=6 (DDR3-800E-3DS1A)	CWL= 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		2.5	3.3	2.5	3.3	ns	1, 2, 3, 4, 6, 12
CL= 7, nRCD=7, nRP=6	CWL= 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1, 2, 3, 6, 12
CL= 8, nRCD=7, nRP=7 (DDR3-1006F-3DS1A)	CWL= 6	$t_{CK(AVG)}$	1.875	<2.5	Reserved		Reserved		Reserved		ns	1, 2, 3, 4
CL= 8, nRCD=8, nRP=7 (DDR3-1066F-3DS1B)	CWL= 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1, 2, 3, 4
CL= 9, nRCD=7, nRP=7 (DDR3-1066F-3DS2A)	CWL= 6	$t_{CK(AVG)}$	1.875	<2.5	Reserved		1.875	<2.5	Reserved		ns	1, 2, 3, 4
CL= 9, nRCD=8, nRP=8 (DDR3-1066G-3DS1A)	CWL= 6	$t_{CK(AVG)}$	1.875	<2.5	Reserved		1.875	<2.5	1.875	<2.5	ns	1, 2, 3, 4
Supported CL Settings			6, 7, 8, 9		7, 8		7, 9		6, 7, 9		n_{CK}	
Supported nRCD Timings minimum			5		7		6		5		n_{CK}	16
Supported nRP Timings minimum			5		6		6		5		n_{CK}	17
Supported CWL Settings			5, 6		5, 6		5, 6		5, 6		n_{CK}	

Table 30 — DDR3-1333 3D Stacked Speed Bins and Operating Conditions

For specific Notes See "Speed Bin Table Notes" on page 61.													
Speed Bin			**DDR3-1333H-3DS1A (optional)**		**DDR3-1333H-3DS1B (optional)**		**DDR3-1333H-3DS2A**		**DDR3-1333J-3DS1A (optional)**		**Unit**	**Notes**
CL - nRCD - nRP									**11-10-10**			
Parameter		**Symbol**	**10-9-9**		**10-10-9**		**11-9-9**		**min**	**max**		
Internal read command to first data		t_{AA}	15	26.4	15	26.4	16.5	26.4	16.5	26.4	ns	
ACT to internal read or write delay time		t_{RCD}	13.5	—	15	—	13.5	—	15	—	ns	
PRE command period		t_{RP}	13.5	—	13.5 (13.125) (optional)	—	13.5	—	15	—	ns	13
ACT to ACT or REF command period		t_{RC}	51	—	51 (50.625) (optional)	—	51	—	52.5	—	ns	13
ACT to PRE command period		t_{RAS}	37.5	9*tREFI_slr	37.5	9*tREFI_slr	37.5	9*tREFI_slr	37.5	9*tREFI_slr	ns	
CL = 6, nRCD=5, nRP=5 (667Mbps function)	CWL=5	$t_{CK(AVG)}$	3.0	3.3	Reserved		Reserved		3.0	3.3	ns	1, 2, 3, 4, 7, 10
CL = 7, nRCD=6, nRP=6 (DDR3-800E-3DS1A)	CWL=5	$t_{CK(AVG)}$	2.5	3.3	Reserved		2.5	3.3	2.5	3.3	ns	1, 2, 3, 4, 7, 12
CL = 7, nRCD=7, nRP=6	CWL=5	$t_{CK(AVG)}$	Reserved		2.5	3.3	2.5	3.3	2.5	3.3	ns	1, 2, 3, 4 7, 12
CL= 8, nRCD=8, nRP=7 (DDR3-1066F-3DS1B)	CWL=6	$t_{CK(AVG)}$	Reserved		(1.875) (optional)	(< 2.5)	Reserved		Reserved		ns	1, 2, 3, 4, 7, 13
CL = 9, nRCD=8, nRP=8 (DDR3-1066G-3DS1A)	CWL=6	$t_{CK(AVG)}$	1.875	<2.5.	Reserved		1.875	<2.5.	1.875	<2.5.	ns	1, 2, 3, 4, 7
CL=10, nRCD=9, nRP=9 (DDR3-1333H-3DS1A)	CWL=7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		Reserved		Reserved		ns	1, 2, 3, 4
CL=10, nRCD=10, nRP=9 (DDR3-1333H-3DS1B)	CWL=7	$t_{CK(AVG)}$	1.5	< 1.875	1.5	< 1.875	Reserved		Reserved		ns	1,,2, 3, 4
CL=11, nRCD=9, nRP=9 (DDR3-1333H-3DS2A)	CWL=7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		1.5	< 1.875	Reserved		ns	1, 2, 3, 4
CL=11, nRCD=10, nRP=10 (DDR3-1333J-3DS1A)	CWL=7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		1.5	<1.875	1.5	<1.875	ns	1, 2, 3, 4
Supported CL Settings			6, 7, 9, 10, 11		7, 8, 10		7, 9, 11		6, 7, 9, 11		n_{CK}	
Supported nRCD Timings minimum			5		7		6		5		n_{CK}	16
Supported nRP Timings minimum			5		6		6		5		n_{CK}	17
Supported CWL Settings			5, 6, 7		5, 6, 7		5, 6, 7		5, 6, 7		n_{CK}	

Table 31 — DDR3-1600 3DS Speed Bins and Operating Conditions

For specific Notes See "Speed Bin Table Notes" on page 61..											
Speed Bin			**DDR3-1600K-3DS1A (optional)**		**DDR3-1600K-3DS1B (optional)**		**DDR3-1600K-3DS2A**		**Unit**	**Note**
CL - nRCD - nRP			**12-11-11**		**12-12-11**		**13-11-11**			
Parameter		**Symbol**	**min**	**max**	**min**	**max**	**min**	**max**		
Internal read command to first data		t_{AA}	15	26.4	15	26.4	16.25	26.4	ns	
ACT to internal read or write delay time		t_{RCD}	13.75	—	15	—	13.75	—	ns	
PRE command period		t_{RP}	13.75	—	13.75 (13.125) (13.5) (optional)	—	13.75	—	ns	13, 14
ACT to ACT or REF command period		t_{RC}	48.75	—	48.75 (48.125) (48.5) (optional)	—	48.75	—	ns	13, 14
ACT to PRE command period		t_{RAS}	35	9*tREFI_slr	35	9*tREFI_slr	35	9*tREFI_slr	ns	
CL = 6, nRCD=5, nRP=5 (667 Mbps function)	CWL=5	$t_{CK(AVG)}$	3.0	3.3	Reserved		Reserved		ns	1, 2, 3, 4, 10
CL = 7, nRCD=6, nRP=6 (DDR3-800E-3DS1A)	CWL=5	$t_{CK(AVG)}$	2.5	3.3	Reserved		2.5	3.3	ns	1, 2, 3, 4, 8, 12
CL = 7, nRCD=7, nRP=6	CWL=5	$t_{CK(AVG)}$	Reserved		2.5	3.3	2.5	3.3	ns	1, 2, 3, 4, 8, 12
CL= 8, nRCD=8, nRP=7 (DDR3-1066F-3DS1B)	CWL=6	$t_{CK(AVG)}$	Reserved		(1.875) (optional)	(< 2.5)	Reserved		ns	1, 2, 3, 4, 8, 13
CL = 9, nRCD=8, nRP=8 (DDR3-1066G-3DS1A)	CWL=6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		1.875	< 2.5	ns	1, 2, 3, 4, 8,
CL=10, nRCD=10, nRP=9 (DDR3-1333H-3DS1B)	CWL=7	$t_{CK(AVG)}$	Reserved		(1.5) (optional)	(< 1.875)	Reserved		ns	1, 2, 3, 4, 8, 14
CL=11, nRCD=10, nRP=10 (DDR3-1333J-3DS1A)	CWL=7	$t_{CK(AVG)}$	1.5	< 1.875	Reserved		1.5	< 1.875	ns	1, 2, 3, 4, 8
CL=12, nRCD=11, nRP=11 (DDR3-1600K-3DS1A)	CWL=8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		Reserved		ns	1, 2, 3, 4
CL=12, nRCD=12, nRP=11 (DDR3-1600K-3DS1B)	CWL=8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	Reserved		ns	1, 2, 3, 4
CL=13, nRCD=11, nRP=11 (DDR3-1600K-3DS2A)	CWL=8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		1.25	< 1.5	ns	1, 2, 3, 4
Supported CL Settings			6, 7, 9, 11, 12, 13		7, 8, 10, 12		7, 9, 11, 13		n_{CK}	
Supported nRCD Timings minimum			5		7		6		n_{CK}	16
Supported nRP Timings minimum			5		6		6		n_{CK}	17
Supported CWL Settings			5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		n_{CK}	

Table 32 — DDR3-1866 3DS Speed Bins and Operating Conditions

For specific Notes See "Speed Bin Table Notes" on page 61..									
Speed Bin			**DDR3-1866M-3DS1B (optional)**		**DDR3-1866M-3DS2A**		**Unit**	**Note**
CL - nRCD - nRP			**14-14-13**		**15-13-13**			
Internal read command to first data		tAA	15	26.4	16.06	26.4	ns	
ACT to internal read or write delay time		tRCD	15	—	13.91	—	ns	
PRE command period		tRP	13.91 (13.125) (13.5) (13.75) (optional)	—	13.91 (13.75) (optional)	—	ns	13, 14, 15
ACT to ACT or REF command period		tRC	47.91 (47.125) (47.5) (47.75) (optional)	—	47.91 (47.75) (optional)	—	ns	13, 14, 15
ACT to PRE command period		tRAS	34	9*tREFI_slr	34	9*tREFI_slr	ns	
CL= 7, nRCD=6, nRP=6 (DDR3-800E-3DS1A)	CWL=5	$t_{CK(AVG)}$	Reserved		2.5	3.3	ns	1, 2, 3, 9, 12
CL= 7, nRCD=7, nRP=6	CWL=5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1, 2, 3, 9, 12
CL= 8, nRCD=8, nRP=7 (DDR3-1066F-3DS1B)	CWL=6	$t_{CK(AVG)}$	(1.875) (optional)	(< 2.5) (optional)	Reserved		ns	1, 2, 3, 4, 9, 13
CL= 9, nRCD=8, nRP=8 (DDR3-1066G-3DS1A)	CWL=6	$t_{CK(AVG)}$	Reserved		1.875	< 2.5	ns	1, 2, 3, 4, 9
CL=10, nRCD=10, nRP=9 (DDR3-1333H-3DS1B)	CWL=7	$t_{CK(AVG)}$	(1.5) (optional)	(< 1.875) (optional)	Reserved		ns	1, 2, 3, 4, 9, 14
CL=11, nRCD=10, nRP=10 (DDR3-1333J-3DS1A)	CWL=7	$t_{CK(AVG)}$	Reserved		1.5	<1.875	ns	1, 2, 3, 4, 9
CL=12, nRCD=12, nRP=11 (DDR3-1600K-3DS1B)	CWL=8	$t_{CK(AVG)}$	(1.25) (optional)	(< 1.5) (optional)	Reserved		ns	1, 2, 3, 4, 5, 9, 15
CL=13, nRCD=11, nRP=11 (DDR3-1600K-3DS2A)	CWL=8	$t_{CK(AVG)}$	Reserved		(1.25) (optional)	(< 1.5) (optional)	ns	1, 2, 3, 4, 5, 9, 15
CL=14, nRCD=14, nRP=13 (DDR3-1866M-3DS1B)	CWL=9	$t_{CK(AVG)}$	1.071	<1.25	Reserved		ns	1, 2, 3, 4
CL=15, nRCD=13, nRP=13 (DDR3-1866M-3DS2A)	CWL=9	$t_{CK(AVG)}$	Reserved		1.071	<1.25	ns	1, 2, 3, 4
Supported CL Settings			7, 8, 10, 12, 14		7, 9, 11, 13, 15		n_{CK}	
Supported nRCD Timings minimum			7		6		n_{CK}	16
Supported nRP Timings minimum			6		6		n_{CK}	17
Supported CWL Settings			5, 6, 7, 8, 9		5, 6, 7, 8, 9		n_{CK}	

12.3.1 Speed Bin Table Notes

NOTE 1.The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

NOTE 2.tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, 1.25 or 1.071 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 6 calculation.

NOTE 3.tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.5 nsor 1.25 ns or 1.071 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.

NOTE 4.'Reserved' settings are not allowed. User must program a different value.

NOTE 5.'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

NOTE 6.Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 7.Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 8.Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 9.Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 10.DDR3 800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.

NOTE 11. For devices supporting optional speed bin, Additive Latency (AL) of CL-3 is supported only when CL > nRCD.

NOTE 12. Common CAS latency is 7 at 800MT/s or below.

NOTE 13. For devices supporting optional down binning nRP=7, tRPmin must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1866M-3DS1B devices supporting down binning to DDR3-1066F-3DS1B must be programmed 13.125ns in SPD bytes for tRPmin (byte 20). Once tRP (byte 20) is programmed to 13.125ns, tRCmin (bytes 21, 23) also must be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34ns + 13.125ns)

NOTE 14. For devices supporting optional down binning nRP=9, tRPmin must be 13.5ns. SPD setting must be programmed to match. For example, DDR3-1866M-3DS1B devices supporting down binning to DDR3-1333H-3DS1B must be programmed 13.5ns in SPD bytes for tRPmin (byte 20). Once tRP (byte 20) is programmed to 13.5ns, tRCmin (bytes 21, 23) also must be programmed accordingly. For example,

47.5ns (tRASmin + tRPmin = 34ns + 13.5ns)

NOTE 15. For devices supporting optional down binning nRP=11, tRPmin must be 13.75ns. SPD setting must be programmed to match. For example, DDR3-1866M-3DS1B devices supporting down binning to DDR3-1600K-3DS1B must be programmed 13.75ns in SPD bytes for tRPmin (byte 20). Once tRP (byte 20) is programmed to 13.75ns, tRCmin (bytes 21, 23) also must be programmed accordingly. For example, 47.75ns (tRASmin + tRPmin = 34ns + 13.75ns)

NOTE 16. Any integer which is equal to or larger than supported minimum value of nRCD is available as long as tRCDmin and other parameters are satisfied.

NOTE 17. Any integer which is equal to or larger than supported minimum value of nRP is available as long as tRPmin and other parameters are satisfied.

13 Electrical Characteristics and AC Timings

Table 33 — Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800-3DS		DDR3-1066-3DS		DDR3-1333-3DS		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row Active to Row Active Delay									
ACTIVE to ACTIVE command period to different banks in the same logical rank for 1KB page size	tRRD_slr	max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	ns	2
ACTIVE to ACTIVE command period to different banks in the same logical rank for 2KB page size	tRRD_slr	max(4nCK, 10ns)	-	max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-	ns	2 3
ACTIVE to ACTIVE command period to different logical ranks for 1KB page size	tRRD_dlr	4	-	4	-	4	-	nCK	2
ACTIVE to ACTIVE command period to different logical ranks for 2KB page size	tRRD_dlr	4	-	4	-	4	-	nCK	2 3
Four Active Window									
Four active window to the same logical rank for 1KB page size	tFAW_slr	40	-	37.5	-	30	-	ns	2
Four active window to the same logical rank for 2KB page size	tFAW_slr	50	-	50	-	45	-	ns	2 3
Four active window to different logical ranks for 1KB page size	tFAW_dlr	16	-	16	-	16	-	nCK	2
Four active window to different logical ranks for 2KB page size	tFAW_dlr	16	-	16	-	16	-	nCK	2 3
Self-Refresh Timings									
Exit Self-Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC_slr(min) + 10ns)		max(5nCK, tRFC_slr(min) + 10ns)		max(5nCK, tRFC_slr(min) + 10ns)			4

Table 33 — Timing Parameters by Speed Bin (Continued)[1]

Parameter	Symbol	DDR3-1600-3DS		DDR3-1866-3DS		Units	Notes
		Min	Max	Min	Max		
Row Active to Row Active Delay							
ACTIVE to ACTIVE command period to different banks in the same logical rank for 1KB page size	tRRD_slr	max(4nCK, 6ns)	-	max(4nCK, 5ns)	-	ns	2
ACTIVE to ACTIVE command period to different banks in the same logical rank for 2KB page size	tRRD_slr	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	ns	2 3
ACTIVE to ACTIVE command period to different logical ranks for 1KB page size	tRRD_dlr	4	-	4	-	nCK	2
ACTIVE to ACTIVE command period to different logical ranks for 2KB page size	tRRD_dlr	4	-	4	-	nCK	2 3
Four Active Window							
Four active window to the same logical rank for 1KB page size	tFAW_slr	30	-	27	-	ns	2
Four active window to the same logical rank for 2KB page size	tFAW_slr	40	-	35	-	ns	2 3
Four active window to different logical ranks for 1KB page size	tFAW_dlr	16	-	16	-	nCK	2
Four active window to different logical ranks for 2KB page size	tFAW_dlr	16	-	16	-	nCK	2 3
Self-Refresh Timings							
Exit Self-Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC_slr(min) + 10ns)		max(5nCK, tRFC_slr(min) + 10ns)			4

1. The general notes from JESD79-3, section 13.4 apply.
2. Please refer to Specific Note e of Jitter Notes in JESD79-3.
3. 8Gb logical rank density only
4. Upon exit from Self-Refresh, the 3D Stacked DDR3 SDRAM requires a minimum of one extra refresh command to all logical ranks before it is put back into Self-Refresh Mode.

Standard Improvement Form

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