JEDEC STANDARD

Driver Specifications for 1.8 V Power Supply Point-to-Point Drivers

JESD8-17

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DRIVER SPECIFICATIONS FOR 1.8 V POWER SUPPLY POINT-TO-POINT DRIVERS

From JEDEC Board Ballot JCB-20-106 and JCB-02-107, formulated under the guidance of JC-16 Committe on Interface Technology

1 Scope

This material is intended to be reflected in supplier specifications for point to point DDR devices ranging from 400 Mb/s to 800 Mb/s operation.

It is a method to specify driver impedance with something other than a number that does not necessarily define how it operates in a real net This standard addresses this issue using net lengths and specifies how much uncertainty can exist in the data for each speed supported.

The purpose of this standard is to provide a standard of specification for uniformity, multiplicity of sources, elimination of confusion and ease of device specification and design by users

2 Standard specifications

Table 1 identifies the driver specifications for 1.8 V point-to-point devices.

Table 1 — Driver specifications for 1.8V Point-to-Point devices

Nominal Data Rate	Net Length (Class-X/ Class-Y)	tAC Un-Terminated	tDQSQ Un-Terminated	Notes
400Mb/s	1250ps/833ps	tAC +/-150ps	tDQSQ +/-150ps	1,2,3,4,5
600Mb/s	833ps/556ps	tAC +/-125ps	tDQSQ +/-125ps	1,2,3,4,5
800Mb/s	625ps/417ps	tAC +/-100ps	tDQSQ +/-100ps	1,2,3,4,5

NOTE 1 A part may use either the tDQSQ method (strobe based) or the tAC method (clock based)

NOTE 2 This test is not meant to be a production test criteria.

NOTE 3 Each design can be simulated for how much tAC/tDQSQ should grow and each die revision can and should be characterized into test net structures (terminated and un-terminated)

NOTE 4 Only one DQ pin at a time is to be simulated/characterized (all other DQ's quiet).

NOTE 5 The growth in tAC (or tDQSQ) is on a per edge basis. The total growth of uncertainty in the data eye is the sum of both the plus and minus value.

3 Outline of jitter modulation test test method for point-to-point devices

- Attach a driver to an un-terminated transmission line, of 0.5X the resonance length for Class-X and 0.33X resonance length for Class-Y.
- Assert a constant frequency signal onto the line, consistent with data rate of the device.
- Measure jitter at far-end of the transmission line using input clock as reference (effectively tAC).

  NOTE Jitter is measured at Vddq/2 and not at crosspoint. The bit pattern in Figure 1 must be used.
- Next perform the same test but into a terminated transmission line.
- Compare the results of the two situations.

The standard specification is a limit on how much the tAC envelope can grow from the terminated case to the un-terminated case. Alternately, the growth in tDQSQ could be characterized instead of tAC. The un-terminated case is meant to represent real application conditions. The amount of growth can be simulated and characterized in this fashion and should be due only to net effects, driver characteristics, and inter-symbol interference.

Other DQ's	Data Pattern for DQ Under Test
000.....0	00000101010011001100110001110001110001110101

Figure 1 — Bit pattern

To eliminate system board effects, only one driver at a time is to be characterized in such a fashion. Since application requirements vary significantly, a target driver impedance and associated application range of net impedances must be chosen from the table below and identified with the component. More than one range can be supported through various means, but a minimum of one range must be supported.

3 Outline of jitter modulation test test method for point-to-point devices (cont'd)

Table 2 — Driver Impedance Values

Driver Impedance(s) Supported	Target Net Impedance	Net Impedance Range	Notes
30 ohms	30 ohms	27 - 33 ohms	1,2,3,4
40 ohms	40 ohms	36 - 44 ohms	1,2,3,4
50 ohms	50 ohms	45 - 55 ohms	1,2,3,4
60 ohms	60 ohms	54 - 66 ohms	1,2,3,4
80 ohms	80 ohms	72 - 88 ohms	1,2,3,4
"X" ohms	"X" ohms	X +/- 10% ohms	1,2,3,4

NOTE 1 A device compliant with the point to point specification must support at least one of the driver impedance values across its associated net impedance range.

NOTE 2 The device must support either class-X and class-Y net topologies (for class-X devices) or class-Y net topologies (for class-Y devices).

NOTE 3 Timing values are guaranteed by design and characterization against open-ended (no load) net structures. Performance in real applications will vary as a result of true loading conditions. Device verification against real application conditions is the responsibility of the consumer.

NOTE 4 A device may support more than one impedance value through the use of variable impedance (or impedance adjustment). However, such functionality is not required.

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Standard Improvement Form **JEDEC JESD8-17**

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1. I recommend changes to the following:

☐ Requirement, paragraph number _____

☐ Test method number _____ Paragraph number _____

The referenced paragraph number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

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