JEDEC STANDARD

HSUL_12 LPDDR2 and LPDDR3 I/O with Optional ODT

JESD8-22B

(Revision of JESD8-22A, October 2012)

APRIL 2014

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by

3103 North 10th Street

Suite 240 South

Arlington, VA 22201-2107

PRICE: Contact JEDEC

Printed in the U.S.A.

HSUL_12 LPDDR2 and LPDDR3 I/O with Optional ODT

(From JEDEC Board Ballot JCB-14-01, formulated uder the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the High Speed Unterminated Logic (HSUL_12) logic switching range, nominally 0 V to 1.2 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages.

1.1 Standard structure

The standard is defined in four clauses:

The first clause defines absolute maximum DC rating requirements common to all compliant ICs.

The second clause defines pertinent supply voltage requirements.

The third clause defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.

The fourth clause specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments.

Input parametric requirements and Output specifications are devided into two classes where necessary, Class I for LPDDR2, and Class II for LPDDR3 which operates at higer frequency than LPDDR2.

1.2 Rationale and assumptions

The HSUL_12 standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve the bus power consumption when operating at higher speed. This bus is mainly for point-to-point unterminated bus topology.

The standard defines both the ac and dc input signal values. Making this distinction is important for the design of the high gain, differential receivers that are required.The ac values indicate the voltage levels at which the receiver must meet its timing specifications.The dc values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the ac value, the receiver will change to the new logic state. The new logic state will then be maintained as long as the input stays beyond the dc threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform.

2 Absolute Maximum Ratings

2.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 1 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	1
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
NOTE 1 VREFDQ ≤ 0.6 x VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV. NOTE 2 VREFCA ≤ 0.6 x VDDCA; however, VREFCA may be ≥ VDDCA provided that VREFCA ≤ 300mV.					

3 AC & DC Operating Conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

3.1 Recommended DC Operating Conditions

Table 2 — Recommended HSUL_12 DC Operating Conditions

Symbol	Min	Typ	Max	DRAM	Unit
VDDCA	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	I/O Buffer Power	V

4 AC and DC Input Measurement Levels

4.1 AC and DC Logic Input Levels for Single-Ended Signals

4.1.1 AC and DC Input Levels for Single-Ended CA and CS_n Signals

Table 3 — Single-Ended AC and DC Input Levels for CA and CS_n Inputs, Class I

Symbol	Parameter	1066 to 466 Mbps		400 to 200 Mbps		Unit	Notes
		Min	Max	Min	Max		
V_{IHCA}(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1, 2
V_{IHCA}(DC)	DC input logic high	Vref + 0.130	VDDCA	Vref + 0.200	VDDCA	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	Vref - 0.130	VSSCA	Vref - 0.200	V	1
V_{RefCA}(DC)	Reference Voltage for CA and CS_n inputs	0.49 * VDDCA	0.51 * VDDCA	0.49 * VDDCA	0.51 * VDDCA	V	3, 4

NOTE 1 For CA and CS_n input only pins. Vref = VrefCA(DC).
NOTE 2 See 5.5, Overshoot and undershoot specifications
NOTE 3 The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
NOTE 4 For reference: approx. VDDCA/2 +/- 12 mV.

Table 4 — Single-Ended AC and DC Input Levels for CA and CS_n inputs, Class II

Symbol	Parameter	1333/1600		1866/2133		Unit	Notes
		Min	Max	Min	Max		
V_{IHCA}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V_{Ref} + 0.135	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	Note 2	V_{Ref} - 0.135	V	1, 2
V_{IHCA}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDCA}	V_{Ref} + 0.100	V_{DDCA}	V	1
V_{ILCA}(DC)	DC input logic low	V_{SSCA}	V_{Ref} - 0.100	V_{SSCA}	V_{Ref} - 0.100	V	1
V_{RefCA}(DC)	Reference Voltage for CA and CS_n inputs	0.49 * V_{DDCA}	0.51 * V_{DDCA}	0.49 * V_{DDCA}	0.51 * V_{DDCA}	V	3, 4

NOTE 1 For CA and CS_n input only pins. V_{Ref} = $V_{RefCA(DC)}$.
NOTE 2 See 5.5, Overshoot and undershoot specifications
NOTE 3 The ac peak noise on V_{RefCA} may not allow V_{RefCA} to deviate from $V_{RefCA(DC)}$ by more than +/-1% V_{DDCA} (for reference: approx. +/- 12 mV).
NOTE 4 For reference: approx. V_{DDCA}/2 +/- 12 mV.

4.1 AC and DC Logic Input Levels for Single-Ended Signals

4.1.2 AC and DC Input Levels for CKE

Table 5 — Single-Ended AC and DC Input Levels for CKE,Class I

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.8 * VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * VDDCA	V	1
NOTE 1 See 5.5, Overshoot and undershoot specifications					

Table 6 — Single-Ended AC and DC Input Levels for CKE,Class II

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.65 * VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.35 * VDDCA	V	1
NOTE 1 See 5.5, Overshoot and undershoot specifications					

4.1.3 AC and DC Input Levels for Single-Ended Data Signals

Table 7 — Single-Ended AC and DC Input Levels for DQ and DM,Class I

Symbol	Parameter	1066 to 466 Mbps		400 to 200 Mbps		Unit	Notes
		Min	Max	Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1, 2
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1, 2
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	Vref + 0.200	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref - 0.130	VSSQ	Vref - 0.200	V	1
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDDQ	0.51 * VDDQ	0.49 * VDDQ	0.51 * VDDQ	V	3, 4

NOTE 1 For DQ input only pins. Vref = VrefDQ(DC).
NOTE 2 See 5.5, Overshoot and undershoot specifications
NOTE 3 The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDDQ (for reference: approx. +/- 12 mV).
NOTE 4 For reference: approx. VDDQ/2 +/- 12 mV.

4.1 AC and DC Logic Input Levels for Single-Ended Signals (cont'd)

4.1.3 AC and DC Input Levels for Single-Ended Data Signals (cont'd)

Table 8 — Single-Ended AC and DC Input Levels for DQ and DM,Class II

Symbol	Parameter	1333/1600		1866/2133		Unit	Notes
		Min	Max	Min	Max		
V_{IHDQ}(AC)	AC input logic high	V_{Ref} + 0.150	Note 2	V_{Ref} + 0.135	Note 2	V	1, 2, 5
V_{ILDQ}(AC)	AC input logic low	Note 2	V_{Ref} - 0.150	Note 2	V_{Ref} - 0.135	V	1, 2, 5
V_{IHDQ}(DC)	DC input logic high	V_{Ref} + 0.100	V_{DDQ}	V_{Ref} + 0.100	V_{DDQ}	V	1
V_{ILDQ}(DC)	DC input logic low	V_{SSQ}	V_{Ref}- 0.100	V_{SSQ}	V_{Ref}- 0.100	V	1
$V_{RefDQ(DC)}$ (DQ ODT disabled)	Reference Voltage for DQ, DM inputs	0.49 * V_{DDQ}	0.51 * V_{DDQ}	0.49 * V_{DDQ}	0.51 * V_{DDQ}	V	3, 4
$V_{RefDQ(DC)}$ (DQ ODT enabled)	Reference Voltage for DQ, DM inputs	V_{ODTR}/2 - 0.01 * V_{DDQ}	V_{ODTR}/2 + 0.01 * V_{DDQ}	V_{ODTR}/2 - 0.01 * V_{DDQ}	V_{ODTR}/2 + 0.01 * V_{DDQ}	V	3, 5, 6

NOTE 1 For DQ input only pins. $V_{Ref} = V_{RefDQ(DC)}$.

NOTE 2 See 5.5, Overshoot and undershoot specifications

NOTE 3 The ac peak noise on V_{RefDQ} may not allow V_{RefDQ} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% V_{DDQ} (for reference: approx. +/- 12 mV).

NOTE 4 For reference: approx. V_{DDQ}/2 +/- 12 mV.

NOTE 5 For reference: approx. V_{ODTR}/2 +/- 12 mV.

NOTE 6 The nominal mode register programmed value for R_{ODT} and the nominal controller output impedance R_{ON} are used for the calculation of V_{ODTR}. For testing purposes a controller R_{ON} value of 50 W is used.

$$V_{ODTR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

4.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 1. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time.

(V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise). VDD stands for VDDCA for V_{RefCA} and VDDQ for V_{RefDQ}. $V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g., 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirements in Table 3, Table 4, Table 7, and Table 8. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref(DC)}$ by no more than +/- 1% VDD. Vref(t) cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.:

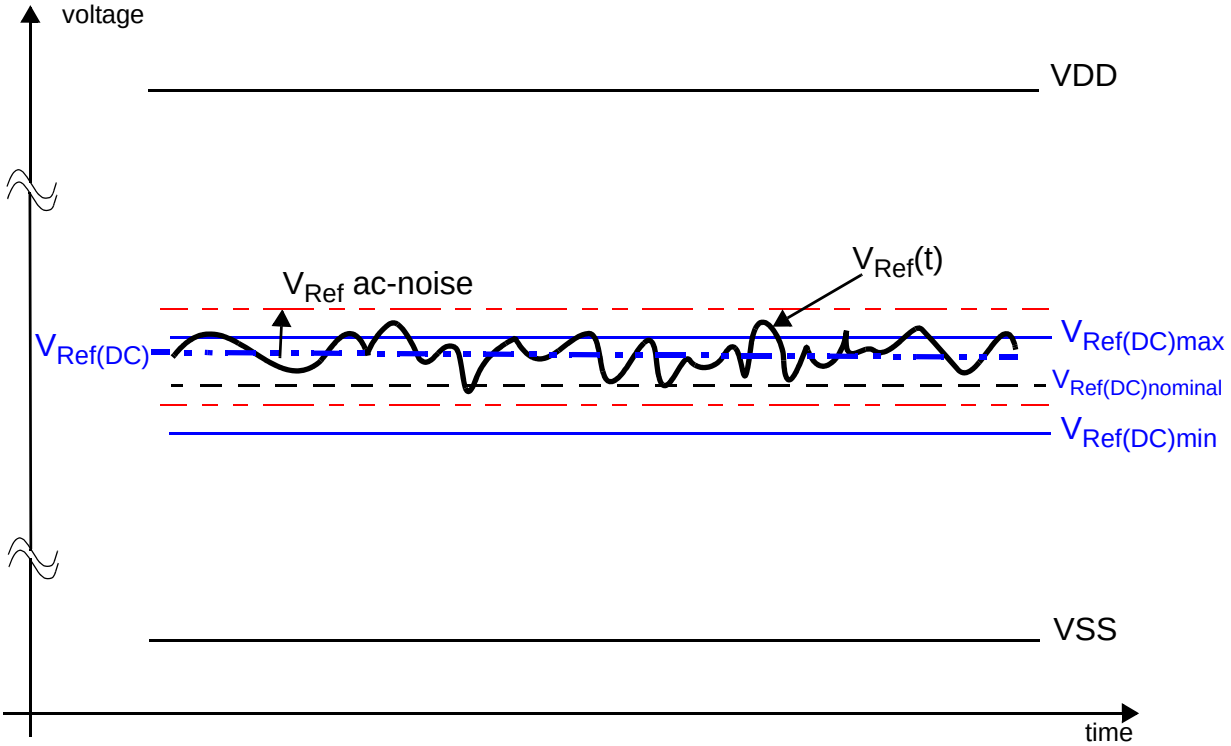


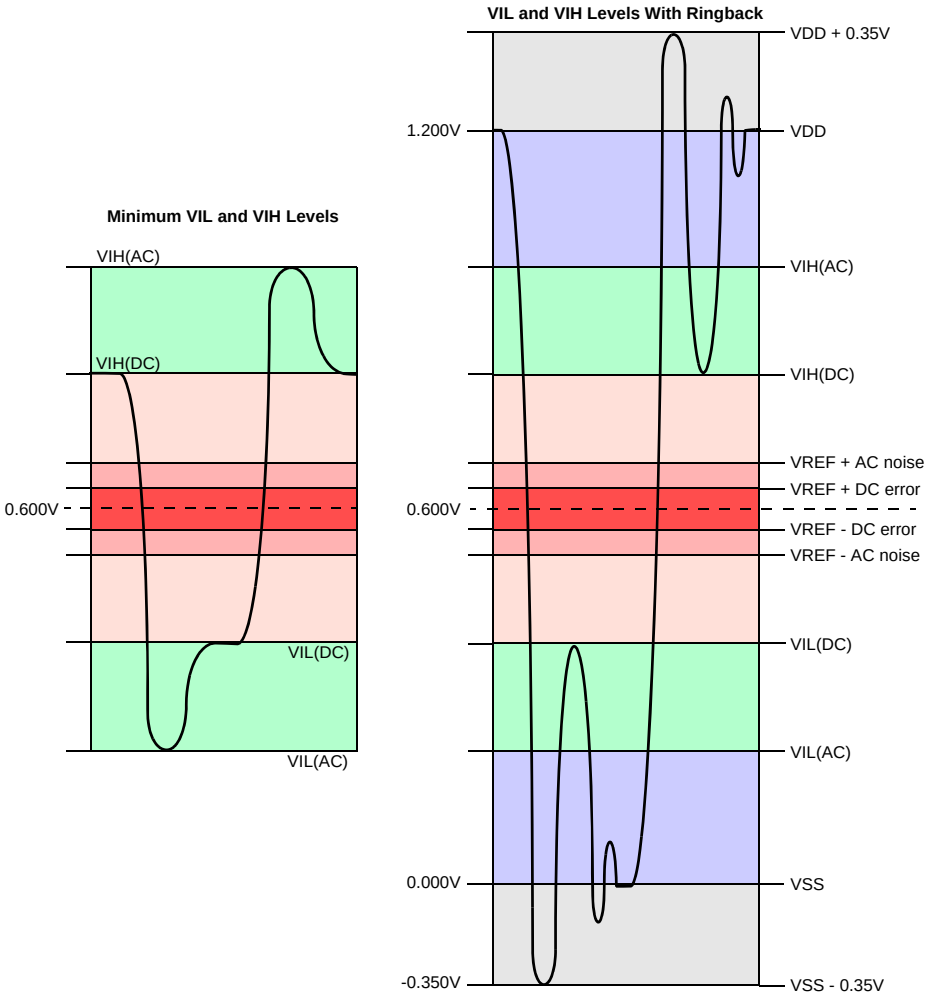
Figure 1 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{Ref}. "V_{Ref} " shall be understood as $V_{Ref(DC)}$, as defined in Figure 1.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF} deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the LPDDR2 and LPDDR3 setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/-1% of VDD) are included in LPDDR2 and LPDDR3 timings and their associated deratings.

4.3 Input Signal



NOTE 1 Numbers reflect nominal values.

NOTE 2 For CA0-9, CK_t, CK_c,and CS_n, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.

NOTE 3 For CA0-9, CK_t, CK_c, and CS_n, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands for VSSQ.

Figure 2 — Input Signal

4.4 AC and DC Logic Input Levels for Differential Signals

4.4.1 Differential signal definition

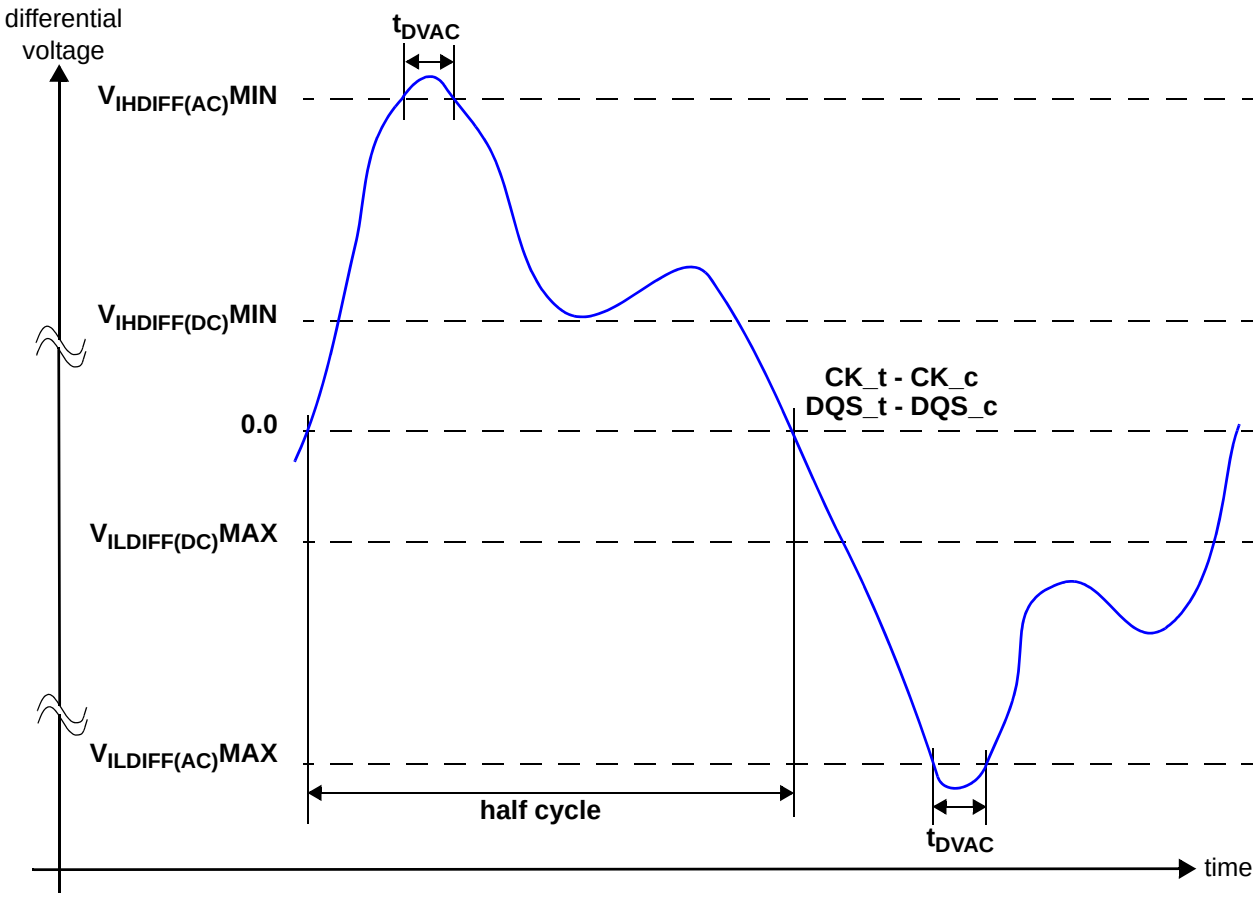


Figure 3 — Definition of differential ac-swing and "time above ac-level" t_{DVAC}

4.4 AC and DC Logic Input Levels for Differential Signals (cont'd)

4.4.2 Differential swing requirements for clock (CK_t-CK_c) and strobe (DQS_t-DQS_c)

Table 9 — Differential AC and DC Input Levels

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IHdiff(dc)}$	Differential input high	2 x (VIH(dc) - Vref)	note 3	V	1
$V_{ILdiff(dc)}$	Differential input logic low	Note 3	2 x (Vref - VIL(dc))	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	note 3	2 x (Vref - VIL(ac))	V	2

NOTE 1 Used to define a differential signal slew-rate.
NOTE 2 For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
NOTE 3 These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and undershoot specifications" on oage 20.
NOTE 4 For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

Table 10 — Allowed time before ringback (tDVAC) for CK_t-CK_c and DQS_t-DQS_c, Class

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 440mV	tDVAC [ps] @ |VIH/Ldiff(ac)| = 600mV
	min	min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

4.4 AC and DC Logic Input Levels for Differential Signals (cont'd)

4.4.2 Differential swing requirements for clock (CK_t - CK_c) and strobe (DQS_t - DQS_c)

Table 11 — Allowed time before ringback (tDVAC) for CK_t-CK_c and DQS_t-DQS_c, Class II

Slew Rate [V/ns]	t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 300mV 1333Mbps		t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 300mV 1600Mbps		t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 270mV 1866Mbps		t_{DVAC} [ps] @ $\|V_{IH/Ldiff(ac)}\|$ = 270mV 2133Mbps	
	min	max	min	max	min	max	min	max
> 8.0	58	-	48	-	40	-	34	-
8.0	58	-	48	-	40	-	34	-
7.0	56	-	46	-	39	-	33	-
6.0	53	-	43	-	36	-	30	-
5.0	50	-	40	-	33	-	27	-
4.0	45	-	35	-	29	-	23	-
3.0	37	-	27	-	21	-	15	-
< 3.0	37	-	27	-	21	-	15	-

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4.4 AC and DC Logic Input Levels for Differential Signals (cont'd)

4.4.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle.

DQS_t, DQS_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle preceeding and following a valid transition.

NOTE The applicable ac-levels for CA and DQ's are different per speed-bin.

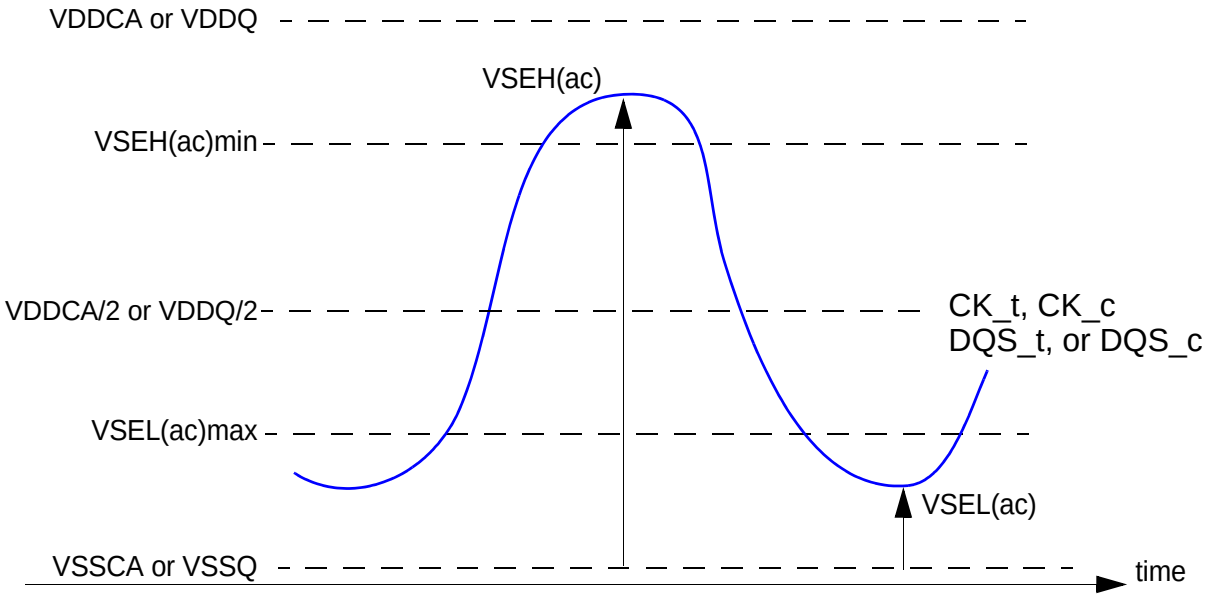


Figure 4 — Single-ended requirement for differential signals.

NOTE While CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS_t, DQS_c and VDDCA/2 for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(ac)max, VSEH(ac)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

The single ended requirements for CK_t, CK_c, DQS_t, and DQS_c are found in Table 3, Table 4, Table 7, and Table 8 respectively.

4.4 AC and DC Logic Input Levels for Differential Signals (cont'd)

4.4.3 Single-ended requirements for differential signals (cont'd)

Table 12 — Single-ended levels for CK_t, DQS_t, CK_c, DQS_c,Class I

Symbol	Parameter	1066 to 466 Mbps		400 to 200 Mbps		Unit
		Min	Max	Min	Max	
VSEH(AC)	Single-ended high-level for strobes	(VDDQ / 2) + 0.220	note 1	(VDDQ / 2) + 0.300	note 1	V
	Single-ended high-level for CK_t, CK_c	(VDDCA / 2) + 0.220	note 1	(VDDCA / 2) + 0.300	note 1	V
VSEL(AC)	Single-ended low-level for strobes	note 1	(VDDDQ / 2) - 0.220	note 1	(VDDQ / 2) - 0.300	V
	Single-ended low-level for CK_t, CK_c	note 1	(VDDCA / 2) - 0.220	note 1	(VDDCA / 2) - 0.300	V

NOTE 1 These values are not defined, ho\wever the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to 5.5, Overshoot and undershoot specifications.

Table 13 — Single-ended levels for CK_t,DQS_t,CK_c,DQS_c, Class II

Symbol	Parameter	Value		Unit	Notes
		Min	Max		
$V_{SEH(AC150)}$	Single-ended high-level for strobes	(V_{DDQ} / 2) + 0.150	note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	(V_{DDCA} / 2) + 0.150	note 3	V	1, 2
$V_{SEL(AC150)}$	Single-ended low-level for strobes	note 3	(V_{DDQ} / 2) - 0.150	V	1, 2
	Single-ended low-level for CK_t, CK_c	note 3	(V_{DDCA} / 2) - 0.150	V	1, 2
$V_{SEH(AC135)}$	Single-ended high-level for strobes	(V_{DDQ} / 2) + 0.135	note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	(V_{DDCA} / 2) + 0.135	note 3	V	1, 2
$V_{SEL(AC135)}$	Single-ended low-level for strobes	note 3	(V_{DDQ} / 2) - 0.135	V	1, 2
	Single-ended low-level for CK_t, CK_c	note 3	(V_{DDCA} / 2) - 0.135	V	1, 2

NOTE 1 For CK_t, CK_c use $V_{SEH}/V_{SEL(ac)}$ of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use $V_{IH}/V_{IL(ac)}$ of DQs.

NOTE 2 $V_{IH(ac)}/V_{IL(ac)}$ for DQs is based on V_{REFDQ}; $V_{SEH(ac)}/V_{SEL(ac)}$ for CA is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3 These values are not defined, ho\wever the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits ($V_{IH(dc)max}$, $V_{IL(dc)min}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to 5.5, Overshoot and Undershoot Specifications.

4.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in Table 14. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

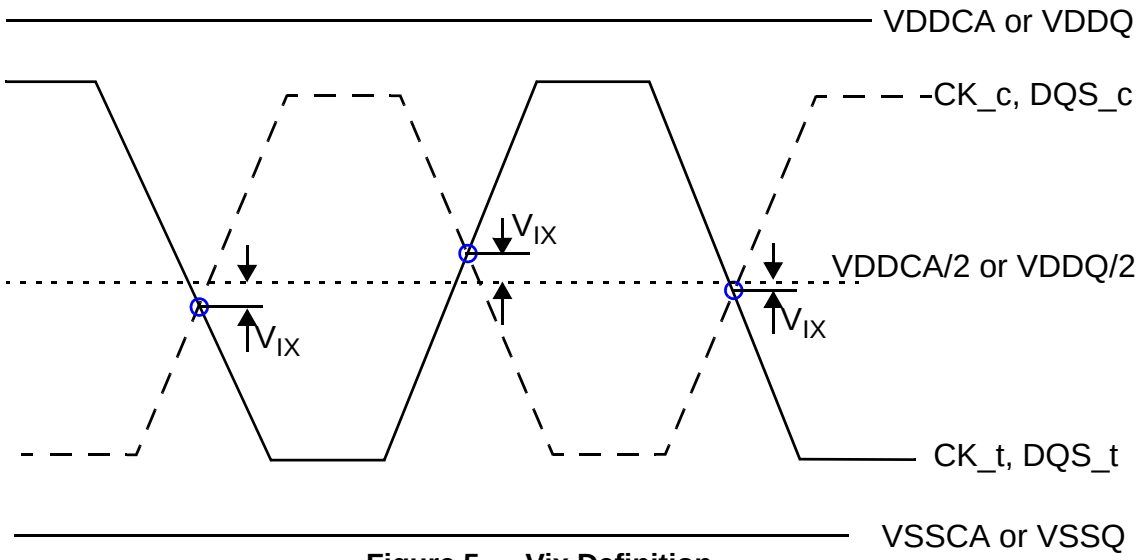


Figure 5 — Vix Definition

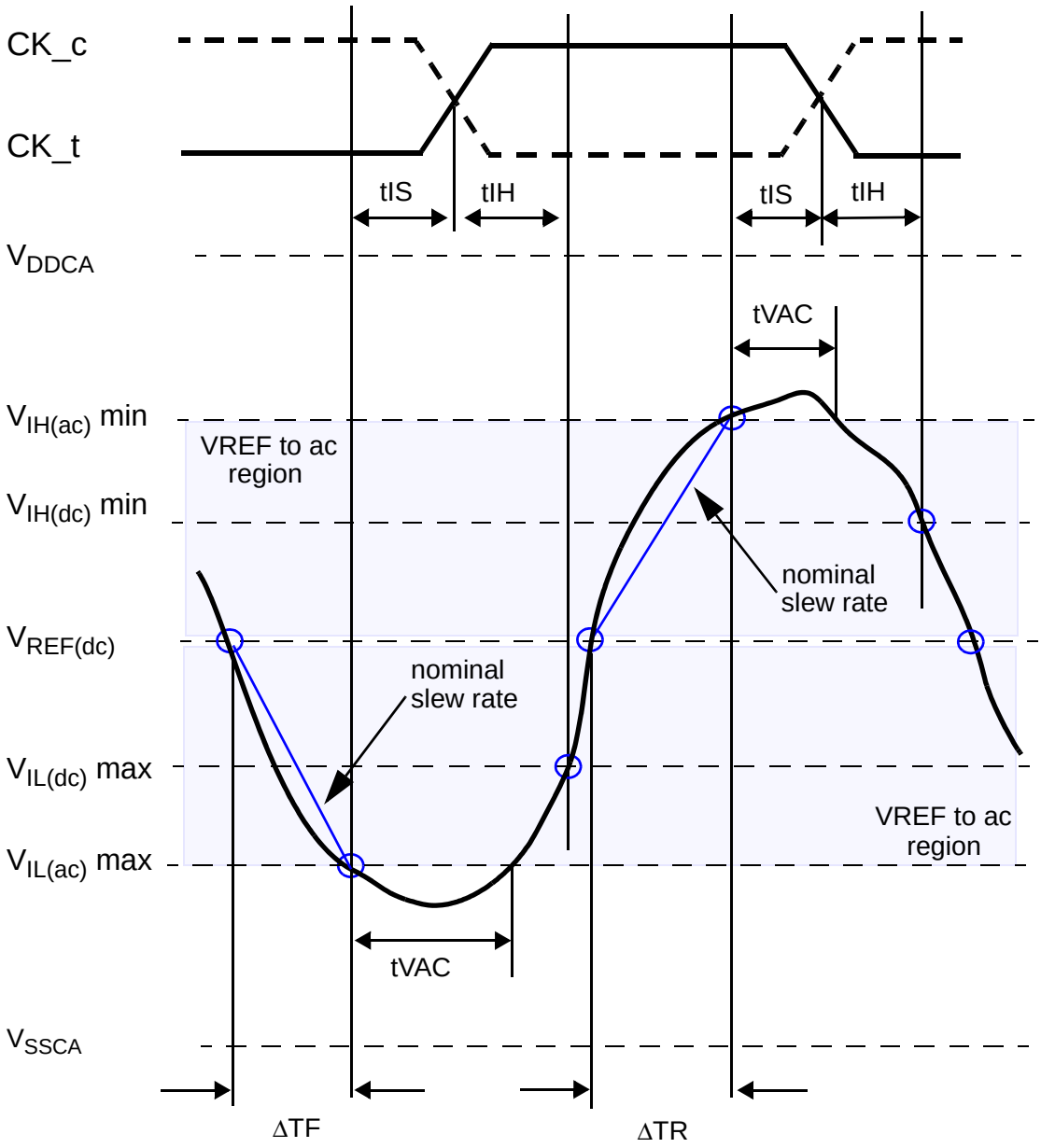
Table 14 — Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IXCA}	Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t, CK_c	- 120	120	mV	1,2
V_{IXDQ}	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t, DQS_c	- 120	120	mV	1,2

NOTE 1 The typical value of VIX is expected to be about 0.5 × VDD of the transmitting device, and VIX is expected to track variations in VDD. VIX indicates the voltage at which differential input signals must cross.

NOTE 2 For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

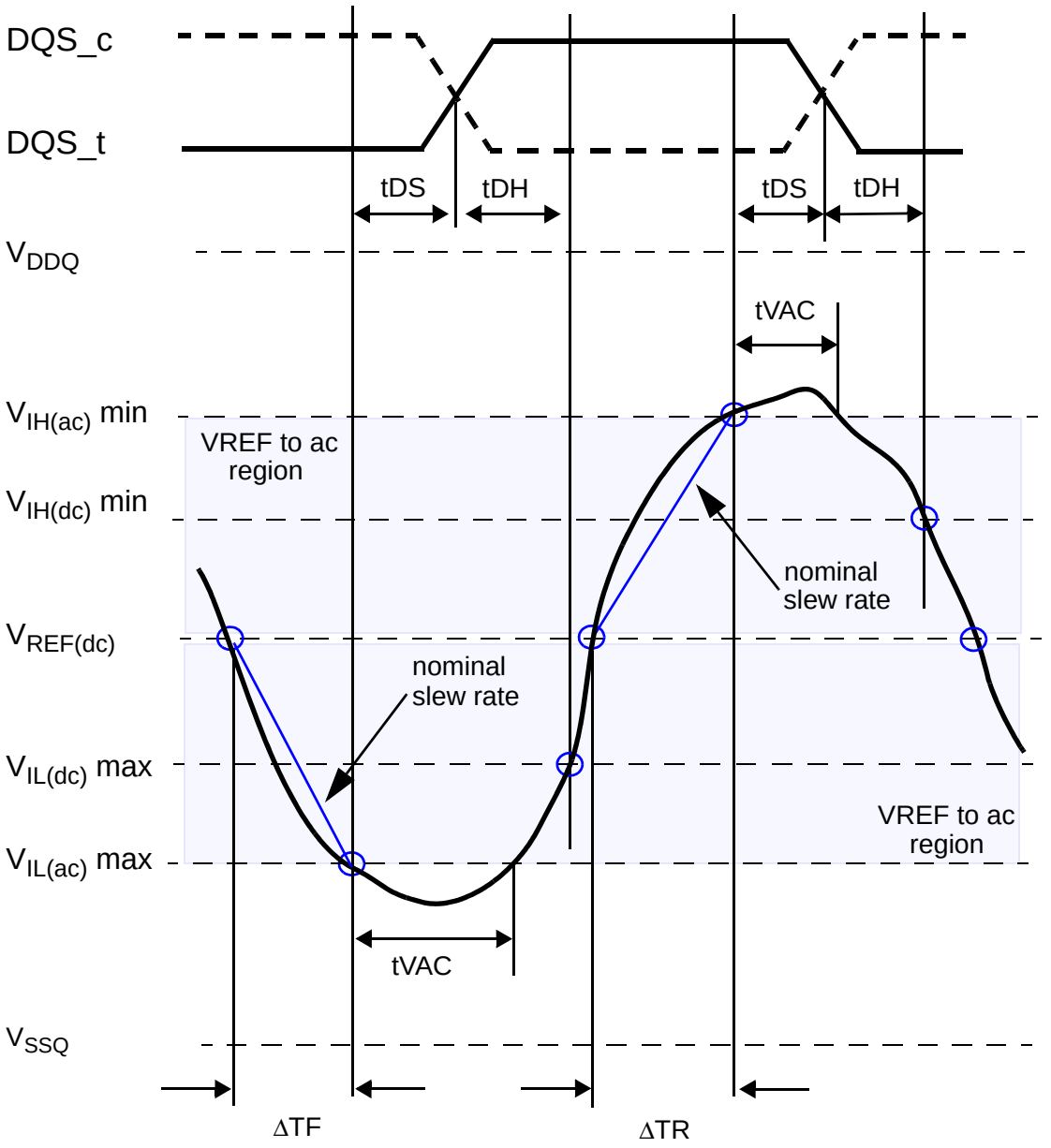
4.6 Slew rate Definitions for Single-Ende Input Signals



$$\text{Setup Slew Rate}_{\text{Falling Signal}} = \frac{V_{REF(dc)} - V_{IL(ac)}\text{max}}{\Delta TF} \qquad \text{Setup Slew Rate}_{\text{Rising Signal}} = \frac{V_{IH(ac)}\text{min} - V_{REF(dc)}}{\Delta TR}$$

Figure 6 — Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock.

4.6 Slew rate Definitions for Single-Ende Input Signals (cont'd)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}\text{max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}\text{min} - V_{REF(dc)}}{\Delta TR}$$

Figure 7 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe

4.7 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table 15 and Figure 8.

Table 15 — Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff
NOTE 1 The differential signal (i.e., CK_t - CK_c and DQS_t - DQS_c) must be monotonic between these thresholds.			

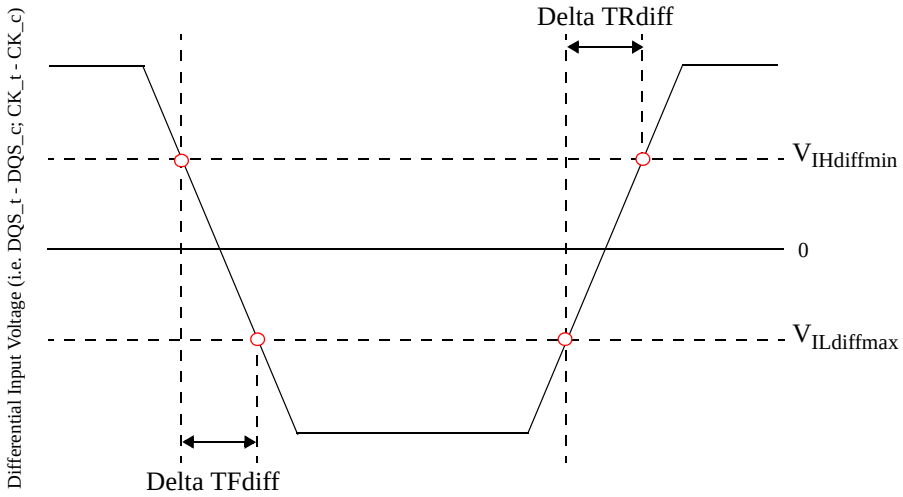


Figure 8 — Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t,

5 AC and DC Output Measurement Levels

5.1 Single Ended AC and DC Output Levels

Table 16 shows the output levels used for measurements of single ended signals for Class I.

Table 16 — Single-ended AC and DC Output Levels,Class I

Symbol	Parameter		Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)		V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)		V_{REFDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c)	Min	-5	uA	
	(DQ, DQS_t, DQS_c are disabled; 0V ≤ VOUT ≤ VDDQ	Max	5	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	
NOTE 1 IOH = -0.1mA. NOTE 2 IOL = 0.1mA.					

Table 17 shows the output levels used for measurements of single ended signals for Class II.

Table 17 — Single-ended AC and DC Output Levels,Class II

Symbol	Parameter		Value	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$ ODT disabled	DC output low measurement level (for IV curve linearity)		0.1 x V_{DDQ}	V	2
$V_{OL(DC-ODT)}$ ODT enabled	DC output low measurement level (for IV curve linearity)		(0.1+0.9xRon/ (Rtt+Ron))xV_{DDQ}	V	3
$V_{OH(AC)}$	AC output high measurement level (for output slew rate)		V_{REFDQ} + 0.12	V	
$V_{OL(AC)}$	AC output low measurement level (for output slew rate)		V_{REFDQ} - 0.12	V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c)	Min	-5	uA	
	(DQ, DQS_t, DQS_c are disabled; 0V ≤ VOUT ≤ VDDQ	Max	5	uA	
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Min	-15	%	
		Max	15	%	
NOTE 1 IOH = -0.1mA. NOTE 2 IOL = 0.1mA. NOTE 3 Ron,Rtt tolerance see I-V curve section					

5.2 Differential AC and DC Output Levels

Table 18 shows the output levels used for measurements of differential signals (DQS_t, DQS_c).

Table 18 — Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	
NOTE 1 IOH = -0.1mA. NOTE 2 IOL = 0.1mA				

5.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 19 and Figure 9.

Table 19 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

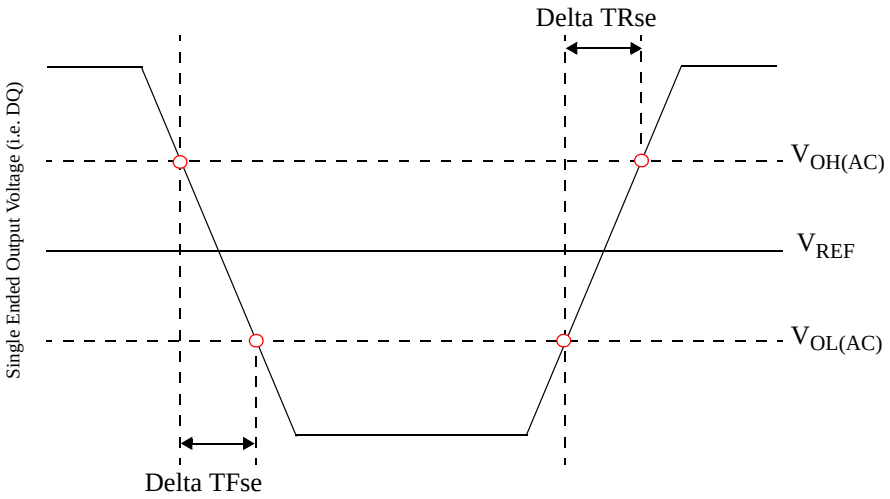


Figure 9 — Single Ended Output Slew Rate Definition

5.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 20 and Figure 10.

Table 20 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTFdiff
NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.			

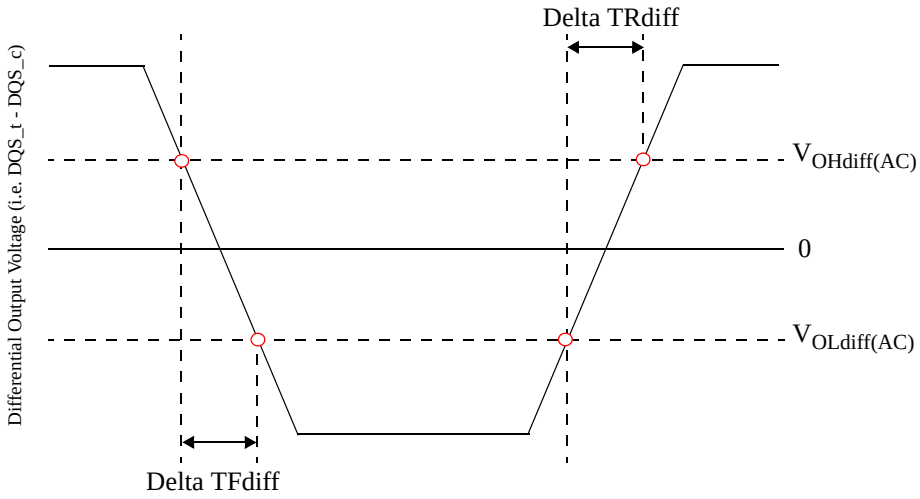


Figure 10 — Differential Output Slew Rate Definition

5.5 Overshoot and Undershoot Specifications

Table 21 — AC Overshoot/Undershoot Specification

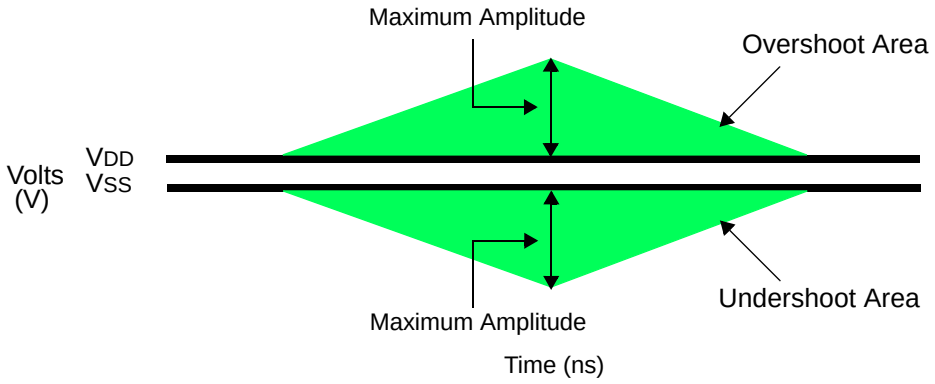
Parameter		2133	1866	1600	1333	1066	933	800	667	533	466	400	333	266	200	Units
Maximum peak amplitude allowed for overshoot area.(See Figure 11)	Max	0.35														V
Maximum peak amplitude allowed for under-shoot area. (See Figure 11)	Max	0.35														V
Maximum area above VDD.(See Figure 11)	Max	0.10	0.10	0.10	0.12	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns
Maximum area below VSS. (See Figure 11)	Max	0.10	0.10	0.10	0.12	0.15	0.17	0.20	0.24	0.30	0.35	0.40	0.48	0.60	0.80	V-ns

(CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM/DNV)

NOTE 1 For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.

NOTE 2 For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands for VSSQ.

NOTE 3 Values are referenced from actual VDDQ, VDDCA, VSSQ, and VSSCA levels.



NOTE 1 For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t, and DQS_c, VDD stands for VDDQ.

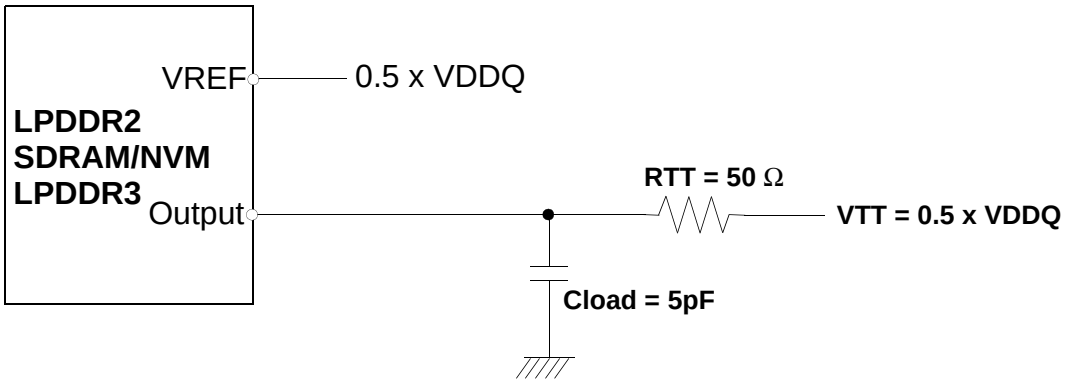
NOTE 2 For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM/DNV, DQS_t, and DQS_c, VSS stands for VSSQ.

Figure 11 — Overshoot and Undershoot Definition

5.6 Output Buffer Characteristics

5.6.1 HSUL_12 Driver Output Timing Reference Load

These ‘Timing Reference Loads’ are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



NOTE 1 All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE} etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Figure 12 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

5.7 RON_{PU} and RON_{PD} Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

NOTE 1 This is under the condition that RON_{PD} is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

NOTE 1 This is under the condition that RON_{PU} is turned off

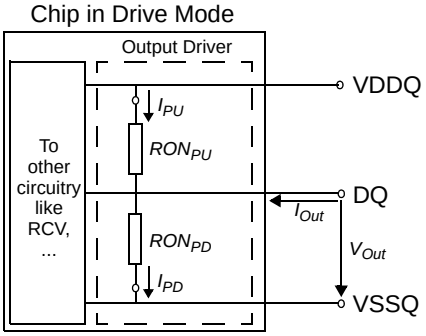


Figure 13 — Output Driver: Definition of Voltages and Currents

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.1 RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240W.

Table 22 — Output Driver DC Electrical Characteristics with ZQ Calibration,Class I

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
60.0Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
80.0Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
120.0Ω (optional)	RON120PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
	RON120PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5

NOTE 1 Across entire operating temperature range, after calibration.

NOTE 2 RZQ = 240W.

NOTE 3 The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 4 Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.

NOTE 5 Measurement definition for mismatch between pull-up and pull-down, MMPUPD: Measure RON_{PU} and RON_{PD}, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.1 RON_{PU} and RON_{PD} Characteristics with ZQ Calibration(cont'd)

Table 23 — Output Driver DC Electrical Characteristics with ZQ Calibration,Class II

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4,6
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4,6
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4,6
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4,6
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4,6
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4,6
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5,6

NOTE 1 Across entire operating temperature range, after calibration.

NOTE 2 RZQ = 240W.

NOTE 3 The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 4 Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.

NOTE 5 Measurement definition for mismatch between pull-up and pull-down, MMPUPD: Measure RON_{PU} and RON_{PD}, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

NOTE 6 Output driver strength measured without ODT.

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 24 — Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD RONPU	0.5 x VDDQ	$85 - (dRONdT \times \lvert\Delta T\rvert) - (dRONdV \times \lvert\Delta V\rvert)$	$115 + (dRONdT \times \lvert\Delta T\rvert) + (dRONdV \times \lvert\Delta V\rvert)$	%	1,2
NOTE 1 $\Delta T = T - T$ (@ calibration), $\Delta V = V - V$ (@ calibration) NOTE 2 dRONdT and dRONdV are not subject to production test but are verified by design and characterization.					

Table 25 — Output Driver Temperature and Voltage Sensitivity, Class I

Symbol	Parameter	MIn	Max	Unit	Notes
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

Table 26 — Output Driver Temperature and Voltage Sensitivity, Class II

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	% / °C
$dR_{ON}dV$	R_{ON} Voltage Sensitivity	0.00	0.20	% / mV
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.75	% / °C
$dR_{TT}dV$	R_{TT} Voltage Sensitivity	0.00	0.20	% / mV

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.3 RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table 27 — Output Driver DC Electrical Characteristics without ZQ Calibration,Class I

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON34PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1
120.0Ω (optional)	RON120PD	0.5 x VDDQ	84	120	156	Ω	1
	RON120PU	0.5 x VDDQ	84	120	156	Ω	1
NOTE 1 Across entire operating temperature range, without calibration.							

Table 28 — Output Driver DC Electrical Characteristics without ZQ Calibration,Class II

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON34PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
NOTE 1 Across entire operating temperature range, without calibration. NOTE 2 Output driver strength measured without ODT.							

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.4 RZQ I-V Curve, Class I

Table 29 — RZQ I-V Curve, Class I

Voltage [V]	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.4 RZQ I-V Curve, Class I (cont'd)

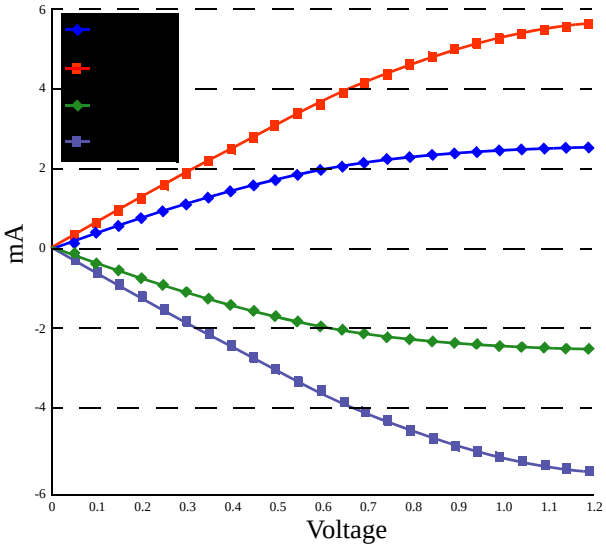


Figure 14 — RON = 240 Ohms IV Curve after ZQReset

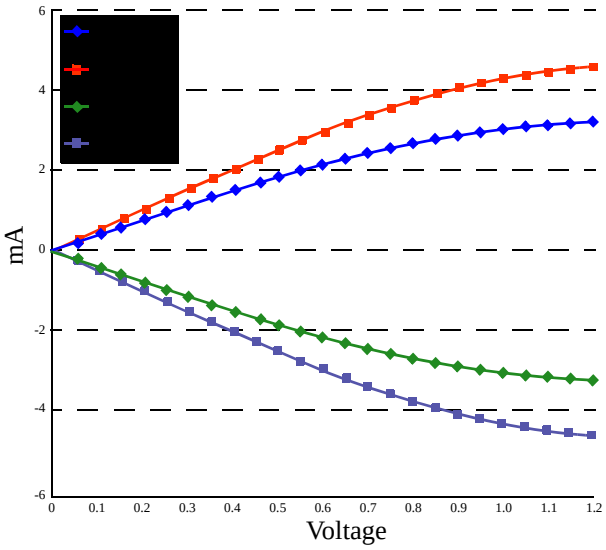


Figure 15 — RON = 240 Ohms IV Curve after calibration

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.5 RZQ I-V Curve, Class II

Table 30 — RZQ I-V Curve, Class II

Voltage [V]	R_{ON} = 240Ω (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current [mA] / R_{ON} [Ohms]				Current [mA] / R_{ON} [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	n/a	n/a	0.00	0.00	n/a	n/a
0.05	0.17	0.35	n/a	n/a	-0.17	-0.35	n/a	n/a
0.10	0.34	0.70	n/a	n/a	-0.34	-0.70	n/a	n/a
0.15	0.50	1.03	n/a	n/a	-0.50	-1.03	n/a	n/a
0.20	0.67	1.39	n/a	n/a	-0.67	-1.39	n/a	n/a
0.25	0.83	1.73	n/a	n/a	-0.83	-1.73	n/a	n/a
0.30	0.97	2.05	n/a	n/a	-0.97	-2.05	n/a	n/a
0.35	1.13	2.39	n/a	n/a	-1.13	-2.39	n/a	n/a
0.40	1.26	2.71	n/a	n/a	-1.26	-2.71	n/a	n/a
0.45	1.39	3.01	n/a	n/a	-1.39	-3.01	n/a	n/a
0.50	1.51	3.32	n/a	n/a	-1.51	-3.32	n/a	n/a
0.55	1.63	3.63	n/a	n/a	-1.63	-3.63	n/a	n/a
0.60	1.73	3.93	2.17	2.94	-1.73	-3.93	-2.17	-2.94
0.65	1.82	4.21	n/a	n/a	-1.82	-4.21	n/a	n/a
0.70	1.90	4.49	n/a	n/a	-1.90	-4.49	n/a	n/a
0.75	1.97	4.74	n/a	n/a	-1.97	-4.74	n/a	n/a
0.80	2.03	4.99	n/a	n/a	-2.03	-4.99	n/a	n/a
0.85	2.07	5.21	n/a	n/a	-2.07	-5.21	n/a	n/a
0.90	2.11	5.41	n/a	n/a	-2.11	-5.41	n/a	n/a
0.95	2.13	5.59	n/a	n/a	-2.13	-5.59	n/a	n/a
1.00	2.17	5.72	n/a	n/a	-2.17	-5.72	n/a	n/a
1.05	2.19	5.84	n/a	n/a	-2.19	-5.84	n/a	n/a
1.10	2.21	5.95	n/a	n/a	-2.21	-5.95	n/a	n/a
1.15	2.23	6.03	n/a	n/a	-2.23	-6.03	n/a	n/a
1.20	2.25	6.11	n/a	n/a	-2.25	-6.11	n/a	n/a

5.7 RON_{PU} and RON_{PD} Resistor Definition (cont'd)

5.7.5 RZQ I-V Curve, Class II (cont'd)

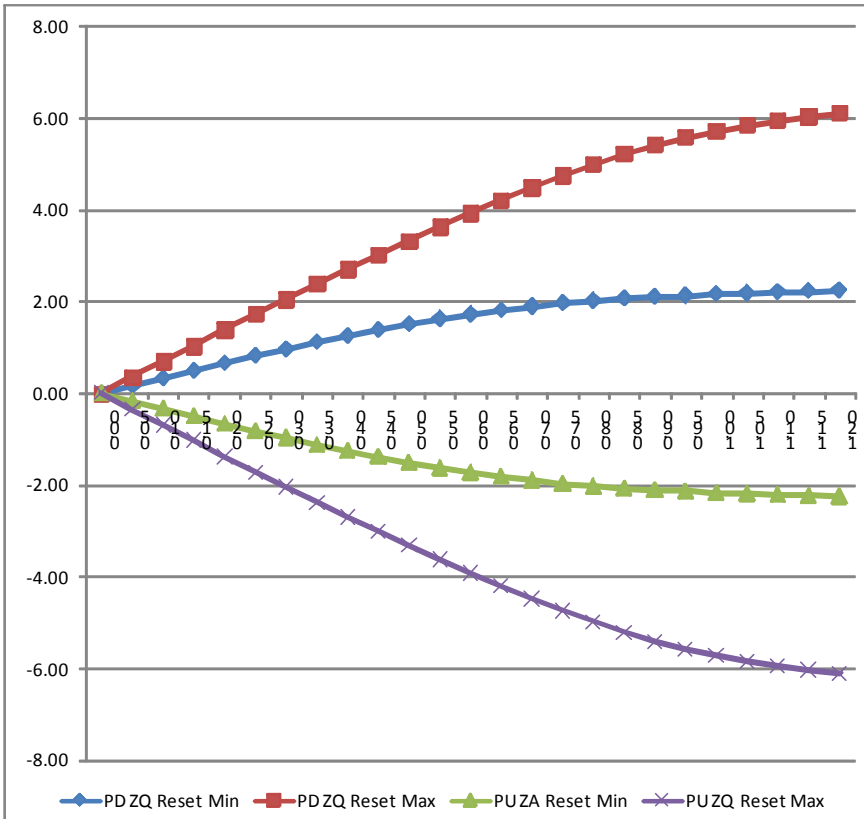


Figure 15 — I-V Curve After ZQ Reset

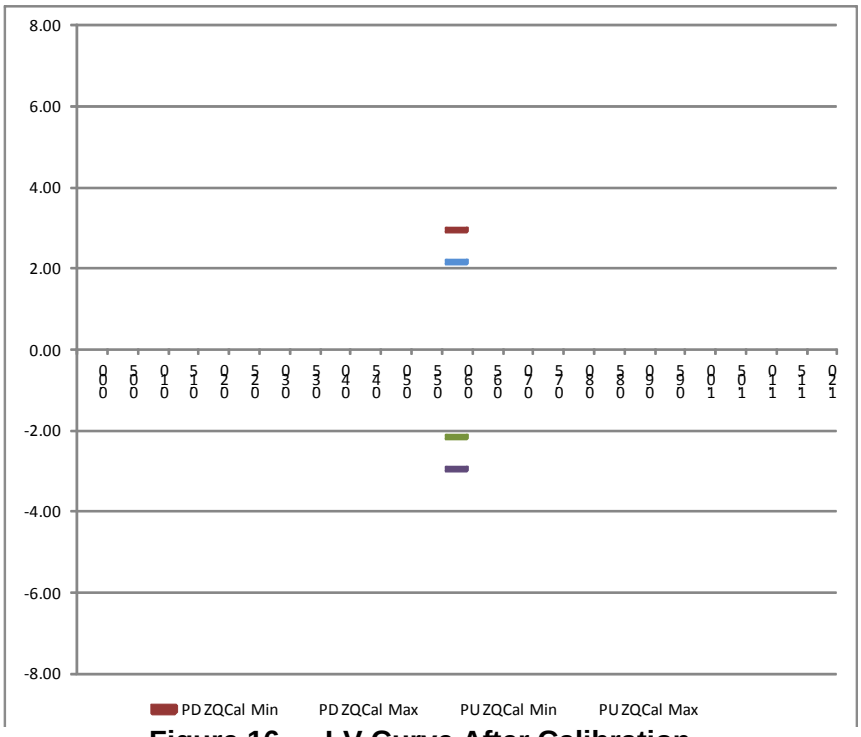


Figure 16 — I-V Curve After Calibration

5.8 ODT Levels and I-V Characteristics

On-Die Termination effective resistance, R_{TT}, is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_c pins. A functional representation of the on-die termination is shown in Figure 18. R_{TT} is defined by the following formula:

$R_{TTPU} = (V_{DDQ} - V_{Out}) / | I_{Out} |$

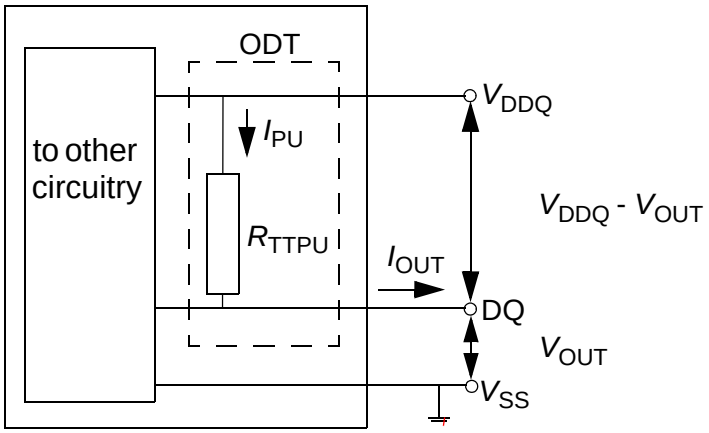


Figure 17 — Functional representation of on-die termination

Table 31 — ODT DC Electrical Characteristics, assuming R_{ZQ}=240 ohm after proper ZQ calibration

R_{TT} (ohm)	V_{OUT} (V)	I_{OUT}	
		Min (mA)	Max (ma)
R_{ZQ}/1	0.6	2.17	2.94
R_{ZQ}/2	0.6	4.34	5.88

Annex A (informative) Differnces between JESD8-22B and JESD8-22A

This annex briefly describes most of the changes made to entries that appear in this standard, JESD8-22B, compared to its predecessor, JESD8-22A (October 2012). Some punctuation changes are not included.

Clause	Description of Change
4.1.1	Table 4, added material for 1866/2133 and added new header for 1333/1600
4.1.3	Table 8, added material for 1866/2133 and added new header for 1333/1600
4.4.2	Table 11, added material for 1866 Mbps and 2133Mbps
4.4.3	Table 13, Updated table and added notes
5.5	Table 21, added material for parameters 1866 and 2133
5.7.2	Table 26, add 3rd and 4th line items

A.1 Differences between JESD8-22A and JESD8-22 (August 2009)

Clause	Description of Change
Througout	Added additional material to include LPDDR3

Standard Improvement Form JEDEC JESD8-22B

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

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_____

3. Other suggestions for document improvement:

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