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DDR5 Registering Clock Driver Definition (DDR5RCD01)

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CONTENTS

1 Scope 1

2 Mechanical Outline 2
2.1 Pinout 3
2.2 Terminal Functions 4

3 Device Standard 6
3.1 Description 6
3.2 Logic Diagram Positive Logic 6
3.3 Register Operation 6
3.3.1 Chip Select Operation 6
3.3.2 ODT Operation 6
3.3.3 QCA Bus Operation 8
3.3.4 QCS Operation 9
3.3.5 Output Inversion and Mirroring 9
3.3.6 ZQ Calibration 10
3.3.7 Latency Equalization Support 10
3.3.8 Output Delay Control 11
3.3.9 Power Down Operation 11
3.3.10 VHost Mode 11
3.3.11 Transparent Mode 12
3.3.12 CA Validation Pass-Through Mode 12
3.3.13 DRAM Interface and Data Buffer Interface Training Support 13
3.4 Command Address Bus 13
3.4.1 Double Data Rate DCA 14
3.4.2 Single Data Rate DCA 17
3.4.3 SDR to DDR Transition 18
3.5 Parity 18
3.5.1 Single UI DRAM commands with Parity Enabled 19
3.5.2 2UI DRAM commands with Parity Enabled 20
3.5.3 ALERT_n Assertion 23
3.6 DCA Decision Feedback Equalization 24
3.6.1 DFE Tap Configurations 24
3.6.2 DFE Gain and Tap Range 24
3.7 RX Loopback 25
3.7.1 Loopback Mode 25
3.7.2 Loopback Ports 25
3.7.3 Pin Assignment for Loopback 26
3.8 Device Initialization 28
3.9 Reset Initialization with Stable Power 31

4 Power Down operation 33
4.1 Power Savings Modes 33
4.1.1 PDE Power Down Mode 33
4.1.2 PDE Power Down Mode with ODT control 34
4.2 Self Refresh Modes 35
4.2.1 Self Refresh Mode with Clock Stop Entry 35
4.2.2 Exit from Self Refresh Mode with Clock Stop 36
4.2.3 Self Refresh Mode without Clock Stop Entry 36

Contents (cont'd)

4.2.4 Self Refresh Mode without Clock Stop Exit 36

5 Training Modes 42
5.1 CS Training Modes 42
5.1.1 DCS Training Mode (DCSTM) - Host Interface 42
5.1.2 QCS Training Mode (QCSTM) - DRAM Interface 44
5.2 CA Training Modes 45
5.2.1 DCA Training Mode (DCATM) - Host Interface 45
5.2.2 QCA Training - DRAM Interface 48
5.2.3 CA Pass-through Mode 48
5.2.4 BCS and BCOM Training - Data Buffer Interface 49
5.2.5 BCOM Pass-Through Mode 49
5.3 DFE Training Mode (DFETM) 51
5.3.1 DFE Training Pattern Comparison and feedback Features: 53
5.3.2 DFE Parameter Sweep Acceleration 55
5.3.3 Method to update RW in-band during training 57
5.4 Dual Frequency Support 59
5.4.1 Initial Frequency Setting 60
5.4.2 Input Clock Frequency Change 60

6 Data Buffer Control Bus 61
6.1 Control Bus Signals 61
6.1.1 Control Bus Signal Termination 61
6.2 Control Bus Timing 62
6.3 Control Bus Commands 63
6.3.1 Data Buffer Control Bus Command Truth Table 63
6.3.2 Command Sequences 63
6.4 Command Sequence Descriptions 63
6.4.1 WR/RD Burst Length Processing 65
6.4.2 MRR Burst Length Processing 65
6.4.3 MRW Commands 66
6.4.4 MRR Commands 67
6.4.5 WR Commands 72
6.4.6 RD Commands 73
6.4.7 PDE Commands 75
6.4.8 MPC Command 75
6.4.9 NOP / Power Down Exit 76

7 SidebandBus Interface 77
7.1 SidebandBus Requirements During Initialization of RCD 77
7.2 Feature Summary 77
7.3 Operating Ranges 78
7.4 External Pins 78
7.4.1 Serial Clock (SCL) 78
7.4.2 Serial Data (SDA) 78
7.5 System Management Access 78
7.5.1 Target Address 78
7.5.2 Supported SidebandBus Commands 79
7.5.3 Register Access Protocols 80
7.5.4 Sequence for switching from I2C mode to I3C Basic 82

Contents (cont'd)

7.5.5 Parity Error Checking 82
7.5.6 PEC Support 82
7.5.7 Sideband Control Word Read Protocol 83
7.5.8 Sideband Control Word Write Protocol 90
7.5.9 In-Band Interrupts 96
7.5.10 I/O Operation 100
7.6 I2C and I3C Basic Reset 100
7.6.1 Sideband Interface and DRST_n RCD Reset Events 101
7.7 I2C Bus Clear 101
7.8 I2C Bus Error Handling 102
7.9 Error Handling in I3C Basic 102
7.9.1 Write Command Data Packet Error Handling - PEC Is Disabled 102
7.9.2 Read Command Data Packet Error Handling - PEC Is Disabled 102
7.9.3 Write Command Data Packet Error Handling - PEC Is Enabled 103
7.9.4 Read Command Data Packet Error Handling - PEC Is Enabled 103
7.9.5 CCC Packet Error Handling 104
7.10 Supported I3C Basic Common Command Codes (CCCs) 104
7.10.1 Enable/Disable Events Command (ENEC/DISEC) Operation 105
7.10.2 Reset Dynamic Address Assignment Command (RSTDAA) Operation 106
7.10.3 Set All Addresses to Static Address Command (SETAASA) Operation 107
7.10.4 Get Device Status Command (GETSTATUS) Operation 107
7.10.5 Get Device Capability Command (DEVCAP) Operation 109
7.10.6 Set HID Command (SETHID) Operation 110
7.10.7 Configure SPD Hub and All Devices Behind Hub Command (DEVCTRL) Operation 110

8 Control Words 114
8.1 Reading Control Words 115
8.2 Control Word Decoding 116
8.3 Control Word Decoding 117
8.4 Paged Control Word Decoding 119
8.4.1 Page 0 DFE Paged Control Word Decoding 119
8.4.2 Page 1 DFE Paged Control Word Decoding 120
8.4.3 Page 2 DFE Paged Control Word Decoding 121
8.4.4 Page 3 Manufacturing ID Control Word Decoding 122
8.4.5 Page 4 VHost Paged Control Word Decoding 123
8.5 Sticky Bits 123
8.5.1 Direct 123
8.5.2 Paged 124
8.6 Mode and Command Control Words 125
8.6.1 RW00 - Global Features Control Word 125
8.6.2 RW01 - Parity, CMD Blocking, and Alert Control Word Global Control Word CA 125
8.6.3 RW02 - Host Interface Training Mode Global Control Word 127
8.6.4 RW03 - DRAM & DB Interface Training Modes Global Control Word 127
8.6.5 RW04 - Command Space Global Control Word 128
8.7 Clocking Control Words 129
8.7.1 RW05 - DIMM Operating Speed Global Control Word 129
8.7.2 RW06 - Fine Granularity DIMM Operating Speed Global Control Word 130
8.8 Validation and Lockout Control Words 131
8.8.1 RW07 - Validation Pass-Through and Lockout Protection Global Control Word 131

Contents (cont'd)

8.9 Output Enable Control Words 131
8.9.1 RW08 - Clock Driver Enable Control Word 131
8.9.2 RW09 - Output Address and Control Enable Control Word 132
8.10 Output Driver Strengths 132
8.10.1 RW0A - QCK Signals Driver Characteristics Control Word 132
8.10.2 RW0C - QxCA and QxCS_n Signals Driver Characteristics Control Word 133
8.10.3 RW0D - Data Buffer Interface Driver Characteristics Control Word 133
8.11 Output Slew Rate Control 133
8.11.1 RW0E - QCK, QCA and QCS Output Slew Rate Control Word 134
8.11.2 RW0F - BCK, BCOM and BCS Output Slew Rate Control Word 135
8.12 Input Bus Termination Strengths 135
8.12.1 RW10 - IBT Global Control Word 135
8.13 Timing Control Words 136
8.13.1 RW11 - Command Latency Adder Configuration Control Word 136
8.13.2 RW12 - QACK Output Delay Control Word 136
8.13.3 RW13 - QBCK Output Delay Control Word 137
8.13.4 RW14 - QCCK Output Delay Control Word 137
8.13.5 RW15 - QDCK Output Delay Control Word 138
8.13.6 RW17 - QACS0_n Output Delay Control Word 138
8.13.7 RW18 - QACS1_n Output Delay Control Word 139
8.13.8 RW19 - QBCS0_n Output Delay Control Word 139
8.13.9 RW1A - QBCS1_n Output Delay Control Word 140
8.13.10 RW1B - QACA Output Delay Control Word 140
8.13.11 RW1C - QBCA Output Delay Control Word 141
8.13.12 RW1D - BCS_n and BCOM[2:0] Output Delay Control Word 141
8.13.13 RW1E - BCK Output Delay Control Word 142
8.14 RW[24:20] - Error Log Register 142
8.15 SidebandBus 143
8.15.1 RW25 - SidebandBus Global Control Word 143
8.16 RX Loopback 144
8.16.1 RW26 - RX Loopback Global Control Word 144
8.16.2 RW27 - Loop-back I/O Global Control Word 144
8.17 SidebandBus Error Status 145
8.17.1 RW28: I2C & I3C Basic Error Status Global Word 145
8.17.2 RW29: I2C & I3C Basic Clear Error Status Global Word 145
8.17.3 RW2A: Vendor Specific Global Word 146
8.18 DFE Control Words 146
8.18.1 RW30 - DFE_Vref Range Limit Global Status Word 146
8.18.2 RW31 - DFE Configuration Control Word 147
8.18.3 RW32 - DPAR and DCA[6:0] DFE Training Mode Control Word 148
8.18.4 RW33 - Additional Filtering for DFE Training Mode Control Word 148
8.18.5 RW34 - LFSR DFE Training Mode Control Word 149
8.18.6 RW35 - LFSR State for DFE Training Mode Control Word 149
8.18.7 RW36 - DFETM Inner Loop Start Value Control Word 150
8.18.8 RW37 - DFETM Outer Loop Start Value Control Word 150
8.18.9 RW38 - DFETM Inner Loop Current Value Control Word 151
8.18.10 RW39 - DFETM Outer Loop Current Value Control Word 151
8.18.11 RW3A - DFETM Inner and Outer Loop Step Size Control Word 152
8.18.12 RW3B - DFETM Inner Loop Number of Increments Control Word 152

Contents (cont'd)

8.18.13 RW3C - DFETM Outer Loop Number of Increments Control Word 153
8.18.14 RW3D - DFETM Inner Loop Current Increment Control Word 153
8.18.15 RW3E - DFETM Outer Loop Current Increment Control Word 153
8.18.16 RW3F - DFE Vref Range Selection Control Word 154
8.19 Vref Control Words 154
8.19.1 RW[47:40] - Internal VrefCA Control Word 154
8.19.2 RW[49:48] - Internal VrefCS Control Word 155
8.19.3 RW4A - DERROR_IN_n Vref Control Word 155
8.19.4 RW4B - Loop-Back Vref Control Word 156
8.20 Read and Paging Control Words 156
8.20.1 RW5E - CW Read Pointer Control Word 156
8.20.2 RW5F - CW Page Control Word 156
8.21 DFE Paged Control Words 157
8.21.1 PG[1:0]RW[60, 68, 70, 78] - DPAR and DCA[6:0] Receiver DFE Gain Offset 157
8.21.2 PG[1:0]RW[61, 69, 71, 79] - DPAR and DCA[6:0] Receiver DFE Tap 1 Coefficients 158
8.21.3 PG[1:0]RW[62, 6A, 72, 7A]- DPAR and DCA[6:0] Receiver DFE Tap 2 Coefficients 160
8.21.4 PG[1:0]RW[63, 6B, 73, 7B] - DPAR and DCA[6:0] Receiver DFE Tap 3 Coefficients 161
8.21.5 PG[1:0]RW[64, 6C, 74, 7C]- DPAR and DCA[6:0] Receiver DFE Tap 4 Coefficients 162
8.21.6 PG[2]RW[60, 64, 68, 6C, 70, 74, 78, 7C] DFE Error Counter Lower 8 Bits 163
8.21.7 PG[2]RW[61, 65, 69, 6D, 71, 75, 79, 7D] - DFE Error Counter Upper 8 Bits 163
8.21.8 PG[2]RW[62, 66, 6A, 6E, 72, 76,7A, 7E] - DFE Vref 164
8.21.9 PG[2]RW[63, 67, 6B, 6F, 73, 77, 7B, 7F] - LFSR Seed for DFE Training Mode Control Word 165
8.22 OTP Paged Global Control Words 165
8.22.1 PG[3]RW60 - Date Code Byte 0 Global Word 165
8.22.2 PG[3]RW61 - Date Code Byte 1 Global Word 166
8.22.3 PG[3]RW62 - Date Code Byte 2 Global Word 166
8.22.4 PG[3]RW63 - Vendor Specific Unique Unit Code Byte 0 Global Word 167
8.22.5 PG[3]RW64 - Vendor Specific Unique Unit Code Byte 1 Global Word 167
8.22.6 PG[3]RW65 - Vendor Specific Unique Unit Code Byte 2 Global Word 167
8.22.7 PG[3]RW66 - Vendor Specific Unique Unit Code Byte 3 Global Word 168
8.22.8 PG[3]RW67 - Vendor Specific Unique Unit Code Byte 4 Global Word 168
8.22.9 PG[3]RW68 - Vendor Specific Unique Unit Code Byte 5 Global Word 168
8.22.10 PG[3]RW69 - Vendor Specific Unique Unit Code Byte 6 Global Word 169
8.22.11 PG[3]RW6A - Vendor ID Byte 0 Global Word 169
8.22.12 PG[3]RW6B - Vendor ID Byte 1 Global Word 169
8.22.13 PG[3]RW6C - Device ID Byte 0 Global Word 170
8.22.14 PG[3]RW6D - Device ID Byte 1 Global Word 170
8.22.15 PG[3]RW6E - Revision ID Global Word 171
8.23 VHost Paged Control Words 171
8.23.1 PG[4]RW[6E,6C,6A,68,66,64,62,60] - VHost Cmd[3:0] CA[7:0] Control Word 171
8.23.2 PG[4]RW[6F,6D,6B,69,67,65,63,61] - VHost Cmd[3:0] CS[1:0]/CA[13:8] Control Word 171
8.23.3 PG[4]RW70 - VHost [1:0] Cmd to Cmd Delay Control Word 172
8.23.4 PG[4]RW71 - VHost [3:2]Cmd to Cmd Delay Control Word 172
8.23.5 PG[4]RW72 - VHost Repeat Mode Control Word 173
8.23.6 PG[4]RW73 - VHost Start and Stop Global Control Word 173

9 Absolute maximum ratings 175

10 Electrical - Timing Requirements 176
10.1 Operating Electrical Characteristics 176

Contents (cont'd)

10.2 Input Timing Requirements 177
10.3 Output Timing Requirements 181

11 VrefCA and Vref CS Specifications 183
11.1 DFE_Vref INL Tolerance 188
11.2 Measurement Steps 191
11.3 DFE Tap Coefficient and Gain Adjustment tolerances (DNL and INL) 192

12 AC & DC Global Definitions 193
12.1 Transmitter (Tx), Receiver (Rx) and Channel Definitions 193
12.1.1 Bit Error Rate 194
12.1.2 General Equation 194
12.1.3 Minimum Bit Error Rate (BER) Requirements 195
12.1.4 Unit Interval and Jitter Definitions 195
12.1.5 Unit Interval 195
12.1.6 UI Jitter Definition 196
12.1.7 UI-UI Jitter Definition 196
12.1.8 Accumulated Jitter (Over "N" UI) 197

13 Electrical - Input AC and DC Specifications 198
13.1 Input Clock Architecture 198
13.1.1 Input Clock SSC and PLL Loop Filter 198
13.1.2 Input Single-ended Swing Requirements for Differential Clock 198
13.1.3 Input Slew Rate for Differential Clock 198
13.1.4 Input Clock Differential Cross point voltage 199
13.2 Input Voltage Levels for DERROR_IN_n Signals 200
13.3 Overshoot and Undershoot Specifications 200
13.4 Input Bus Termination (IBT) Characteristics for DCA, DPAR, DCS, and DERROR_IN_n 201
13.5 DLBD and DLBS Loopback Input Termination 202
13.6 Input CMOS Rail-to-Rail Levels for DRST_n 203
13.7 Differential Input Clock and DCA Voltage Sensitivity 204
13.7.1 Differential Input Clock and DCA Voltage Sensitivity Parameter 204
13.8 Input Clock Jitter 205
13.8.1 Overview 205
13.8.2 Specification for RCD Input Clock Jitter 206
13.9 RX Clock Jitter Sensitivity 207
13.9.1 Rx Clock Jitter Sensitivity Specification 208
13.9.2 Test Conditions for RX Clock Jitter Sensitivity Tests 210
13.10 Input Stressed Eye 211
13.10.1 Overview 211
13.10.2 Input Stressed Eye Parameters 212
13.11 DCS Input Receiver Specification 213
13.11.1 DCS Input Receiver Voltage Margin and AC Timing by Speed Bin 214
13.12 DLBD Input Receiver Specification 215

14 Electrical - Output AC and DC Specifications 217
14.1 Single-Ended Output Slew Rate 217
14.2 Output Clock Differential Slew Rate 218
14.3 Output Differential Clock Cross Point Voltage 220
14.4 Output R-on Drive Specifications per Drive Strength Setting 221
14.5 Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity 223

Contents (cont'd)

15 IDD Specification Parameters 230
15.1 IDD Specification Parameters and Test Conditions 230

16 Input/Output Capacitance 235
16.1 Electrostatic Discharge Sensitivity Characteristics 238

17 SidebandBus Interface Electrical and Timing Specifications 239
17.1 Operating Conditions 239
17.2 Measurement Test Conditions 239
17.3 DC Electrical Characteristics 239
17.4 AC Electrical Characteristics 241

18 Test Circuits and Switching Waveforms 247
18.1 Alert Output Voltage Measurement Information 247
18.2 DDR5RCD01 Reference Load 248

19 Reference to other applicable JEDEC standards and publications 249

Figures

Figure 1: Ball Configuration, TOP VIEW 2
Figure 2: RCD Output Inversion 9
Figure 3: Latency Equalizer Delays 10
Figure 4: Validation Pass-Through Mode - DDR 13
Figure 5: Validation Pass-Through Mode - SDR1 13
Figure 6: RCD DCA and QCA Ports 14
Figure 7: One UI DRAM Command Timing Diagram 15
Figure 8: Two UI DRAM Command Timing Diagram 15
Figure 9: DDR CA Multi-Command Timing Diagram Example 16
Figure 10: Qn Output Skew 16
Figure 11: SDR1 mode example of DRAM WR Command with RW00[1] = 0 17
Figure 12: SDR2 Mode example of DRAM WR Command with RW00[1] = 1 18
Figure 13: 1 UI DRAM Command with parity checking enabled and CLA = 0 19
Figure 14: SDR mode 1 UI DRAM command with parity checking enabled and CLA = 0 20
Figure 15: Error in 1st UI of 2 UI DRAM Command with parity checking enabled 20
Figure 16: SDR mode error in 1st UI of 2 UI DRAM command with parity checking enabled 21
Figure 17: Error in 2nd UI of 2 UI DRAM Command with parity checking enabled 22
Figure 18: SDR1 mode error in 2nd UI of 2 UI DRAM command with parity checking enabled. 22
Figure 19: RCD Loopback Ports 26
Figure 20: External Loopback Timing Diagram 26
Figure 21: Internal Loopback A & B Phase 27
Figure 22: Loopback Output Timing Parameters 27
Figure 23: Timing of Clock and Data During Initialization Sequence 29
Figure 24: Reset Initialization With Stable Power 31
Figure 25: Power Down Mode Entry and Exit 35
Figure 26: Self Refresh Entry Exit with Clock Stop With DCK Frequency Change 38
Figure 27: Self Refresh Entry Exit with Clock Stop in SDR1 Mode With DCK Frequency Change 39
Figure 28: Self Refresh Entry Exit with Clock Stop Without DCK Frequency Change 40
Figure 29: Self Refresh Entry Exit with Clock Stop in SDR1 Mode Without DCK Frequency Change 41
Figure 30: Self Refresh Entry and Exit without Clock Stop 42
Figure 31: Timing Diagram for DCS Training Mode with Consecutive Output Samples = 0 44
Figure 32: Timing Diagram for DCS Training Mode with Output Sample Toggle 45
Figure 33: Timing Diagram for QCSTM with Output Sample Toggle 46
Figure 34: Timing Diagram for DCA Training Mode SMBus Exit 47

Contents (cont'd)

Figure 35: Timing Diagram for DCA Training Mode Double CS Exit 48
Figure 36: MRW example of MRW on DCS0 and CA Pass-Through on DCS1 49
Figure 37: SDR CA Pass-Through mode 50
Figure 38: BCOM PASS Through 51
Figure 39: BCOM Pass-Through Mode when RCD is in SDR 51
Figure 40: DFE Training Circuitry 52
Figure 41: DFE Summer 52
Figure 42: Logical representation of the Galois LFSR of polynomial x8+x6+x5+x4+1 for DCA Training 53
Figure 43: LFSR CA DFE Training Pattern 54
Figure 44: CA DFE UI Filter Pattern 54
Figure 45: RCD Operation During DFE Parameter Sweep Acceleration 56
Figure 46: RWUPD State Machine 58
Figure 47: RWUPD Timing Diagram for Channel A 59
Figure 48: Control Bus Termination 61
Figure 49: Example BCOM WR Command 62
Figure 50: MRW command sequence 67
Figure 51: MRR Command Sequence to Data Buffer address space 68
Figure 52: MRR Command Sequence to DRAM Address Space 70
Figure 53: RD to MRR Command Sequence to Data Buffer Address Space 71
Figure 54: WR to MRR Command Sequence to Data Buffer Address Space 72
Figure 55: WRITE Timing 73
Figure 56: READ Timing 74
Figure 57: SidebandBus Wiring Diagram 78
Figure 58: RCD Interrupt Request - Controller ACK followed by RCD IBI Payload 97
Figure 59: RCD Interrupt Request - Controller NACK followed by STOP 97
Figure 60: I2C or I3C Basic Reset 101
Figure 61: DxCSx_n Assertion during ALERT_n Pulse Width 126
Figure 62: Vref operating range (Vrefmin, Vrefmax) 183
Figure 63: Example of Vref set tolerance (max case only shown) and step size 184
Figure 64: Vref_time timing diagram 185
Figure 65: Vref step single step size increment case 185
Figure 66: Vref step single step size decrement case 186
Figure 67: Vref full step from Vrefmin to Vrefmax case 186
Figure 68: Vref full step from Vrefmax to Vrefmin case 187
Figure 69: Example of DFE_Vref INL Tolerance 188
Figure 70: DFE_Vref_step time timing diagram 189
Figure 71: DFE_Vref Increment Case 189
Figure 72: DFE_Vref Decrement Case 190
Figure 73: Illustration Example of DFE_Vref INL Tolerance 191
Figure 74: Example of Tap Coefficient and Gain Adjustment tolerances (DNL and INL) 193
Figure 75: UI Definition in Terms of Adjacent Edge Timings 195
Figure 76: UI definition Using Clock Waveforms 196
Figure 77: UI Jitter of the "nth" UI Definition (in terms of ideal UI) 196
Figure 78: UI - UI Jitter Definitions 196
Figure 79: Definition of Accumulated Jitter (over "N" UI) 197
Figure 80: Definition of UI 197
Figure 81: Differential Input Slew Rate Definition for DCK_t/DCK_c 199
Figure 82: Vix Definition (DCK) 200
Figure 83: Input Bus Termination: Definition of Voltages and Currents 201
Figure 84: DLBD and DLBS Termination: Definition of Voltages and Currents 202
Figure 85: DRST_n Input Slew Rate Definition 203
Figure 86: Example of DDR5 Memory Interconnect 204
Figure 87: VRx_CK 205

Contents (cont'd)

Figure 88: VRx_DCA_V 205
Figure 89: Host driving clock signals to the RCD 205
Figure 90: RCD RX Forward Clock for Jitter Sensitivity 207
Figure 91: Example of Rx Stressed Test Setup in Presence of ISI, Jitter and Crosstalk 211
Figure 92: DCS Receiver (RX) Mask 213
Figure 93: DCS TcIPW and SRIN_clVW definition (for each input pulse) 213
Figure 94: DLBD Receiver (RX) Mask 215
Figure 95: DLBD Timings at the RCD 215
Figure 96: DLBD TcIPW definition (for each input pulse) 216
Figure 97: Output Single-Ended Slew Rate Definition 217
Figure 98: Differential Output Slew Rate Definition for QnCK_t / QnCK_c and BnCK_t / BnCK_c 219
Figure 99: Vox Definition (QnCKx and BnCK) 220
Figure 100: Output Driver: Definition of Voltages and Currents 221
Figure 101: Definition for tstaoff and tdynoff in DDR Mode 226
Figure 102: Definition for tstaoff and tdynoff in SDR Mode 227
Figure 103: Clock Output (QxCK) Skew 228
Figure 104: Example of QCK TX Interconnectt 228
Figure 105: Measurement Setup and Test Load for IDD Measurements 231
Figure 106: Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDD Measurement 231
Figure 107: AC Measurement I/O Waveform 239
Figure 108: I2C and I3C Basic AC Input Timing Parameter Definitions 242
Figure 109: I2C Bus AC Output Timing Parameter Definitions 242
Figure 110: I3C Basic AC Output Timing Parameter Definitions 243
Figure 111: Rise and Fall Timing Parameter Definitions 243
Figure 112: Output Slew Rate Measurement Points 243
Figure 113: Test Load for Output Slew Rate and Output Timing Measurement 243
Figure 114: I3C Basic Hand-off Operation - RCD Open Drain (ACK) to Controller Push-Pull 244
Figure 115: I3C Basic Hand-off Operation - Controller Open Drain (ACK) to RCD Push-Pull 244
Figure 116: I3C Basic T=0 Transition from RCD Read Operation to Controller STOP bit 245
Figure 117: I3C Basic T = 1 Transition from RCD Read Operation Interrupted by Controller Repeated START and STOP bit 245
Figure 118: Controller Push Pull to Target Open Drain Hand Off Operation 246
Figure 119: Voltage waveforms, tALERT Measurement 247
Figure 120: Voltage waveforms, tALERT_HL Measurement 247
Figure 121: Voltage waveforms, tDCSTM_ALERT_Window and tDCATM_ALERT_Window Measurements 247
Figure 122: Test Load 248

TABLES

Table 1: Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW 3
Table 2: Terminal functions 4
Table 3: DCS - QxCS Mapping 6
Table 4: ODT encoding on the chip select 6
Table 5: DIMM Termination Write 8
Table 6: DIMM Termination Read 8
Table 7: Command Address Rates 13
Table 8: DDR CA Mapping DCA to QCA 14
Table 9: Blocking Commands on Parity Error 23
Table 10: DFE Tap Configurations 24
Table 11: DFE Gain and Tap Total Control Word Range 24
Table 12: DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin 24

Contents (cont'd)

Table 13: DDR5RCD01 Device Initialization Sequence at Power-on Ramping....30
Table 14: DDR5RCD01 Device Initialization Sequence when Power and Clock are Stable....31
Table 15: ODT Control during Power Down Mode....34
Table 16: Sample Evaluation for Intermediate Output[0]....43
Table 17: Sample Evaluation for Intermediate Output[1]....43
Table 18: Sample Evaluation for final DCSTM Output....44
Table 19: DCA Training Mode Output....48
Table 20: BCOM bus mapping....50
Table 21: Post-cursor Bias Ctrl Definition....53
Table 22: Control Words Duplicated for Frequency Context Support....59
Table 23: List of Signals for Data Buffer Control Signals....61
Table 24: BCOM bus Mapping....62
Table 25: Data Buffer Control Bus Command Truth Table....63
Table 26: Data Buffer PG[1:0] Rank Training Control Word Decoding....64
Table 27: WR/RD Burst Length Processing....65
Table 28: MRR Burst Length Processing....65
Table 29: PBA Enumerate ID Programming Burst Length Processing....66
Table 30: Multi-cycle Sequence for MRW Commands....66
Table 31: Multi-cycle Sequence for MRR Commands....67
Table 32: Short MRR Command for SDR Training....68
Table 33: MRR Read Format for Data Buffer Return....69
Table 34: MRR Read Format for Data Buffer Return with Read CRC Enabled....69
Table 35: Multi-cycle Sequence for WR Commands....72
Table 36: Multi-cycle Sequence for RD Commands....74
Table 37: Multi-cycle Sequence for PDE Commands....75
Table 38: Multi-cycle Sequence for MPC Commands....75
Table 39: Multi-cycle Sequence for NOP/PDX Commands....76
Table 40: SidebandBus Command Format in I2C Mode....79
Table 41: SidebandBus Command Format in I3C Basic Mode....79
Table 42: SidebandBus Protocol Addressing Fields....81
Table 43: SidebandBus Address Map....81
Table 44: Double Word Byte Order for SidebandBus Control Word Access....82
Table 45: Status Field Encoding for SidebandBus Reads....84
Table 46: I2C Read Command Packet Example (Block Mode, PEC Disabled, Legacy Format)....84
Table 47: I2C Read Command Packet Example (Block Mode, PEC Enabled, Legacy Format)....85
Table 48: I2C Read Command Packet Example (Block Mode, PEC Disabled, Optimized Format)....85
Table 49: I2C Read Command Packet Example (Byte Mode, PEC Disabled, Legacy Format)....86
Table 50: I2C Read Command Packet Example (Byte Mode, PEC Enabled, Legacy Format)....87
Table 51: I3C Basic Read Command Packet Example (PEC Disabled)....88
Table 52: I3C Basic Read Command Packet Example (Block Mode, PEC Enabled)....89
Table 53: I3C Basic Read Command Packet Example with IBI Header and No Pending Interrupt (Block Mode, PEC Enabled)....90
Table 54: I2C Write Command Packet Example (Write DWord, Block Mode, PEC Disabled)....91
Table 55: I2C Write Command Packet Example (Write DWord, Block Mode, PEC Enabled)....91
Table 56: I2C Write Command Packet Example (Write Byte, Block Mode, PEC Disabled)....91
Table 57: I2C Write Command Packet Example (Write Word, Block Mode, PEC Enabled)....92
Table 58: I2C Write Command Packet Example (Write DWord, Byte Mode, PEC Disabled)....92
Table 59: I2C Write Command Packet Example (Write Word, Byte Mode, PEC Enabled)....93
Table 60: I3C Basic Write Command Packet Example (Write DWord, PEC Disabled)....94
Table 61: I3C Basic Write Command Packet Example (Write DWord, Block Mode, PEC Enabled)....94
Table 62: I3C Basic Write Command Packet Example (Write Byte, PEC Disabled)....95
Table 63: I3C Basic Write Command Packet Example (Write Word, Block Mode, PEC Enabled)....95
Table 64: I3C Basic Write Command Packet Example with IBI Header and No Pending Interrupt (Write Word, Block

Contents (cont'd)

Mode, PEC Enabled)....96
Table 65: Interrupt Response (PEC disabled)....98
Table 66: Interrupt Response (PEC enabled)....98
Table 67: RCD Device Dynamic I/O Operation Mode Switching; I3C Basic Mode....100
Table 68: Supported I3C Basic Common Command Codes (CCCs)....105
Table 69: ENEC/DISEC CCC (I3C Basic, Broadcast, PEC Disabled)....105
Table 70: ENEC/DISEC CCC (I3C Basic, Broadcast, PEC Enabled)....105
Table 71: ENEC/DISEC CCC (I3C Basic, Direct, PEC Disabled)....106
Table 72: ENEC/DISEC CCC (I3C Basic, Direct, PEC Enabled)....106
Table 73: RSTDAA CCC (I3C Basic, Broadcast, PEC Disabled)....107
Table 74: RSTDAA CCC (I3C Basic, Broadcast, PEC Enabled)....107
Table 75: SETAASA CCC (I2C, Broadcast)....107
Table 76: GETSTATUS MSb-LSb Format....108
Table 77: GETSTATUS CCC (I3C Basic, Direct, PEC Disabled)....108
Table 78: GETSTATUS CCC (I3C Basic, Direct, PEC Enabled)....108
Table 79: DEVCAP CCC (I3C Basic, Direct, PEC Disabled)....109
Table 80: DEVCAP CCC (I3C Basic, Direct, PEC Enabled)....109
Table 81: DEVCAP MSb-LSb Format....110
Table 82: SETHID CCC (I2C, Broadcast)....110
Table 83: DEVCTRL Command Operation (I2C or I3C Basic, Broadcast, PEC Disabled)....111
Table 84: DEVCTRL Command Operation (I3C Basic. Broadcast, PEC Enabled)....111
Table 85: DEVCTRL Command Definition....112
Table 86: DEVCTRL Command Definition....113
Table 87: DEVCTRL Command Example (I3C Basic, Broadcast, PEC Enabled)....113
Table 88: Control Word Addressing....114
Table 89: RCD and DB Control Word Spaces....115
Table 90: Control Word Read Sequence....115
Table 91: DDR MRW Command to RCD....126
Table 92: Control Word Decoding....117
Table 93: Page 0 DFE Control Word Decoding....119
Table 94: Page 1 DFE Control Word Decoding....120
Table 95: Page 2 DFE Control Word Decoding....121
Table 96: Page 3 Manufacturing ID Control Word Decoding....122
Table 97: Page4 VHost Control Word Decoding,,....123
Table 98: RW00 - Global Features Control Word....125
Table 99: RW01 - Parity, CMD Blocking, and Alert Global Control Word....125
Table 100: ALERT_n Pulse Width for Parity Error....126
Table 101: RW02: Host Interface Training Mode Global Control Word....127
Table 102: RW03: DRAM & DB Interface Training Modes Global Control Word....127
Table 103: RW04: Command Space Global Control Word definition....128
Table 104: RW05: DIMM Operating Speed Global Control Word....129
Table 105: RW06: Fine Granularity DIMM Operating Speed Global Control Word....130
Table 106: RW07: Validation Pass-Through and Lockout Protection Global Control Word....131
Table 107: RW08: Clock Driver Enable Control Word....131
Table 108: RW09: Output Address and Control Enable Control Word....132
Table 109: RW0A: QCK Signals Driver Characteristics Control Word....132
Table 110: RW0C: QxCA and QxCS_n Signals Driver Characteristics Control Word....133
Table 111: RW0D: Data Buffer Interface Driver Characteristics Control Word....133
Table 112: RW0E - QCK, QCA and QCS Output Slew Rate Control Word....134
Table 113: RW0F - BCK, BCOM and BCS Output Slew Rate Control Word....135
Table 114: RW10: IBT Global Control Word....135
Table 115: RW11: Command Latency Adder Configuration Control Word....136
Table 116: RW12: QACK Output Delay Control Word....136

Contents (cont'd)

Table 117: RW13: QBCK Output Delay Control Word 137
Table 118: RW14: QCCK Output Delay Control Word 137
Table 119: RW15: QDCK Output Delay Control Word 138
Table 120: RW17: QACS0_n Output Delay Control Word 138
Table 121: RW18: QACS1_n Output Delay Control Word 139
Table 122: RW19: QBCS0_n Output Delay Control Word 139
Table 123: RW1A: QBCS1_n Output Delay Control Word 140
Table 124: RW1B: QACA Output Delay Control Word 140
Table 125: RW1C: QBCA Output Delay Control Word 141
Table 126: RW1D: BCS_n and BCOM[2:0] Output Delay Control Word 141
Table 127: RW1E: BCK Output Delay Control Word 142
Table 128: RW[24:20]: Error Log Register Encoding for DDR Mode, ... 142
Table 129: RW[24:20]: Error Log Register Encoding for SDR Mode, ... 143
Table 130: RW25: SidebandBus Global Control Word 143
Table 131: RW26: RX Loopback Global Control Word 144
Table 132: RW27: Loop-back I/O Global Control Word 144
Table 133: RW28: I2C & I3C Basic Error Status Global Word 145
Table 134: RW29: I2C & I3C Basic Clear Error Status Global Word 145
Table 135: RW2A: Vendor Specific Global Word 146
Table 136: RW30: DFE_Vref Range Limit Global Status Word 146
Table 137: RW31: DFE Configuration Control Word 147
Table 138: RW32 DPAR and DCA[6:0] DFE Training Mode Control Word 148
Table 139: RW33 Additional Filtering for DFE Training Mode Control Word 148
Table 140: RW34 LFSR DFE Training Mode Control Word 149
Table 141: RW35 LFSR State for DFE Training Mode Control Word 149
Table 142: RW36 DFETM Inner Loop Start Value Control Word 150
Table 143: RW37 DFETM Outer Loop Start Value Control Word 150
Table 144: RW38 DFETM Inner Loop Current Value Control Word 151
Table 145: RW39 DFETM Outer Loop Current Value Control Word 151
Table 146: RW3A DFETM Inner and Outer Loop Step Size Control Word 152
Table 147: RW3B DFETM Inner Loop Number of Increments Control Word 152
Table 148: RW3C DFETM Outer Loop Number of Increments Control Word 153
Table 149: RW3D DFETM Inner Loop Current Increment Control Word 153
Table 150: RW3E DFETM Outer Loop Current Increment Control Word 153
Table 151: RW3F DFE Vref Range Selection Control Word 154
Table 152: RW[47:40]: Internal VrefCA Control Word, ... 154
Table 153: RW[49:48]: Internal VrefCS Control Word, ... 155
Table 154: RW4A: DERROR_IN_n Vref Control Word 155
Table 155: RW4B: Loop-Back Vref Control Word 156
Table 156: RW5E - CW Read Pointer Control Word 156
Table 157: RW5F - CW Page Control Word 156
Table 158: PG[1:0]RW[60, 68, 70, 78]: DPAR and DCA[6:0] Receiver DFE Gain Offset Adjustment 157
Table 159: PG[1:0]RW[61, 69, 71, 79]: DPAR and DCA[6:0] Receiver DFE Tap 1 Coefficients 158
Table 160: PG[1:0]RW[62, 6A, 72, 7A]: DPAR and DCA[6:0] Receiver DFE Tap 2 Coefficients 160
Table 161: PG[1:0]RW[63, 6B, 73, 7B]: DPAR and DCA[6:0] Receiver DFE Tap 3 Coefficients 161
Table 162: PG[1:0]RW[64, 6C, 74, 7C]: DPAR and DCA[6:0] Receiver DFE Tap 4 Coefficients 162
Table 163: PG[2][60, 64, 68, 6C, 70, 74, 78, 7C]- DFE Error Counter Lower 8 Bit 163
Table 164: PG[2][61, 65, 69, 6D, 71, 75, 79, 7D] DFE Error Counter Upper 8 Bit 163
Table 165: PG[2]RW[62, 66, 6A, 6E, 72, 76,7A, 7E]: DFE Vref 164
Table 166: PG[2]RW[63, 67, 6B, 6F, 73, 77, 7B, 7F] LFSR Seed for DFE Training Mode Control Word, ... 165
Table 167: PG[3]RW60: Date Code Byte 0 Global Word 165
Table 168: PG[3]RW61: Date Code Byte 1 Global Word 166
Table 169: PG[3]RW62: Date Code Byte 2 Global Word 166

Contents (cont'd)

Table 170: PG[3]RW63: Vendor Specific Unique Unit Code Byte 0 Global Word....167
Table 171: PG[3]RW64: Vendor Specific Unique Unit Code Byte 1 Global Word....167
Table 172: PG[3]RW65: Vendor Specific Unique Unit Code Byte 2 Global Word....167
Table 173: PG[3]RW66: Vendor Specific Unique Unit Code Byte 3 Global Word....168
Table 174: PG[3]RW67: Vendor Specific Unique Unit Code Byte 4 Global Word....168
Table 175: PG[3]RW68: Vendor Specific Unique Unit Code Byte 5 Global Word....168
Table 176: PG[3]RW69: Vendor Specific Unique Unit Code Byte 6 Global Word....169
Table 177: PG[3]RW6A: Vendor ID Byte 0 Global Word....169
Table 178: PG[3]RW6B: Vendor ID Byte 1 Global Word....169
Table 179: PG[3]RW6C: Device ID Byte 0 Global Word....170
Table 180: PG[3]RW6D: Device ID Byte 1 Global Word....170
Table 181: PG[3]RW6E: Revision ID Global Word....170
Table 182: PG[4]RW[6E,6C,6A,68,66,64,62,60] - VHost Cmd[3:0] CA[7:0] Control Word....171
Table 183: PG[4]RW[6F,6D,6B,69,67,65,63,61] - VHost Cmd[3:0] CA[7:0] Control Word....171
Table 184: PG[4]RW70 - VHost [1:0] Cmd to Cmd Delay Control Word....172
Table 185: PG[4]RW71 - VHost [3:2] Cmd to Cmd Delay Control Word....172
Table 186: PG[4]RW72 - VHost Repeat Mode Control Word....173
Table 187: PG[4]RW73 - VHost Start and Stop Global Control Word....173
Table 188: Absolute maximum ratings over operating free-air temperature range[1]....175
Table 189: Operating Electrical Characteristics....176
Table 190: Input Timing requirements....177
Table 191: Output timing requirements....181
Table 192: Internal VrefCA & VrefCS Specifications....187
Table 193: DFE_Vref Specification....190
Table 194: DFE_Vref INL Tolerance....190
Table 195: Estimated Number of Transmitted Bits (n) for confidence level of 70% to 99.5%....194
Table 196: Minimum BER Requirements for RX and TX Timing and Voltage Tests....195
Table 197: SSC and PLL Loop Filter Characteristics....198
Table 198: Differential Input Slew Rate Definition for DCK_t/DCK_c....198
Table 199: Differential Input Slew Rate DCK_t/DCK_c....199
Table 200: Cross point voltage (VIX) for differential input signals (DCK)....200
Table 201: Input Voltage Levels for DERROR_IN_n Signals....200
Table 202: IBT Electrical Characteristics for DCA, DPAR, DCS, and DERROR_IN_n....201
Table 203: Electrical Characteristics for DLBD and DLBS Input Termination....202
Table 204: CMOS Rail-to-Rail Input Levels for DRST_n....203
Table 205: Rx Input Voltage Sensitivity Parameters for DDR5-3200 to 4800....204
Table 206: Input Clock Differential Jitter....206
Table 207: Rx Clock Jitter Sensitivity Option-1 Specification for DDR5-3200 to 4800....208
Table 208: Rx Clock Jitter Sensitivity Option-2 Specification for DDR5-3200 to 4800....209
Table 209: Rx Clock Jitter Sensitivity Specification for DDR5-3200 to 4800....210
Table 210: Test Conditions for Rx Stressed Eye Tests for DDR5-3200 to 4800....212
Table 211: DCS Input Receiver Voltage Margin and AC Timing by Speed Bin....214
Table 212: Loopback RX Receiver Voltage Margin and AC Timing by Speed Bin for DDR5 3200 - 4800....216
Table 213: Output Single-ended Slew Rate Definition....217
Table 214: Output Single-Ended Edge Rates Over Specified Operating Temperature Range....218
Table 215: Output Clock Differential Slew Rate Definition for QnCK_t / QnCK_c and BnCK_t / BnCK_c....218
Table 216: Output Differential Edge Rates....219
Table 217: Output Cross Point Voltage for QnCK_t/QnCK_c and BnCK_t/BnCK_c....220
Table 218: Output Ron Drive....221
Table 219: Output Driver DC Electrical Characteristics, entire operating temperature range....222
Table 220: Output Driver and Termination Resistor Sensitivity Definition....223
Table 221: Output Driver and Termination Resistor Temperature and Voltage Sensitivity....224
Table 222: Output Clock Driver Characteristics at Application Mode (Frequency Band 1)....225

Table 223: Output Clock Driver Characteristics at Test Mode (Frequency Band 2) 226
Table 224: Tx QCK Jitter Specifications for DDR5-3200 to 4800....229
Table 225: ALERT_n Output Driver DC Electrical Characteristics....229
Table 226: Basic IDD Measurement Conditions 232
Table 227: IDD3NA. IDD3NB, IDD3P1, and IDD3P2 Measurement-Loop Pattern....233
Table 228: IDD4A, IDD4B Measurement-Loop Pattern....234
Table 229: Silicon pad I/O Capacitance values....235
Table 230: Package Electrical Parameters 236
Table 231: Electrostatic Discharge Sensitivity Characteristics....238
Table 232: Operating Conditions for the SidebandBus Interface 239
Table 233: AC Measurement Conditions for SidebandBus interface 239
Table 234: Output Ron Spec 239
Table 235: Input Parameters for SidebandBus interface....240
Table 236: DC Characteristics for SidebandBus Interface 240
Table 237: AC Characteristics for SidebandBus interface....241

DDR5 REGISTERING CLOCK DEFINITION (DDR5RCD01)

(From JEDEC Board Ballot JCB-20-46 and JCB-21-18, formulated under the cognizance of the JC-40.4 Subcommittee on Registered & Fully Buffered Memory Support Logic.)

1 Scope

This document defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR5 Registering Clock Driver (RCD) with parity for driving address and control nets on DDR5 RDIMM and LRDIMM applications. The DDR5RCD01 Device ID is DID = 0x0051.

The terms ‘Registering Clock Driver’, ‘RCD’, ‘register’ or ‘device’ are used interchangeably to refer to this device in the remainder of this specification.

The purpose is to provide a standard for the DDR5RCD01 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR5RCD01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Mechanical Outline

Package options include a 240-ball Flip-Chip Fine-Pitch BGA (FCBGA) with 0.60 mm/0.70 mm ball pitch, 14 x 19 grid. The package has a number of depopulated balls. Package size is 8.70 mm x 13.50 mm as defined in MO-330 Issue A, Variation 10013.50x8.70-70x6030-240A[1]. The device pinout supports outputs on the top and outer left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way to match the corresponding pin location on the connector.

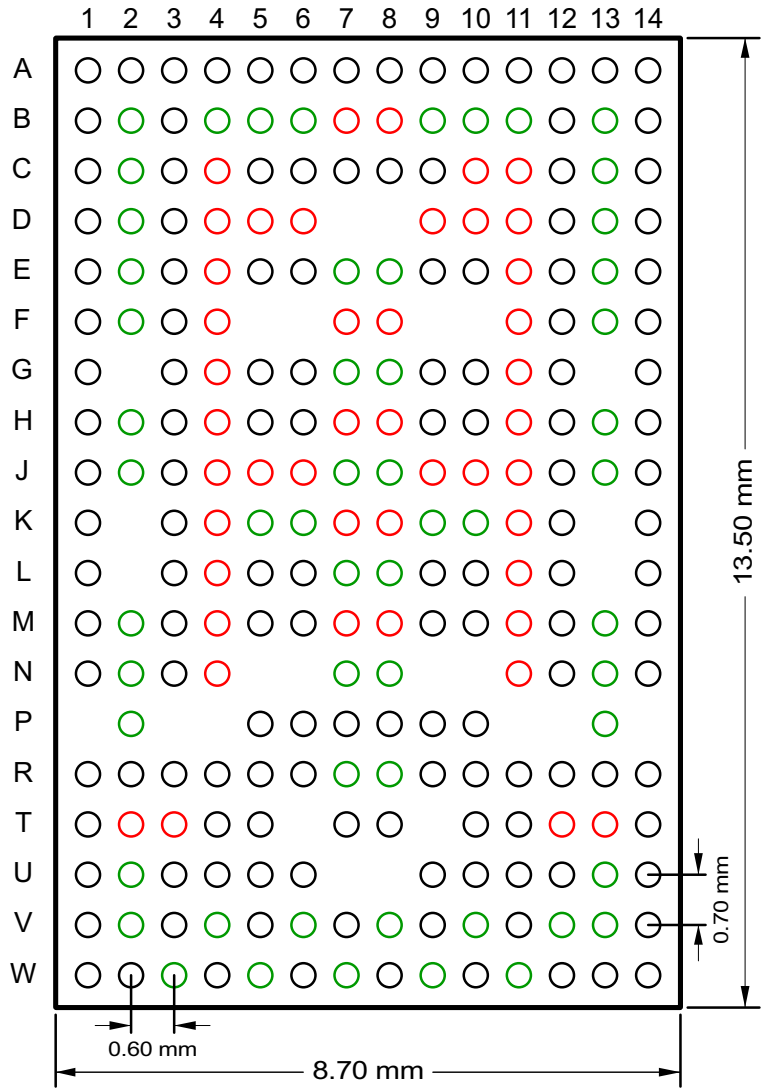


Figure 1 — Ball Configuration, TOP VIEW

Ball pitch: 0.60 mm x 0.70 mm, Size (ø 0.3 mm), SMD Pad SRO (ø 0.275 mm)
X-ray view from topside

1. This variation defines a maximum package thickness of 1.00 mm. The DDR5RCD01 must comply with a minimum thickness of 0.80 mm.

2.1 Pinout

Table 1 specifies the pinout for the DDR5RCD01.

Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA3_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA3_B	QB CA7_B	NU	**A**
B	QB CA1_A	V_{SS}	QB CA9_A	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	QB CA9_B	V_{SS}	QB CA1_B	**B**
C	QB CA6_A	V_{SS}	QB CA8_A	V_{DD}	ZQ CAL	SCL	DERROR_IN_A_n	DERROR_IN_B_n	SDA	V_{DDIO}	V_{DD}	QB CA8_B	V_{SS}	QB CA6_B	**C**
D	QB CA5_A	V_{SS}	QB CA2_A	V_{DD}	V_{DD}	V_{DD}			V_{DD}	V_{DD}	V_{DD}	QB CA2_B	V_{SS}	QB CA5_B	**D**
E	QB CA0_A	V_{SS}	QB CA4_A	V_{DD}	QBCK_A_c	QBCK_A_t	V_{SS}	V_{SS}	QBCK_B_t	QBCK_B_c	V_{DD}	QB CA4_B	V_{SS}	QB CA0_B	**E**
F	QBCS0_A_n	V_{SS}	QBCS1_A_n	V_{DD}			V_{DD}	V_{DD}			V_{DD}	QBCS1_B_n	V_{SS}	QBCS0_B_n	**F**
G	QA CA11_A		QA CA13_A	V_{DD}	QDCK_A_c	QDCK_A_t	V_{SS}	V_{SS}	QDCK_B_t	QDCK_B_c	V_{DD}	QA CA13_B		QA CA11_B	**G**
H	QA CA9_A	V_{SS}	QA CA12_A	V_{DD}	**RFU**	**RFU**	V_{DD}	V_{DD}	**RFU**	**RFU**	V_{DD}	QA CA12_B	V_{SS}	QA CA9_B	**H**
J	QA CA10_A	V_{SS}	QA CA3_A	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	QA CA3_B	V_{SS}	QA CA10_B	**J**
K	QA CA6_A		QA CA7_A	V_{DD}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	QA CA7_B		QA CA6_B	**K**
L	QA CA1_A		QA CA4_A	V_{DD}	QA CA2_A	QA CA8_A	V_{SS}	V_{SS}	QA CA8_B	QA CA2_B	V_{DD}	QA CA4_B		QA CA1_B	**L**
M	QA CA5_A	V_{SS}	QA CA0_A	V_{DD}	QACK_A_c	QACK_A_t	V_{DD}	V_{DD}	QACK_B_t	QACK_B_c	V_{DD}	QA CA0_B	V_{SS}	QA CA5_B	**M**
N	QACS0_A_n	V_{SS}	QACS1_A_n	V_{DD}			V_{SS}	V_{SS}			V_{DD}	QACS1_B_n	V_{SS}	QACS0_B_n	**N**
P		V_{SS}			QCCK_A_c	QCCK_A_t	QLBD	QLBS	QCCK_B_t	QCCK_B_c			V_{SS}		**P**
R	**BCS_A_n**	**BCOM1_A**	**BCOM2_A**	**BRST_A_n**	**BCK_A_c**	**BCK_A_t**	V_{SS}	V_{SS}	**BCK_B_t**	**BCK_B_c**	**BRST_B_n**	**BCOM2_B**	**BCOM1_B**	**BCS_B_n**	**R**
T	**BCOM0_A**	V_{DD}	V_{DD}	DCS1_A_n	QRST_A_n		DCK_t	DCK_c		QRST_B_n	DCS0_B_n	V_{DD}	V_{DD}	**BCOM0_B**	**T**
U	DCA0_A	V_{SS}	DCS0_A_n	DLBD_A	DLBS_A	ALERT_n			DRST_n	DLBS_B	DLBD_B	DCS1_B_n	V_{SS}	DPAR_B	**U**
V	DCA1_A	V_{SS}	DCA3_A	V_{SS}	DPAR_A	V_{SS}	DCA6_A	V_{SS}	DCA1_B	V_{SS}	DCA3_B	V_{SS}	V_{SS}	DCA6_B	**V**
W	NU	DCA2_A	V_{SS}	DCA4_A	V_{SS}	DCA5_A	V_{SS}	DCA0_B	V_{SS}	DCA2_B	V_{SS}	DCA4_B	DCA5_B	NU	**W**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	

2.2 Terminal Functions

Table 2 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.
Loopback	DLBD_[B:A] DLBS_[B:A]	POD V_{REF} based	Loopback Inputs to RCD DLBD - loopback Data DLBS - loopback Strobe
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Error input	DERROR_IN_[B:A]_n	Low voltage swing POD input	DRAM CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. There is a separate signal per channel.
Data buffer control and communication outputs	BCS_[B:A]_n	POD	Data buffer chip selects. Indicate a valid command on the BCOM bus, and used to signal non-target termination. Separate per DRAM channel.
	BCOM[2:0]_[B:A]	POD	Data buffer command. The start of each command is signaled by an active chip select. Separate per DRAM channel.
	BRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD BRST to reset the DDR5 Data Buffer on all DIMM topologies.
	BCK_[B:A]_t BCK_[B:A]_c	POD differential	Differential clock output pair to the data buffer. Separate per DRAM channel.
Output Control bus	Q[B:A]CS[1:0]_[B:A]_n	POD	Chip Select signals to the DRAMs. 2 copies of each signal.
Output Address and Command bus	Q[B:A]CA[13:0]_[B:A]	POD	Command/Address bus outputs to the DRAMs, valid after the specified clock count and immediately following a rising edge of the clock. Two copies of each signal. When Output Inversion is enabled in RW00[5], Copy B output signals get inverted during all commands other than Deselect. Both copies drive High during idle cycles (i.e., Deselect).
Clock outputs	Q[D:A]CK_[B:A]_t Q[D:A]CK_[B:A]_c	POD differential	Clock outputs to the DRAMs. Four copies per channel.
Loopback	QLBD QLBS	POD	Loopback outputs to Host QLBD - loopback Data QLBS - loopback Strobe
Reset output	QRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD QRST_n to reset the DDR5 SDRAM on all DIMM topologies. The QRST outputs are asserted at power up. RCD requires MRW to independently de-assert to allow staggering of sub-channels.
Error out	ALERT_n	POD	When LOW, this output indicates that a parity error was identified associated with the CA inputs when parity checking is enabled or that the DERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not. One signal for the two channels.
SidebandBus pins[1]	SDA SCL	Open drain or push-pull I/O[2] CMOS input[3]	SidebandBus Data SidebandBus Clock
	V_{DDIO}	Power input	SidebandBus power input

Table 2 — Terminal functions

Signal Group	Signal Name	Type	Description
Miscellaneous pins	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in RCD

1. SA pins are not required for DDR5RCD01 as the address will be hard-coded. Refer to Section 7.5.1, “Target Address,” on page 78 for details.
2. SDA driver operation is dynamic. Depending on the SidebandBus mode of operation (I^2C RW25[5] = ‘0’ or I3C Basic RW25[5] = ‘1’), and even on the specific step (byte or bit) of a SidebandBus transaction packet, the SDA output driver can operate either in open-drain mode or push-pull mode.
3. These inputs are 1.0-V inputs.

Naming Convention:

Input Example:
DCAy_N - where ‘y’ is the signal number and ‘N’ is the sub-channel.

Output Example:
QxCAy_N - where ‘y’ is the signal number, ‘x’ is the output copy (A or B) and ‘N’ is the sub-channel.

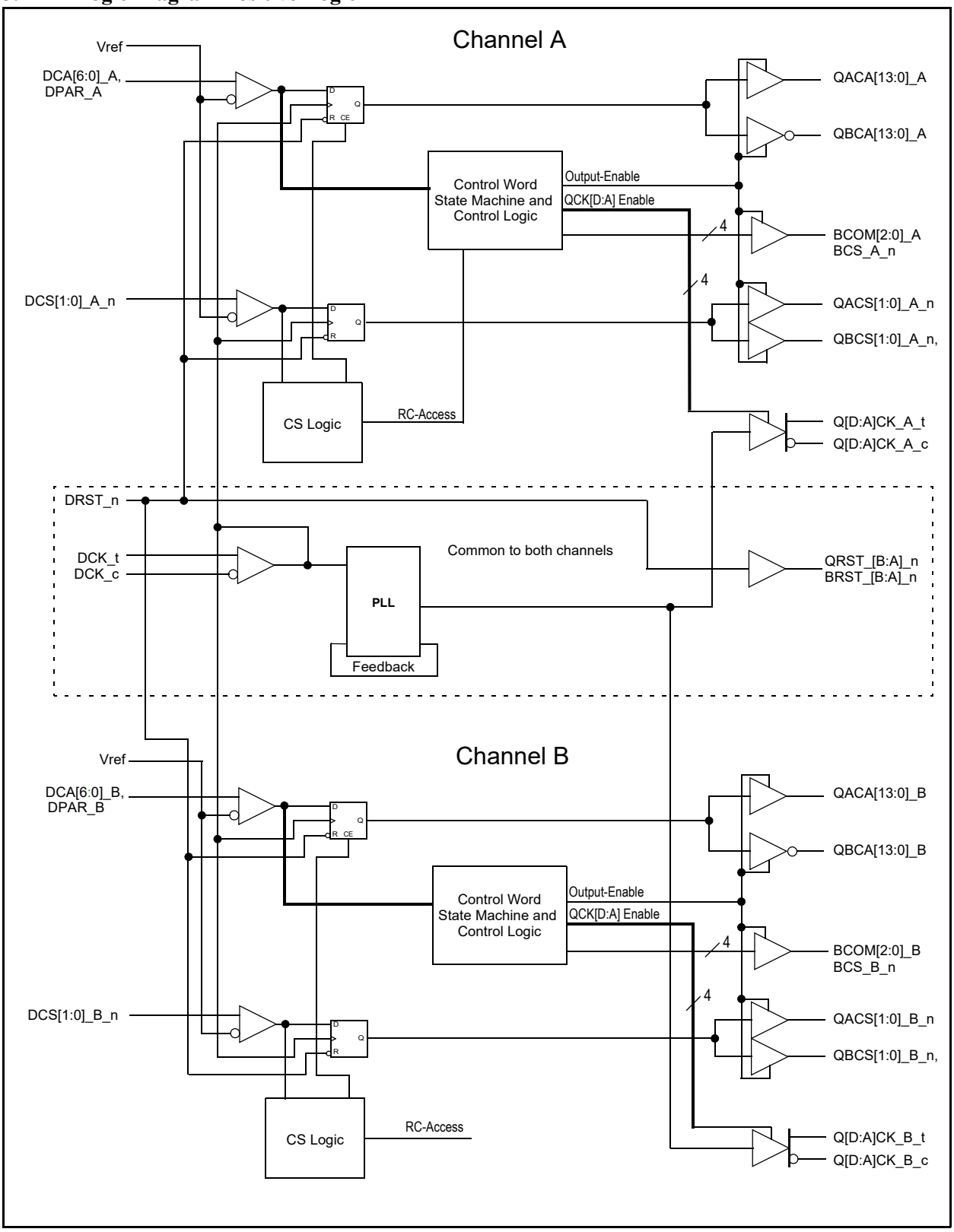
3 Device Standard

3.1 Description

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.

3.2 Logic Diagram Positive Logic



3.3 Register Operation

3.3.1 Chip Select Operation

The component has two chip select inputs per channel, DCS0_n and DCS1_n, and two copies of each chip select output, QCS0_A_n, QCS1_A_n, QCS0_B_n and QCS1_B_n. Commands are sent to a single rank or multiple ranks, as determined by the DCS[1:0]_n inputs. The number of input chip selects matches the number of output chip selects in each of the two sets (A-outputs and B-outputs).

Table 3 — DCS - QxCS Mapping

Input CS	Output CS
DCS0_N_n	QxCS0_N_n
DCS1_N_n	QxCS1_N_n

3.3.2 ODT Operation

DDR5 does not have a separate ODT (On Die Termination) signal going to the DIMM or the DRAMs. The ODT control is encoded into the chip selects. All commands that utilize the data bus require 2UI on the DCA bus in order to transfer the appropriate number of command and addressing bits. This requirement is used to signal ODT control by how the chip selects are asserted for the two UI.

Table 4 — ODT encoding on the chip select

DCS_n on 1st UI	DCS_n on 2nd UI	QxCS[1:0]_n	DRAM DQ Terminations
Active	Inactive	Target of command	Read: none (device drives data) Write: RTT_WR.
Active	Active	Non-Target Termination should be applied.	Read: RTT_NOM_RD Write: RTT_NOM_WR
Inactive	Inactive	DRAM ignores commands and the Parked termination will be maintained	RTT_PARK
Inactive	Active	Illegal	Illegal

The host controller will determine the termination at the time of the command, by activating the chip selects appropriately.

3.3.2.1 Data Buffer DQ Bus Termination in LRDIMM Application

The RCD supports DQ bus termination in LRDIMM applications. DDR5 does not have a discrete ODT signal. The ODT function is encoded on the Chip Select for RD, WR, and MRR commands. A RD, WR, MRW or MRR command will normally have the BCS_n signal active for only the first UI of the command. The data buffers will terminate the host bus as is appropriate for the command (RTT_WR for write, and driving the bus for reads).

The DIMM terminations for DRAM and Data Buffer are shown in Table 5 and Table 6.

Table 5 — DIMM Termination Write

DCS0		DCS1		BCS		DRAM Termination		Buffer Termination
UI 0	UI 1	U 0	UI 1	U 0	UI 1	Rank 0	Rank 1	
L	H	H	H	L	H	RTT_WR	RTT_PARK	RTT_WR
L	H	L	L	L	H	RTT_WR	RTT_NOM_WR	RTT_WR
H	H	L	H	L	H	RTT_PARK	RTT_WR	RTT_WR
L	L	L	H	L	H	RTT_NOM_WR	RTT_WR	RTT_WR
L	L	H	H	L	L	RTT_NOM_WR	RTT_PARK	RTT_NOM_WR
H	H	L	L	L	L	RTT_PARK	RTT_NOM_WR	RTT_NOM_WR
L	L	L	L	L	L	RTT_NOM_WR	RTT_NOM_WR	RTT_NOM_WR

Table 6 — DIMM Termination Read

DCS0		DCS1		BCS		DRAM Termination		Buffer Termination
UI 0	UI 1	U 0	UI 1	U 0	UI 1	Rank 0	Rank 1	Host-side DQ
L	H	H	H	L	H	Target	RTT_PARK	Target
L	H	L	L	L	H	Target	RTT_NOM_RD	Target
H	H	L	H	L	H	RTT_PARK	Target	Target
L	L	L	H	L	H	RTT_NOM_RD	Target	Target
L	L	H	H	L	L	RTT_NOM_RD	RTT_PARK	RTT_NOM_RD
H	H	L	L	L	L	RTT_PARK	RTT_NOM_RD	RTT_NOM_RD
L	L	L	L	L	L	RTT_NOM_RD	RTT_NOM_RD	RTT_NOM_RD

If the DCS_n signal is active during the 2nd UI of a command, it indicates a non-target termination for the DIMM. The command is targeting a different DIMM and the DRAMs or data buffers should terminate with either RTT_NOM_WR for writes or RTT_NOM_RD for reads.

For a non-target operation, the DRAMs or data buffers should remain in RTT_PARK, the command will not be sent on the BCOM bus at all. The RCD will not have received any DCS_n signals active in this case and will see Deselects.

3.3.3 QCA Bus Operation

Under normal operation, the RCD passes commands through from the D inputs to the Q outputs when a command is present on the bus, and drives HIGH on the QCA outputs when no command is being sent. The RCD passes the DCA bus through when either DCS input is active but there are exceptions to this:

- If the register detects a parity error and parity checking is enabled, the DCA bus is still passed through to DRAM and QCS is blocked.

- During the 2nd UI of a 2 UI command, the DCA bus must be passed through. There will only be a DCS signal active for the 2nd UI if a non-target termination is being signaled to a rank.
- When DRAM interface Block MR Mode is enabled RW01[1] = 0.
- When CA Pass-through mode is enabled RW00[2] = 1.

3.3.4 QCS Operation

Under normal operation the RCD passes the DCS signals through to the QCS outputs. There are several exceptions to this:

- If the register detects a parity error with parity checking enabled, on a one-cycle command or the 1st UI of two-cycle command, the DCS signal is not passed through, and the QCS outputs remain inactive.
- If the register detects a parity error with parity checking enabled, on the 2nd UI of a two-cycle command, the same QCS outputs that were active on the 1st UI will be active on the 2nd UI. This causes the command to be canceled in the DRAM. For read and write commands it causes the command to be converted to non-target termination.
- When DRAM interface Block MR Mode is enabled RW01[1] = 0.
- When CA Pass-through mode is enabled RW00[2] = 1.

3.3.5 Output Inversion and Mirroring

Output Inversion is enabled by default, after DRST_n is de-asserted, to reduce simultaneous output switching current.

- All QACA[13:0]_[B:A] outputs will follow the equivalent inputs. All QBCA[13:0]_[B:A] outputs will be inverted. In other words, when sending commands, the “B” copy will be the invert of the “A” copy.
- When no commands are being sent, both the “A” and “B” copies will drive HIGH.
- The DRAM devices connected to the “B” outputs will un-invert the signals internally before using them. This eliminates the need for the host controller to send separate MRW commands for the two CA output sets, and allows every CA output to be inverted on the “B” set.

Address mirroring is also handled by the DRAM device, so there is no RCD requirements for mirroring.

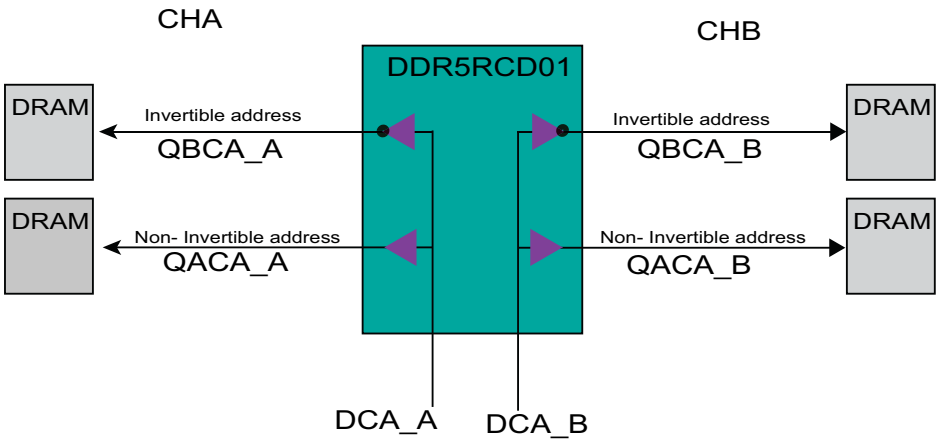


Figure 2 — RCD Output Inversion

3.3.6 ZQ Calibration

The RCD snoops the MPC command to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation.

There are two ZQ Calibration commands initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the RCD's calibration procedure, and ZQCal Latch captures the result and loads it into the RCD's drivers.

A ZQCal Start command may be issued anytime the DDR5-SDRAM is not in a power-down state. There are two timing parameters associated with ZQ Calibration. t_{ZQCAL} is the time from when the ZQCal Start MPC command is sent to when the host can send the ZQCal Latch MPC command. t_{ZQLAT} is the time from when the ZQCal Latch MPC command is sent by the host to when the CA bus (and subsequently the DQ bus) can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after t_{ZQCAL} has expired and all CA bus operations have completed. The CA Bus must maintain a Deselect state during t_{ZQLAT} to allow CA ODT calibration settings to be updated.

After a ZQCal Start and until t_{ZQCAL} finishes, neither another ZQCal Start nor a ZQCal Latch is allowed.

To use the ZQ calibration function, a 240 Ω ± 1% tolerance external resistor must be connected between the ZQ pin and VSS.

3.3.7 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility, it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR5 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR5 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence, this DDR5 register mechanism does not by itself allow mixing DDR5 RDIMMs and LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR5 register supports a programmable latency adder of 0 nCK, 1 nCK, 2 nCK, 3 nCK or 4 nCK for all DRAM commands—see conceptual diagram in Figure 3. The power-up default is 0 nCK latency adder.

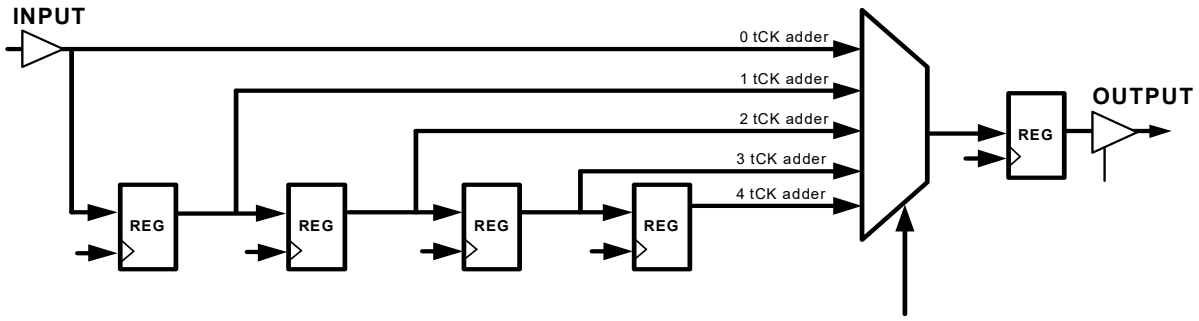


Figure 3 — Latency Equalizer Delays

With a latency adder enabled, the DDR5 register will delay assertion of the QxCSy_N_n and QxCAy_N outputs by the corresponding number of clock cycles. The output timing is determined by the Command Latency Adder control word RW11 regardless of whether the device has parity checking enabled or disabled.

3.3.8 Output Delay Control

The RCD supports output delay control for output signal groups defined and located in RW12 to RW1E. The output delay settings are incremental CK fractions of 1/64 tCK. Each signal group can be enabled or disable independently through RCD Control Words. The Host must wait t_{ODU} after the Output Delay Control Word has been written to a signal group before the output becomes stable. The output delay feature controlled by RW12 to RW1E is not supported when the RCD is configured in Test Frequency mode (Band 2, RW05[7] = 1) or in PLL bypass mode (RW05[3:0] = 1111).

3.3.9 Power Down Operation

DDR5 does not have a separate CKE signal going to the DIMM or the DRAMs. Power Down Entry, including Self Refresh, is signaled via a single UI command. Following the Power Down Entry command, the CS signal effectively becomes the equivalent of the CKE signal. An inactive CS keeps the DRAM devices in the Power Down state. CS going active will take the DRAMs out of the Power Down state. A NOP command is placed on the CA bus along with CS going active so that no commands are executed by the DRAM devices. DRAMs can be put in Power Down mode with or without non-target ODT control, see Chapter 4.

3.3.10 VHost Mode

The Virtual Host mode or “VHost mode” allows a sequence of commands to be sent on the DRAM interface without receiving commands via the host interface. Commands to be sent on the DRAM interface are programmed by writing RCD control words. The intention is to operate this RCD feature via SidebandBus in a test environment. VHost mode is not intended for normal operation. A sequence of commands is programmed into the RCD, then executed by writing a START MRW bit.

Virtual host mode has the following features:

- Up to 4 commands may be programmed.
- Each command may be a 1 or 2 UI command.
- Control words specify the complete CA[13:0] bus and the two chip selects for each UI of the commands.
- There is a programmable number of clocks between commands, programmed separately for the spacing between each command.
- Command spacing can be 2, 4, 8, 16, 64, 256, or 1024 clock.
- Following the last command, the sequence may then optionally repeat starting at command 0, 1, 2, or 3.
- Shorter sequences can be supported by programming Deselects (neither chip select active) for some of the commands.
- Non-target termination can be signaled by programming the chip select to be active for both UI of a command that supports non-target termination.

Each command is programmed using four 8-bit control words, to specify the state if CA[13:0], CS0_n and CS1_n for each of the 2 UI. For a 1UI command, the 2nd UI is programmed as a Deselect, with both chip selects inactive. Note that two back to back one UI commands can be programmed instead of a 2UI command, but these will always be back to back, with no programmable spacing.

There are four three-bit delay fields to specify the delay between commands 0 and 1, commands 1 and 2, commands 2 and 3, and command 3 to start of the repeat sequence.

Following the execution of command 3, the sequence will optionally repeat. The sequence can repeat starting at any command (0 through 3) and will continue again through command 3.

16 control words specify the four commands (4 registers each). Two registers specify the gap between commands. One register specifies the command to repeat from and enables repeating. One register contains a start bit for each channel. Writing a 1 to a start bit begins the sequence on that channel. Writing a 0 stops the sequence. The sequencer

is common to the two channels, so the sequence cannot be started on the two channels at different times. The commands operate in either 1N or 2N mode as specified by the existing 1N/2N mode bit. VHost Commands are sent across the BCOM bus to the data buffers. VHost is not supported during SRE/PDE/Initialization or when any training mode is enabled. The commands processed by the VHost logic are not interpreted by the RCD. For example, if the programmed commands include PDE or SRE, those commands will be sent to the DRAMs but they will not cause the RCD to power down. VHost settings can-not be modified while the VHost state machine is running. The RCD will auto stop after cmd3 executes if repeat is not enabled. RST, DCK signals must be applied on the host interface during VHost mode.

3.3.10.1 VHost Lockout mode

When the RCD receives an In-band MRW to RW01 the RCD will Lockout the VHost mode until the next DRST_n assertion. SMBus sideband write to RW01 will not trigger the lockout mechanism.

Suppliers must guarantee a permanent lock out with a fuse option.

3.3.11 Transparent Mode

The DDR5RCD01 supports a transparent mode feature of the data buffer that enables testing of LRDIMMs. The RCD will disable parity checking automatically when this mode is entered.

To enter transparent mode, the host first sends an MRW command with RW82[0] = 1 to enable transparent mode in the DDR5DB01. Then it sends an MRW command with RW00[7] = 1 to enable transparent mode in the RCD.

While in transparent mode, the DDR5DB01 does not interpret BCS_n and BCOM commands. For BCS_n input value of “1” and BCOM[2:0] input values of “111”, it directs the data flow from host interface to DRAM interface. For BCS_n input value of “1” and BCOM[2:0] input values of “000”, it directs the data flow from DRAM interface to host interface. Any other input values of BCS_n and BCOM[2:0] are invalid.

While in transparent mode, the RCD drives BCS_n statically to “1” and BCOM[2:0] statically to “111” (DES) when the DPAR input is LOW, and BCS_n to “1” and BCOM[2:0] to “000” when the DPAR input is HIGH. All output signals in the RCD, other than BCS_n and BCOM[2:0], continue working as they do in the normal mode of operation. In other words, all the RCD features and functions not directly related to DPAR, BCS_n and BCOM[2:0] remain operational in transparent mode. In addition, all the clock frequencies and PLL operational modes available in low-speed test mode and normal operation mode will be supported in transparent mode. Input DPAR_A controls outputs BCOM[2:0]_A and input DPAR_B controls outputs BCOM[2:0]_B, correspondingly.

To exit transparent mode, the host sends an MRW command with RW00[7] = 0 to exit RCD transparent mode following by issuing a Data Buffer reset command via RW04 to exit DDR5DB01 transparent mode.

3.3.12 CA Validation Pass-Through Mode

To facilitate DRAM or RCD validation the RCD will be required to support a validation pass-through mode. In this mode, the DCA signals are passed through to QCA, regardless of DCS assertion. In this mode, the DCS0_n and DCS1_n signals are passed through to QCS0_n and QCS1_n respectively, regardless of DCA signal state. Parity checking must be disabled prior to and during validation pass-through mode. Validation pass-through mode is entered when RW07[4]=1. When RW07[5]=1 in CA Validation Pass-through mode, all MRW which write to the RCD are blocked and further configuration is expected via the SMBus. This SMBus is not required to be driven by the controller.

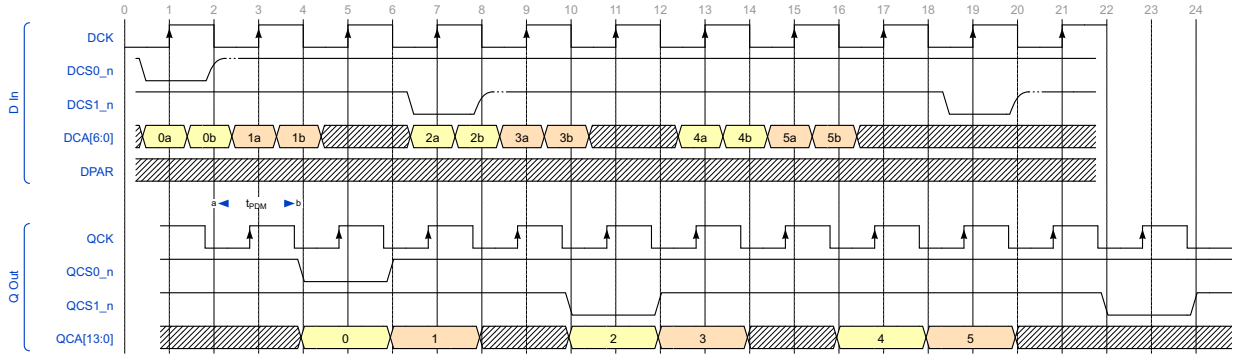


Figure 4 — Validation Pass-Through Mode - DDR

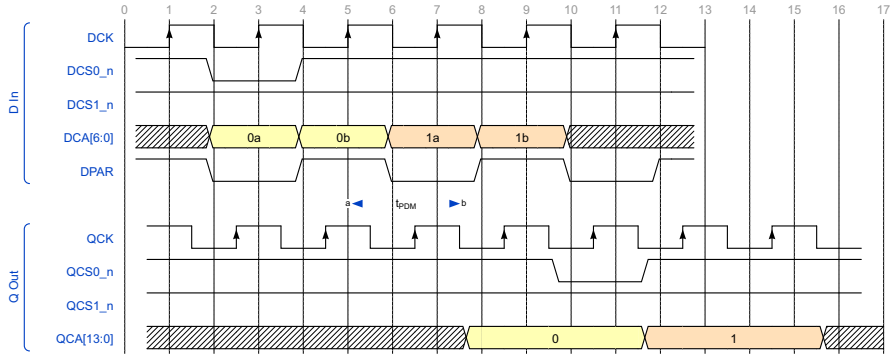


Figure 5 — Validation Pass-Through Mode - SDR1

Similar to CA Pass-Through Mode described in Section 5.2.3, when Validation Pass-Through Mode is enabled in SDR Mode, the DPAR signal will be used to indicate 1st UI QCA[6:0] (DPAR = LOW) and 2nd UI QCA[13:7] (DPAR = HIGH).

3.3.13 DRAM Interface and Data Buffer Interface Training Support

In order for the Host to train the DRAM and Data Buffer interfaces, the RCD will support two Pass Through modes: CA Pass-Through mode, described in Section 5.2.3, and BCOM Pass-Through mode, described in Section 5.2.5.

3.4 Command Address Bus

The DDR5RCD01 can support two data rates on the Host Command Address signals. The first setting is Double Data Rate (DDR) on the DCA with 1N timing on the QCA. The second is Single Data Rate (SDR) on DCA with 2N timing on the QCA to the DRAM interface. Chip Select is SDR for both settings on DCA and QCA.

Table 7 — Command Address Rates

RW00[1:0]	DCA	QCA
00	SDR1	2N timing (extra setup time)
01	DDR	1N timing
10	SDR2	2N timing (extra hold time)

3.4.1 Double Data Rate DCA

The DDR5 RCD will support DDR (Double Data Rate) on the host-interface DCA signals. The host-interface CA bus is 7 bits, plus parity. The DRAM-interface CA bus remains SDR (Single Data Rate) and is 14 bits and without parity. The RCD will expand the incoming host-interface 7-bit DCA bus to 14 bits on the DRAM interface. Table 8 shows the mapping of the incoming DCA bits to the output QCA. The Chip Selects remain SDR on both the host-interface and DRAM interface. The two channel DDR5RCD has six CA ports, two DCA input ports and four QCA output ports as shown in Figure 6.

Table 8 — DDR CA Mapping DCA to QCA

UI	DCA0	DCA1	DCA2	DCA3	DCA4	DCA5	DCA6
0	QCA0	QCA1	QCA2	QCA3	QCA4	QCA5	QCA6
1	QCA7	QCA8	QCA9	QCA10	QCA11	QCA12	QCA13

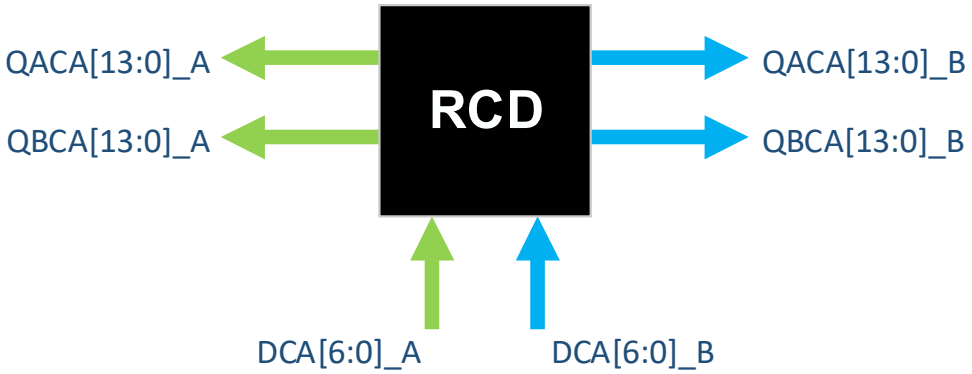
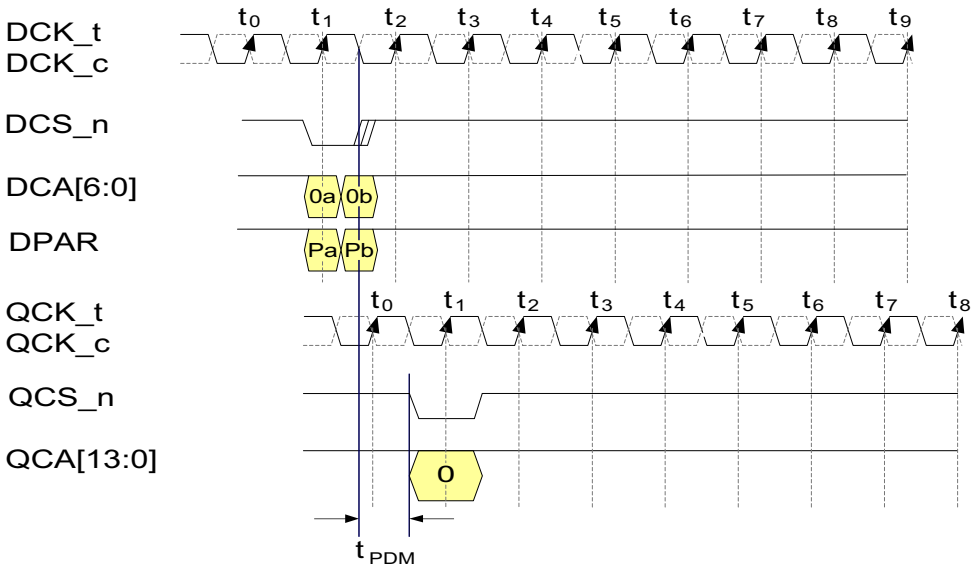


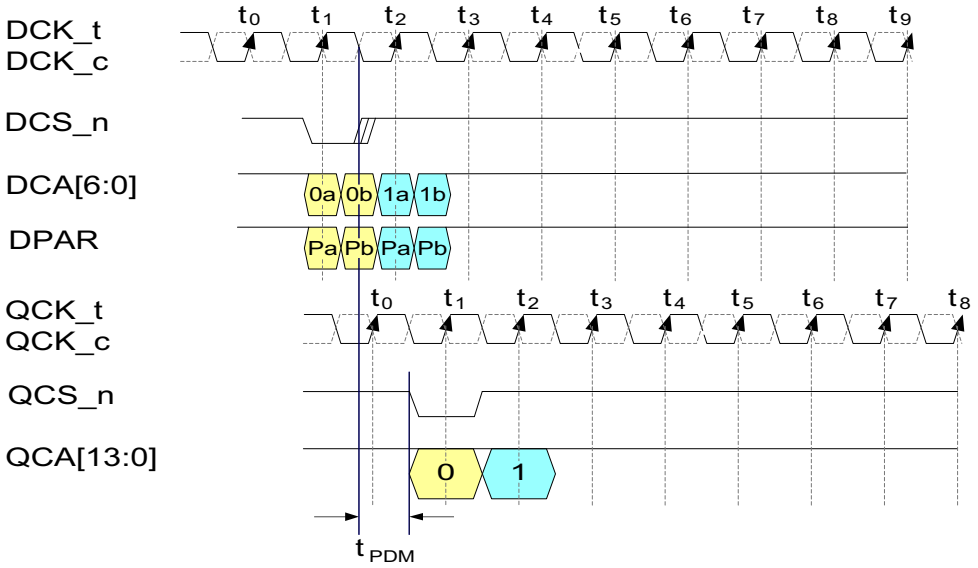
Figure 6 — RCD DCA and QCA Ports

The following timing diagrams in Figures 7, 8 and 9, show the timing relationship from the Dn inputs to the Qn outputs for a 1UI command, a 2UI command, and multiple commands.



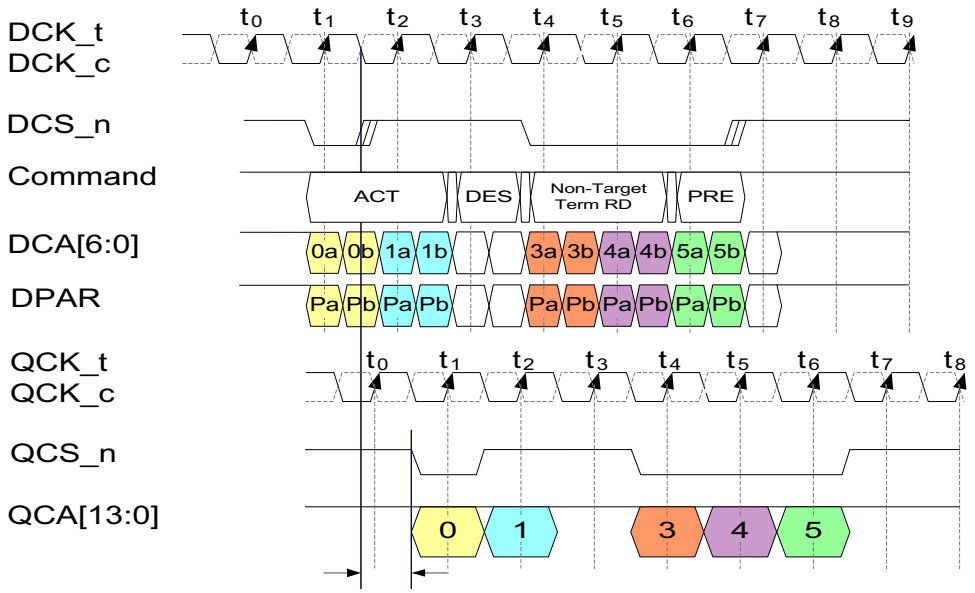
NOTE Timing Diagram for 0 nCK command latency adder.

Figure 7 — One UI DRAM Command Timing Diagram



NOTE Timing Diagram for 0 nCK command latency adder.

Figure 8 — Two UI DRAM Command Timing Diagram



NOTE Timing Diagram for 0 nCK command latency adder.

Figure 9 — DDR CA Multi-Command Timing Diagram Example

The DCS_n signal is SDR and is sampled by the RCD on the rising edge of DCK. See Section 13.11 on page 213 for details on DCS input receiver electrical and timing parameters. The DDR5RCD must maintain output timings to the DRAM and comply with the output tolerance skew parameter t_{QSK} as shown in Figure 10.

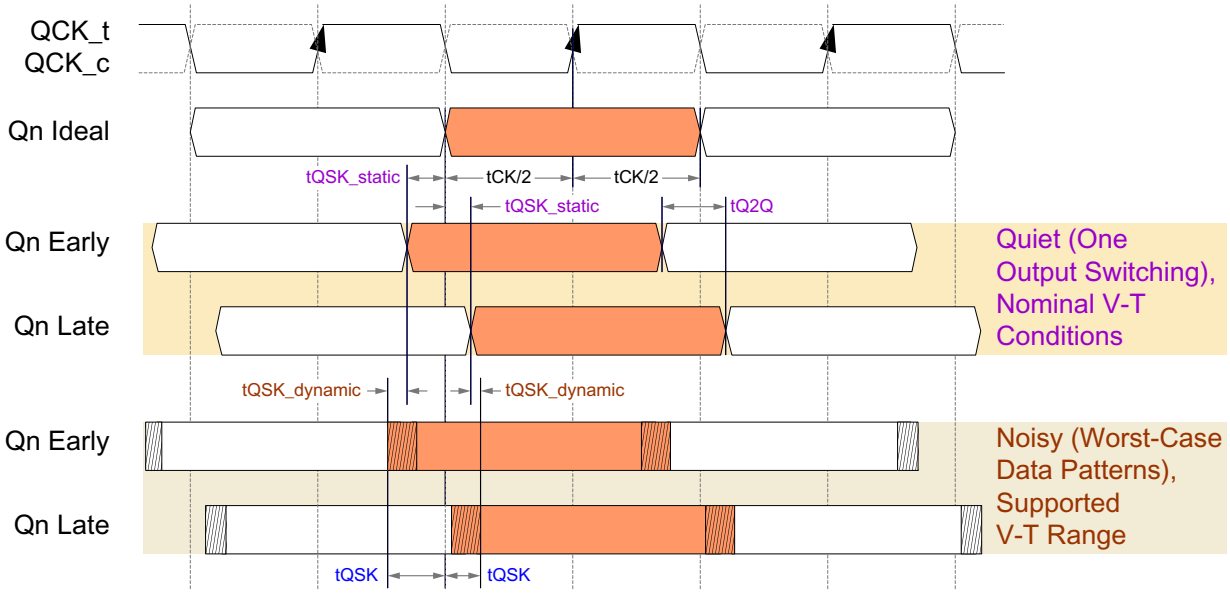


Figure 10 — Qn Output Skew

NOTE For Figure 10 outputs as specified in Table 191, “Output timing requirements” Footnote 6.

3.4.2 Single Data Rate DCA

The DDR5RCD01 will support SDR (Single Data Rate) on the host-interface DCA signals. In this case, the RCD will apply 2N timing to the DRAM interface signals. This allows more setup or more hold time on the QCA bus. This mode is enabled when RW00[0] = 0. DDR5 has defined two-cycle commands that require the RCD to capture the commands differently between DDR and SDR modes. In both modes, the first half of the command is sampled on the rising edge of clock when the chip select is active. In SDR mode, the second half of the command is sampled on the next rising clock edge. Non-target ODT signaling (through chip select inputs) is also delayed by a clock in SDR mode. For applications that require SDR on the Host interface but do not need extra setup time on the DRAM interface, QCS pulses can be pulled earlier by one clock cycle by setting RW00[1] = 1.

The QCA will follow the DRAM specification for 2N mode.

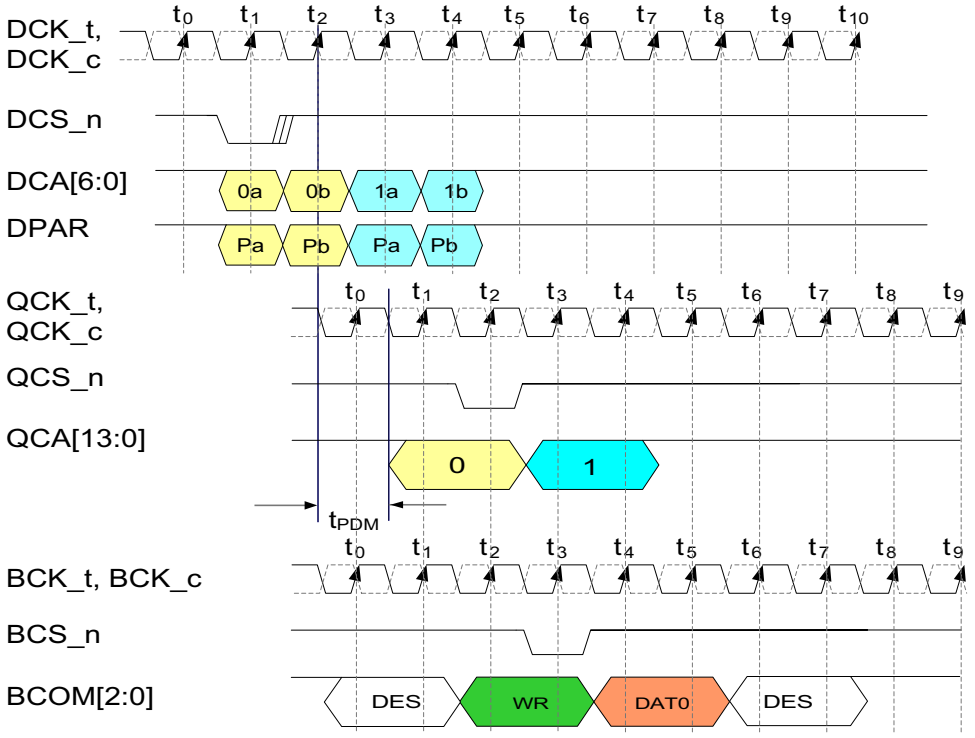


Figure 11 — SDR1 mode example of DRAM WR Command with RW00[1] = 0

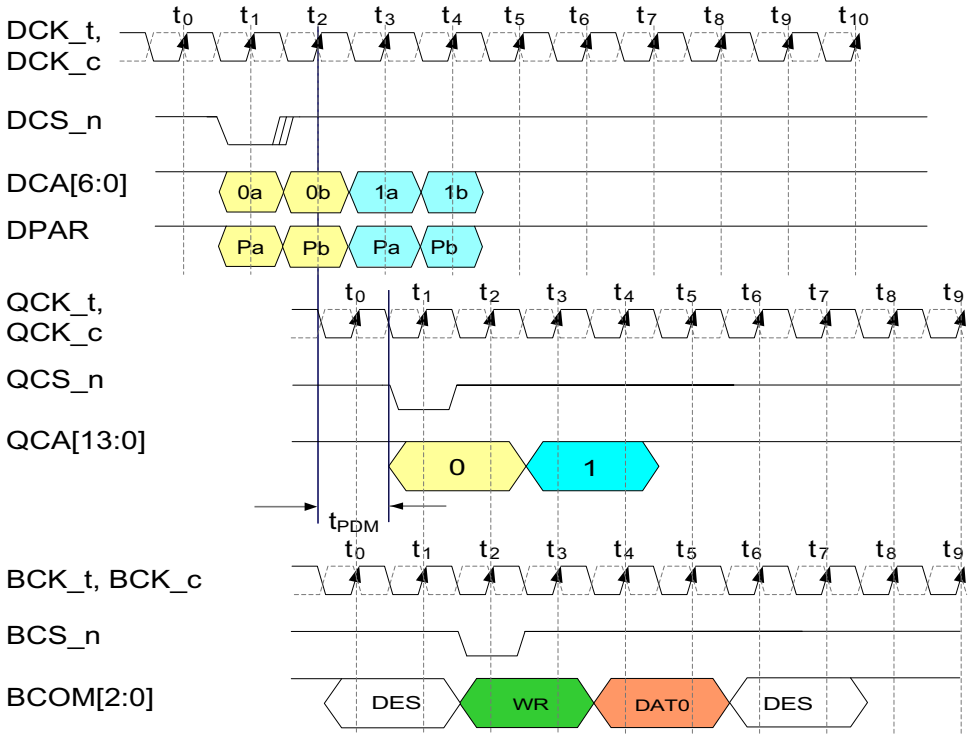


Figure 12 — SDR2 Mode example of DRAM WR Command with RW00[1] = 1

3.4.3 SDR to DDR Transition

This mode will be set through SMBus during initialization between t_{STAB01} and t_{STAB02}, or after t_{STAB01} following Exit from Self Refresh Mode with Clock Stop (see Section 4.2.2 on page 36). There is no transition during normal operation. Transitions for SDR to DDR or SDR1 to SDR2 occur prior to Host Interface Training.

3.5 Parity

The Parity function in DDR5 differs from DDR4 in several ways

- The parity signal is received on the same cycle as the command/address bits rather than one cycle later.
- 2UI DRAM commands require a different protocol to block commands when the parity error is on the 2nd UI.
- No parity signal is sent on to the DRAMs.

The convention of parity is even parity across the DCA_N[6:0] and DPAR_N signals. The Parity is checked separately per UI on the DCA bus.

Parity is checked separately on the two sub channels. A parity error on one sub channel does not affect the operation of the other sub channel.

When DDR Command Address Rate is selected, RW00[0] = 1, ALERT_n will be asserted three input clocks after rising edge of first UI of DCA in which the erroneous command is registered.

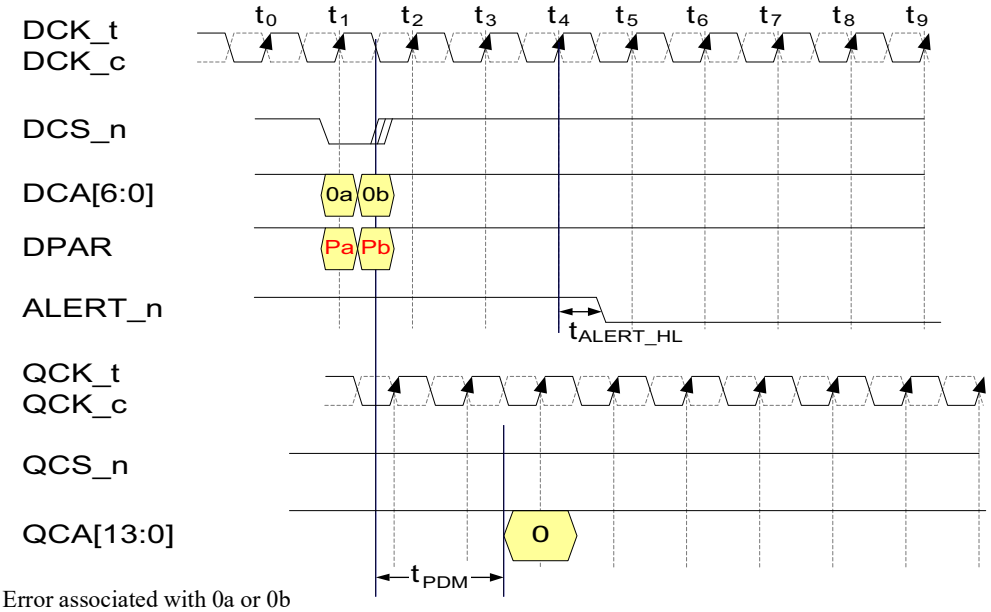
In SDR mode, RW00[0] = 0, ALERT_n will be asserted three input clocks after the rising edge corresponding to the second half of the erroneous command. This is the case regardless of the error being in the first, second or both halves.

If parity checking is disabled, the register forwards sampled commands to the outputs unconditionally, the command appears on the outputs regardless of whether a parity error occurred or not.

For single and 2 UI DRAM commands, if parity checking is enabled and there is no parity error, the register will forward the sampled commands to the outputs.

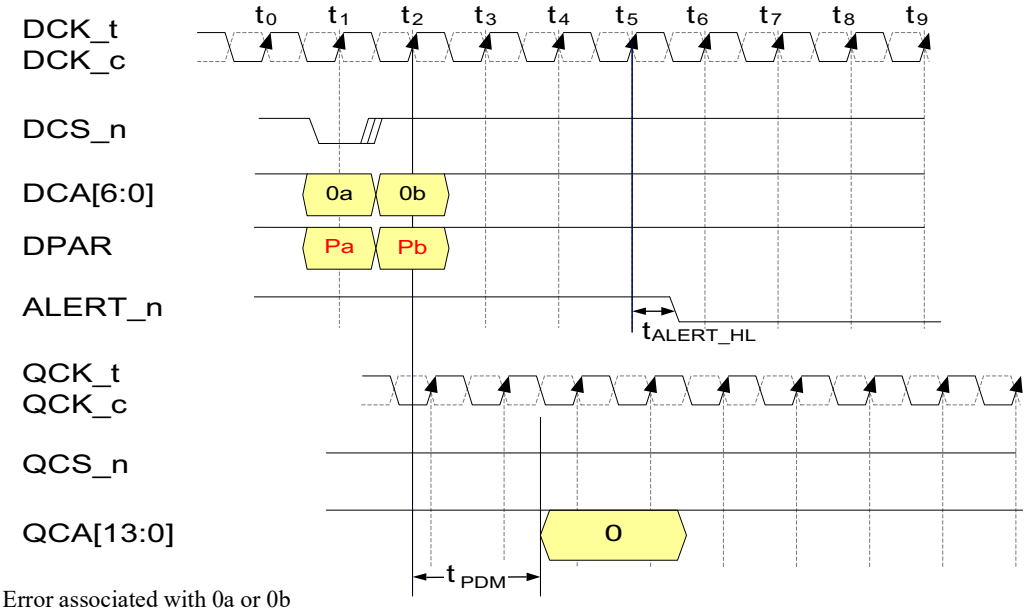
3.5.1 Single UI DRAM commands with Parity Enabled

For single UI DRAM commands, if parity checking is enabled and a parity error is detected on either UI of the DCA bus, the register will forward the command on QCA bus but will not assert any chip select to output.



Parity Error associated with 0a or 0b

Figure 13 — 1 UI DRAM Command with parity checking enabled and CLA = 0

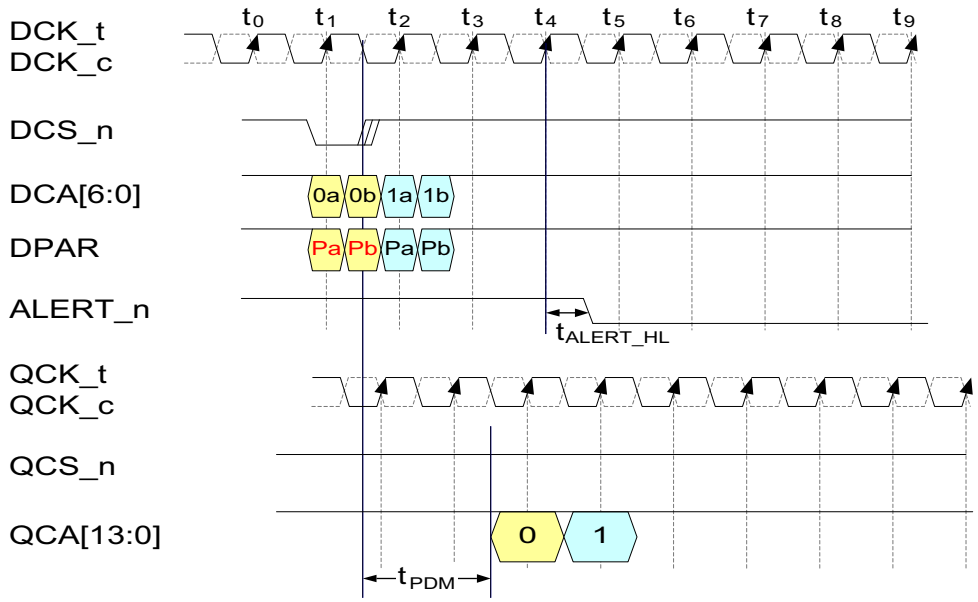


Parity Error associated with 0a or 0b

Figure 14 — SDR mode 1 UI DRAM command with parity checking enabled and CLA = 0

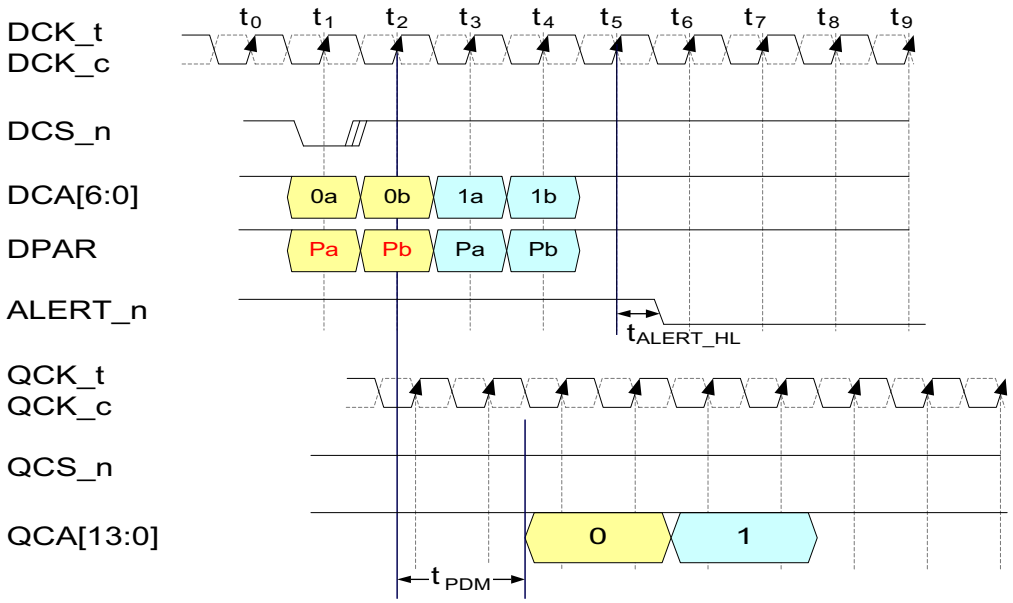
3.5.2 2UI DRAM commands with Parity Enabled

For 2UI DRAM commands, if parity checking is enabled and a parity error is detected on either UI of the DCA bus for the 1st UI of the DRAM command the register will forward the command on the QCA but will not assert any chip select output as shown in Figure 15.



Parity Error associated with 0a or 0b

Figure 15 — Error in 1st UI of 2 UI DRAM Command with parity checking enabled



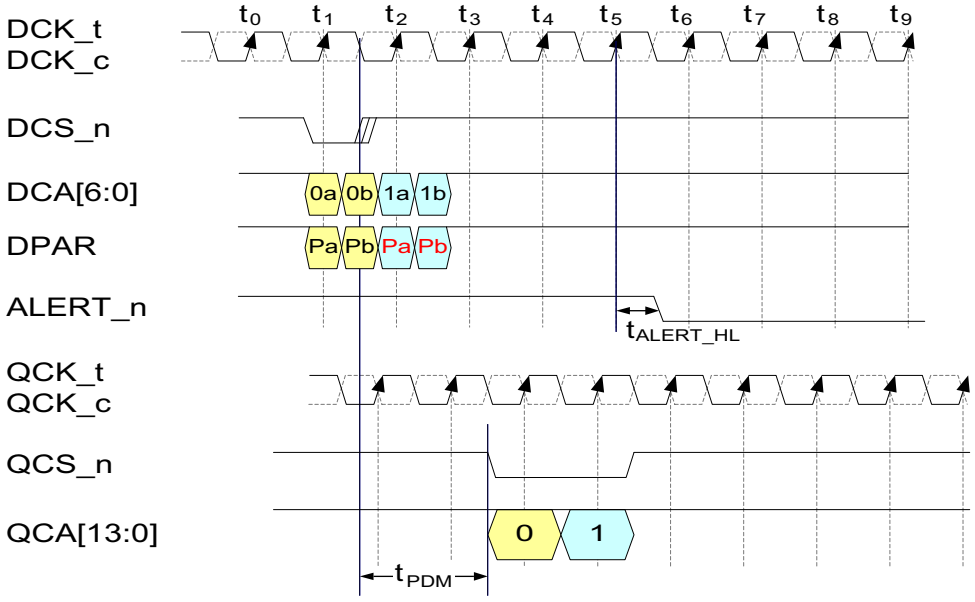
Parity Error associated with 0a or 0b

Figure 16 — SDR mode error in 1st UI of 2 UI DRAM command with parity checking enabled

For 2UI DRAM commands, if the parity error occurs in either UI of the DCA bus for the 2nd UI of the DRAM command and the 1st had correct parity, the command will have already been sent to the DRAMs. In this case the command itself will be known to be correct, but the additional address information contained in the 2nd UI will be incorrect. In order to prevent the command from being executed by the DRAM the RCD will assert the chip select in the 2nd UI also for all ranks which received a chip select in the 1st UI as shown in Figure 17.

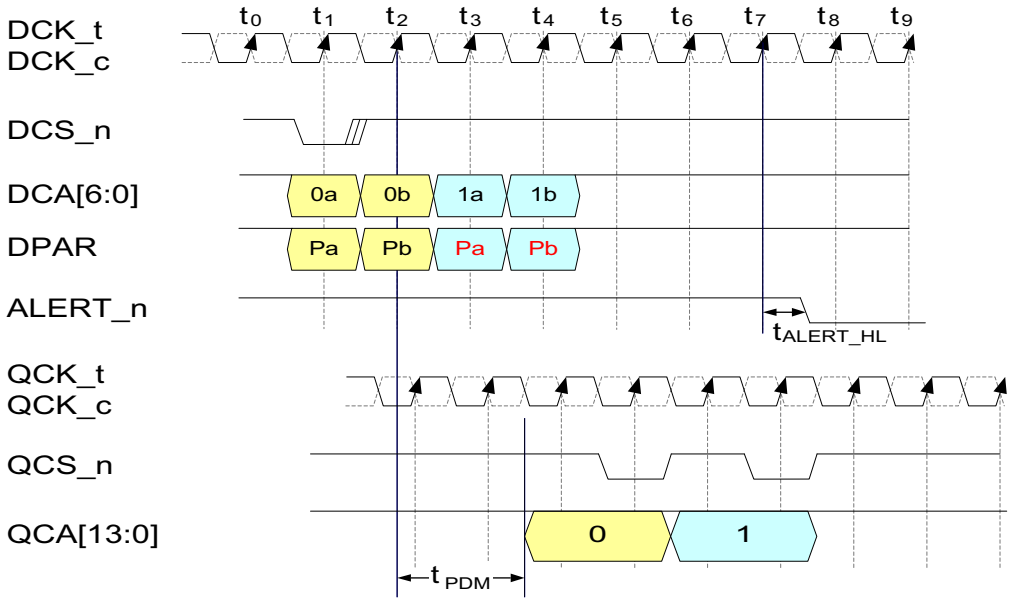
For RD, WR, and MRR commands this will convert the command to a non-target termination encoding. All ranks receiving the chip select will terminate for this command, but no rank will execute the command.

The only other 2 UI DRAM commands are the Activate, MRW, and Write Pattern commands. A DRAM seeing the chip select active for both UI of an Activate or Write Pattern command will ignore the command. Note that an MRW command will not use the data bus. The DRAM will not execute the MRW command if the chip select is asserted in both UI.



Parity Error associated with 1a or 1b

Figure 17 — Error in 2nd UI of 2 UI DRAM Command with parity checking enabled



Parity Error associated with 1a or 1b

Figure 18 — SDR1 mode error in 2nd UI of 2 UI DRAM command with parity checking enabled

If a parity error occurs on the 1st UI of a DRAM command, regardless of the command length, the command encoding itself may be corrupt. The register will be required to block all future commands until command forwarding is re-enabled. When commands are re-enabled, the register must not enable commands until it sees a UI with all CS inactive in order to avoid re-enabling in the middle of a command.

Table 9 — Blocking Commands on Parity Error

Parity error on 1st DRAM UI	Parity error on 2nd DRAM UI	Outputs
No	No	Command is forward to DRAM
No	Yes	First UI of command forward to DRAM. 2nd UI of command forward to DRAM, but with QCS asserted on ALL ranks which received a DCS on the 1st UI. Future commands not sent until parity checking is re-enabled.
Yes	Yes or No	First UI and Second UI of the command forward to DRAM but QCS is not asserted. Future commands not sent until parity checking is re-enabled.

3.5.3 ALERT_n Assertion

The behavior of ALERT_n with parity checking disabled is the same as when parity checking is enabled with the exception that ALERT_n is never asserted as result of a CA parity error. However, when parity checking is disabled, ALERT_n can still be asserted as a result of an assertion of the DERROR_IN_n input.

After the RCD receives DPAR_N from the memory controller, it compares it with the data received on the CA inputs and indicates on its open-drain ALERT_n pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[1:0]_n signals being Active, or the 2nd UI of a 2UI DRAM Command.

The convention of parity is even parity across the DCA and DPAR signals. Parity is checked independently for the two channels.

If a parity error occurs and parity checking is enabled in RW01, the RCD sets the ‘CA Parity Error Status’ bit in RW24 to ‘1’and disables parity checking. ALERT_n is asserted three input clocks after the erroneous command is registered.

If the ‘CA Parity Error Status’ bit is ‘0’, the RCD logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a ‘Clear CA Parity Error Status’ command is sent if the ‘ALERT_n Assertion’ bit in the Parity Control Word RW01 is ‘0’. In this case the erroneous command and all subsequent commands are not forwarded (i.e., QxCSy_N_n are not asserted) to the DRAM until the memory controller issues a ‘Clear CA Parity Error’ command, which will also clear the ‘CA Parity Error Status’ bit in the Error Log Register.

If the ‘ALERT_n Assertion’ bit is ‘1’, the ALERT_n pulse width is as defined in Table 100 on page 126 with start of the ALERT_n pulse width counted from the third input clock edge after the 1st parity error. The erroneous command and all subsequent commands are not forwarded (i.e. QxCSy_N_n are not asserted) to the DRAM until the end of the ALERT_n pulse width. After the ALERT_n pulse, the device will automatically resume forwarding commands to the DRAM.

- If the ‘ALERT_n Re-enable’ bit is ‘0’, parity checking remains disabled until a ‘Clear CA Parity Error’ command is sent, which will also clear the ‘CA Parity Error Status’ bit in the Error Log Register.
- If the ‘ALERT_n Re-enable’ bit is ‘1’, the device will re-enable parity checking after the ALERT_n pulse. The ‘CA Parity Error Status’ bit will remain set. If a subsequent parity error is detected, the device will re-enter the parity error state and set the ‘> 1 Error’ bit. The other bits in the Error Log Register are not updated on this subsequent error. Both the ‘CA Parity Error Status’ bit as well as the ‘> 1 Error’ bit will be cleared by sending a ‘Clear CA Parity Error’ command.

3.6 DCA Decision Feedback Equalization

Since the DCA will be Double Data Rate the RCD will support a 4 Tap DFE on the DCA host-interface receivers. The 4-tap DFE subsystem consists of a gain amplifier, a DFE summer, 4 CA slicers (also called Taps) with outputs that loop back to the DFE summer, and a coefficient multiplier for each Tap. The gain control of the front end is used to ensure that the cursor or the current bit is in a congruent relationship with the ISI correction required for the channel. The taps C1, C2, C3, C4 coefficients provide the corrections needed to the current bit by adding or subtracting the effects of ISI of the previous bits. The host can enable 1, 2, 3 or 4 taps in a consecutive order always starting with Tap 1 as shown in Table 10, “DFE Tap Configurations”. DFE input gain adjustment and DFE Tap Coefficients 1 through 4 are set by control words located in PG[1:0]. These DFE control words allow programming of each parameter on a DCA I/O-specific basis, and they are intended to be trained by the host. The DDR5RCD01 device does not support adaptive DFE, and it only supports DFE when its DCA host interface is configured in DDR mode (i.e., RW00[0] = 1).

3.6.1 DFE Tap Configurations

Table 10 — DFE Tap Configurations

RW31 OP4	RW31 OP5	RW31 OP6	RW31 OP7	Tap 1	Tap 2	Tap 3	Tap 4
0	x	x	x	Disabled	Disabled[1]	Disabled[1]	Disabled[1]
1	0	x	x	Enabled	Disabled	Disabled[2]	Disabled[2]
1	1	0	x	Enabled	Enabled	Disabled	Disabled[3]
1	1	1	0	Enabled	Enabled	Enabled	Disabled
1	1	1	1	Enabled	Enabled	Enabled	Enabled

1. DDR5RCD01 hardware disabled when RW31[4] = 0 and RW31[7:5] are don't care and ignored by the RCD.
2. DDR5RCD01 hardware disabled when RW31[5] = 0 and RW31[7:6] are don't care and ignored by the RCD.
3. DDR5RCD01 Hardware disabled when RW31[6] = 0, and RW31[7] is a don't care and ignored by the RCD.

3.6.2 DFE Gain and Tap Range

Table 11 — DFE Gain and Tap Total Control Word Range

DFE Parameter	Min	Max	Unit
Gain	-6	6	dB
Tap1	- 150	45	mV
Tap 2	- 60	45	mV
Tap 3	- 45	45	mV
Tap 4	- 45	45	mV

Table 12 — DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin

DFE Parameter	DDR5-3200 - 4800			Unit
	Min	Typ	Max	
DFE Gain Bias Step Size[1,2]	1.7	2	2.3	dB
DFE Gain Bias Tolerance (INL)[1,2]	- 0.5	-	0.5	dB
DFE Gain Bias Step Size Tolerance (DNL)[1,2]	- 0.3	-	0.3	dB
DFE Gain Bias Step Time[1]	-	-	300	ns
DFE Tap Bias Step Size[1,2]	1	3	5	mV
DFE Tap Bias Tolerance (INL) (-150 mV to 0 mV)[1,2]	Min (V_ideal x 115%, V_ideal - 3 * LSB)[3,4]	-	Max (V_ideal x 85%, V_ideal + 3 * LSB)[3,4]	mV
DFE Tap Bias Tolerance (INL) (0 mV to 45 mV)[1,2]	V_ideal - 3 * LSB[3,4]	-	V_ideal + 3 * LSB[3,4]	mV
DFE Tap Bias Step Size Tolerance (DNL)[2]	- 66.67	-	66.67	% of Step Size
DFE Tap Bias Step Time	-	-	64	tCK

1. Host Vref fixed at 0.75 x V_{DD}, typical Voltage-Temperature condition (i.e., V_{DD} = 1.1 V, 25 °C), and default gain setting.
2. These parameters are neither subject to silicon validation nor production testing.
3. V_ideal refers to the ideal DFE Tap value based on the setting.
4. LSB = 3 mV.

3.7 RX Loopback

3.7.1 Loopback Mode

When the loopback circuit is enabled in RW26 the DDR5RCD01 can feed a received signal or internal data back to the host for debugging, testing, and/or training purposes. Loopback Mode and DFE Training Mode shall not be enabled simultaneously. Loopback is necessary in order for the host memory controller or test instrument to immediately read back data that was written to the RCD, DRAM or Data Buffer without having to issue multiple DRAM WRITE/READ commands. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis.

For example, at BER=10^{-16}:

1. There is not enough memory depth in the DRAM to store all the 10^{16} data.
2. The amount of time to perform multiple WRITE/READ commands to and from the array is prohibitively long.
3. Since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the host or memory controller must also manage Refreshes during testing to ensure data retention.
4. Limited pattern depth means limited Inter symbol Interference (ISI). Loopback is a necessity for characterizing the receiver without the limitations and complexities of other traditional methods.

3.7.2 Loopback Ports

There are five RCD loopback ports, four input ports and one output port. The input ports consist of two internal and two external port as shown in Figure 19. Each port contains one data signal and one strobe signal. RW26 selects the internal or external signals to loopback to the Host on the output port. Transitions in the incoming data signal are aligned to the rising edges of the incoming strobe. The RCD will sample incoming data with the falling edges of the incoming strobe and it will drive the strobe and data signals out to the host controller. The RCD will apply logic inversion in the outgoing strobe signal to ensure output data signal transitions are aligned to the rising edges of the corresponding strobe signal as shown in Figure 20.

Internal RCD Loopback is only intended to send back the output of the functional path slicer. Internal RCD Loopback is independent from RW32[2:1] Training Source selection field.

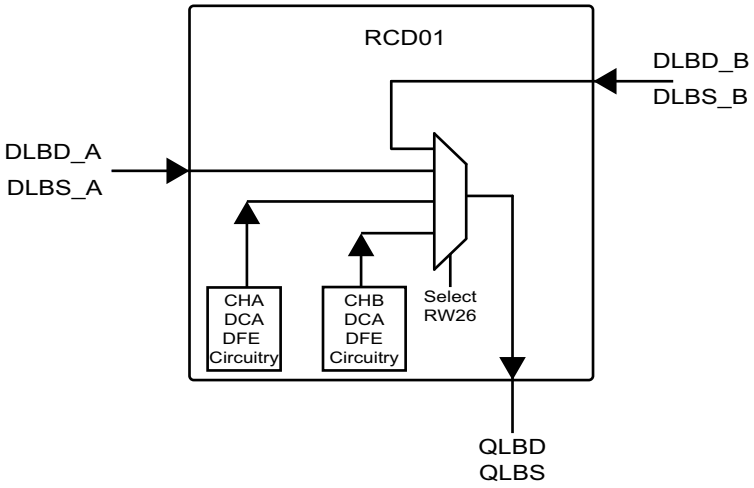
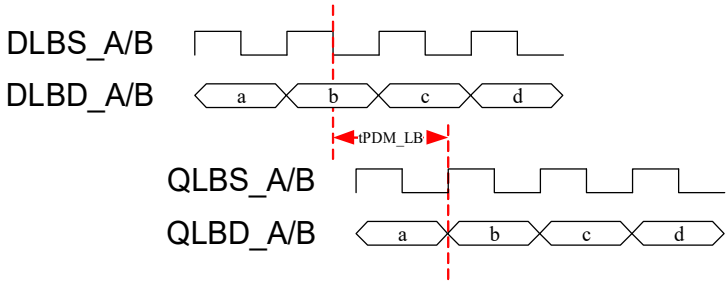


Figure 19 — RCD Loopback Ports

3.7.3 Pin Assignment for Loopback

Inputs (From DB or DRAM)
DLBD_A
DLBS_A
DLBD_B
DLBS_B

Outputs (To Host)
QLBD
QLBS



NOTE A waiting time $t_{Ext_LB_Entry}$ applies when External Loopback is enabled in RW26[2:0].

Figure 20 — External Loopback Timing Diagram

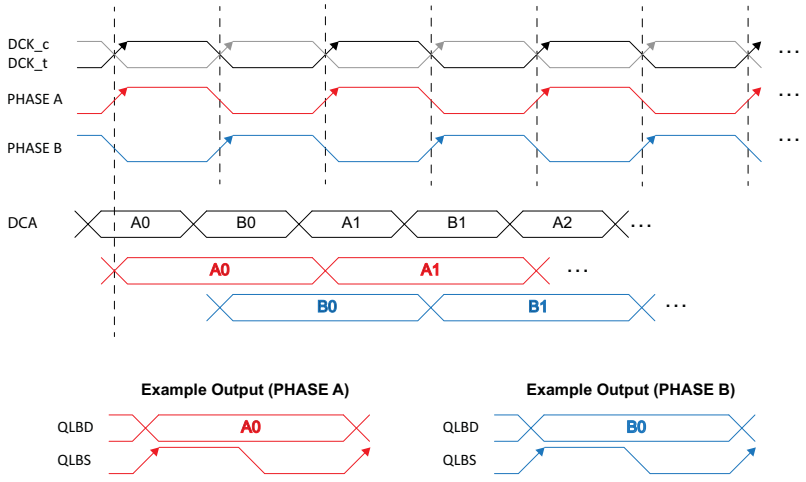


Figure 21 — Internal Loopback A & B Phase

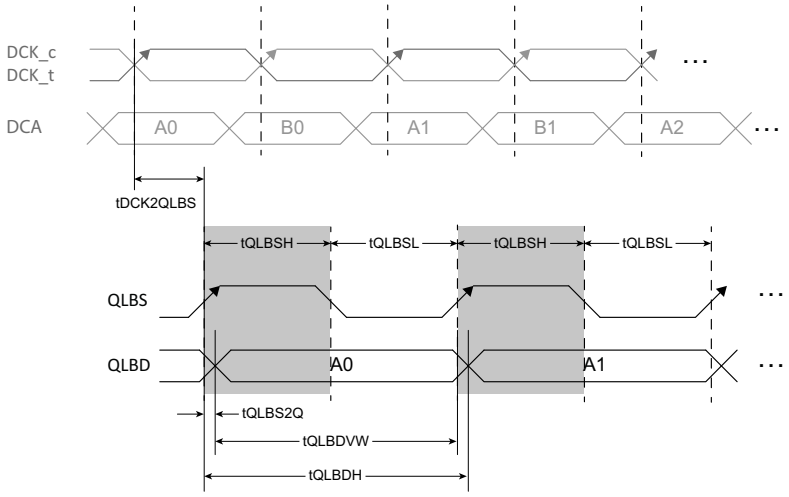


Figure 22 — Loopback Output Timing Parameters

3.8 Device Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. After the voltage ramp, stable power is provided for a minimum of t_{RINIT1} µs with DRST_n asserted. When the reset input DRST_n is LOW, all input receivers are disabled, and shall be left floating. In addition, when DRST_n is LOW, all non-sticky control registers are restored to their default states, which is all '0's unless explicitly stated otherwise. The outputs QRST_n, and BRST_n must drive LOW. All other Qx outputs must float with the exception of the QCS[x]_n outputs, which are driven LOW. The RCD must float QLBD, QLBS and ALERT_n outputs. As long as the DRST_n input is pulled LOW, the register is in low-power state and input termination is not present.

The DDR5RCD01 device will not affect DRST_n signal voltage levels even when V_{DD} is not powered on. An RCD with V_{DD} powered off shall not prevent other devices connected to the same DRST_n net from receiving the correct High and Low logic voltage levels driven by the host on that net. Also, the DDR5RCD01 device will not sustain permanent damage if DRST_n is driven HIGH (to V_{IH} levels) when V_{DD} is powered off, and it must be able to support all the specified features and functions once power is restored.

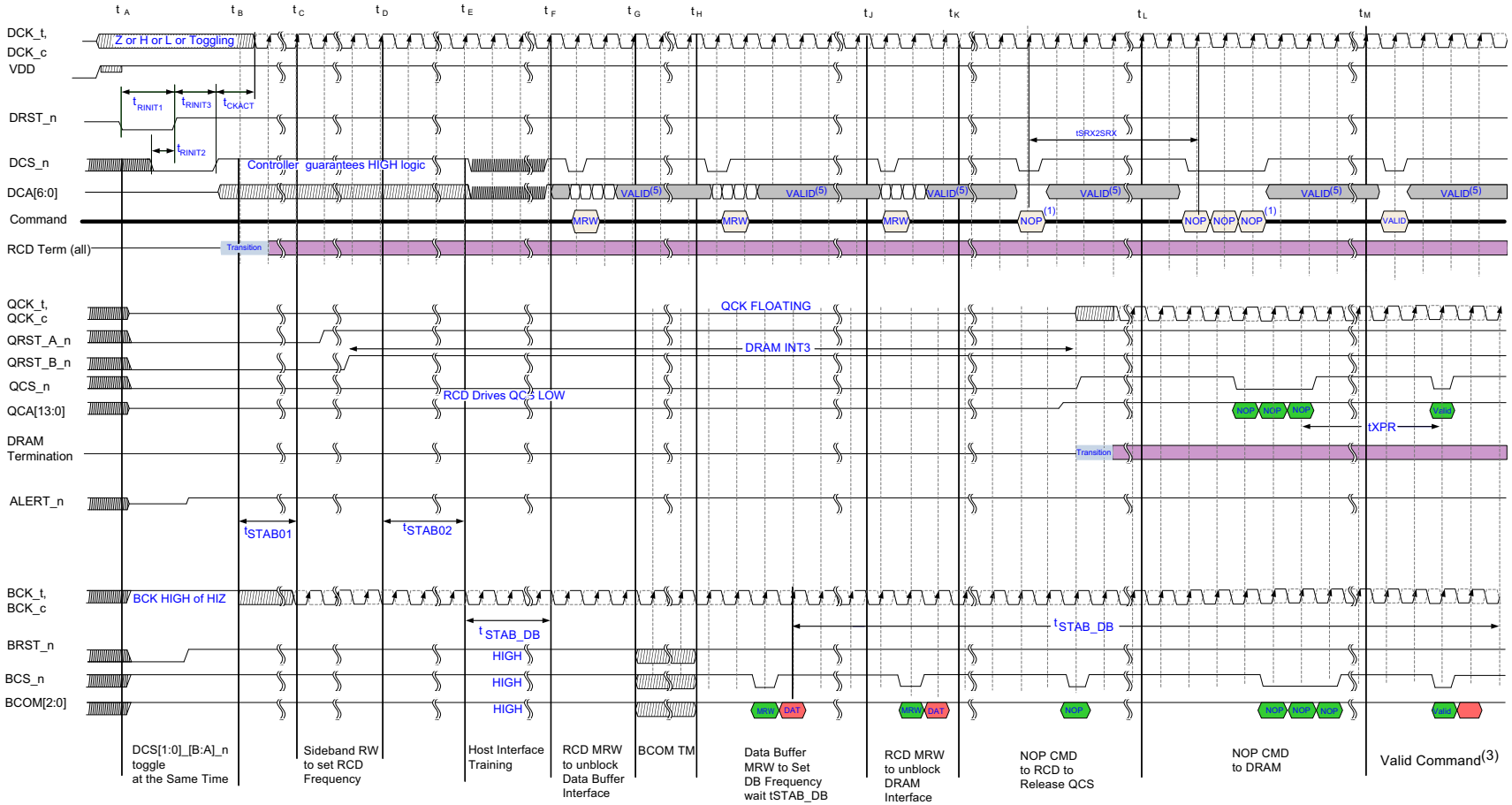
Before the DRST_n signal goes HIGH, all DCS_n inputs are driven LOW by the host controller. This puts the signals in a similar state as self refresh allowing the initialization and self refresh protocol to be similar. After DRST_n goes HIGH, the DCS_n input signals will go HIGH. The host may stagger (i.e., delay) this transition between sub-channels by up to $t_{DCSLHSK1}$, but DCS0_n and DCS1_n within each sub-channel can only be staggered by up to $t_{DCSLHSK2}$. This transition will enable the termination on the DCS_n, DCA, and DCLK inputs. The host will start the DCK clock early enough to meet t_{CKACT}[1]. After t_{STAB01}, the SidebandBus Interface is operational and the host controller will write the coarse and fine grain frequency registers and put the RCD in the proper DCA input mode (DDR or SDR). The host controller must then wait t_{STAB02} to allow the PLL to re-lock.

Training of the DCS and DCA signals now takes place, followed by BCS and BCOM training if applicable. Commands to the DRAMs are blocked by default, and the DRAM QCS signals will remain LOW.

The QRST_n outputs will remain LOW after DRST_n goes HIGH. The QRST_n signals do not go HIGH until the host writes the Command Control Word with the commands to do so. This may be done via the SidebandBus or in-band. The QRST_n signal for each sub channel is controlled separately to allow staggering of the signals for power supply inrush control.

As part of the power-on initialization, all control words are reset to their default state. After initialization, the Host must write to those control registers whose contents are required for frequency and DIMM configuration.

1. Since DCS_n Low-to-High transitions can be staggered by up to $t_{DCSLHSK1}$ (for the entire chip) or $t_{DCSLHSK2}$ (within the same sub-channel), t_{CKACT} must be met with respect to the DCS_n signal with the earliest rising transition.



1. The NOP (SRX) Commands that release QCS outputs, and the consecutive NOP Commands sent to the DRAM after that, are required to meet RCD parameters tDCSLHSK1 and tDCSLHSK2 as well as DRAM parameter tCSH_SRexit.
2. QRST outputs remain LOW until RCD receives RW04 command to de-assert reset.
3. Valid command shown in diagram, includes the MPC command, DRAM default 2N mode.
4. Sideband Interface becomes enabled for Private Write/Read access and DEVCTRL CCC with RegMode = 1 at time tC.
5. Valid signal timing and levels required if DFE is enabled.

NOTE For RDIMM, Steps t_F through t_J are not required.

Figure 23 — Timing of Clock and Data During Initialization Sequence

From a device perspective, the initialization sequence must be as shown in Table 13.

Table 13 — DDR5RCD01 Device Initialization Sequence at Power-on Ramping

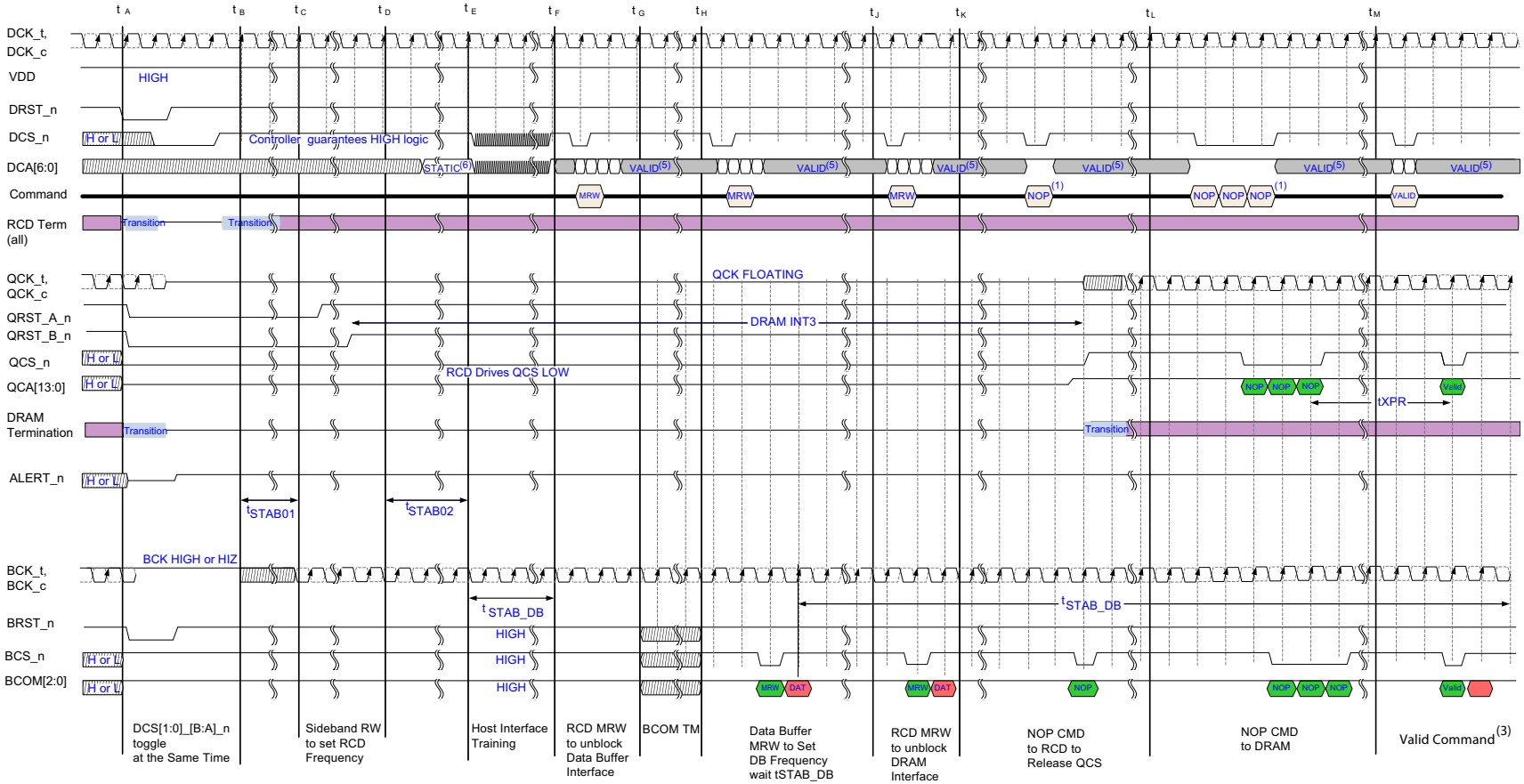
Step	Power	Inputs: Signals provided by the controller					RCD Input Termination	Outputs: Signals provided by the device				
	V_{DD}	DRST_n	DCS[1:0]_n	DA/C	DPAR	DCK_t, DCK_c	DCS, DCA, DCK Term	QCS[1:0]_n	QRST_n	QCA	ALERT_n	QCK_t, QCK_c
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	OFF	Z	Z	Z	Z	Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	OFF	X or Z	X or Z	X or Z	X or Z	X or Z
2	V_{DD}	L	X or Z	X or Z	X or Z	X	OFF	L	L	Z	H	Z
3	V_{DD}	L	L	X or Z	X or Z	X	OFF	L	L	Z	H	Z
4	V_{DD}	H	L	X or Z	X or Z	X	OFF	L	L	Z	H	Z
5	V_{DD}	H	H	X	X	running	ON	L	Note 2	Z	H	Z

NOTE 1 X = Logic LOW or Logic HIGH. Z = Floating

NOTE 2 QRST_n goes HIGH with the proper Command Control Word write.

3.9 Reset Initialization with Stable Power

The timing diagram in Figure 24 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. DRST_n will be asserted for minimum 1 µs. This DRST_n timing is based on DDR5 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual DRST_n timing can vary based on specific system requirement, but it cannot be less than 1 µs. Some of the steps in Figure 24 could be skipped by taking advantage of control words with sticky attributes.



1. The NOP (SRX) Commands that release QCS outputs, and the consecutive NOP Commands sent to the DRAM after that, are required to meet RCD parameters tDCSLHSK1 and tDCSLHSK2 as well as DRAM parameter tCSH_SRexit.
2. QRST outputs remain LOW until RCD receives RW04 command to de-assert reset.
3. Valid command shown in diagram, includes the MPC command.
4. Sideband interface is not operational for Private Write/Read access and DEVCTRL CCC with RegMode = 1 between times tA to tC.
5. Valid signal timing and levels required if DFE is enabled.
6. HIGH or Valid signal levels required to be held static for a minimum tDFE_PRD time prior to first assertion of DCS if DFE enabled.

NOTE For RDIMM, Steps t_F through t_J are not required.

Figure 24 — Reset Initialization With Stable Power

Table 14 — DDR5RCD01 Device Initialization Sequence when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller					RCD Input Termination	Outputs: Signals provided by the device				
	V_{DD}	DRST_n	DCS[1:0]_n	DA/C	DPAR	DCK_t, DCK_c	DCS, DCA, DCK Term	QCS[1:0]_n	QRST_n	QCA	ALERT_n	QCK__t, QCK__c
1	V_{DD}	H	X	X	X	running	ON	X	H	X	X	running
2	V_{DD}	L	X	X	X	X	Transitioning	L	L	Z	H	Z
3	V_{DD}	L	L	X	X	X	OFF	L	L	Z	H	Z
4	V_{DD}	H	L	X	X	X	OFF	L	L	Z	H	Z
5	V_{DD}	H	H	X	X	running	ON	L	Note 2	Z	H	Z

NOTE 1 X = Logic LOW or Logic HIGH. Z = Floating

NOTE 2 QRST_n goes HIGH with the proper Command Control Word write.

4 Power Down operation

DDR5 does not have a separate CKE signal going to the DIMM or the DRAMs. Power Down Entry, including self refresh, is signaled via a single UI command. Following the Power Down Entry command, the CS signal effectively becomes the equivalent of the CKE signal. An inactive CS keeps the DRAM devices in the power down state. CS going active will take the DRAMs out of the power down state. A NOP command is placed on the CA bus along with CS going active so that no commands are executed by the DRAM devices. DRAMs can be put in power down mode with or without non-target ODT control.

4.1 Power Savings Modes

The DDR5RCD01 device supports the following power saving mechanisms:

- PDE Power Down Mode. The RCD goes into a low-power mode when all DRAM ranks are put into PDE Power Down.
- PDE Power Down with ODT control. In this mode ranks can be in power down mode but will still require ODT commands for termination, therefore the RCD and Data buffer will remain in normal operating mode.
- Self Refresh Modes. With and without Clock Stop.

The DRST_n input has priority over all other power saving mechanisms. When DRST_n is driven LOW, the RCD will force the Qn outputs to float (except QCS_n, QRST_n and BRST_n, which are driven LOW), de-asserts the ALERT_n output, disables Input Bus Termination (IBT) and forces BCK_t/BCK_c, BCS_n, and BCOM[2:0] HIGH or HI-Z.

4.1.1 PDE Power Down Mode

The RCD Power Down mode is handled independently between the sub-channels.

The RCD device enters power down mode when all DRAM ranks on the sub-channel have entered power down. The host controller puts DRAM ranks into PDE Power Down Mode by sending a PDE command to the rank. Due to the V_{DD} termination, all input termination remains enabled during PDE power down mode and all outputs may remain enabled. The QCA bus outputs will be all HIGH during PDE Power Down mode as they are for Deselect commands. The RCD may reduce power internally as it is able. No command may be sent on the clock cycle following the PDE command to allow the RCD to safely update its configuration for command decoding, because the DCA input receivers will be disabled and require a clock cycle to be ready to receive the NOP (PDX) command without checking parity.

Power down exit is signaled by taking one or both DCS inputs active with a PDX on the bus. The RCD will not check CA Parity when the PDX command is received while both ranks are in power down as the DCA input receivers would be disabled.

The PDE command is sent to the Data Buffers on the BCOM bus only when the last rank has entered PDE mode. The PDX command is sent to the Data Buffers on the BCOM bus when the first rank receives the PDX command. Therefore, the Data Buffers are in power down mode only when ALL ranks on the sub channel are in power down mode.

4.1.2 PDE Power Down Mode with ODT control

In PDE Power Down Mode with ODT control, the powered down rank(s) and the Data Buffers may still receive non-target termination commands. The RCD itself does not power down if either rank is in PDE with ODT control, as it must pass on the non-target termination commands. QCA11 determines whether the DRAMs are put into PDE with or without ODT control. QCA11 = 1 for no ODT control, and QCA11 = 0 for ODT control.

While in PDE with ODT control, RD, WR, and MRR commands may be sent to the DRAM rank with non-target termination signaled (CS active for both UI of the command). It is the responsibility of the host controller to not send commands to the DRAMs which are "Not Allowed", as defined in Table 15.

In case of Parity Error state in '*Static ALERT_n Assertion Mode*' (RW01[6] = '0'), the host needs to send MRW to the exit the Error state before the RCD can forward a PDX command on any sub-channel that had Parity Error. To avoid violating the restrictions defined in Table 15 below, MRW must not be sent to DRAMs in PDE state with ODT Control. Therefore, it is necessary to first send PDX commands so that the sub-channels that are not in parity error state can take their DRAMs out from Power-Down state with ODT control. After sending MRW to RW04, it will be necessary to send PDX for the sub-channels that were in Parity Error state initially. Based on these requirements, an example of a recovery sequence for this case could be the following.

If parity error is detected during PDE with ODT control:

1. Send PDX (NOP) to CH_A and CH_B.
2. Send MRW for RW04 CMD10 'CH_B Clear Parity Error'.
3. Send MRW for RW04 CMD9 'CH_A Clear Parity Error'.
4. Send PDX (NOP) to CH_A and CH_B.

The above example sequence in is intended to work for any combination of parity error state and PDE with ODT control per sub-channel (error or PDE in CH_A only, CH_B only, or CH_A and CH_B at the same time).

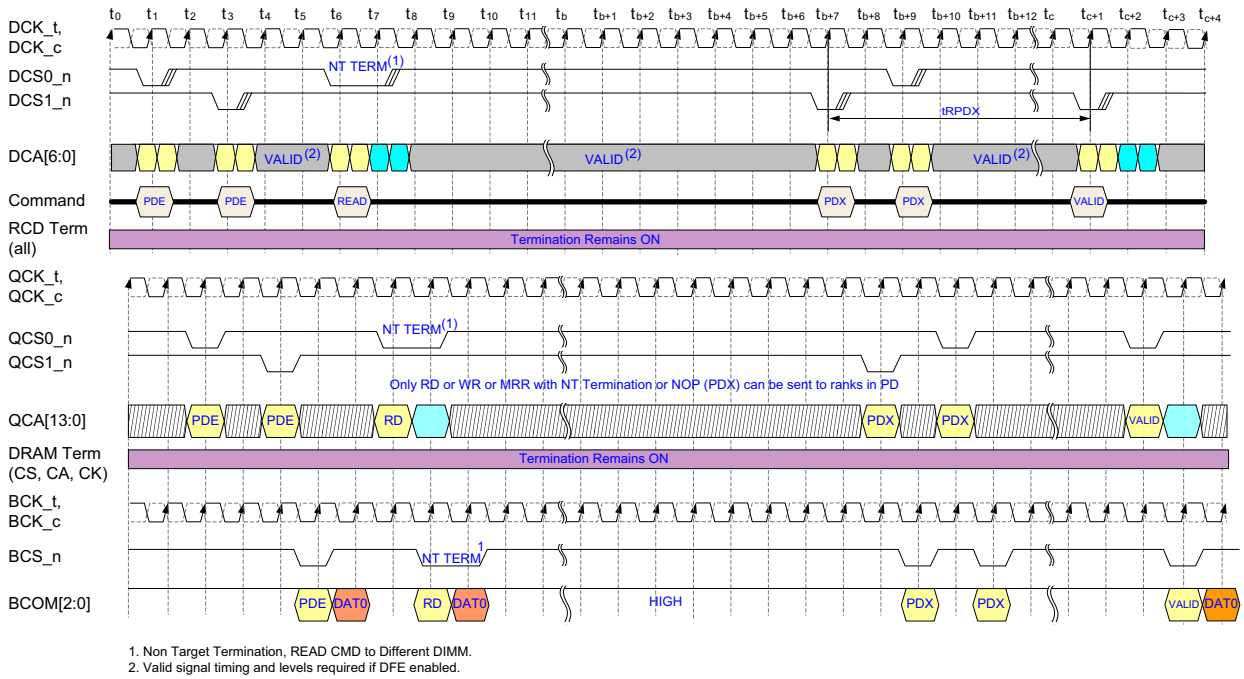
In case of Parity Error state in '*Pulsed ALERT_n Assertion Mode*' (RW01[6] = '1'), the recovery procedure can be reduced simply to the first step in the list because the DDR5RCD01 device resumes execution of DCA commands automatically after the end of the ALERT_n pulse.

The non-target termination commands must be sent to the Data Buffers if either rank is in PDE with ODT control.

Table 15 — ODT Control during Power Down Mode[1]

Mode	NOP/PDX command	RD w/ non-target term	WR w/ non-target term	MRR w/ non-target term	All Others
PDE w/o ODT control	Allowed. Exits PDE mode	Not Allowed	Not Allowed	Not Allowed	Not Allowed
PDE w/ODT control	Allowed. Exits PDE Mode	Allowed	Allowed	Allowed	Not Allowed

1. This table applies to the commands sent from the RCD to the DRAMs when the DRAMs are in PDE state with ODT Control.



1. Non Target Termination, READ CMD to Different DIMM.
2. Valid signal timing and levels required if DFE enabled.

Figure 25 — Power Down Mode Entry and Exit

4.2 Self Refresh Modes

Following the sending of SRE command, the host will EITHER assert the DCS[x]_n signals for a single clock pulse (indicating Self Refresh WITHOUT clock stop), or for the t_{CSSR} minimum (indicating Self Refresh WITH clock stop). No pulse width in between is permitted. All DCS[x]_n signals must be asserted in the same manner.

4.2.1 Self Refresh Mode with Clock Stop Entry

Self Refresh Mode is a very low power state in which the input clocks will stop, and both the RCD and DRAM inputs terminations are disabled.

Self-refresh entry is signaled when the host sends SRE commands to both ranks within a sub-channel at the same time.

After all ranks on both sub-channels have been put into self refresh with no parity error detected, the host controller will pulse the DCS[1:0]_[B:A]_n inputs for t_{CSSR} to maintain self refresh. No parity checking is done on this operation, as the DCA bus is not used.

Unlike the DDR4 RCD, there is no detection done on the clock inputs, instead the RCD will detect the last DCS_n transitions to LOW of the CS pulse to disable DCK, DCA and DCS_n terminations. The host controller will stop the clock. DCK_t and DCK_c can be driven LOW or can be floating. The PLL is disabled and DCS[1:0]_[B:A]_n inputs are kept LOW to maintain self refresh.

The RCD outputs will be disabled with the exception of the QRST_n, BRST_n and QCS[x]_n signals to keep the DRAMs in self refresh. QCS_n signals are driven LOW. BCK_t/BCK_c, BCS_n, and BCOM[2:0] signals will be driven High or HI-Z by RCD during the clock-stop event. Note that the BCS_n is NOT driven LOW when in self refresh.

If a parity error is detected on any of the self refresh entry commands the host will take any DIMMs or sub-channels already in self refresh out of self refresh and retry the entry operation.

4.2.2 Exit from Self Refresh Mode with Clock Stop

Exiting Self Refresh Mode is accomplished when the first DCS_n input transitions HIGH. The host may stagger (i.e., delay) this transition between sub-channels by up to $t_{DCSLHSK1}$, but DCS0_n and DCS1_n within each sub-channel can only be staggered by up to $t_{DCSLHSK2}$. This transition will re-enable the termination on the DCK, DCS, and DCA inputs and enable the PLL. The host will start the DCK clock early enough to meet t_{CKACT}[1], and wait for the PLL(s) to lock. After t_{STAB01}, the SidebandBus Interface is operational. Note that the DCS[x]_n inputs going HIGH does NOT pass through to the DRAMs at this point.

Once the PLL is locked, using the SidebandBus Interface, the host is allowed to change the Command/Address bus rate settings in RW00[1:0] (requires meeting Footnote 7 in Table 190). The host is also allowed to use DCS, DCA, and DFE Training Modes, including DFE Sweep Accelerator, through SidebandBus to train the DCS and DCA signals if needed due to a modification of the DCK frequency. In case of LRDIMM, if there was a change in DCK frequency, it may also be necessary for the host to train the BCOM signal timings from RCD to Data Buffers using BCOM Pass-Through Mode in the RCD and BCOM Training Mode in the DB. The host controller will send NOP (SRX) commands to each rank, which will take the QCS[x]_n outputs HIGH. This will enable the termination on the DRAMs. The RCD starts the QCLK outputs at this time and begins passing commands through to the DRAMs. The host controller will then send three back-to-back NOP commands to each rank, which completes the exit of self refresh in the DRAMs.

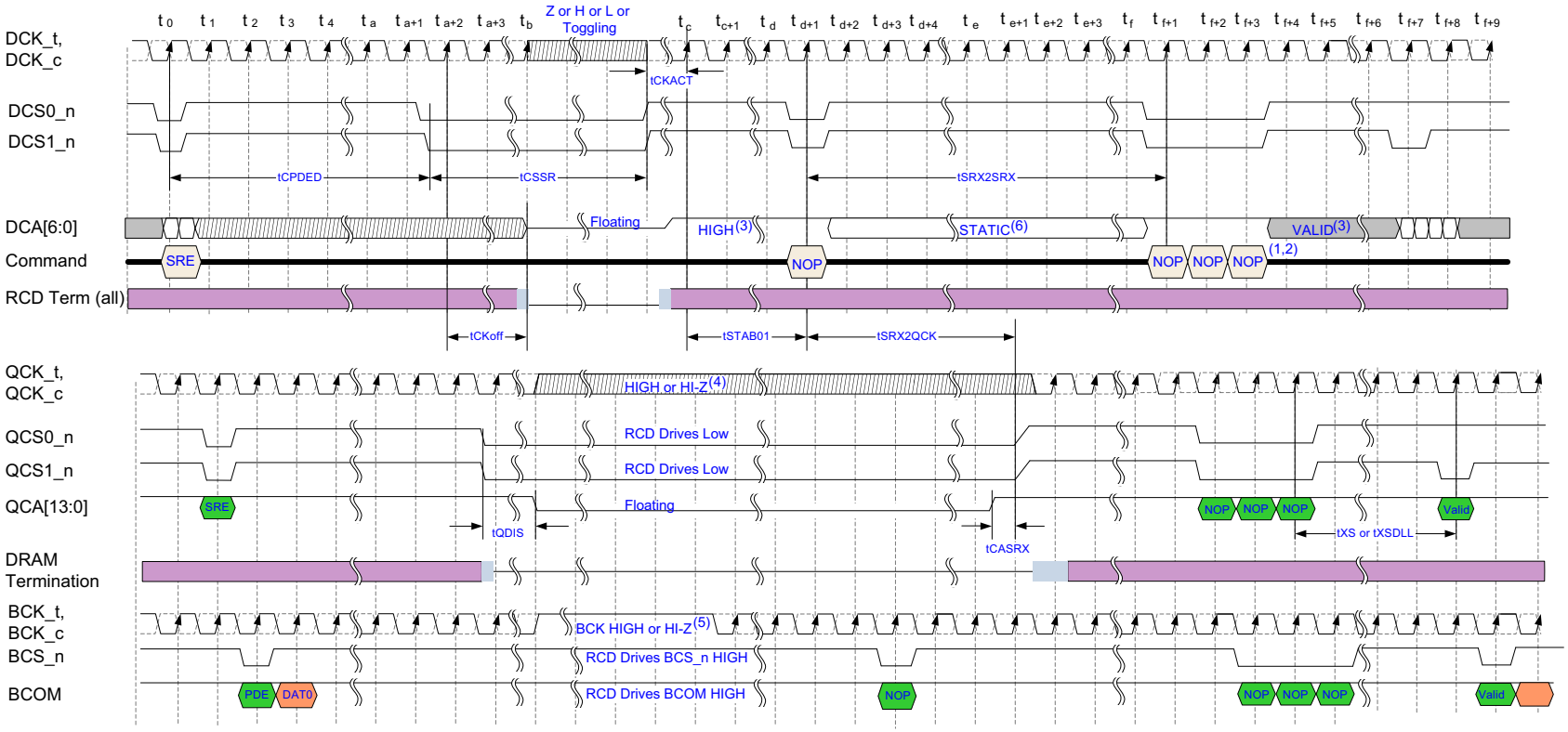
4.2.3 Self Refresh Mode without Clock Stop Entry

Self Refresh without Clock Stop is similar to Self Refresh with Clock Stop mode except that the host controller will not stop the DCK input. After both sub-channels have received, the SRE command the host signals the RCD to enter this mode by sending a one clock wide pulse on DCS[1:0]_[B:A]_n instead of holding it LOW for multiple cycles at t_7 in Figure 30. The RCD will not disable any of its terminations and will not disable the PLL during Self Refresh without clock stop. The RCD will also not stop the QCK or BCK clock outputs in this mode.

4.2.4 Self Refresh Mode without Clock Stop Exit

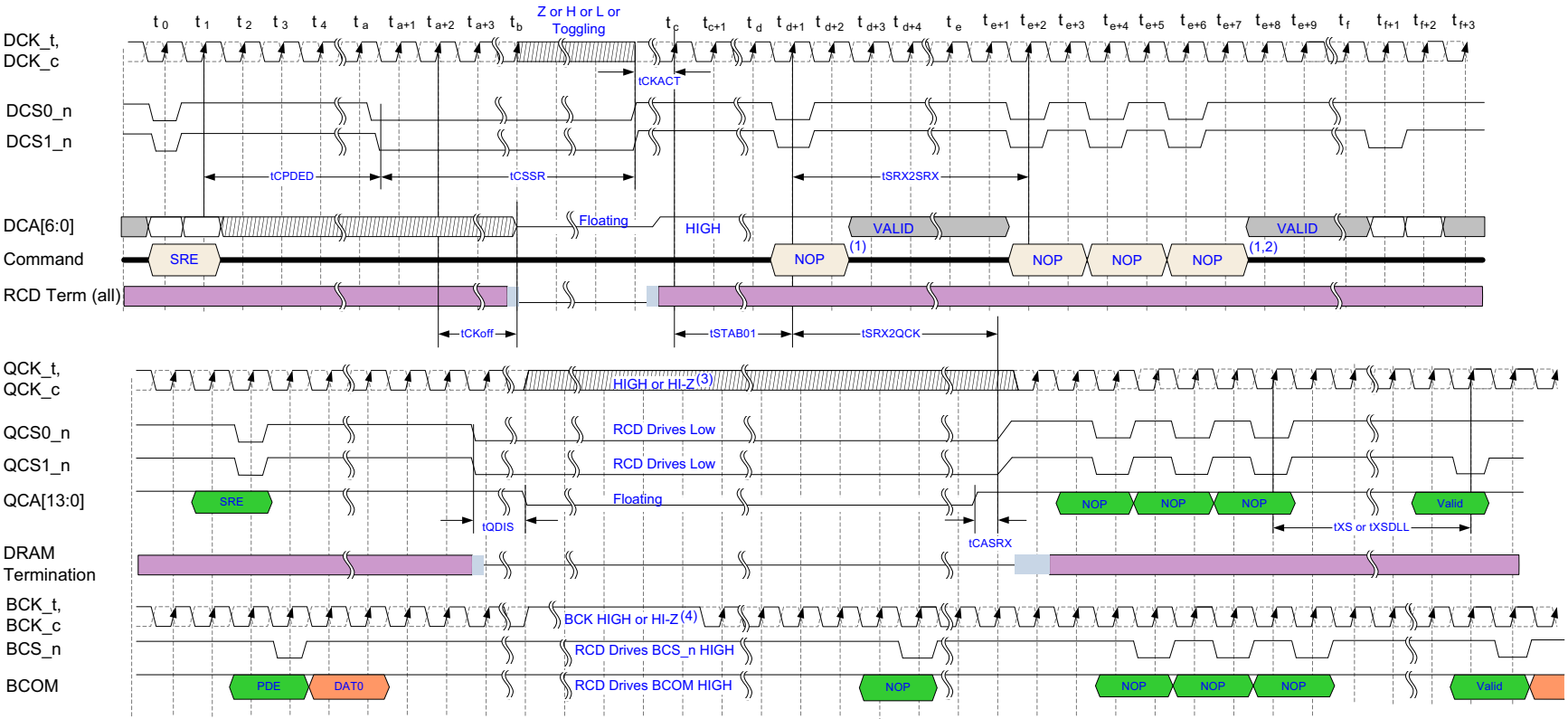
Exiting this mode is similar to Self Refresh with Clock Stop, except that the host will not wait t_{STAB} upon exit, as the PLL is already locked. Since the DCS[x]_n signals are already HIGH, the first indication of the exit is the NOPs that release the QCS[x]_n signals.

1. Since DCS_n Low-to-High transitions can be staggered by up to $t_{DCSLHSK1}$ (for the entire chip) or $t_{DCSLHSK2}$ (within the same sub-channel), t_{CKACT} must be met with respect to the DCS_n signal with the earliest rising transition.



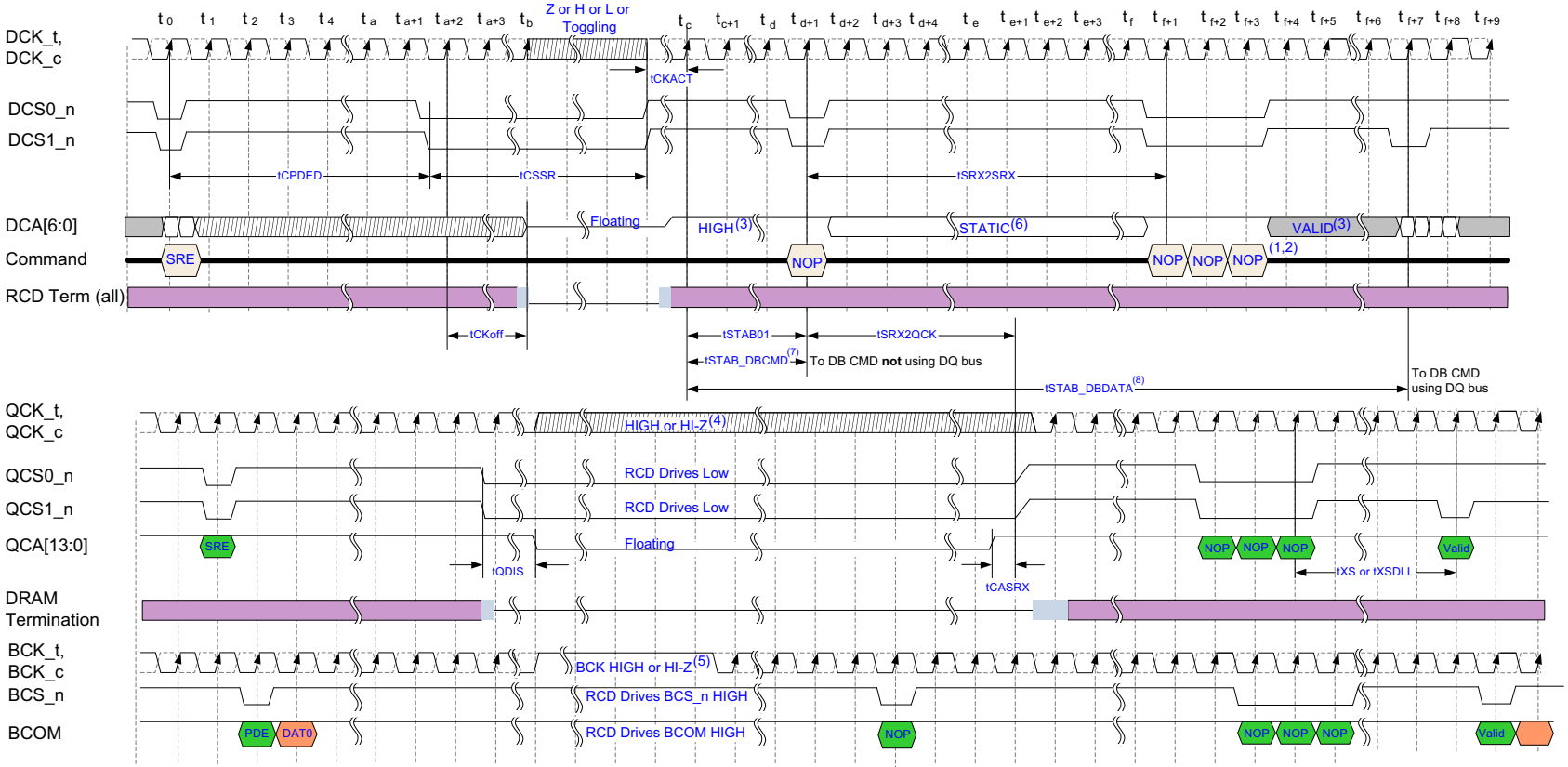
1. The NOP (SRX) Commands that release QCS outputs, and the consecutive NOP Commands sent to the DRAM after that, are required to meet RCD parameters tDCSLHSK1 and tDCSLHSK2 as well as DRAM parameter tCSH_SRexit.
2. NOP (SRX) Command to DRAM Rank 0 & 1 to take the DRAM out of Self Refresh.
3. HIGH or Valid signal timing and levels required if DFE enabled.
4. The RCD is allowed to drive HIGH or HI-Z.
5. The RCD is allowed to drive HIGH or HI-Z. The clock nets will be pulled HIGH by either the RCD output drivers or by the external termination to VDD which is required on the module PCB.
6. HIGH or Valid signal levels required to be held static for a minimum tDFE_PRD time prior to first assertion of DCS if DFE enabled.

Figure 26 — Self Refresh Entry Exit with Clock Stop With DCK Frequency Change



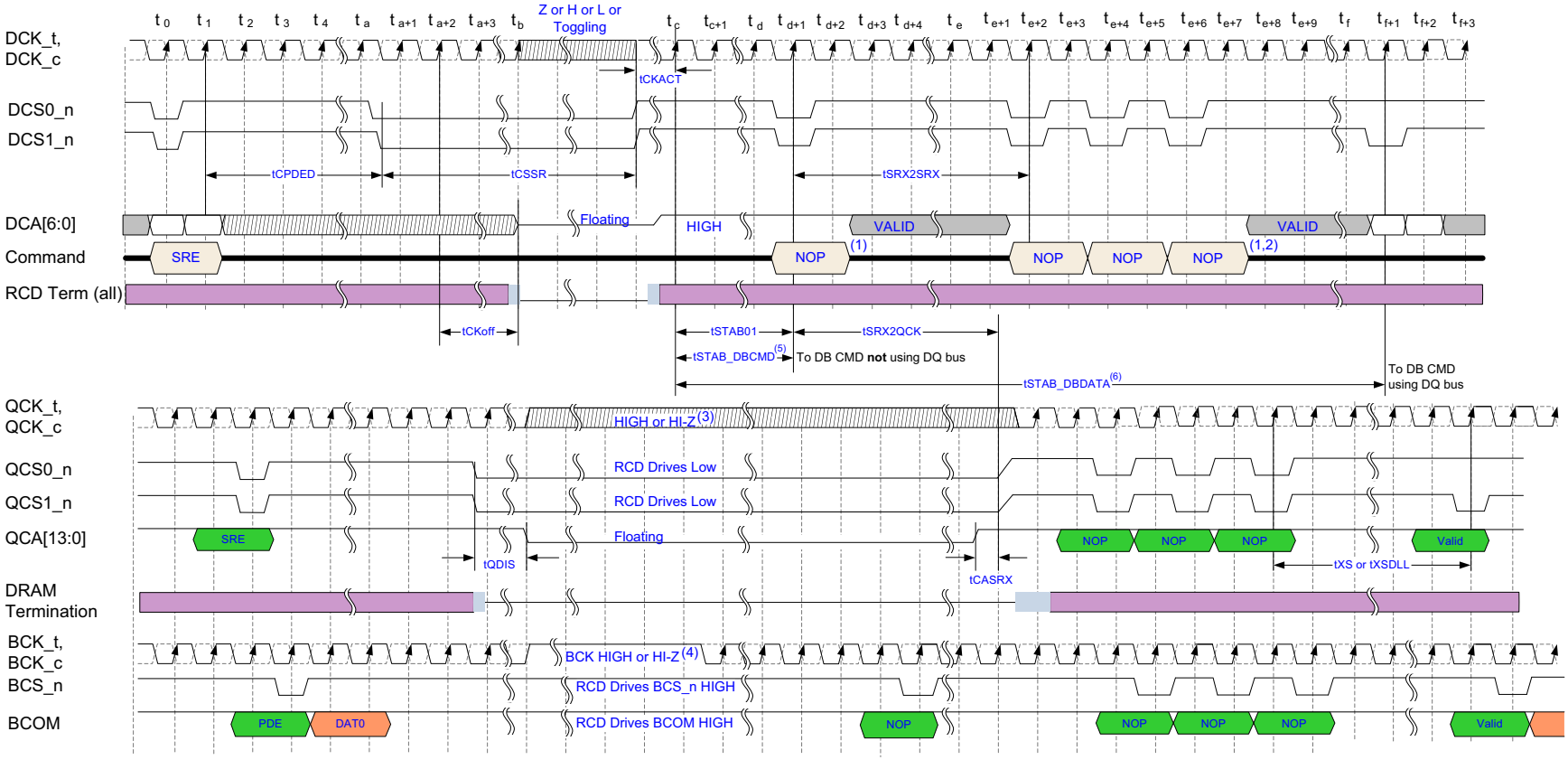
1. The NOP (SRX) Commands that release QCS outputs, and the consecutive NOP Commands sent to the DRAM after that, are required to meet RCD parameters tDCSLHSK1 and tDCSLHSK2 as well as DRAM parameter tCSH_SRexit.
2. NOP (SRX) Command to DRAM Rank 0 & 1 to take the DRAM out of Self Refresh.
3. The RCD is allowed to drive HIGH or HI-Z.
4. The RCD is allowed to drive HIGH or HI-Z. The clock nets will be pulled HIGH by either the RCD output drivers or by the external termination to VDD which is required on the module PCB.

Figure 27 — Self Refresh Entry Exit with Clock Stop in SDR1 Mode With DCK Frequency Change



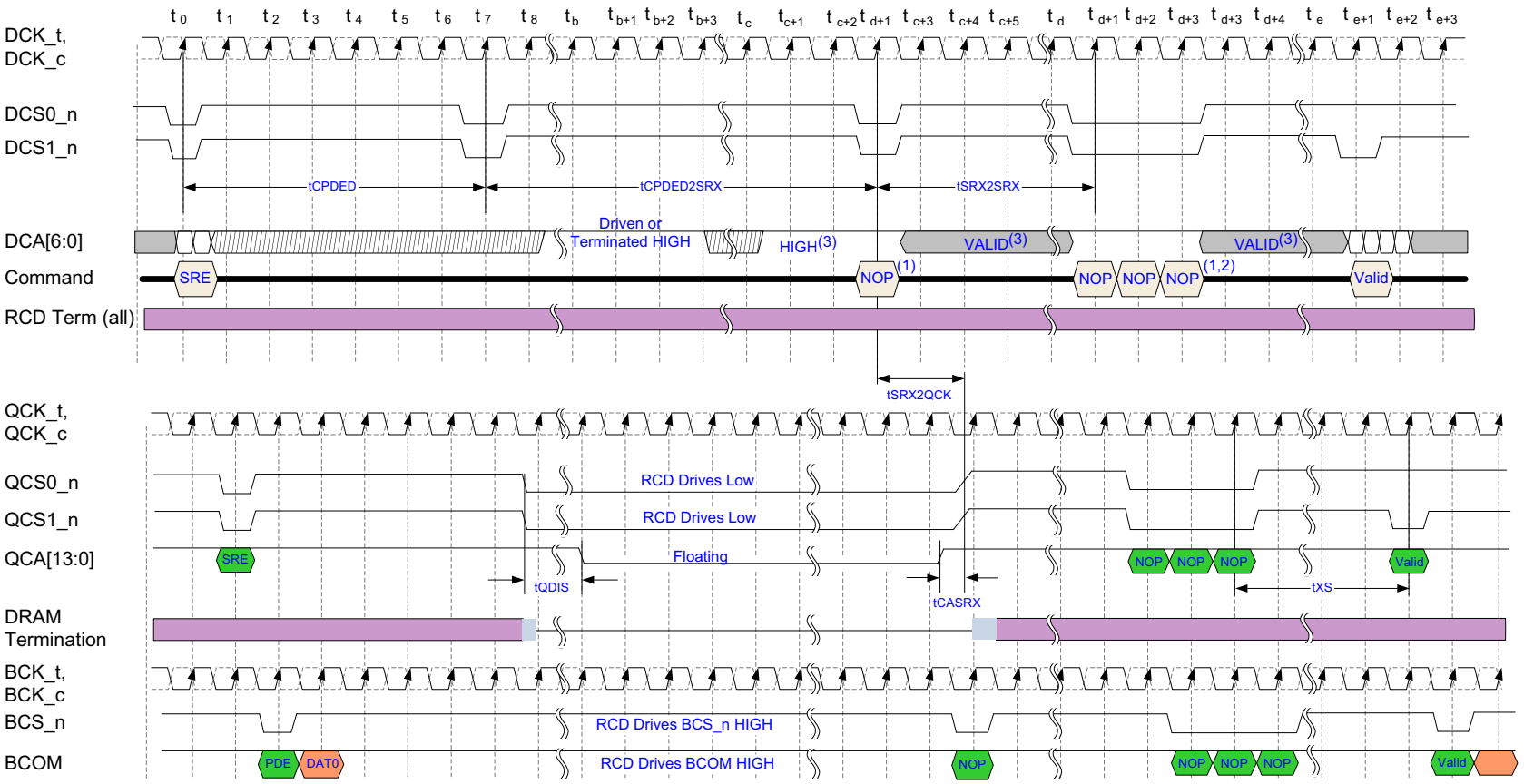
1. The NOP (SRX) Commands that release QCS outputs, and the consecutive NOP Commands sent to the DRAM after that, are required to meet RCD parameters tDCSLHSK1 and tDCSLHSK2 as well as DRAM parameter tCSH_SRexit.
2. NOP (SRX) Command to DRAM Rank 0 & 1 to take the DRAM out of Self Refresh.
3. HIGH or Valid signal timing and levels required if DFE enabled.
4. The RCD is allowed to drive HIGH or HI-Z.
5. The RCD is allowed to drive HIGH or HI-Z. The clock nets will be pulled HIGH by either the RCD output drivers or by the external termination to VDD which is required on the module PCB.
6. HIGH or Valid signal levels required to be held static for a minimum tDFE_PRD time prior to first assertion of DCS if DFE enabled.
7. In LRDIMM, tSTAB_DBCMD must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does **not** use the DQ data path (e.g., SRX, NOP, etc.).
8. In LRDIMM, tSTAB_DBDATA must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

Figure 28 — Self Refresh Entry Exit with Clock Stop Without DCK Frequency Change



1. The NOP (SRX) Commands that release QCS outputs, and the consecutive NOP Commands sent to the DRAM after that, are required to meet RCD parameters tDCSLHSK1 and tDCSLHSK2 as well as DRAM parameter tCSH_SRexit.
2. NOP (SRX) Command to DRAM Rank 0 & 1 to take the DRAM out of Self Refresh.
3. The RCD is allowed to drive HIGH or HI-Z.
4. The RCD is allowed to drive HIGH or HI-Z. The clock nets will be pulled HIGH by either the RCD output drivers or by the external termination to VDD which is required on the module PCB.
5. In LRDIMM, tSTAB_DBCMD must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does **not** use the DQ data path (e.g., SRX, NOP, etc.).
6. In LRDIMM, tSTAB_DBDATA must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

Figure 29 — Self Refresh Entry Exit with Clock Stop in SDR1 Mode Without DCK Frequency Change



1. In order to meet DRAM tCSH_SRexit, NOP (SRX) Command to RCD to release QCS0 & QCS1 and NOP Command must not be staggered per Rank.
2. NOP (SRX) Command to DRAM Rank1 & 2 out of Self Refresh.
3. HIGH or Valid signal timing and levels required if DFE enabled.

Figure 30 — Self Refresh Entry and Exit without Clock Stop

5 Training Modes

5.1 CS Training Modes

5.1.1 DCS Training Mode (DCSTM) - Host Interface

The DCS Training Mode is a method to facilitate the loopback of a sampled sequence of the DCS_n signal. In this mode, the DCK is running, and the DCA and DPAR signals are ignored by the RCD. Once this mode is enabled, the RCD is selected to actively sample and drive feedback. The RCD will sample the DCS_n signal on the rising edge of DCK. Every set of four DCK rising edge samples will be included in a logical computation to determine the DCSTM Output result that is sent back to the host on ALERT_n or QLBx configured in RW01[5]. Once sampling begins, the RCD must maintain the consecutive grouping of the samples every 4 tCK. When the DCS_n Sample[0] and Sample[2] results in a logic 0 and the DCS_n Sample[1] and Sample[3] results in a logic 1, the RCD will drive a 0 on ALERT_n or QLBx. The output signal can transition as often as every 4 tCK. All commands to DRAM and Data Buffer are blocked by the RCD when DCS Training mode is enabled. The host shall not enable Power Down mode in RW00 until after all Host Interface Training is complete.

5.1.1.1 Entry and Exit for DCS Training Mode

The DCS Training Mode is enabled by a SMBus write to RW02[3:0]. The signal used to provide the feedback is configured by RW01[5]. RCD can be configured to use ALERT_n (which requires training each sub-channel independently and one after the other), or use both QLBD and QLBS (which allows training both sub-channels in parallel). For the remainder of this section, we assume ALERT_n was selected for feedback. Once the RCD has DCS Training Mode enabled, the RCD begins sampling on every rising CK edge, with the 4-sample groups looping consecutively. Depending on the value of the samples, ALERT_n is driven HIGH or LOW. RCD hardware will block the signals coming from the DERROR_IN_n receivers if ALERT_n has been selected for feedback in RW01[5]. Prior to entering DCS Training Mode, the ALERT_n or QLBx shall remain High. The DCS Training Mode is disabled by a SMBus write to RW02[3:0].

5.1.1.2 DCS Training Mode Operation

In DCS Training Mode, the DCS_n values are sampled on all DCK rising edges. Each group of 4 consecutive samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending on ALERT_n. The samples evaluation to determine the output is as follows:

Table 16 — Sample Evaluation for Intermediate Output[0]

Output[0]	DCS_n Sample[0]	DCS_n Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 17 — Sample Evaluation for Intermediate Output[1]

Output[1]	DCS_n Sample [2]	DCS_n Sample[3]
1	0	0
0	0	1
1	1	0
1	1	1

Table 18 — Sample Evaluation for final DCSTM Output

DCSTM Output[1,2]	Output[0]	Output[1]
0	0	0
1	0	1
1	1	0
1	1	1

1. When there is no change on the DCSTM Output from previous evaluation, ALERT_n shall continue to drive same value continuously with no switching on the bus.
2. These values are driven asynchronously, but may switch as often as every 4 tCK.

As shown in Table 16 through Table 18, DCSTM Output will only be 0 when DCS_n Sample[0] = Sample[2] = 0 and Sample[1] = Sample[3] = 1. The DCSTM output will be 1 in all other cases.

During DCS Training Mode the DCS ODT is enabled as for functional operation. The VrefCS is set in RW[49:48]. The delay from when the DCS signals are sampled during the fourth DCK rising edge (Sample[3]) to when the output of the sample evaluation is driven to a stable value on ALERT_n is specified as tDCSTM_Valid, as shown in the following figure. The details of the tDCSTM_Entry, tDCSTM_Exit, and tDCSTM_ALERT_Window are also illustrated.

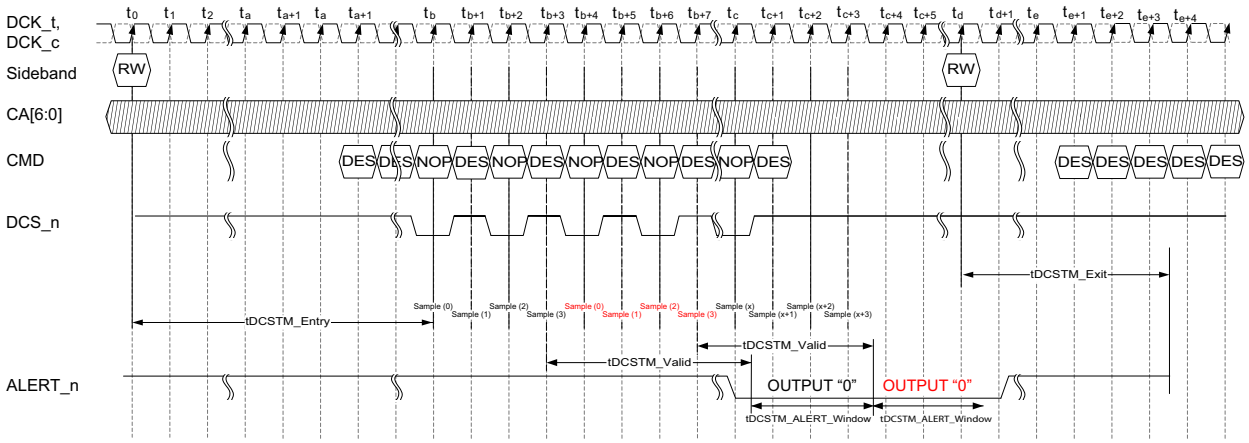


Figure 31 — Timing Diagram for DCS Training Mode with Consecutive Output Samples = 0

The following figure illustrates an example where the ALERT_n Output switches from a logic 0 to a logic 1 value, demonstrating the minimum tDCSTM_ALERT_Window:

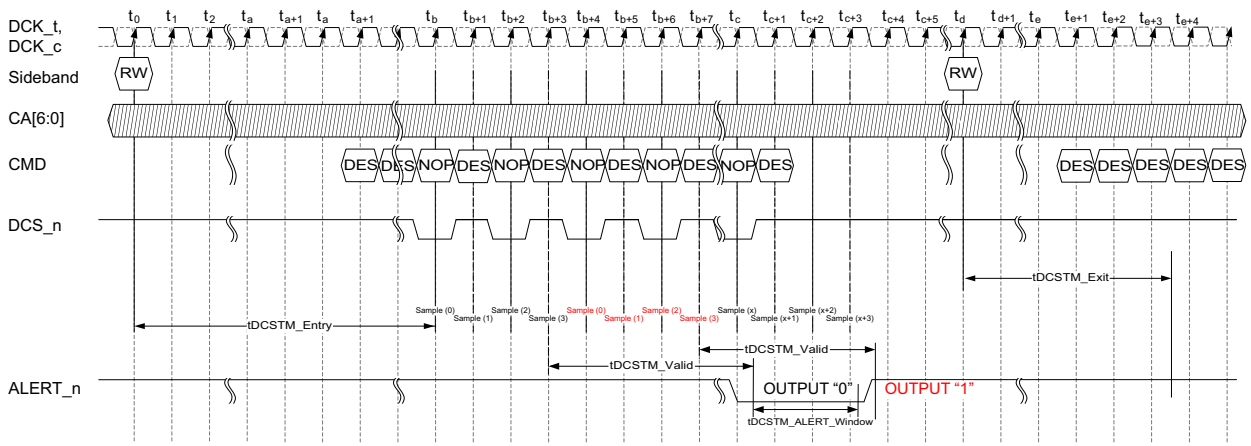


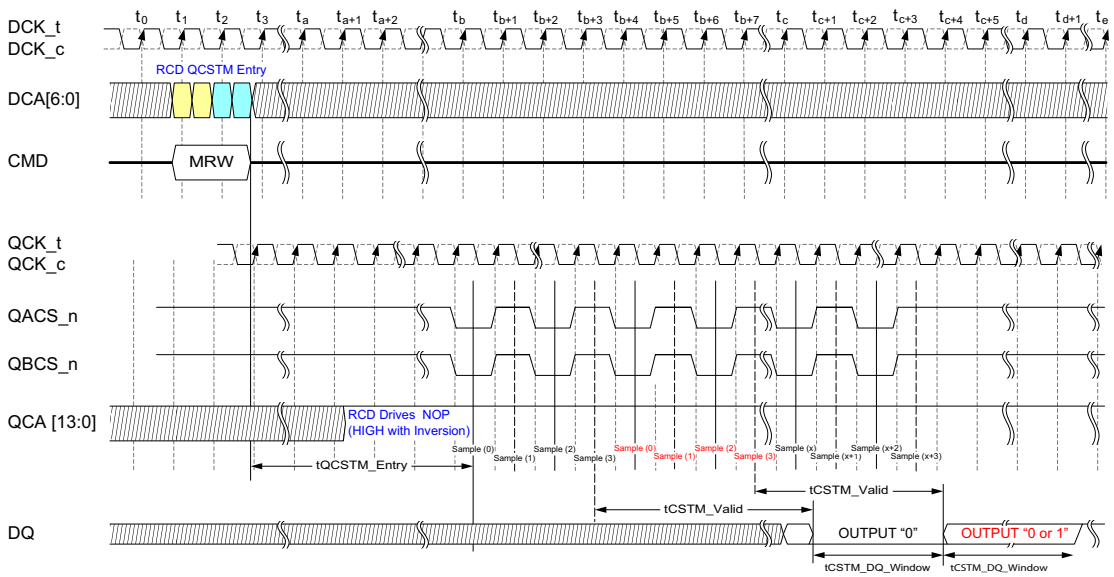
Figure 32 — Timing Diagram for DCS Training Mode with Output Sample Toggle

5.1.2 QCS Training Mode (QCSTM) - DRAM Interface

The DDR5RCD01 must support the DRAM CS training mode. Since the MPC command must be sent to the DRAM prior to completing training of the QCS and QCA signals, the RCD shall support the forwarding of DRAM MPC and VrefCA commands with extended setup and hold CA timings by using the RCD CA Pass-through mode set in the Global Features Control word. The host must disable Power Down mode in RCD prior and during QCS Training.

During QCSTM the RCD must be able to support the DDR5 DRAM CS training Mode with the following features:

- QCS_n pattern generation. When the QCS_n signal is selected in RW03 the RCD will generate a continuous clock pattern to the DRAM, while sending a NOP encoding with proper inversion applied according to RW00 on the associated QCA signals
- The host does not need to set the DRAM Interface blocking explicitly. The QCSTM mode will automatically block commands to the DRAM Interface.
- The RCD must adjust the QCS_n output delay when the host sends an MRW to RW[1A:17].
- It is recommended that the host block commands to the Data Buffer when in this mode. The host must send an MRW to RW01 to set the BCOM blocking.



Note: By the end of tQCSTM_Entry, all commands to DRAM are Blocked by the RCD and the QCA[13:0] outputs are driven HIGH (with Output Inversion applied). The host may configure the RCD to block Data Buffer commands by sending MRW to RW01.

Figure 33 — Timing Diagram for QCSTM with Output Sample Toggle

5.2 CA Training Modes

5.2.1 DCA Training Mode (DCATM) - Host Interface

The DCA Training Mode is a method to facilitate the loopback of a logical combination of the sampled DCA[6:0] and DPAR signals. This mode can only be entered after DCS training has been performed. In DCATM, the DCK is running, and the DCS0_n qualifies when the DCK samples the DCA signals. A loopback equation that includes all the DCA and DPAR signals results in an output value that is sent asynchronously on the ALERT_n or QLBx signal back to the host memory controller. The host timings between DCS_n, DCK, DCA[6:0] and DPAR signals can then be optimized for proper alignment. DCK must stay valid with constant phase and frequency. When the RCD is in this mode, no functional commands are executed. The functional command interface is restored only after exiting this mode. All commands to DRAM and Data Buffer are blocked by the RCD during DCA Training mode. The host must ensure Parity Checking is disabled in RCD prior to and during DCA training. Power Down mode must be disabled in RCD prior and during DCA Training.

5.2.1.1 Entry and Exit for DCA Training Mode

The DCA Training Mode is enabled through an SMBus write to RW02[3:0]. The signal used to provide the feedback is configured by RW01[5]. RCD can be configured to use ALERT_n (which requires training each sub-channel independently and one after the other), or use both QLBD and QLBS (which allows training both sub-channels in parallel). For the remainder of this section, we assume ALERT_n was selected for feedback. Once this SMBus command has executed, no other commands will be interpreted by the RCD in the sub-channel that enters DCA Training Mode. The sub-channel that is not in Training Mode will interpret commands as in normal mode of operation. The host is responsible for avoiding undesirable signal events or commands on the RCD sub-channel that is not in Training Mode. That includes avoiding commands that may interfere with the resources needed to support DCA Training Mode such as, for example, MRW to enable the Parity Checking. For the sub-channel that is in Training Mode, only the sampling of the DCA signals, evaluation of the XOR result, and loop back to the ALERT_n will occur. While in DCA Training Mode, the DCS0_n signal will only assert for a single tCK at a time. The maximum sampling rate on the DCA signals will be every 4tCK. RCD hardware will block the signals coming from the DERROR_IN_n receivers if ALERT_n has been selected for feedback in RW01[5].

The DCA Training Mode is disabled by SMBus write to RW02[3:0] or by asserting DCS0_n for 2 or more cycles in a row, while sending a NOP command on the DCA bus.

5.2.1.2 DCA Training Mode (DCATM) Operation

In DCA Training Mode, the DCA and DPAR values are only sampled when DCS0_n is asserted. The sample is captured by the rising, falling or both DCK edges. The DCA XOR sampling edge is selected in RW02[5:4]. Unlike functional operation, there is no concept of multiple cycle commands in DCA Training Mode. Once the DCA and DPAR signals are sampled, the values are XORed to produce an output value. This output value is driven on the ALERT_n signal, as a static value. This output value will be held until the next sample is captured on the DCA bus, according to the DCS0_n assertion.

During DCA Training Mode the DCA ODT is enabled as for functional operation. The VrefCA is set according to RW[47:40]. The timing requirements for the Host Interface signals are the same as for functional operation.

The delay from when the DCA and DPAR signals are sampled during the DCS0_n assertion and when the output of the XOR computation is driven on the ALERT_n signal is specified as t_{DCATM_Valid}, as shown in the following figure. DCS_n may be asserted every 4tCK, and thus the DCA XOR output may transition every 4tCK. The following figure demonstrates an example where two DCS0_n assertions occur within 4tCK. The RCD will exit DCA Training Mode by SMBus write to RW02[3:0] or when the DCS0_n is asserted for 2 or more consecutive cycles but limited to 8 cycles.

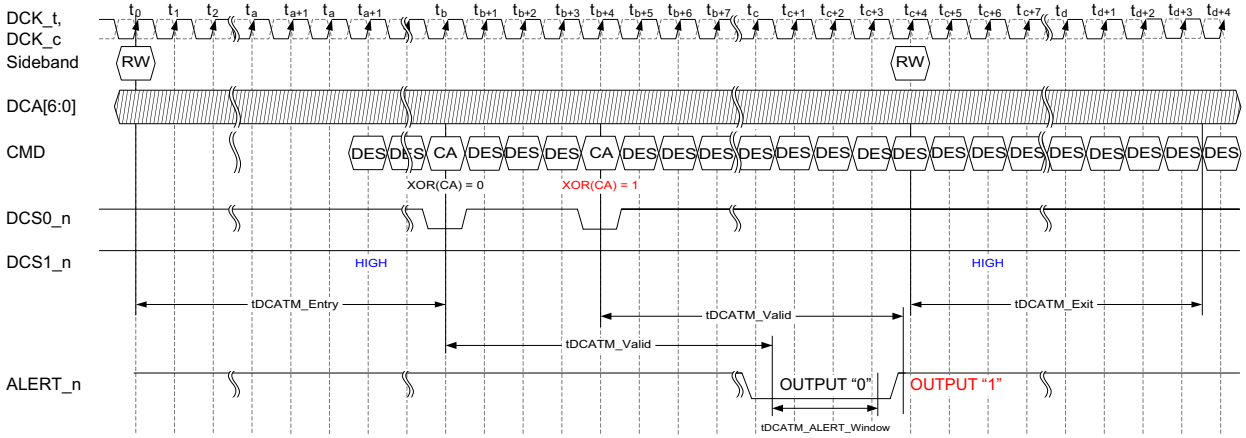


Figure 34 — Timing Diagram for DCA Training Mode SMBus Exit

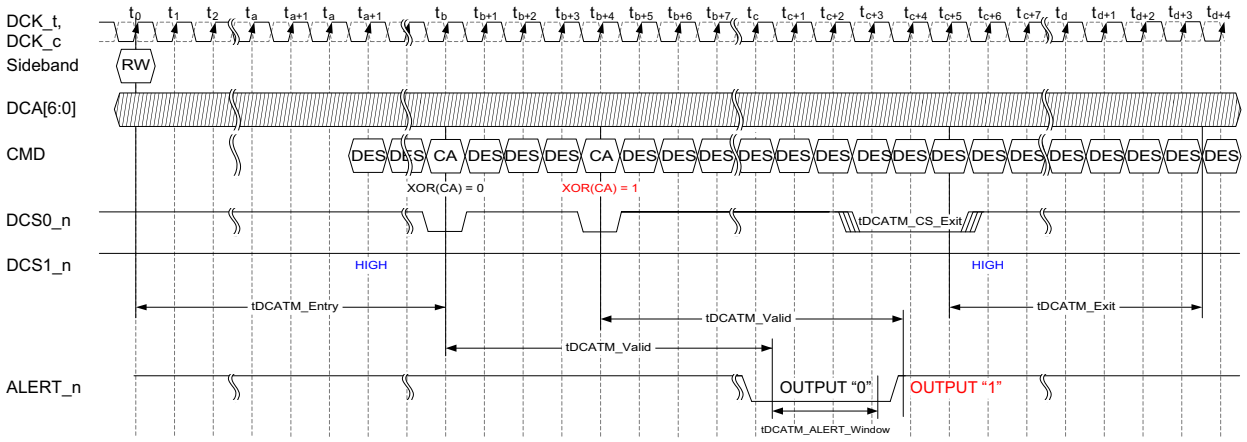


Figure 35 — Timing Diagram for DCA Training Mode Double CS Exit

5.2.1.3 DCA Training Mode Loopback Equation

The DCATM Output is computed based on the DCS_n assertion and the values of the DCA and DPAR inputs. Table 19 clarifies the output computation.

Table 19 — DCA Training Mode Output

DCS_n	DCATM Output
0	XOR (DPAR, DCA[6:0])[1,2,3,4]
1	Hold Previous value

1. For any DCA or DPAR signals not supported (i.e., disabled) in the RCD, the logical value of these signals shall be considered 0 for the XOR computation
2. Clock sampling edge for XOR computation can be DCK rising, DCK falling or both DCK rising and falling edges and is selected in RW02[5:4].
3. The DCK rising edge that captures DCS_n LOW must be used in cases with rising edges enabled in RW02[5:4]. The DCK falling edge immediately following the rising edge that captures DCS_n LOW must be used in cases with falling edges enabled in RW02[5:4].
4. When both rising and falling DCK edges are enabled, 'XOR (rising edge DPAR, rising edge CA[6:0], falling edge DPAR, falling edge CA[6:0]).

5.2.2 QCA Training - DRAM Interface

There is no RCD QCA Training Mode. In order for the RCD to align the QCA signals to QCK, the RCD must be able to support the DDR5 DRAM CA training Mode. During RCD QCA Training the host will enable CA Pass-Through mode in RW00[2]. The RCD will need to process MRW commands and block DRAM MRW commands while in CA Pass-Through mode. The RCD must be capable of QCA output delay adjustment when the host sends an MRW to RW[1C:12]. Power Down Mode and CA Parity Checking must be disabled in RCD prior to QCA Training, however the DPAR receivers will remain enabled to support SDR CA Pass-Through mode. CA Pass-Through mode can only be enabled when the RCD is forwarding DRAM commands, RW01[1] = 1.

5.2.3 CA Pass-through Mode

In order to train the DRAM interface, the RCD will be required to support a pass-through mode. In this mode the DCA signals are passed through to QCA regardless of DCS assertion. This allows the host to send multiple cycles of QCA setup/hold and multiple cycles of QCS assertion, while also controlling the duration and timing relationship of these signals at a clock cycle granularity. The Host Interface DCA must be stable before the RCD can be placed into CA Pass-through mode. Parity checking must be disabled prior to and during Pass-Through mode. CA Pass-Through is performed on a per Rank basis and entered via MRW RW00. The Host is only allowed to enable one Rank at a time for CA Pass-through mode, to ensure the ability to still send MRWs on the other Rank. The RCD executes DCS_n/ DCA commands on the rank that is not selected for Pass-Through mode, but it is illegal for the host to send commands other than MRW targeting the RCD. MRW to DRAM MR63 (for RCD Control Word read sequence) is not supported in CA pass-through mode. When Pass-Through mode is enabled for Rank 0 or Rank 1 all DCA signals will pass through to QCA. When RW00[3] = 0, Rank 0 is selected then only DCS0 will get passed through to QCS0 and the RCD will process RW commands on Rank 1 and not process any commands for Rank 0. When RW00[3]=1, Rank 1 is selected then only DCS1 will get passed through to QCS1 and the RCD will process RW commands on Rank 0 and not process any commands for Rank 1. The RCD keeps QCS_n static High for the rank that is not selected for Pass-Through mode. If the DRAM Interface Block all CMDs feature is enabled (RW01[1] = 0), the DCS_n input will not be passed through to QCS_n because all QCS_n outputs will be held statically HIGH by the RCD. The host must ensure Power Down mode is disabled in RW00[6] prior to and during Pass-Through mode. CA Pass-through mode is exited by disabling CA Pass-Through mode via RW00.

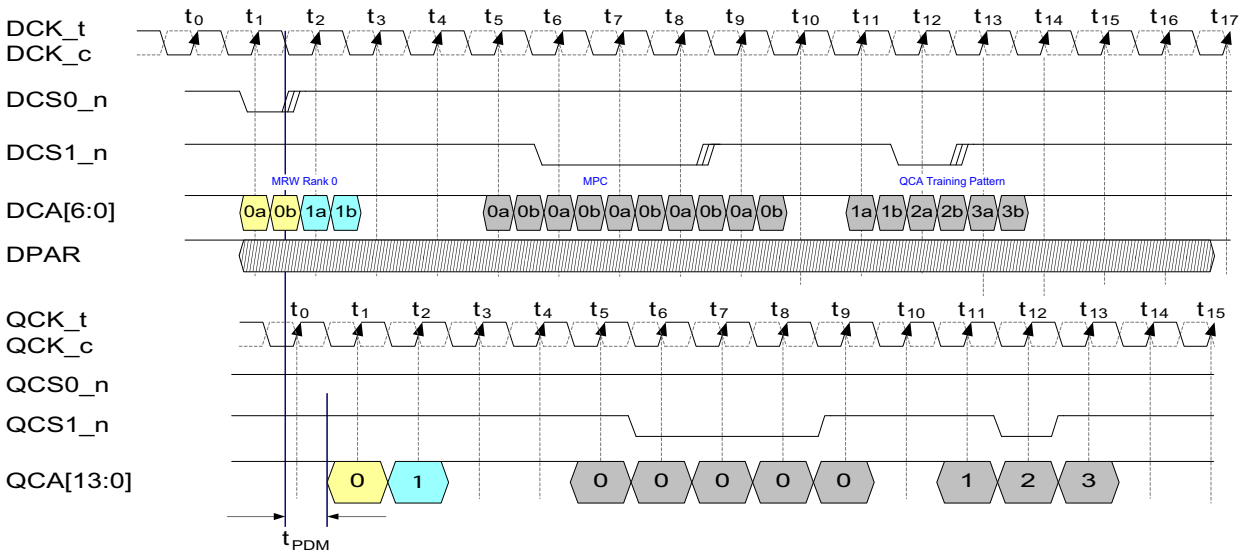


Figure 36 — MRW example of MRW on DCS0 and CA Pass-Through on DCS1

In SDR Mode when Pass-Through mode is enabled, DPAR will be used to indicate 1st UI QCA[6:0] (DPAR = LOW) and 2nd UI QCA[13:7] (DPAR = HIGH) as shown in Figure 37. When the DPAR signal starts toggling, it may take up to two cycles for the correct bit sequence to get established at the QCA[13:0] outputs of the RCD. The DDR5RCD01 device cannot guarantee the logic values of QCA[13:0] outputs unless the DPAR input is toggling regularly (i.e., once per DCK clock cycle) as shown in Figure 37. Because of this, it is preferred if the DPAR signal continues to toggle without interruptions. The host is responsible for allowing the data path to get established in SDR mode, without asserting DCS, each time the DPAR signal starts toggling after an interruption. To help this process, it is suggested to keep the DCA[6:0] input signals static HIGH during the transition. In addition to the beginning of DPAR toggling, the above requirements and suggestions also apply when CA Pass-Through is first entered, or when the rank selection bit (RW00[3]) is modified.

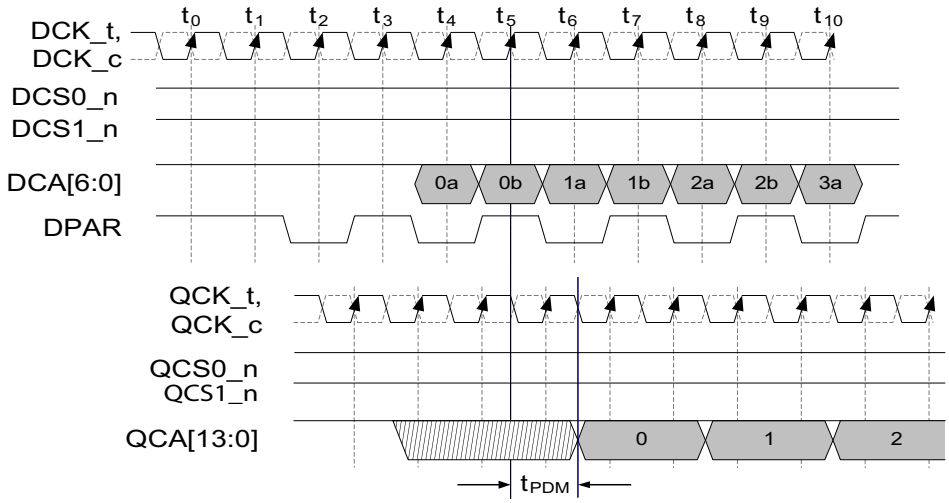


Figure 37 — SDR CA Pass-Through mode

5.2.4 BCS and BCOM Training - Data Buffer Interface

In order for the RCD to align the BCS and BCOM signals to BCK, the RCD must be able to support the DDR5 Data Buffer BCOM training mode. During RCD BCOM Training, the host will enable BCOM pass-through mode in RW00[4]. The RCD will need to process MRW command and block DRAM commands while in BCOM pass-through mode. Power down mode must be disabled in RCD prior to BCOM training.

5.2.5 BCOM Pass-Through Mode

In order to train the Data buffer interface, the RCD will be required to support a BCOM Pass-Through mode. In this mode the DCA4, DCA3, DCA1signals are passed on the BCOM bus regardless of DCS assertion. DCS0_n is passed through to BCS_n but DCS1_n does not get passed through in this mode. Instead the RCD will process RCD targeted MRWs to Rank1 shown in Figure 38. This allows the host to control combinations of BCOM and BCS patterns during BCOM Training. The DRAM interface Blocking must be set by the Host during BCOM Training. The DDR5RCD01 is not required to transfer commands to the QCA outputs when BCOM pass-through mode is enabled.

The RCD BCOM Pass-through mode is enabled when RW00[4] = 1. The DDR5RCD01 does not support BCOM pass-through mode and CA pass-through mode enabled at the same time.

In BCOM Pass-Through mode the RCD samples the DCA4, DCA3 and DCA1 inputs on DCK rising edge in both

SDR and DDR Modes.

Table 20 — BCOM bus mapping

DDR5RCD DCA bit	BCOM bit
DCA4	BCOM0
DCA3	BCOM1
DCA1	BCOM2

To achieve 2N timing on the BCOM Interface the Host must hold the value for two tCK.

The RCD will exit BCOM Pass-Through with MRW to RW00[4] = 0.

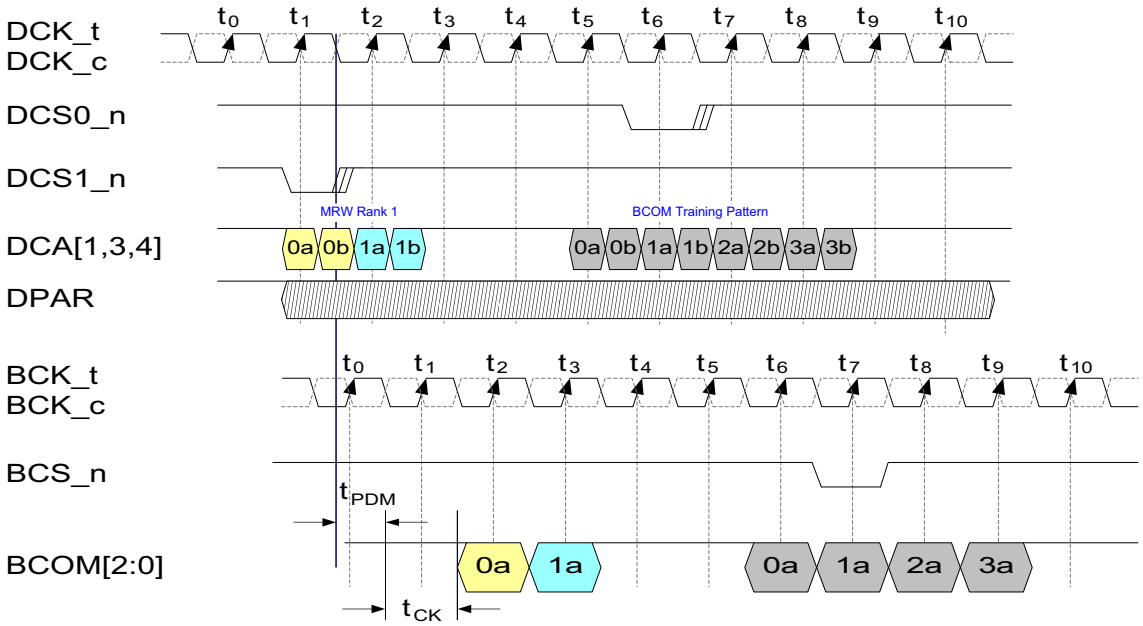


Figure 38 — BCOM PASS Through

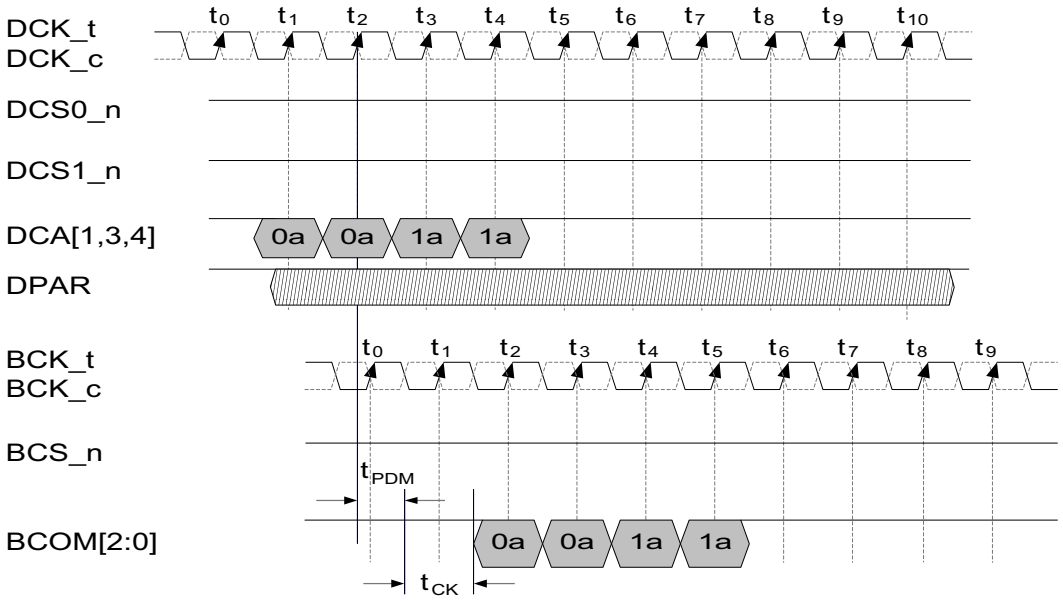


Figure 39 — BCOM Pass-Through Mode when RCD is in SDR

5.3 DFE Training Mode (DFETM)

The DDR5RCD01 will support a DCA DFE training mode. This Training Mode enables the use of pattern comparison and feedback features within the RCD during training. Figure 40 shows some of the DFE Training Circuitry associated with each individual DCA receiver. These features include a margin monitor, an XOR to compare the functional receive path to the monitor output, and LFSR pattern generator and XOR to compare the monitor output to a known expected pattern, an error counter, and a path to the ALERT_n signal, QLBD signal, and QLBS signal to provide feedback to the host controller.

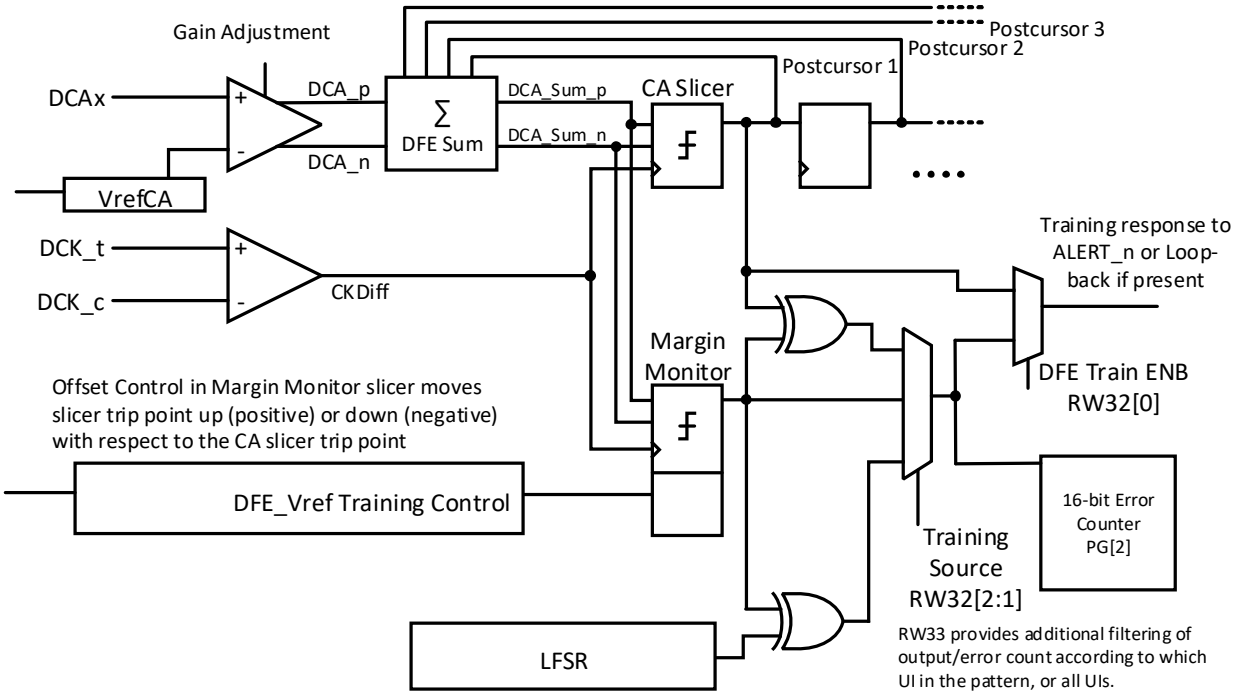


Figure 40 — DFE Training Circuitry

In addition to this fundamental set of DFE training features, the RCD supports an accelerator to sweep combinations of DFE Tap settings, Vref settings, and UI filters to enable more efficient DCA DFE Training.

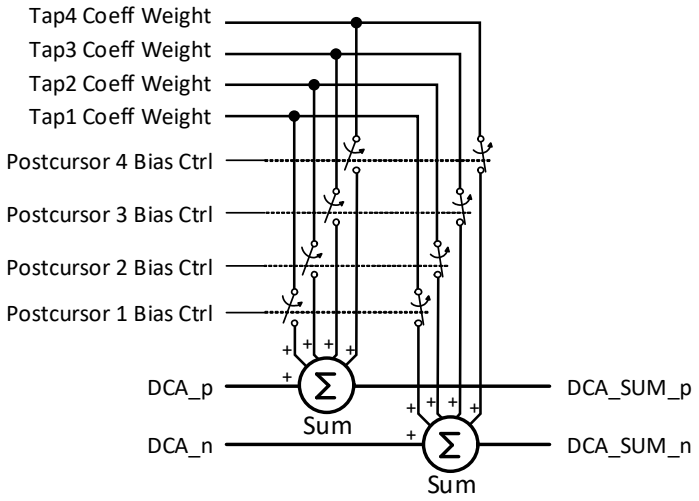


Figure 41 — DFE Summer

Table 21 — Post-cursor Bias Ctrl Definition

Tap k Sign Bit	Post-cursor k	Switch to DCA_p Sum	Switch to DCA_n Sum
0	0	Open	Closed
	1	Closed	Open
1	0	Closed	Open
	1	Open	Closed

5.3.1 DFE Training Pattern Comparison and feedback Features:

The DFE Training Pattern Comparison features include many different configuration options to compare the output of the receiver to an expected pattern, and the ability to change the monitor DFE_Vref setting, for margining. The RCD also supports the ability to filter the comparison based on UI location in the pattern sequence. Some of these configuration settings are included in RW32 DPAR and DCA[6:0] DFE Training Mode Control Word. The UI Filtering configuration are included in RW33 Additional Filtering for DFE Training Mode Control Word. The LFSR Seed Value sets the initial state of the LFSR, and all UI's of the DCA pattern are compared to the output of the LFSR. A new seed setting is only applied when the PG[2]RW[63, 67, 6B, 6F, 73, 77, 7B, 7F] LFSR Seed value is written. This seed is never restored as the LFSR state during training unless the host writes the value to the PG[2]RW[63, 67, 6B, 6F, 73, 77, 7B, 7F] register again.

The LFSR is reset to its default state under the following conditions:

- Power-up initialization
- DRST_n assertion

Other reset conditions, like Self Refresh and Power-down Entry, are not applicable because the LFSR training pattern generator of the RCD is only supported in DFE Training Mode, where command decoding is not supported.

The LFSR is an 8-bit Galois LFSR. The polynomial for the Galois LFSR is $x^8+x^6+x^5+x^4+1$. When a seed is programmed in the PG[2] register field, the source of the LFSR pattern must take into account the Galois LFSR implementation. The LFSR state advances once per UI in the DFE pattern, only when DCS0_n is asserted.

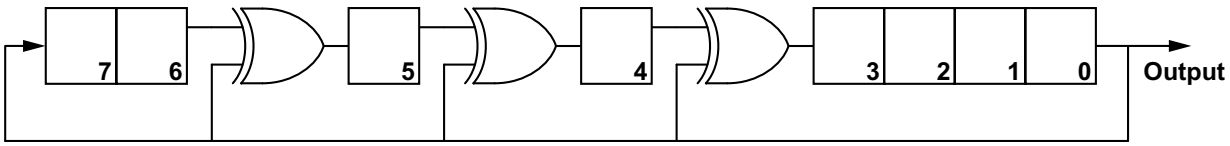


Figure 42 — Logical representation of the Galois LFSR of polynomial $x^8+x^6+x^5+x^4+1$ for DCA Training

When UI Filtering is enabled, only the XOR comparison or the LFSR comparison, or the raw data (based on Training Source setting) corresponding to the UI Filter Setting is fed back to the ALERT_n (or QLBD or QLBS) signal. This is also the only UI (or group of UI's for the even/odd configuration) that triggers any events in the error counter. When UI Filtering is enabled and set to UI[n] as the UI Filter Setting, only the nth UI of the DCA pattern will be compared/ recorded/looped back. When Per-UI Filtering is enabled, only patterns that are 8 UI in length can be sent to the RCD by the host. For all other patterns, the pattern length must be a multiple of 8 UI. When either the Even UI Filtering is

enabled or the Odd UI Filtering is enabled, the pattern length must also be a multiple of 8 UI. The even UI's are all rising edge samples. The odd UI's are all falling edge samples.

The following timing diagram shows an example of the LFSR pattern sent by the host to the RCD. Within each tDFETM_Interval time period (which is 4tCK), if any miscompares occur, the RCD will pull the ALERT_n (or QLBD or QLBS) signal LOW after tDFETM_Valid. If no miscompares occur during the tDFETM_Interval time period, the ALERT_n (or QLBD or QLBS) signal will remain HIGH.

Configuration of the output signal for the DFETM output is set in the RW01 Parity and Alert Global Control Word.

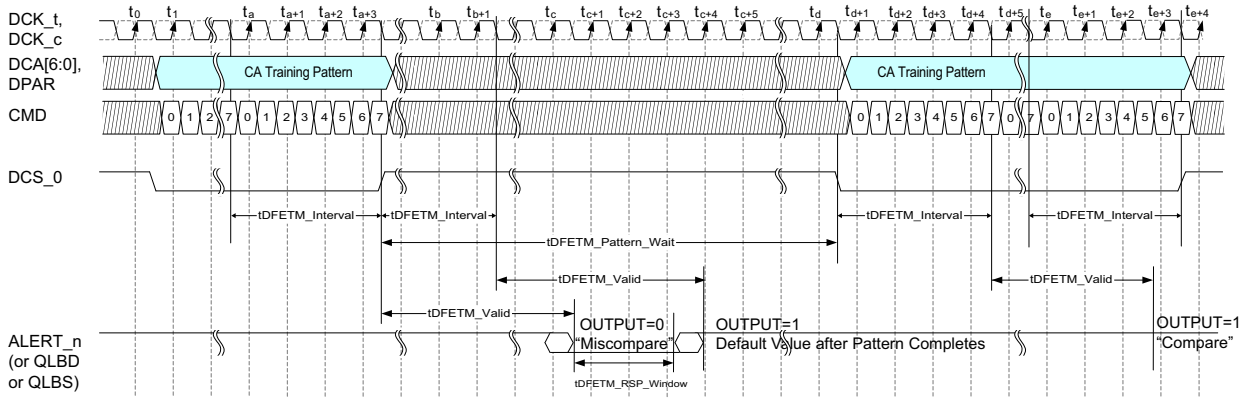


Figure 43 — LFSR CA DFE Training Pattern

The first tDFETM_Interval begins on the first UI of the pattern. Once the first tDFETM_Interval has elapsed (an additional 8 UI, or 4tCK) the first Output is generated on the ALERT_n (or QLBD or QLBS) pin, following the tDFETM_Valid time. Every tDFETM_Interval after will also generate a new Output value. For the different training configuration options, the following feedback will apply:

LFSR XOR - If any XOR result in the tDFETM_Interval = 1, the ALERT_n (or QLBD or QLBS) output will be 0.

Monitor XOR - If any XOR result in the tDFETM_Interval = 1, the ALERT_n (or QLBD or QLBS) output will be 0.

Monitor - If any Monitor sample in the tDFETM_Interval = 1, the ALERT_n (or QLBD or QLBS) output will be 0.

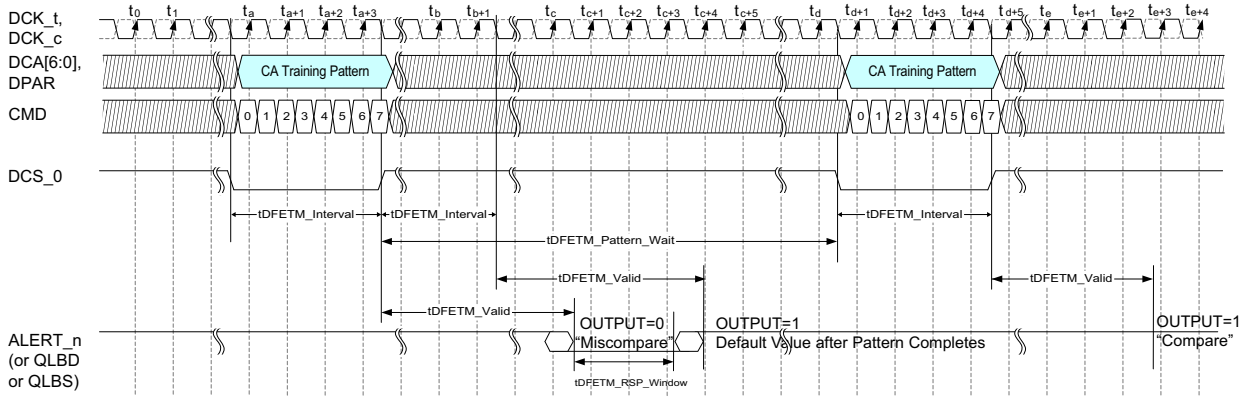


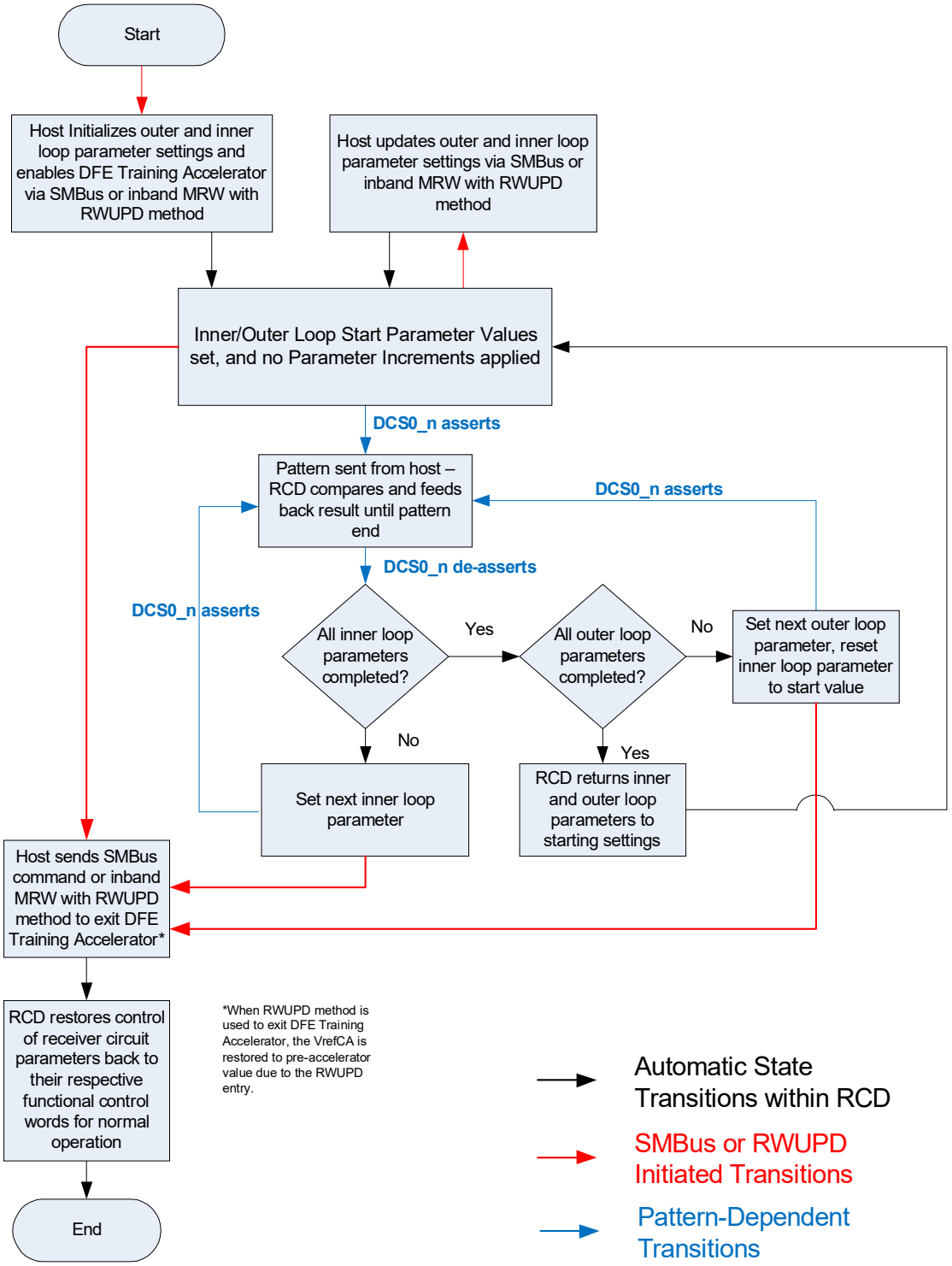
Figure 44 — CA DFE UI Filter Pattern

When UI filtering is enabled, only the (Monitor or LFSR) XOR result or the Monitor sample associated with the

selected UI is fed back on the ALERT_n (or QLBD or QLBS) signal. As described above, the (Monitor or LFSR) XOR or Monitor sample result is inverted on the ALERT_n (or QLBD or QLBS) signal.

5.3.2 DFE Parameter Sweep Acceleration

In addition to the features used to compare patterns and record or feedback the results of those comparisons, the RCD shall support the ability to accelerate the training sweeps of the critical DFE training parameters.



NOTE To read Loop Parameter Current Values when DFE Parameter Sweep Acceleration is enabled in the RCD, the host must use the sideband management interface and it must keep DCS0_n HIGH to stop training patterns. If these conditions are satisfied, the RCD shall provide the Loop Parameter Values intended for the next training pattern.

Figure 45 — RCD Operation During DFE Parameter Sweep Acceleration

The parameters that are included as options for the outer loop sweep are:

- UI - (RW33[4:2])
- Tap1 - (PG[1:0]RW[61,69,71,79], depending on DCA or DPAR signal selected for training in the RW32[5:3] register)
- Tap2 - (PG[1:0]RW[62,6A,72,7A], depending on DCA or DPAR signal selected for training in the RW32[5:3] register)
- Tap3 - (PG[1:0]RW[63,6B,73,7B], depending on DCA or DPAR signal selected for training in the RW32[5:3] register)
- Tap4 - (PG[1:0]RW[64,6C,74,7C], depending on DCA or DPAR signal selected for training in the RW32[5:3] register)
- Null

The parameters that are included as options for the inner loop sweep are:

- VrefCA - (RW[47:40])
- DFE_Vref - (PG[2]RW[62,66,6A,6E,72,76,7A,7E], depending on DCA or DPAR signal selected for training in the RW32[5:3] register)
- Null

The tDFETM_Pattern_Wait time is the amount of time the host must wait between de-assertion of DCS0 for one pattern to DCS0 assertion of the next pattern. The tDFETM_Pattern_Wait_Accel restriction only applies when the DFE Training Accelerator is operating, and is defined to allow for enough time in the RCD to change settings for the inner and outer loop parameters. The actual register values associated with the inner and outer loop parameters may or may not change during the execution of the DFE training accelerator. The settings may be applied directly from the accelerator logic output, bypassing the functional operation registers.

The outer loop tap parameters are defined as signed magnitude fields. For the Outer Loop Start Value in RW37, the format is two's complement. This simplifies the logic for incrementing from negative to positive values. The RCD shall convert the final parameter value per increment to the signed magnitude values required by the actual Tap settings.

The host is responsible for avoiding incorrect combinations of the loop parameter control word settings.

When the DFE accelerator exits, the inner and outer loop parameters are returned to the values prior to enabling the accelerator.

5.3.3 Method to update RW in-band during training

When DDR5RCD01 is in the wait state of the DFE training mode and if DCS1_[B:A]_n is asserted then the device shall enter a mode where it allows multi cycle RW writes as specified in the following paragraphs. The wait state of the DFE training mode is defined as any state in which no iteration is active and the RCD can accept changes to the DFE training accelerator parameters.

The mode is referred to as RWUPD and it is specified as follows:

- RWUPD Entry:
  DDR5RCD01 is in training mode non active states (outside of inner and outer loop iterations) and DCS1_[B:A]_n is asserted. On entry, the device shall restore DCAVrefCA trained during DCATM (See Intel Ballot on DCA DFE Training Acceleration) and DFE shall be disabled. Figure1 and Figure2 show how entering RWUPD and being ready to receive the first RW address requires two DCS1_[B:A]_n de-assertions.

- RWUPD Operation:
  After entry in RWUPD mode the DDR5RCD01 will expect pairs of DCS1_[B:A]_n assertions. On the first assertion the device will sample the target RW address on {DCA[6:0]_[B:A], DPAR_[B:A]}. On the second assertion, it will sample the value to write to the target RW.

- RWUPD Exit:
  If RW32[7] is written to 1 then device shall exit the RWUPD branch and return to the starting training mode state. This exit RW32 shall also be SMBUS writable to allow the exit being also triggered out of band. The host is responsible for exiting the RWUPD before exiting the DFE training mode. {DCA[6:0]_[B:A], DPAR_[B:A]} must remain static High during $t_{RWUPD\ Exit}$ to ensure deterministic initialization of DFE circuits as they get re-enabled.

During the entire RWUPD duration the host is not allowed to assert DCS0_[B:A]_n.

RW32[6] will need to be set to 1 to enable this feature.

Figure 46 shows a state machine implementing the described mode and Figure 47 shows a timing diagram demonstrating operation. Table 190 on page 177 has the relevant timing parameters.

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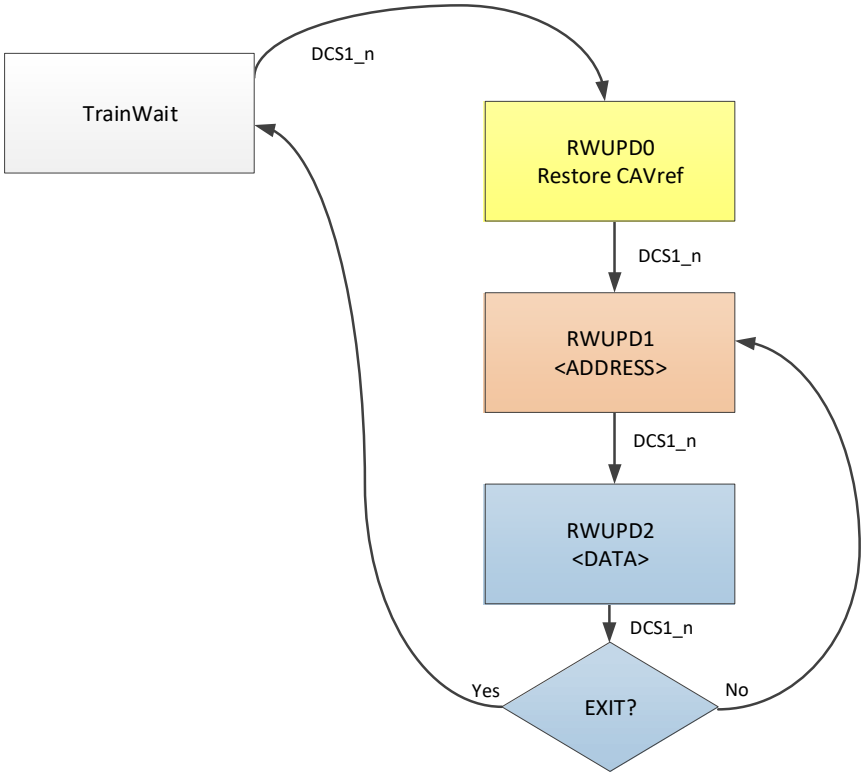

Figure 46 — RWUPD State Machine

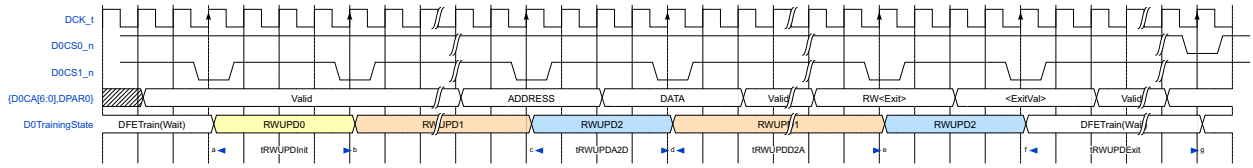

Figure 47 — RWUPD Timing Diagram for Channel A

5.4 Dual Frequency Support

The DDR5 register supports operation at a second, i.e. lower than nominal, frequency as a means to save buffer and DRAM power when the memory bandwidth demand allows.

To enable fast frequency switching without the need for retraining every time the frequency is changed, the DDR5 register can be trained at two, or more, different frequencies at boot up time. When only two frequencies need to be supported, the DDR5RCD01 can retain register settings associated with each of the two frequencies. The two sets of RCD registers are listed in Table 22. The RCD hardware will take care of updating any other frequency-dependent internal settings in each frequency context as needed. In cases where more than two frequencies of operation are necessary, RCD training information will need to be stored in memory space available to the host controller for this purpose since the DDR5RCD01 device only contains two sets of frequency context registers.

Table 22 — Control Words Duplicated for Frequency Context Support

Register Address	Description
RW0A	QCK Signals Driver Characteristics Control Word
RW0C	QxCA and QxCS_n Signals Driver Characteristics Control Word
RW0D	Data Buffer Interface Driver Characteristics Control Word
RW10	IBT Control Word
RW11[3:0]	Command Latency Adder Configuration Control Word
RW12	QACK Output Delay Control Word
RW13	QBCK Output Delay Control Word
RW14	QCCK Output Delay Control Word
RW15	QDCK Output Delay Control Word
RW17 .. RW1A	QxCS_n Output Delay Control Word
RW1B, RW1C	QxCA Output Delay Control Word
RW1D	BCS_n and BCOM[2:0] Output Delay Control Word
RW1E	BCK Output Delay Control Word
RW31[7:4, 0]	DFE Configuration Control Word
RW40 .. RW47	Internal VrefCA Control Word
RW48, RW49	Internal VrefCS Control Word
PG[00, 01]	DFE Gain and Tap 1, Tap 2, Tap 3, Tap 4 Coefficients per Input Receiver

Switching between the two frequency contexts is achieved by writing to control word RW05. RW05[6] = 0 selects the default Frequency Context 1 while RW05[6] = 1 selects Frequency Context 2. Changing the setting in RW05[6] by itself only affects which copy of frequency dependent registers responds to MRW writes, MRR reads and SMBus transactions. However, when RW05[6] is different from the value it had in the previous Exit from Clock Stop event, the new settings any updates in RW05[3:0], RW06, and the dual-context registers listed in Table 22 will not be applied internally in the RCD until after the RCD and DRAMs have entered and exited Self Refresh with Clock Stop mode. The RCD will use the value of RW05[6] at the time of Exit from Self Refresh with Clock Stop to determine which context to switch to. A context switch only occurs when the value of RW05[6] is different from the value it had in the previous Exit from Self Refresh with Clock Stop event.

5.4.1 Initial Frequency Setting

Since RW05[6] is a sticky control bit, that is, only cleared by power cycle, the internal current-context state maintained by the RCD must also be sticky. After DRST_n event with stable power, the internal current-context state and RW05[6] will retain the same values they had prior to the DRST_n event.

After Power-on Reset, the internal current-context state will match the Context-1 setting RW05[6] = '0'. Therefore, in this case, any updates in RW05[3:0], RW06, and the dual-context registers listed in Table 22 will be applied immediately to internal circuits and logic without waiting for Exit from Self Refresh with Clock Stop.

5.4.2 Input Clock Frequency Change

Once the DDR5RCD01 is initialized, the DDR5RCD01 requires the clock to be stable during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the stable state, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate only by going through Self Refresh with Clock Stop power down mode. The sequence must allow the host controller to update the frequency dependent registers in the background during normal operation. The sequence of steps for an input frequency change to an RDIMM is outlined below. Note that additional steps are required for an input frequency change to an LRDIMM, and they are documented in the DDR5DB01 specification.

1. Set RW05[6] to choose a frequency context different from the current one. At the same time, update the Frequency Information settings for the next operating speed in RW05[3:0]. These updates will only be applied internally after the RCD exits from Self Refresh with Clock Stop.[1]
2. Write Fine Granularity Frequency information for the next operating speed in RW06. The new setting will only be applied internally after the RCD exits from Self Refresh with Clock Stop.[1]
3. Set new values for the frequency specific registers listed in Table 22 in the background as needed during normal operation. These changes will only be applied internally after the RCD exits from Self Refresh with Clock Stop mode.
4. Go through Entry and Exit from Self Refresh with Clock Stop. The RCD will apply the new settings upon Exit from Self Refresh with Clock Stop.

With the exception of Self Refresh Entry, normal DRAM traffic and operations are supported intermingled with Steps 2 and 3 of the transition sequence defined above.

1. Due to postponed application of RW05/RW06, a t_{STAB01} waiting time is always sufficient after exit from Self Refresh with Clock Stop (i.e., t_{STAB02} is not required). See timing diagrams in Figure 26 on page 37 and Figure 27 on page 38.

6 Data Buffer Control Bus

This section describes the RCD signals used in the DDR5 LRDIMM application. The Data Buffer interface connects the DDR5 Register with each of the ten DDR5 Data Buffer (DB). This interface is enabled on power-on and can only be disabled by setting both RW08[5] and RW09[3] to '1'.

6.1 Control Bus Signals

Table 23 — List of Signals for Data Buffer Control Signals

Name	Description	Signal Count per channel
B[1:0]CS_n	BCOM Chip Select	1
B[1:0]COM[2:0]	Data buffer command signals	3
B[1:0]RST_n	BCOM Reset	1
B[1:0]CK_t, B[1:0]CK_c	Clock outputs for the data buffers	2
	Total	7

6.1.1 Control Bus Signal Termination

BCK_t, BCK_c, BCS_n and BCOM[2:0] signals are terminated to VDDQ on the DDR5 LRDIMM as shown in Figure 48.

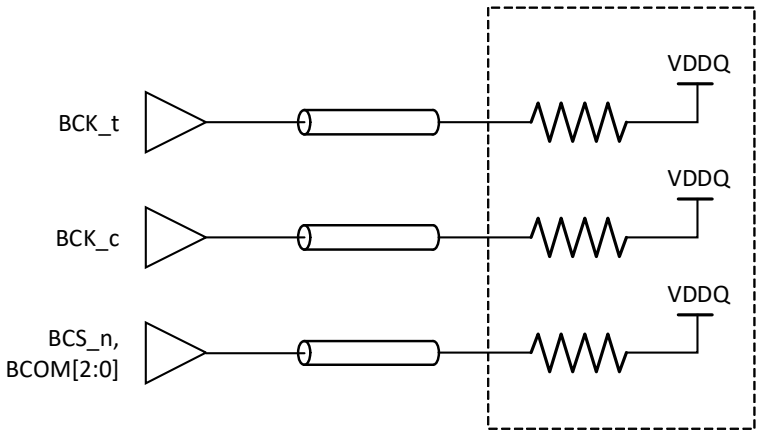

Figure 48 — Control Bus Termination

6.2 Control Bus Timing

The output BCOM signals are driven one clock later than the QxCA_N outputs as shown in Figure 49. Like the QxCA_N outputs, they are delayed by the Command Latency Adder Control Word RW11.

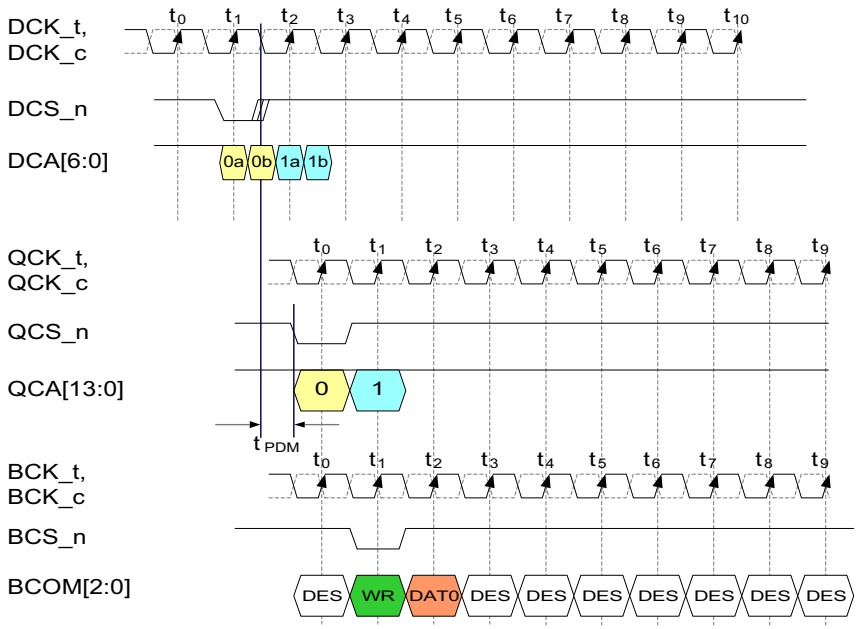

Figure 49 — Example BCOM WR Command

BCOM[2:0] are encoded such that DDR5 command bits can be used directly from the first UI of the command sequence on the RCD host interface. The mapping is as follows:

Table 24 — BCOM bus Mapping

DDR5RCD CA bit	BCOM bit
CA4	BCOM0
CA3	BCOM1
CA1	BCOM2

6.3 Control Bus Commands

6.3.1 Data Buffer Control Bus Command Truth Table

Table 25 — Data Buffer Control Bus Command Truth Table

Command	Description	BCS_n	BCOM[2:0] Encoding
MRW	Mode Register Write	L	000
MRR	Mode Register Read	L	001
WR	Write	L	010
RD	Read	L	011
RFU	Reserved for Future Use	L	100
PDE	Power Down Entry	L	101
MPC	Multi-purpose CMD	L	110
NOP / PDX	Power Down exit if in power down mode.	L	111
DES	BCOM De-select	H	xxx

6.3.2 Command Sequences

Some commands require more than one clock cycle in order to send additional information needed by the Data Buffer in the execution of the command. This succession of command and its corresponding data transfers is called a command sequence. The command sequence for Read or Write commands requires one additional cycle to transfer the rank number corresponding to the write or read command, the sequence for MRW requires seven clock cycles in addition to the basic command, the sequence for the MRR command uses four additional clock cycles. The MPC requires three additional cycles and the PDE command requires only one additional clock cycle. The RCD will drive BCOM DES on the BUS between commands. The Host must guarantee valid DCA[6:0], DPAR, and DCS input signal levels and timings before using BCOM command sequences, including MPC.

6.4 Command Sequence Descriptions

The timing diagrams in this section show only the lower nibble of the Data Buffer. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 16, preamble = 1 nCK and postamble = 0.5 nCK, but equivalent timing relationships exist for burst length = 8 & 18, preamble = 2 nCK and postamble = 1.5 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between second cycle of RD command and the first rising edge of MDQS at the Data Buffer inputs and for the latency between second cycle of WR command and the first rising edge of MDQS at the Data Buffer outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

BCOML = 1 nCK

DB_WL(R) = CWL + DWL(R) - BCOML

DB_RL(R) = CL + MRE(R) - BCOML

Fractional cycle delay equations for DQLDWL and MRE for Ranks 0 and 1 are listed below.

xxx[R].l and xxx[R].u are the equations for the Lower and Upper nibbles, respectively.

DWL[0].l = (PG[0]RWE1[3:0] * 64 + PG[0]RWE8[5:0]) * t_{CK}/64.

DWL[0].u = (PG[0]RWE1[7:4] * 64 + PG[0]RWE9[5:0]) * t_{CK}/64.

DWL[1].l = (PG[1]RWE1[3:0] * 64 + PG[1]RWE8[5:0]) * t_{CK}/64.

DWL[1].u = (PG[1]RWE1[7:4] * 64 + PG[1]RWE9[5:0]) * t_{CK}/64.

MRE[0].l = (PG[0]RWE0[3:0] * 64 + PG[0]RWE2[5:0]) * t_{CK}/64.

MRE[0].u = (PG[0]RWE0[7:4] * 64 + PG[0]RWE3[5:0]) * t_{CK}/64.

MRE[1].l = (PG[1]RWE0[3:0] * 64 + PG[1]RWE2[5:0]) * t_{CK}/64.

MRE[1].u = (PG[1]RWE0[7:4] * 64 + PG[1]RWE3[5:0]) * t_{CK}/64.

Table 26 — Data Buffer PG[1:0] Rank Training Control Word Decoding

DB Control Word	Function
RWE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word
RWE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word
RWE2	Lower Nibble DRAM Interface Receive Enable Training Control
RWE3	Upper Nibble DRAM Interface Receive Enable Training Control
RWE8	Lower Nibble DRAM Interface Write Leveling Control
RWE9	Upper Nibble DRAM Interface Write Leveling Control

The Data Buffer delays tPDM_RD and tPDM_WR are defined as the delay between first effective rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first effective rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per Data Buffer for all ranks and nibbles, however the DB may need to adjust tPDM for non-default register settings in order to maintain the data path fall through time in the device.

Timing parameters that are integer multiples of tCK are shown in **bold blue** letters while timing parameters that are analog non-integer multiples or fractions of tCK are shown in *red italic* letters.

For simplicity the timing diagrams only show one of the possible host interface termination modes and RTT_PARK is never shown even though it is always supported.

6.4.1 WR/RD Burst Length Processing

Table 27 — WR/RD Burst Length Processing

DRAM MR0 Snooped BL Type PG8RWE0[1:0]	DRAM MR50 Snooped WR/RD CRC Enabled PG8RWE8[1:0]	WR/RD Sequence DAT0 BCOM[0]	DB Burst Length Processing (BL)	DB Burst Length Processing Details
00 = BL16 Fixed	Disabled	X	16	
	Enabled	X	18	
01 = BC8 OTF	Disabled	0 = BC8	8	
		1 = BL16	16	
	Enabled	X	18	
10 = BL32 Fixed	Disabled	X	32	The dummy WR/RD command that is 8 tCK after the primary WR/RD command is ignored[1]
	Enabled	X	36	The dummy WR/RD command that is 9 tCK after the primary WR/RD command is ignored.[1]
11 = BL32 OTF	Disabled	0 = BL32	32	The dummy WR/RD command that is 8 tCK after the primary WR/RD command is ignored.[1]
		1 = BL16	16	
	Enabled	0 = BL32	36	The dummy WR/RD command that is 9 tCK after the primary WR/RD command is ignored.[1]
		1 = BL16	18	

1. The dummy WR/RD command is assumed to be to the same rank and of the same burst length type as the primary WR/RD command.

6.4.2 MRR Burst Length Processing

Table 28 — MRR Burst Length Processing

DRAM MR0 Snooped BL Type PG8RWE0[1:0]	DRAM MR50 Snooped Read CRC Enable (PG8RWE8[0])	Control Register Command Sequence	DB Burst Length Processing (BL)	DB Burst Length Processing Details
XX	Disabled	DRAM-Space MRR	16	
	Enabled		18	
XX	Disabled	DB-Space MRR to Control Word	16	
	Enabled		18	The last two bits of the BL18 burst are Don't Care (X).
XX	Disabled	DB-Space MRR to the Read Training Pattern	16	
	Enabled		Illegal	The DB assumes that the host will ensure that read CRC is disabled since it is necessary for the LFSR pattern to be kept continuous. Read CRC is unnecessary since the known LFSR pattern intrinsically allows for error checking.

Table 29 — PBA Enumerate ID Programming Burst Length Processing

DRAM MR0 Snooped BL Type (PG8RWE0[1:0])	DRAM MR50 Snooped Write CRC Enable (PG8RWE8[1])	Control Register Command Sequence	DB Burst Length Processing (BL)	DB Burst Length Processing Details
XX	Disabled	PBA Enumerate ID Programming MRW	16	Used to capture the Enumerate ID.
	Enabled		Illegal	The DB assumes that the host will ensure that Write CRC is disabled.

6.4.3 MRW Commands

The RCD generates MRW commands to the data buffers for each MR command. Table 30 shows the sequence for MRW commands.

Table 30 — Multi-cycle Sequence for MRW Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MRW	MRW Command BCOM[2:0] = 000
2	1	DAT0	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[2:1] = RFU
3	1	DAT1	BCOM[1:0] = MRA[7:6] BCOM[2] = RFU
4	1	DAT2	BCOM[2:0] = MRA[5:3]
5	1	DAT3	BCOM[2:0] = MRA[2:0]
6	1	DAT4	BCOM[1:0] = OP[7:6] BCOM[2] = RFU
7	1	DAT5	BCOM[2:0] = OP[5:3]
8	1	DAT6	BCOM[2:0] = OP[2:0]
9		Next Cmd	Next Command

The sequence for an MRS Write command is shown in Figure 50 below. The timing diagrams show how the MR Write command is followed by seven data transfer cycles. Since the command sequence uses eight cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the MRW command to the following valid command (also shown in the diagrams). The number of additional transfers on the BCOM bus after the MRW command also imposes a limitation on how close consecutive MRW commands can be issued to the Data Buffer.

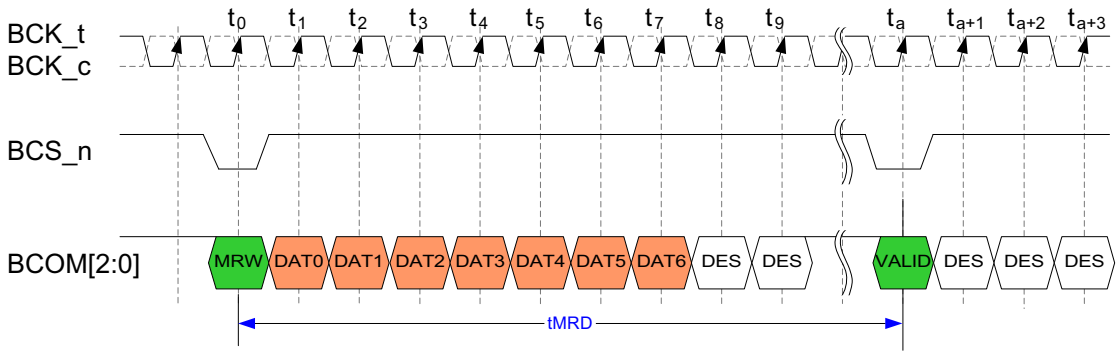

Figure 50 — MRW command sequence

6.4.4 MRR Commands

6.4.4.1 Multi-cycle Sequence for MRR Commands

Table 31 shows the sequence for MRR commands.

Table 31 — Multi-cycle Sequence for MRR Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MRR	Mode Register Read Command BCOM[2:0] = 001
2	1	DAT0	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU NOTE Burst length is fixed BL16
3	1	DAT1	BCOM[1:0] = MRA[7:6] BCOM[2] = RFU
4	1	DAT2	BCOM[2:0] = MRA[5:3]
5	1	DAT3	BCOM[2:0] = MRA[2:0]
6		Next Cmd	Next Command

MRR commands read data from the MR locations in either the DRAM or the data buffer. MR locations in the RCD must be read by first transferring their contents to a DRAM register then reading that DRAM register. If the CW bit is a 0 the read will come from the DRAMs, and the data buffer will treat this command like a read command. The case CW = 1 MRA7 = 0 is not defined. Data Buffer will treat it as invalid address and Read zeros. If the CW = 1 and MRA7 = 1, then read will come from the Data Buffer's MR location. The Data Buffer will send the same data on all DQs for the second 8 UI and drive High or Low on the first 8 UI as shown in Table 33.

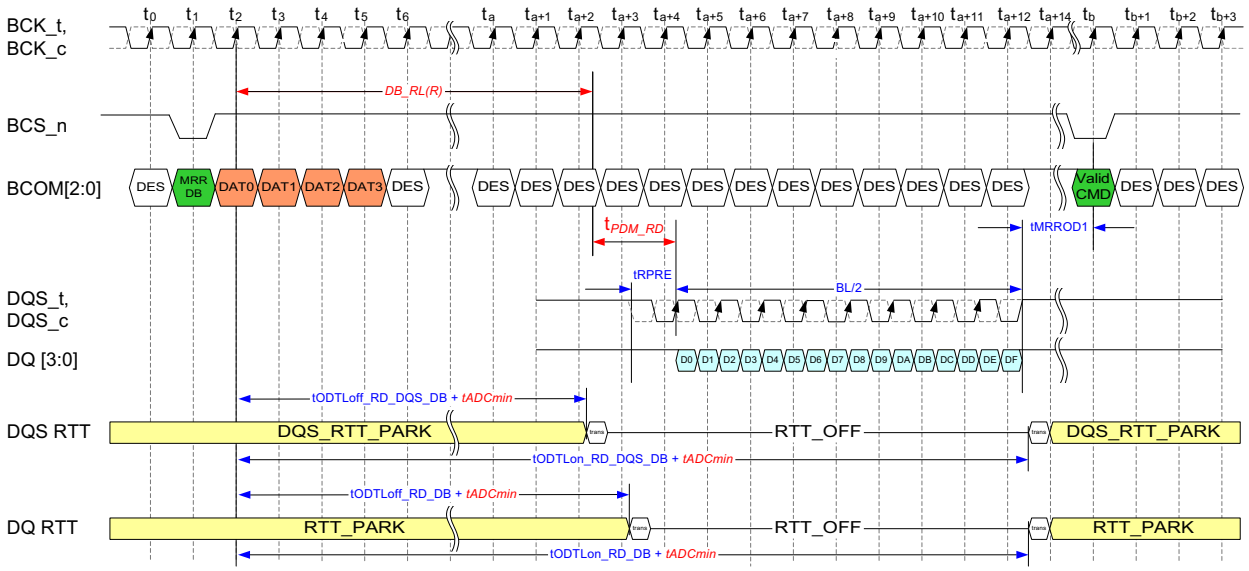

Figure 51 — MRR Command Sequence to Data Buffer address space

6.4.4.2 Short MRR Command for SDR Training

Table 32 — Short MRR Command for SDR Training[1]

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MRR	Mode Register Read Command BCOM[2:0] = 001
2	1	DAT0	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU NOTE Burst length is fixed BL16
3		Next Cmd	Next Command

1. Provides a shorter MRR command for SDR mode Host interface Data Buffer DQ training to maintain a continuous read from Data Buffer pattern generator.

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Table 33 — MRR Read Format for Data Buffer Return

Serial	UI 0-7	UI 8	UI 9	UI 10	UI 11	UI 12	UI 13	UI 14	UI 15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Table 34 — MRR Read Format for Data Buffer Return with Read CRC Enabled

Serial	UI 0-7	UI 8	UI 9	UI 10	UI 11	UI 12	UI 13	UI 14	UI 15	UI 16	UI 17
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x

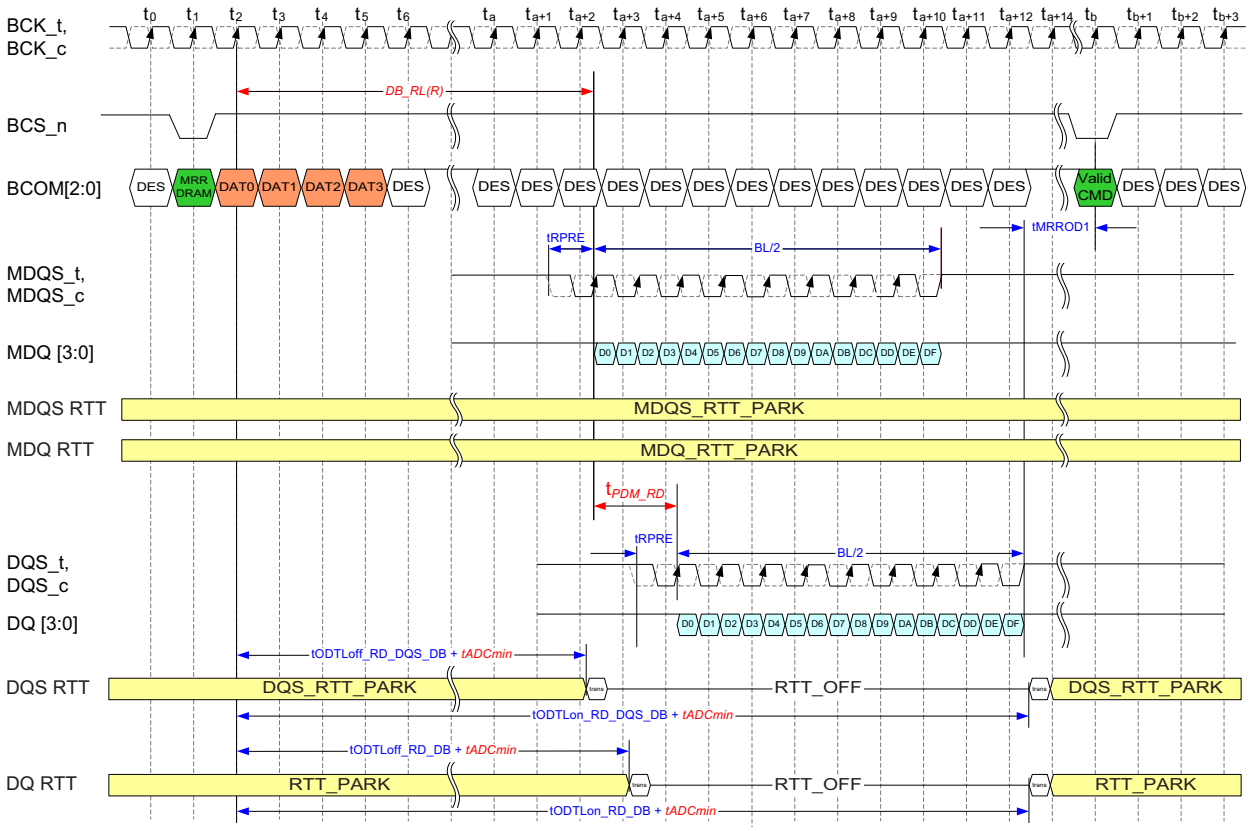


Figure 52 — MRR Command Sequence to DRAM Address Space

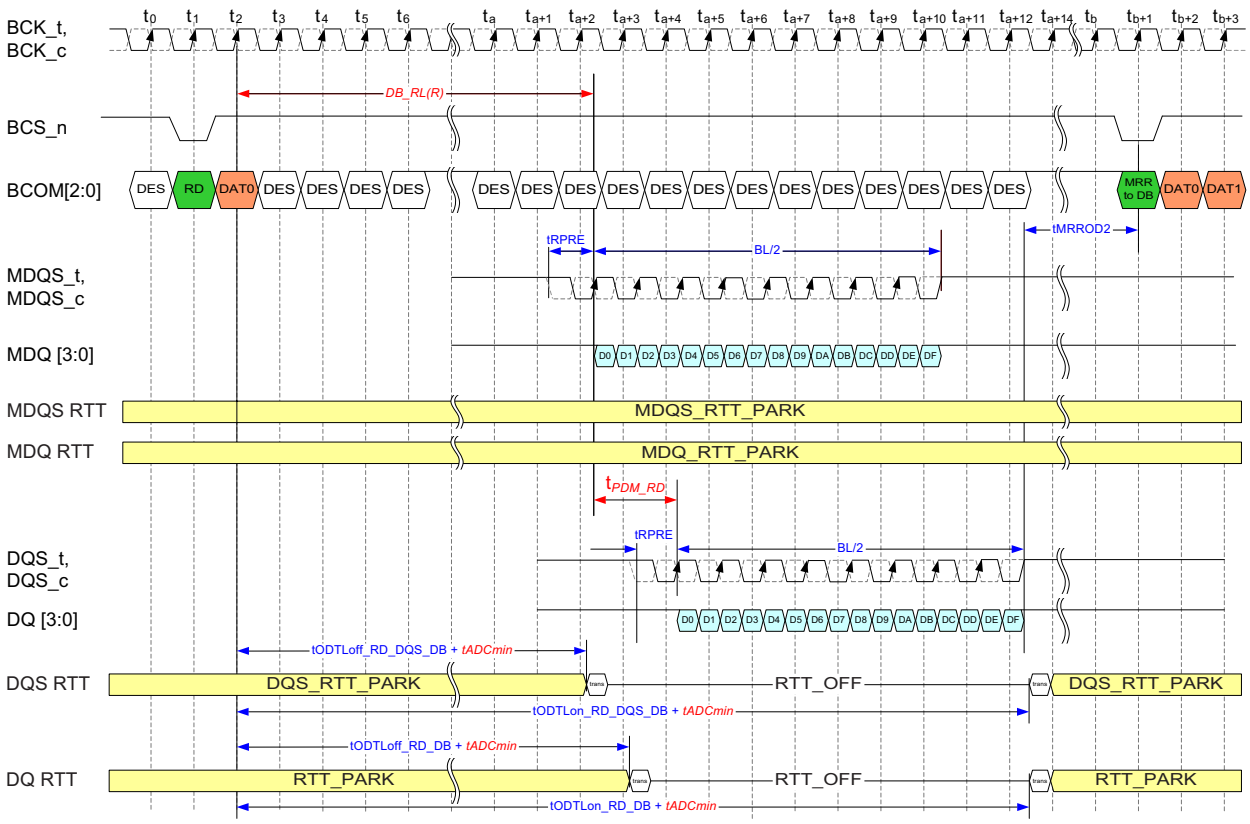
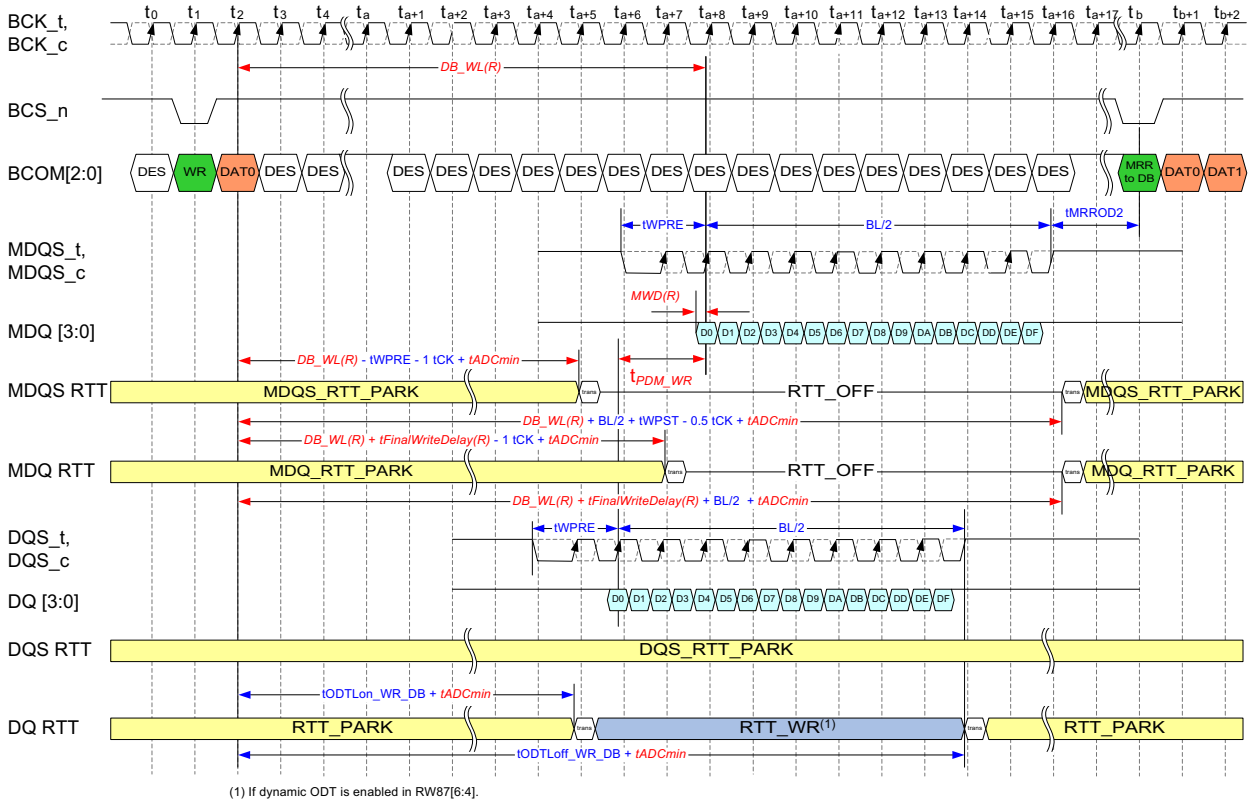


Figure 53 — RD to MRR Command Sequence to Data Buffer Address Space



Note: tFinalWriteDelay(R) = tMdqWriteBaselineDelay(R) + tDram_DqsDelay_Change(R)

Figure 54 — WR to MRR Command Sequence to Data Buffer Address Space

6.4.5 WR Commands

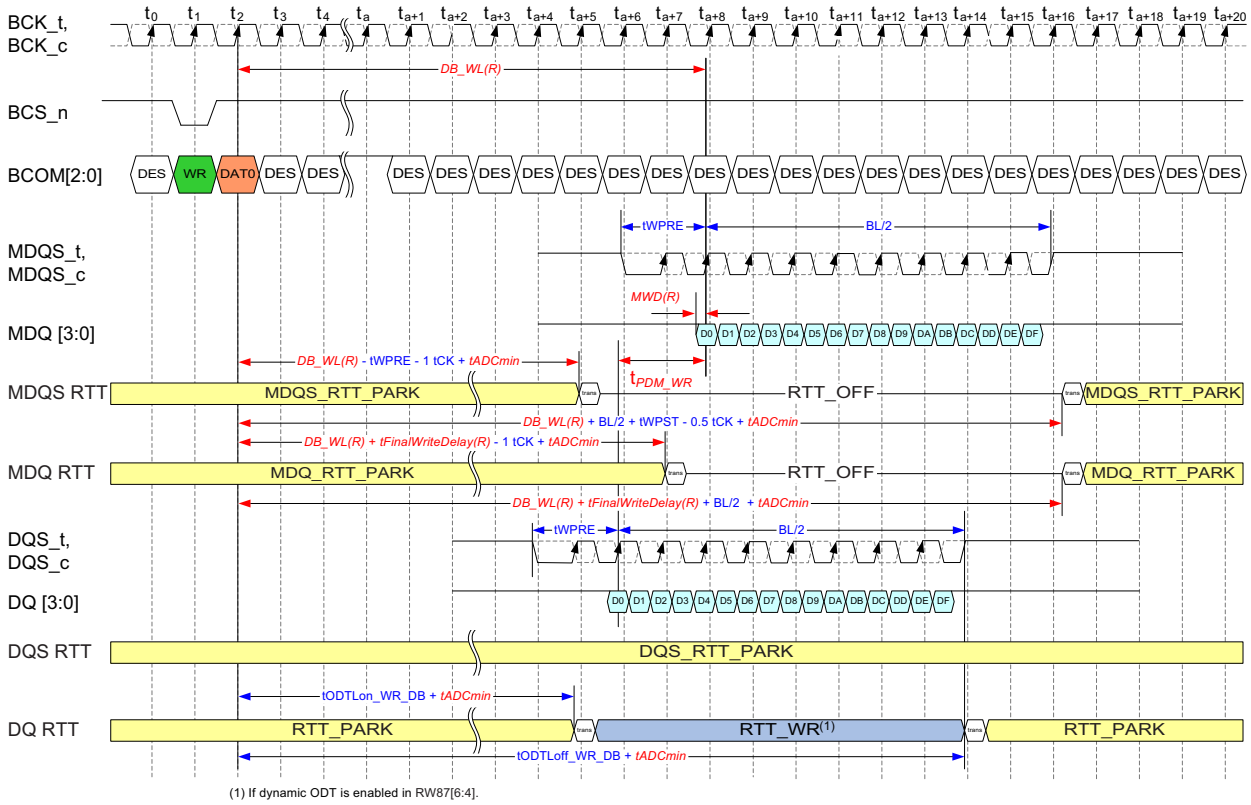
Table 35 shows the sequence for write (WR8, WR16) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 2 that needs to be accessed and the burst length information for the data transfer. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the Data Buffer, the burst length will always be 18 or 36 UI.

Table 35 — Multi-cycle Sequence for WR Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	WR	Write command BCOM[2:0] = 010
2	1	DAT0	Rank ID & BL BCOM[0] = BL; 0=BC8 or BL32, 1=BL16 BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU
3		Next Cmd	Next Command

If BCS_n is active for 2 clock cycles, it indicates a non-target write termination. The Data Buffer will terminate with RTT_NOM_WR and will not transfer data through the buffer. In this case DB will use Rank 0 timing automatically.

Figure 55 shows the timing sequence for a Write command.



Note: tFinalWriteDelay(R) = tMdqWriteBaselineDelay(R) + tDram_DqsDelay_Change(R)

Figure 55 — WRITE Timing

6.4.6 RD Commands

Table 36 shows the sequence for read (RD8, RD16) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 2 that needs to be accessed and the burst length information for the data transfer. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[0] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the Data Buffer if the BL field in the snoop register is set for fixed burst length of 8, 16, or 32. If CRC is enabled in the DRAM and in the Data Buffer, the burst length will always be 18 or 36 UI.

Table 36 — Multi-cycle Sequence for RD Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	RD	Read command BCOM[2:0] = 011
2	1	DAT0	Rank ID & BL BCOM[0] = BL; 0 = BC8 or BL32, 1=BL16 BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU
3		Next Cmd	Next Command

If BCS_n is active for 2 clock cycles, it indicates a non-target read termination. The Data Buffer will terminate with RTT_NOM_RD and will not transfer data through the buffer. In this case DB will use Rank 0 timing automatically.

Figure 56 shows the timing sequence for a Read command.

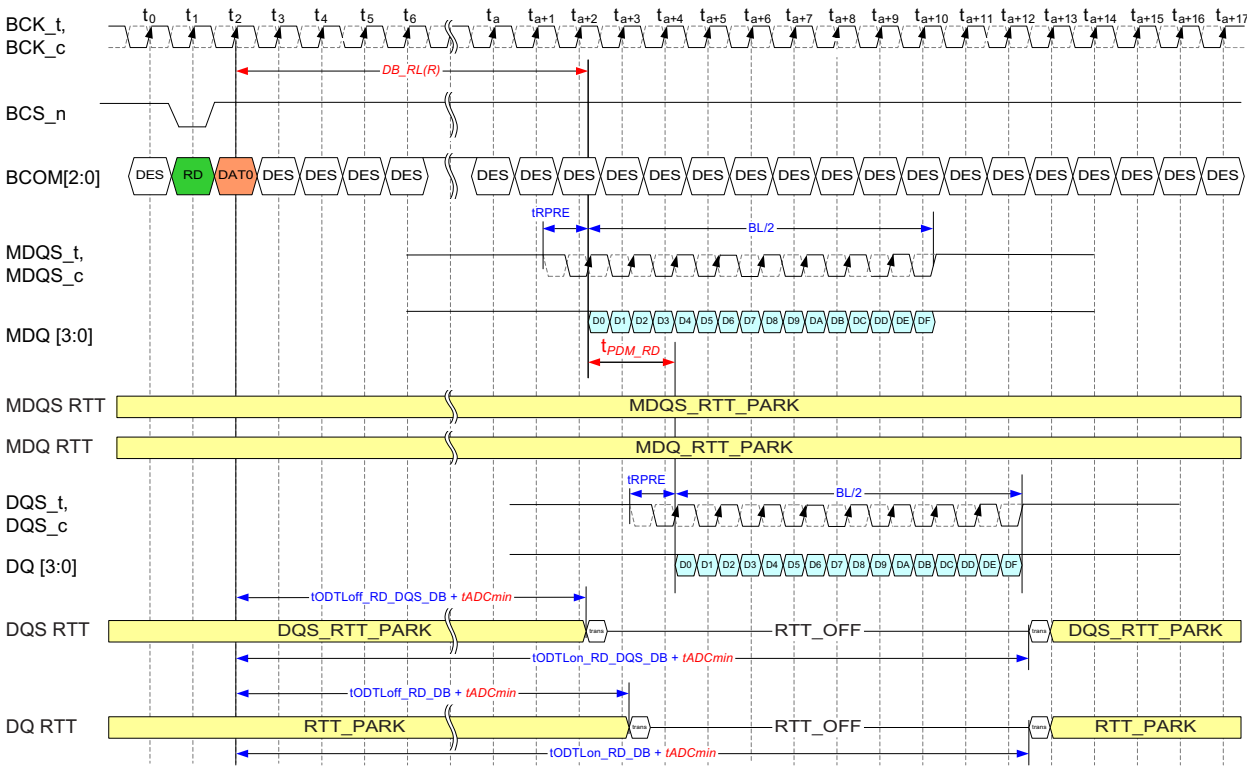


Figure 56 — READ Timing

6.4.7 PDE Commands

The Power Down Entry command is only sent on the BCOM bus when all ranks are being put into or are already in power down. Table 37 shows the sequence for PDE commands.

Table 37 — Multi-cycle Sequence for PDE Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	PDE[1]	Power-Down Entry Command BCOM[2:0] = 101
2	1	DAT0	PDE Modes and ODT BCOM [0] = ODT; 0 = Enabled, 1 = Disabled BCOM [1] = SR/PDE; 0 = Self Refresh, 1 = PDE BCOM [2] = RFU
3		Next Cmd	Next Command

1. Since the PDE command is a 1-Cycle command on the DRAM bus and a 2-Cycle command on the BCOM bus, the host controller must ensure there is enough spacing between the PDE command and the following command that uses the BCOM bus. When the BCOM interface is enabled (RW09[3] = 0), a PDE command received on the DCA bus shall not be followed immediately (i.e. in the following clock cycle) by any command that is processed in the BCOM interface including MRW, MRR, WR, RD, PDE, SRE, MPC, and NOP/PDX.

6.4.8 MPC Command

Table 38 shows the sequence for MPC commands.

Table 38 — Multi-cycle Sequence for MPC Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MPC	Multi-purpose Command BCOM[2:0] = 110
2	1	DAT0	BCOM[1:0] = OP[7:6] BCOM[2]= RFU
3	1	DAT1	BCOM[2:0] = OP[5:3]
4	1	DAT2	BCOM[2:0] = OP[2:0]
5		Next Cmd	Next Command

6.4.9 NOP / Power Down Exit

Table 39 shows the sequence for NOP / PDX commands.

Table 39 — Multi-cycle Sequence for NOP/PDX Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	NOP/PDX	NOP / PDX Command BCOM[2:0] = 111
2		Next Cmd	Next Command

When in power down, an active BCS_n signal will return the Data Buffer to the active state. The BCOM command will indicate NOP so that no other command is executed.

7 SidebandBus Interface

For all configuration registers, the DDR5RCD01 supports register access mechanisms through a SidebandBus in addition to In-band Channel commands. The registers may be read by software from the SidebandBus host at any time the RCD is powered on and receiving valid input clock, except in the Self Refresh power down state with Clock Stop or when the device DRST_n pin is asserted.

The SidebandBus interface of the DDR5RCD01 device is compliant to the JEDEC Module SidebandBus Specification, JESD403-1. See JESD403-1 for details. SidebandBus is a two-wire interface based on SDA and SCL. This section describes the minimum subset of the I3C Basic Specification that must be supported to meet the requirements and usage modes of the SidebandBus in the DDR5 DIMM application space.

The DDR5RCD01 SidebandBus Interface must co-exist with other devices using the same bus on an RDIMM or LRDIMM, including Temperature Sensor, SPD, and PMIC devices, and shall not inhibit the operation of the SidebandBus when the module V_{DD} or V_{DDQ} supply rails are disabled (but V_{DDIO} is available) or when the RCD goes through Self Refresh power down state Entry or Exit with Clock Stop.

DRST_n does not reset the SidebandBus Interface of the DDR5RCD01 device. When it is under Clock Stop condition or when DRST_n is asserted (LOW), the DDR5RCD01 device is required to support the following operations from normal operation:

- Timeout Reset (see Section 7.6 on page 100).
- I2C/I3C Basic Common Command Code (CCC) packets (excluding DEVCTRL with RegMod = 1).

I2C and I3C Basic Write/Read packets are not supported in Clock Stop condition or when DRST_n is asserted and they may result in undefined responses.

7.1 SidebandBus Requirements During Initialization of RCD

- DDR5RCD01 is responsible for staying off the bus when V_{DD} is not powered on but V_{DDIO} is enabled. When V_{DD} is not powered on, the RCD does not respond to any commands or events.
- The host is responsible for keeping the SidebandBus idle (i.e., no traffic) during the time V_{DD} is ramping up (e.g., following a PMIC VR Enable command).
- DDR5RCD01 is required to respond to CCC (excepting DEVCTRL with RegMode = 1) and also to Timeout Reset when V_{DD} is valid and stable (as well as V_{DDIO}) even when DRST_n is still LOW during power-up initialization.
- The RCD is required to support register Write/Read access and DEVCTRL CCC with RegMode = 1 only after t_{STAB01} following stable DCK clock (which happens after DCS_n LOW-to-HIGH transition).

7.2 Feature Summary

- I^2C Fast-mode Plus (FM+) and I3C Basic supported.
- In-band interrupt supported in I3C Basic mode.
- The DDR5RCD01 SidebandBus Interface shall not initiate clock stretching.
- Multi-controller capability not supported.
- Hot join capability not supported.

The DDR5RCD01 is required to support Read and Write Transactions without requiring clock stretching in order to simplify Host controller requirements. For similar reasons, the RCD shall not control SidebandBus transactions in normal operation.

7.3 Operating Ranges

- Speed: support 1 MHz (I^2C FM+) in I^2C Mode and up to 12.5 MHz in I3C Basic mode.
- Voltage: V_{DDIO} Supply from 1.0 V - 0.05 V to 1.0 V + 0.05 V for SDA/SCL I/O levels.

7.4 External Pins

The RCD Sideband Interface uses the following two external device pins.

7.4.1 Serial Clock (SCL)

This input signal is used to strobe data in and out of the device. This signal driven by the bus controller using a push-pull driver. In I^2C mode only, it is also possible to use an open-drain driver in the bus controller, provided that the board has a pull-up resistor connected between SCL and V_{DDIO}, for example.

7.4.2 Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an output capable of operating in open-drain mode or push-pull mode. A pull up resistor may be connected from Serial Data (SDA) to V_{DDIO}, for example. If the pull-up resistor is not present in the board, the bus controller must provide on-chip termination.

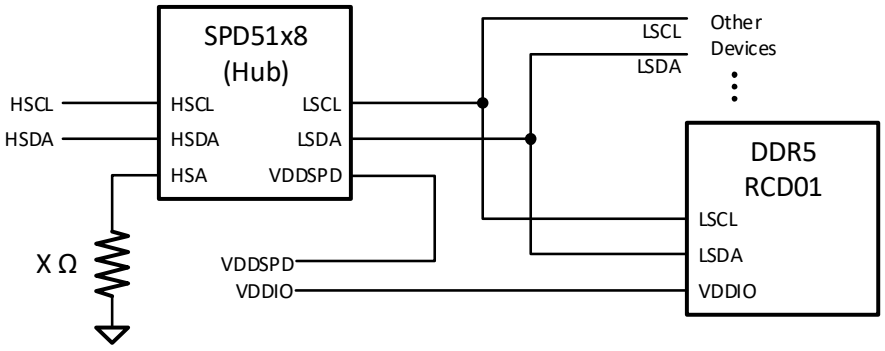


Figure 57 — SidebandBus Wiring Diagram

7.5 System Management Access

System Management software in the platform can initiate system management access to the configuration registers. This can be done through SidebandBus accesses.

DDR5RCD01 components contain a SidebandBus target port and allow access to the configuration registers.

SidebandBus operations are made up of two major steps:

1. Writing information to registers within each component.
2. Reading configuration registers from each component.

The following sections will describe the protocol for a SidebandBus controller to access an RCD component's internal configuration registers.

7.5.1 Target Address

The 7-bit target address used for each primitive SidebandBus transaction is determined by the 4-bit Local Device address (LID) and the 3-bit Host Device address (HID). The HID bits of the RCD device have a default value of '111' but the value of LID is fixed.

- DDR5RCD01 I^2C Bus and I3C Basic Bus address:
  - — Target Address[6:3] = 4'b1011 (LID)
  - — Target Address[2:0] = HID code configured by SETHID command

7.5.2 Supported SidebandBus Commands

The DDR5RCD01 Sideband target port supports register reads and writes built out of the following Management Bus primitive commands:

- I^2C Mode:
  - — **Block Write** — **Byte Write**
  - — **Block Read** — **Byte Read**
- I3C Basic Mode:
  - — **Block Write**
  - — **Block Read**

The DDR5RCD01 device is not required to support block accesses larger than a double word.

Each SidebandBus transaction has an 8-bit command driven by the controller. The format for this command is defined in Table 40, "SidebandBus Command Format in I2C Mode" and Table 41, "SidebandBus Command Format in I3C Basic Mode" below.

Table 40 — SidebandBus Command Format in I^2C Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bits [3:2]	Bits [1:0]
Begin	End	Rsvd	PEC_en[1]	Internal Command: 00 - Read DWord 01 - Write Byte 10 - Write Word 11 - Write DWord	SidebandBus Command: 00 - Byte Mode[2] 01 - Reserved 10 - Block Mode 11 - Reserved

1. See Table 41. The PEC_en bit only applies in I^2C mode. In I3C Basic mode, Bit 4 of the SidebandBus Command is ignored and PEC is controlled by PEC Enable bit received via DEVCTRL CCC (see Table 86 on page 113). In I^2C mode, the value of PEC Enable bit received via DEVCTRL CCC is ignored and PEC is controlled by Bit 4 of the SidebandBus Command.
2. See Table 41. Byte mode transactions are only supported in I^2C mode. When not in I^2C mode, Bits [1:0] of the SidebandBus Command are ignored and all transactions are all conducted in block mode.

Table 41 — SidebandBus Command Format in I3C Basic Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bits [3:2]	Bits [1:0]
Begin	End	Rsvd	Rsvd[1]	Internal Command: 00 - Read DWord 01 - Write Byte 10 - Write Word 11 - Write DWord	Rsvd[2]

1. In I3C Basic mode, Bit 4 of the SidebandBus Command is ignored and PEC is controlled by PEC Enable bit received via DEVCTRL CCC (see Table 86 on page 113).
2. In I3C Basic mode, Bits [1:0] of the SidebandBus Command are ignored and all transactions are all conducted in block mode.

The *Begin* bit indicates the first transaction of a read or write sequence.

The *End* bit indicates the last transaction of a read or write sequence.

The *PEC_en* bit enables the 8-bit PEC generation and checking logic when the interface is running in I^2C mode.[1]

The *Internal Command* field specifies the internal command to be issued by the SidebandBus target logic. Note that the Internal Command must remain consistent (i.e. not change) during a sequence that accesses a configuration register. Operation cannot be guaranteed if it is not consistent when the command setup sequence is done.

The *SidebandBus Command* field specifies the I^2C/I3C Basic command to be issued on the bus. This field is used as an indication of the length of transfer so the target knows when to expect the PEC packet (if enabled).

Reserved bits should be written to zero to preserve future compatibility.

Hosts are required to form commands that are internally self consistent. The length indicated by the internal command should be consistent with the byte count and the DDR5RCD01 behavior will be undefined when the internal command is inconsistent with the byte count.

7.5.3 Register Access Protocols

Sequences of these basic commands will initiate internal accesses to the component's configuration registers.

Each Configuration Read or Write consists of an I^2C/I3C Basic Write sequence which initializes the register's address. The term sequence is used since these variables may be written with a single Block Write (in I^2C or I3C Basic modes) or multiple Byte Writes (in I^2C mode). Once these parameters are initialized, the SidebandBus controller can initiate a Read sequence (which performs a Configuration Read) or a Write sequence (which performs a Configuration Write).

The DDR5RCD01 will generate a BCOM MRW command sequence for each configuration Write Byte Internal Command targeted to address range 80h-FFh. The MRW command will be issued only on the BCOM interface channel selected in the Dev/Function byte of the Sideband command (provided that the BCOM interface is not disabled).

Table 42 — SidebandBus Protocol Addressing Fields

Address Field Name	Bits	Description
Reserved	7:0	Reserved - Device may alias all these bits to 00h
Dev	3:0	Reserved - Device may alias all these bits to 0h
Channel_Num	3:0	Channel Number 0000 = Channel A 0001 = Channel B All others Vendor Specific
Page_Num[15:8]	7:0	Page number when Reg_Num is within 60h-7Fh address range. Ignored if Reg_Num is within 00h-5Fh address range.
Reg_Num[7:0]	7:0	Register Address. Addresses within 60h-7Fh range use the page number above. In case of configuration Write Byte Internal Command, and provided that the Data Buffer interface is enabled in RW09[3], addresses within the 80h-FFh range result in a BCOM MRW command sequence for the selected channel.

1. To keep backwards-compatibility with the DDR4 RCD device, PEC support in I^2C mode is required in the DDR5RCD01 device even though this feature is not described in the JESD403-1 specification.

7.5.3.1 Access Mechanism

For all Configuration and Status registers, the DDR5RCD01 supports register access mechanisms through the SidebandBus Interface as well as through In-band Channel commands. The registers may be read by software from the SidebandBus host at any time the DDR5RCD01 is powered on, except in the Self Refresh power down state with Clock Stop or when the device DRST_n pin is asserted.

Table 43 shows the mapping between DDR5RCD01 control words and I^2C/I3C Basic register numbers. The entire register space of the DDR5RCD01 is accessible with the Channel_Num, Page_Num, and Reg_Num SidebandBus address fields.

Table 43 — SidebandBus Address Map

RW Type	Page_Num [15:8]	Reg_Num [7:0]	RW Page	RW
Direct Control Words	x	00	NA	RW00
	x	01	NA	RW01
	...	...	...	..
	x	5Fh	NA	RW5F
Paged Control Words	00	60h	PG[00]	RW60
	00	61h	PG[00]	RW61
	...	...	...	...
	00	7Fh	PG[00]	RW7F
	01	60h	PG[01]	RW60
	...	...	...	
	FFh	7Fh	PG[FF]	RW7F

Each byte of the DDR5RCD01 register space has its own unique address. For CSR Writes, the RCD registers can be accessed in Byte (8-bit), Word (16-bit) or Double Word (32-bit) quantities. For CSR Reads, the device registers can only be accessed in Double Word (32-bit) quantities.

All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field). As an example Table 44 defines the byte order for double word accesses to the DDR5RCD01 control words.

In this chapter CSRs are defined as 8-bit registers. Since a byte is the smallest access granularity for CSRs, a single 8-bit CSR contains one RCD Control Word.

Table 44 — Double Word Byte Order for SidebandBus Control Word Access

Description	Data[31:24]	Data[23:16]	Data[15:8]	Data[7:0]
RW03 RW00	RW03	RW02	RW01	RW00
RW07 - RW04	RW07	RW06	RW05	RW04
...	...	...	...	...
RW7F - RW7C	RW7F	RW7E	RW7D	RW7C

7.5.4 Sequence for switching from I^{2}C mode to I3C Basic

The DDR5RCD01 device will start with the Sideband Interface enabled to support I^{2}C protocol by default. When I^{2}C protocol is selected in RW25[5] (SidebandBus Mode status bit controlled by SETAASA and RSTDAA commands), the following limitations apply.

1. Operation speed is limited to 1 MHz compatible with FM+ mode I^{2}C, and
2. In-band interrupts are not supported.
3. CCC support limited to DEVCTRL, SETHID, and SETAASA common command codes.
4. In I^{2}C mode, Start or Repeat Start operation followed by 7'h7E with W = 0 is only allowed for the purpose of issuing CCCs that are supported in I^{2}C mode.

In I3C Basic mode, full functionality including 12.5 MHz operation and IBIs are enabled.

The Host puts the DDR5RCD01 device in I3C Basic mode by issuing SETAASA CCC. The host must issue DEVCTRL and SETHID Commands first (if needed) followed by SETAASA. When SETAASA CCC is registered by the device, the DDR5RCD01 updates RW25[5] to '1'.

The Host puts the DDR5RCD01 device in I^{2}C mode by issuing RSTDAA CCC. When RSTDAA CCC is registered by the device, the DDR5RCD01 updates RW25[5] to '0'. Moreover, the RCD is allowed to disable IBI, disable PEC, and enable I3C Basic Parity Checking functions. The host is expected to send DISEC and DEVCTRL commands to disable IBI, disable PEC, and enable Parity Checking prior to issuing the RSTDAA CCC.

7.5.5 Parity Error Checking

By default, when device is put in I3C Basic mode, parity function is automatically enabled. The host can disable the function after it is enabled. Host can also disable the parity function with DEVCTRL CCC. When parity function is disabled, the device simply ignores the "T" bit information from the Host. The host may actually choose to compute the parity and send that information during "T" bit or simply drive static LOW or HIGH in "T" bit.

The device implements ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'. If even number of bits in the byte are '1', the parity bit value is '1'. The host computes the parity for each byte except for the device select code byte and sends it during "T" bit.

7.5.6 PEC Support

DDR5RCD01 devices operate on a standard I3C Basic serial interface. Transactions where the DDR5RCD01 device is the targeted Target device begin with the I3C Basic Host issuing a START condition followed by a 7-bit DDR5RCD01 device type identifier then a Read or Write bit, RW. All I3C Basic data are transmitted with the most significant bit MSB first. During select code transmission, the DDR5RCD01 device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

The optional appended PEC on the data stream covers the information transmission between the host and the DDR5RCD01 device.

If the optional IBI header (7'h7E and W = 0) byte is present, the DDR5RCD01 device will exclude it in its PEC calculation. Other than that, the RCD target device will include all bytes, including the address byte, in its local PEC checking logic.

All DDR5RCD01 devices implement an 8-bit Packet Error Code (PEC) which is appended at the end of all I3C Basic transactions if PECs are enabled through DEVCTRL CCC. The RCD also supports PEC in I^{2}C mode, if enabled in Bit 4 of the Bus Command. The PEC is a CRC-8 value calculated on all the message bytes excluding START, Repeat START, STOP, T-bits, ACK, NACK, and IBI header (7'h7E followed by W = 0) bits. The algorithm for all CRC-8

calculations is:

$$C(x) = x^8 + x^2 + x^1 + 1$$

The seed value for PEC function is all zero.

PECs are disabled by default on power up or RESET. The host may optionally enable PEC function. If enabled, the host must complete the burst length (or byte count) as indicated. In other words, the host must not interrupt the burst length (or byte count) prematurely for Write or Read operation. It is considered an illegal operation.

7.5.7 Sideband Control Word Read Protocol

Configuration Reads are accomplished through an I^2C/I3C Basic Write(s) and later followed by an I^2C/I3C Basic Read. The Write sequence is used to initialize the Device, Channel, Page, and Register Numbers for the configuration access. The writing of this information can be accomplished through any combination of the supported I^2C/I3C Basic write commands (Block command in I^2C and I3C Basic modes or Byte command in I^2C mode). The *Internal Command* field for each write should specify Read DWord.

All I^2C/I3C Basic Configuration Reads should be DWord aligned. The DDR5RCD01 register will ignore the lowest two bits of the Register Address and return the four bytes within a DWord in the byte order shown in the following examples, i.e. Most Significant Byte (Data[31:24]) first and Least Significant Byte (Data[7:0]) last.

After all the information is set up, the last Write (*End* bit is set) initiates an Internal Configuration Read. If an error occurs during the internal access, the last Write Command will receive a NACK. A status field indicates abnormal termination and contains status information such as target abort. The status field encoding is defined in Table 45 below.

Table 45 — Status Field Encoding for SidebandBus Reads

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Internal Target Abort[1]
3:1	Reserved
0	Successful

1. A value of 1 indicates access to invalid internal register address. The only condition for this event is attempting Read access to control/status registers located in Data Buffer space. Access to Reserved locations of the RCD is not considered invalid.

7.5.7.1 I^2C Read Packet Format Definitions

Examples of Configuration Reads are illustrated below. For I^2C Bus read transactions, the last byte of data (or the PEC byte if enabled) is NACKed by the controller to indicate the end of the transaction.

Table 46 — I²C Read Command Packet Example (Block Mode, PEC Disabled, Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11000010								A	
	Byte Count = 4								A	
	Reserved								A	
	Dev/Channel_Num								A	
	Page_Num [7:0]								A	
	Reg_Num [7:0]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11000010								A	
Sr	1	0	1	1	HID			R=1	A	
	Byte Count = 5								A	
	Status								A	
	Rd Data[31:24]								A	
	Rd Data[23:16]								A	
	Rd Data[15:8]								A	
	Rd Data[7:0]								N	P

The above packet format must be supported in I²C Legacy mode for backwards compatibility with older controllers.

Table 47 — I²C Read Command Packet Example (Block Mode, PEC Enabled, Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11010010								A	
	Byte Count = 4								A	
	Reserved								A	
	Dev/Channel_Num								A	
	Page_Num [7:0]								A	
	Reg_Num [7:0]								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11010010								A	
Sr	1	0	1	1	HID			R=1	A	
	Byte Count = 5								A	
	Status								A	
	Rd Data[31:24]								A	
	Rd Data[23:16]								A	
	Rd Data[15:8]								A	
	Rd Data[7:0]								A	
	PEC(8)								N	P

The above packet format must be supported in I²C mode for backwards compatibility with older controllers. The table coloring identifies the portion of the packet covered by each PEC byte.

Table 48 — I²C Read Command Packet Example (Block Mode, PEC Disabled, Optimized Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11000010								A	
	Byte Count = 4								A	
	Reserved								A	
	Dev/Channel_Num								A	
	Page_Num [7:0]								A	
	Reg_Num [7:0]								A	
Sr	1	0	1	1	HID			R=1	A	
	Byte Count = 5								A	
	Status								A	
	Rd Data[31:24]								A	
	Rd Data[23:16]								A	
	Rd Data[15:8]								A	
	Rd Data[7:0]								N	P

The optimized I²C Read packet format is only supported in Block Mode with PEC disabled. This optimized case without redundant bytes must be supported in I²C mode for better protocol efficiency.

Table 49 — I²C Read Command Packet Example (Byte Mode, PEC Disabled, Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 10000000								A	
	Reserved								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00000000								A	
	Dev/Channel_Num								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00000000								A	
	Page_Num [7:0]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 01000000								A	
	Reg_Num [7:0]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 10000000								A	
Sr	1	0	1	1	HID			R=1	A	
	Status								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00000000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[31:24]								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00000000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[23:16]								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00000000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[15:8]								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 01000000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[7:0]								N	P

The package format shown above must be supported in I²C mode for backwards compatibility with older controllers.

Table 50 — I²C Read Command Packet Example (Byte Mode, PEC Enabled, Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 10010000								A	
	Reserved								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00010000								A	
	Dev/Channel_Num								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00010000								A	
	Page_Num [7:0]								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 01010000								A	
	Reg_Num [7:0]								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 10010000								A	
Sr	1	0	1	1	HID			R=1	A	
	Status								A	
	PEC(8)								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00010000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[31:24]								A	
	PEC(8)								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00010000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[23:16]								A	
	PEC(8)								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00010000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[15:8]								A	
	PEC(8)								N	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 01010000								A	
Sr	1	0	1	1	HID			R=1	A	
	Rd Data[7:0]								A	
	PEC(8)								N	P

The packet format shown above must be supported in I²C mode for backwards compatibility with older controllers. The table coloring identifies the portion of the packet covered by PEC.

The case for Optimized Packet format is not supported in Byte Mode I²C Read transactions in byte mode with optimization does not need to be supported due to the inherent inefficiency of Byte Mode.

7.5.7.2 I3C Basic Mode Read Packet Format Definitions

Prior to the Repeated START in the Read command data packet, the “T” bit carries Parity information from the Host for Address Offset bytes. See Section 7.5.5.

After the Host sends the Repeated START, the “T” bit carries information from the device to the Host (“T” bit semantics are compliant with the I3C Basic Specification). The device sends Continue (‘1’) or Stop (‘0’) information to the host to inform whether it is transmitting the last byte or not. The number of bytes transmitted is predetermined by the contents of the SidebandBus Command (see Table 40 on page 79).

Table 51 — I3C Basic Read Command Packet Example (PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	SidebandBus Command = 11000000								T	
	Byte Count = 4								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
Sr	1	0	1	1	HID			R=1	A/N[4,5]	
	Byte Count = 5								T=1	
	Status								T=1	
	Rd Data[31:24]								T=1	
	Rd Data[23:16]								T=1	
	Rd Data[15:8]								T=1	
	Rd Data[7:0]								T=0[6]	Sr[7] or P

1. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
2. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The DDR5RCD01 device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Figure 118 shows the transition from Host Push-Pull Operation to Target Open Drain (ACK).
5. If target device NACKs during Repeat START for any reason, the host may re-try Repeat START again. The host may do the Repeat START as many times as it may desire. If the target device NACKs due to parity error in previous bytes from the Host, it will always NACK regardless of how many times the Host tries Repeat START. If there were no Parity errors, the RCD may eventually ACK (e.g., if delay in access of register caused the first NACK).
6. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.
7. Repeat Start or Repeat Start with 7’h7E.

Table 52 shows the I3C Basic Read Command Packet format for the case PEC is enabled. This packet includes two PEC bytes. The first PEC byte is generated by the Host and it covers from the START bit to the first PEC Byte. The RCD checks the data it receives from the host with respect to the first PEC byte. The second PEC byte is generated by the RCD and it covers from the Repeated START bit to the second PEC byte. The Host checks the data it receives from the RCD with respect to the second PEC byte.

Table 52 — I3C Basic Read Command Packet Example (Block Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	SidebandBus Command = 11000000								T	
	Byte Count = 4								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
	PEC(8)								T	
Sr	1	0	1	1	HID			R=1	A/N[4,5]	
	Byte Count = 5								T=1	
	Status								T=1	
	Rd Data[31:24]								T=1	
	Rd Data[23:16]								T=1	
	Rd Data[15:8]								T=1	
	Rd Data[7:0]								T=1	
	PEC(8)								T=0[6]	Sr[7] or P

1. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
2. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The DDR5RCD01 device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Figure 118 shows the transition from Host Push-Pull Operation to Target Open Drain (ACK).
5. If target device NACKs during Repeat START for any reason, the host may re-try Repeat START again. The host may do the Repeat START as many times as it may desire. If the target device NACKs due to parity error or PEC error in previous bytes from the Host, it will always NACK regardless of how many times the Host tries Repeat START. If there were no Parity or PEC errors, the RCD may eventually ACK (e.g., if delay in access of register caused the first NACK). The PEC calculation by the target device only includes device select code of the ACK response of the Repeat start operation.
6. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.
7. Repeat Start or Repeat Start with 7'h7E.

The table coloring identifies the portion of the packet covered by each PEC byte. In I3C Basic mode, only the block mode optimized format without redundant bytes is supported.

In I3C Basic mode, Bits [4] and [1:0] of the SidebandBus Command are ignored (see Table 40).

The host may optionally allow the DDR5RCD01 device to request IBI. For this case, the transactions to the DDR5RCD01 device begin with the I3C Basic host issuing a START condition followed by 7'h7E and W = 0. If the RCD or any other connected device has a pending IBI, it transmits its 7-bit device select code followed by R = 1. If the RCD has no pending IBI, there is no action taken by the RCD. Table 53 shows the I3C Basic Read Command Packet format from Table 52 with the optional IBI header. As shown in color coding, the IBI header is not included in the calculations to generate PEC.

Table 53 — I3C Basic Read Command Packet Example with IBI Header and No Pending Interrupt (Block Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A[1]	
Sr	1	0	1	1	HID			W = 0	A[1,2,3]	
	SidebandBus Command = 11000000								T	
	Byte Count = 4								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
	PEC(8)								T	
Sr	1	0	1	1	HID			R=1	A/N[4,5]	
	Byte Count = 5								T=1	
	Status								T=1	
	Rd Data[31:24]								T=1	
	Rd Data[23:16]								T=1	
	Rd Data[15:8]								T=1	
	Rd Data[7:0]								T=1	
	PEC(8)								T=0[6]	Sr[7] or P

1. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
3. The DDR5RCD01 device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Figure 118 shows the transition from Host Push-Pull Operation to Target Open Drain (ACK).
5. If target device NACKs during Repeat START for any reason, the host may re-try Repeat START again. The host may do the Repeat START as many times as it may desire. If the target device NACKs due to parity error or PEC error in previous bytes from the Host, it will always NACK regardless of how many times the Host tries Repeat START. If there were no Parity or PEC errors, the RCD may eventually ACK (e.g., if delay in access of register caused the first NACK). The PEC calculation by the target device only includes device select code of the ACK response of the Repeat start operation.
6. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.
7. Repeat Start or Repeat Start with 7'h7E.

7.5.8 Sideband Control Word Write Protocol

Configuration Writes are accomplished through a series of I^2C/I3C Basic Writes. As with Configuration Reads, a Write Sequence is first used to initialize the Device, Channel, Page, and Register Numbers for the configuration access. The writing of this information can be accomplished through any combination of the supported I^2C/I3C Basic write commands (Block command in I^2C and I3C Basic modes or Byte command in I^2C mode).

On SidebandBus, there is no concept of Byte Enables. Therefore, the Register Number written to the target is assumed to be aligned to the length of the Internal Command. In other words, for a Write Byte Internal Command, the Register Number specifies the Byte Address. For a Write DWord Internal Command, the two least-significant bits of the Register Number are ignored. This is different from PCI, where Byte Enables are used to indicate the byte of interest.

After all the information is set up, the SidebandBus Controller initiates one or more Writes which sets up the data to be written. The final Write (*End* bit is set) initiates an Internal Configuration Write. If an error occurred, the SidebandBus interface NACKs the last write operation just before the stop bit.

7.5.8.1 I²C Write Packet Format Definitions

Examples of Configuration Writes are shown below.

Table 54 — I²C Write Command Packet Example (Write DWord, Block Mode, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11001110								A	
	Byte Count = 8								A	
	Reserved								A	
	Dev/Channel_Num								A	
	Page_Num [7:0]								A	
	Reg_Num [7:0]								A	
	Wr Data[31:24]								A	
	Wr Data[23:16]								A	
	Wr Data[15:8]								A	
	Wr Data[7:0]								A	P

The above packet format must be supported in I²C mode for backwards compatibility with older controllers.

Table 55 — I²C Write Command Packet Example (Write DWord, Block Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11011110								A	
	Byte Count = 8								A	
	Reserved								A	
	Dev/Channel_Num								A	
	Page_Num [7:0]								A	
	Reg_Num [7:0]								A	
	Wr Data[31:24]								A	
	Wr Data[23:16]								A	
	Wr Data[15:8]								A	
	Wr Data[7:0]								A	
	PEC(8)								A	P

The above packet format must be supported in I²C mode for backwards compatibility with older controllers. The table coloring identifies the portion of the packet covered by PEC.

Table 56 — I²C Write Command Packet Example (Write Byte, Block Mode, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11000110								A	
	Byte Count = 5								A	
	Reserved								A	
	Dev/Channel_Num								A	
	Page_Num [7:0]								A	
	Reg_Num [7:0]								A	
	Wr Data[7:0]								A	P

The above packet format must be supported in I²C mode for backwards compatibility with older controllers.

Table 57 — I²C Write Command Packet Example (Write Word, Block Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 11011010								A	
	Byte Count = 6								A	
	Reserved								A	
	Dev/Channel_Num								A	
	Page_Num [7:0]								A	
	Reg_Num [7:0]								A	
	Wr Data[15:8]								A	
	Wr Data[7:0]								A	
	PEC(8)								A	P

The above packet format must be supported in I²C mode for backwards compatibility with older controllers. The table coloring identifies the portion of the packet covered by PEC.

Table 58 — I²C Write Command Packet Example (Write DWord, Byte Mode, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 10001100								A	
	Reserved								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00001100								A	
	Dev/Channel_Num								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00001100								A	
	Page_Num [7:0]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00001100								A	
	Reg_Num [7:0]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00001100								A	
	Wr Data[31:24]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00001100								A	
	Wr Data[23:16]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00001100								A	
	Wr Data[15:8]								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 01001100								A	
	Wr Data[7:0]								A	P

The above packet format must be supported in I²C mode for backwards compatibility with older controllers.

Table 59 — I²C Write Command Packet Example (Write Word, Byte Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 10011000								A	
	Reserved								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00011000								A	
	Dev/Channel_Num								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00011000								A	
	Page_Num [7:0]								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00011000								A	
	Reg_Num [7:0]								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 00011000								A	
	Wr Data[15:8]								A	
	PEC(8)								A	P
S	1	0	1	1	HID			W=0	A	
	SidebandBus Command = 01011000								A	
	Wr Data[7:0]								A	
	PEC(8)								A	P

The above packet format must be supported in I²C mode for backwards compatibility with older controllers. The table coloring identifies the portion of the packet covered by PEC.

7.5.8.2 I3C Basic Write Packet Format Definitions

During Write command data packet, the “T” bit carries Parity information from the Host. See Section 7.5.5.

The number of bytes transmitted is predetermined by the contents of the SidebandBus Command (see Table 40 on page 79).

Table 60 — I3C Basic Write Command Packet Example (Write DWord, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	SidebandBus Command = 110011xx								T	
	Byte Count = 8								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
	Wr Data[31:24]								T	
	Wr Data[23:16]								T	
	Wr Data[15:8]								T	
	Wr Data[7:0]								T	Sr[4] or P

1. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
2. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The DDR5RCD01 device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code.The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7’h7E.

In I3C Basic mode, Bits [4] and [1:0] of the SidebandBus Command are ignored (see Table 40).

Table 61 — I3C Basic Write Command Packet Example (Write DWord, Block Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	SidebandBus Command = 110111xx								T	
	Byte Count = 8								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
	Wr Data[31:24]								T	
	Wr Data[23:16]								T	
	Wr Data[15:8]								T	
	Wr Data[7:0]								T	
	PEC(8)								T	Sr[4] or P

1. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
2. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The DDR5RCD01 device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7’h7E.

The table coloring identifies the portion of the packet covered by the PEC byte. In I3C Basic mode, Bits [4] and [1:0] of the SidebandBus Command are ignored (see Table 40).

Table 62 — I3C Basic Write Command Packet Example (Write Byte, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	SidebandBus Command = 110001xx								T	
	Byte Count = 5								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
	Wr Data[7:0]								T	Sr[4] or P

1. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
2. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The DDR5RCD01 device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

In I3C Basic mode, Bits [4] and [1:0] of the SidebandBus Command are ignored (see Table 40).

Table 63 — I3C Basic Write Command Packet Example (Write Word, Block Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	1	HID			W=0	A[1,2,3]	
	SidebandBus Command = 110111xx								T	
	Byte Count = 6								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
	Wr Data[31:24]								T	
	Wr Data[7:0]								T	
	PEC(8)								T	Sr[4] or P

1. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
2. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. The DDR5RCD01 device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
4. Repeat Start or Repeat Start with 7'h7E.

The table coloring identifies the portion of the packet covered by the PEC byte. In I3C Basic mode, Bits [4] and [1:0] of the SidebandBus Command are ignored (see Table 40).

The host may optionally allow the DDR5RCD01 device to request IBI. For this case, the transactions to the DDR5RCD01 device begin with the I3C Basic host issuing a START condition followed by 7'h7E and W = 0. If the RCD or any other connected device has a pending IBI, it transmits its 7-bit device select code followed by R = 1. If the RCD has no pending IBI, there is no action taken by the RCD. Table 64 shows the same I3C Basic Write Command Packet format from Table 63 with the optional byte to allow target devices to issue an IBI request. As shown in color coding, the IBI byte is not included in the calculations to generate PEC.

Table 64 — I3C Basic Write Command Packet Example with IBI Header and No Pending Interrupt (Write Word, Block Mode, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A[1,2]	
Sr	1	0	1	1	HID			W = 0	A[2,3,4]	
	SidebandBus Command = 110111xx								T	
	Byte Count = 6								T	
	Reserved								T	
	Dev/Channel_Num								T	
	Page_Num [7:0]								T	
	Reg_Num [7:0]								T	
	Wr Data[31:24]								T	
	Wr Data[7:0]								T	
	PEC(8)								T	Sr[5] or P

1. Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (Repeat Start).
2. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. Figure 118 shows the transition from Host Push-Pull Operation to Target Open Drain (ACK) and Figure 114 depicts the transition from Target Open Drain (ACK) to Host Push-Pull Operation (1st bit, SidebandBus Command).
4. The DDR5RCD01 device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
5. Repeat Start or Repeat Start with 7'h7E.

7.5.9 In-Band Interrupts

In-Band interrupts may be generated by the RCD device if IBI is enabled by receiving a broadcast or directed ENEC CCC. In I^2C mode, in-band interrupt function is not supported. Only I3C Basic mode supports the in-band interrupt function.

7.5.9.1 Enabling/Disabling In-Band Event Interrupts

By default, all interrupt sources are disabled (i.e. set to '0'). The host may enable interrupts in the DDR5RCD01 device. Once enabled, the RCD device sends an IBI when that event occurs.

1. When any of the bits in RW28[1:0] (Parity Error or PEC Error Status Bits) get set to '1', the RCD device sets RW28[7] (In-band Interrupt Status) to 1 and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.
   a. If IBI is enabled by ENEC CCC, the RCD device sends the IBI at next available opportunity.
   b. If IBI is disabled by ENEC CCC, the device does not send the IBI regardless of the register bit status in RW28.

7.5.9.2 Mechanics of Interrupt Generation

Event interrupts may be generated by the local device if IBI is enabled by receiving a broadcast or directed ENEC CCC. When there is a pending Event In-Band Interrupt (i.e. RW28[7] = '1') and IBI is enabled, the DDR5RCD01 will request an interrupt after detecting a START bit by transmitting its 7-bit binary address (LID bits '1011' followed by HID bits) followed by R/W bit = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If the RCD detects no START bits, but the Host has been inactive (no edges seen) for t_{AVAL} period, the RCD may assert SDA Low by t_{IBI_ISSUE} time to request an interrupt. The Host will respond by toggling SCL. The RCD device transmits its 7-bit binary address (LID bits '1011' followed by HID bits) followed by R/W bit = '1'. This is shown in Figure 58.

When the RCD requests an interrupt, the host may take one of the two actions described below.

- Option 1. The Controller sends ACK on 9th bit to accept the interrupt request. At this point, if the DDR5RCD01 confirms that it has won the arbitration (i.e. the address driven in SDA matches its own Device address) the RCD transmits the IBI payload as shown in Table 65 and Table 66 for PEC disabled and PEC enabled configurations, respectively. Figure 58 depicts this case, but it only shows the first two data bits of the MDB byte (0x00) to illustrate the timing. The host then issues a STOP command. The Controller accepts the IBI payload if it sends an ACK on the 9th bit to accept the interrupt request. The Controller can terminate the IBI payload at T bit as shown in Table 65 or Table 66. If Controller stops the IBI payload after a T bit in the middle of the payload, the RCD will retain the IBI flag internally and will wait for the next opportunity to request an interrupt. If the DDR5RCD01 device successfully transmits the entire IBI payload, it then clears IBI status flag and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.
- Option 2. The Controller sends NACK on the 9th bit as shown in Figure 59 followed by a STOP command. In this case, DDR5RCD01 does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, even though the Controller sent an NACK, it does have knowledge of which device sent the IBI request.

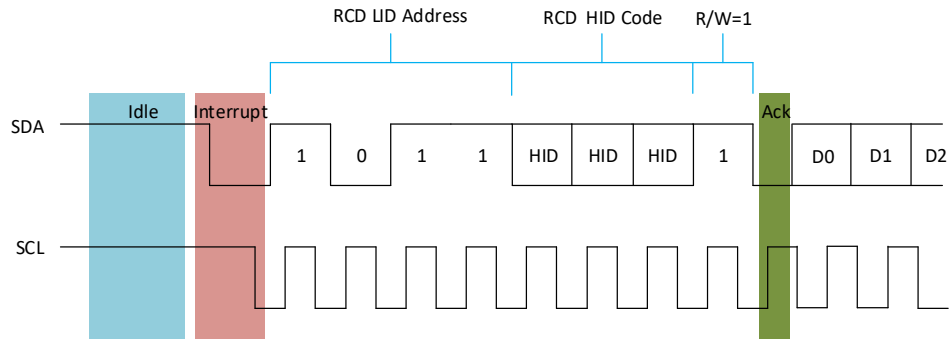


Figure 58 — RCD Interrupt Request - Controller ACK followed by RCD IBI Payload

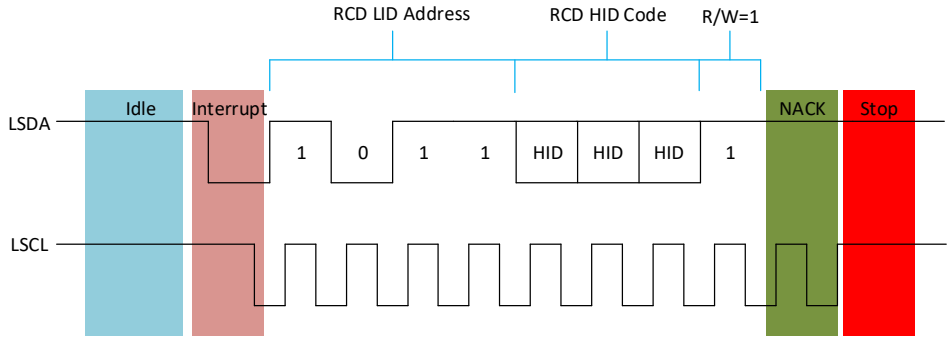


Figure 59 — RCD Interrupt Request - Controller NACK followed by STOP

Table 65 — Interrupt Response (PEC disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	Device Select Code (7)							RW(1)	Host ACK[1]	
	MDB = 0x00								T = 1	
	RW28[7:0] (last error code byte) (8)								T = 0[2]	P

1. Figure 115 illustrates the transition from Controller Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte).
2. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.

Table 66 — Interrupt Response (PEC enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	Device Select Code (7)							RW(1)	Host ACK[1]	
	MDB = 0x00								T = 1	
	RW28[7:0] (last error code byte) (8)								T = 1	
	PEC(8)								T = 0[2]	P

1. Figure 115 illustrates the transition from Controller Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB Byte).
2. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.

7.5.9.3 Interrupt Arbitration

As there are multiple devices in the I3C Basic bus, more than one device may request an interrupt when the Host I3C Basic bus is inactive for t_{AVAL} period. This makes an arbitration process necessary.

There could be up to 13 different devices, including the RCD, in the I3C Basic bus of a DDR5 DIMM application environment.

On a typical DDR5 DIMM application environment, all devices behind the SPD5 Hub device have the same 3-bit HID code. Hence, the arbitration is always won by the lowest 4-bit LID code. For example, if one local target device has LID code of '0010' and other device (RCD) has a LID code of '1011', through the arbitration process, the LID code of '0010' wins. If a higher priority device than the RCD device is serviced, the RCD must release the bus and wait for the next opportunity to request an interrupt.

It is possible for the controller to start a command transaction at the same time as the RCD requests an interrupt. When this happens, the controller participates in the arbitration process along with the other devices in the bus. During the arbitration phase, there will always be only one winning device and it could be one of the target devices (e.g. RCD) or the controller. If the controller wins during the arbitration phase, it continues with normal operation. The losing devices (e.g. RCD) must wait for next opportunity to send an interrupt. If the controller loses the arbitration, it must let go of the bus. When the controller loses during the arbitration, it must allow the winning device (e.g. RCD) to finish sending its 4-bit LID code followed by the 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the controller has the following two options:

- Option 1. The controller sends ACK to accept the interrupt and hence accepts the IBI payload from the winning device (e.g. RCD). After the IBI payload, the controller issues a STOP operation.
- Option 2. Host sends NACK followed by STOP operation.

In the cases when the controller is starting a command transaction to an RCD that is requesting an interrupt at the same time, neither the controller or the RCD know if they are a winner until the 8th bit, and controller always wins. This is because the RCD sends R/W=1 (8th bit) during the interrupt. The controller sets R/W=0 (8th bit) during the operation. As a result, the controller wins and the RCD must let go of the bus and wait for the next opportunity to send an interrupt.

7.5.9.4 Clearing Status Registers

The DDR5RCD01 device provides the device status in Table 133, "RW28: I2C & I3C Basic Error Status Global Word". When the RCD device generates an IBI condition in RW28[1:0], it sets RW28[7] to '1'. The RCD clears RW28[7] to '0' automatically when it sends a complete IBI (including payload and without interruption) the operation gets an ACK from the host. The status information in Table 133 RW28[1:0] are latched and remains valid even after target device sends payload or if the condition that triggered to generate the status is no longer present. The host must explicitly clear the status register through Clear command by writing '1' to register bits in Table 134, "RW29: I2C & I3C Basic Clear Error Status Global Word", respectively. After the Host Clear command, if the condition is still present, the device will again set the status information in Table 133, "RW28: I2C & I3C Basic Error Status Global Word" registers appropriately and will again generate interrupt at next available opportunity. When RW28[1:0] are cleared to '00' as a result of a Clear command in RW29, the IBI Status Register RW28[7] will also get cleared to '0' by the RCD hardware. IBI will get disabled when the RCD receives DISEC CCC. IBI may also get disabled when the RCD receives RSTDAA CCC since the host is expected to disable Error Interrupts by issuing DISEC CCC prior to sending the RSTDAA CCC.

7.5.10 I/O Operation

The DDR5RCD01 device supports configurable IO operation scheme of either Open Drain or Push-Pull on its Host interface (SCL and SDA).

At power on, by default, DDR5RCD01 comes up in I^2C mode of operation with Open Drain I/O for SidebandBus interface. The device shall operate in this mode until put into I3C Basic mode via SETAASA CCC.

After power on, the host may put the SidebandBus interface of the RCD device in I3C Basic mode of operation by issuing a SETAASA command.

In I3C Basic mode, the host may drive the SCL clock input of the RCD device using either Push-Pull output driver or using open-drain output driver.

To support in band interrupt, the RCD device supports dynamic switching between Open Drain mode and Push Pull mode on its SDA I/O for various events. The Table 67 below describes the different mode of operation by the RCD device for each cycle in I3C Basic mode.

Table 67 — RCD Device Dynamic I/O Operation Mode Switching; I3C Basic Mode

Operation	Open Drain Mode	Push-Pull Mode
START + Device Select Codes	Yes	No
START + 7'h7E IBI Header Byte	Yes	No
REPEAT START + Device Select Codes	No	Yes
REPEAT START + 7h'7E Header Byte	No	Yes
CCC Byte (i.e., after 7'h7E + W = 0 + ACK)	No	Yes
STOP	No	Yes
ACK/NACK Responses	Yes	No
Command, Address Operation	No	Yes
Interrupt Request by Target	Yes	No
IBI Payload	No	Yes
Write Data, T-Bit Sequence	No	Yes
Read Data, T-Bit Sequence	No	Yes
PEC, T-Bit Sequence	No	Yes

7.6 I^2C and I3C Basic Reset

To prevent a malfunctioning device from locking up the I3C Basic bus, a bus protocol reset mechanism is defined. It uses a timeout mechanism on HSCL as shown in Figure 60. All devices (including SPD5 Hub and all target devices behind the hub) on an I^2C or I3C Basic bus are RESET simultaneously. Bus reset operation works same way regardless of whether device is operating in I2C or I3C Basic mode.

To guarantee the device resets I^2C bus or I3C Basic bus, the HSCL clock input LOW time has to be greater than or equal to $t_{TIMEOUT(Max)}$.

The device does not reset I^2C bus or I3C Basic bus if the HSCL clock input LOW time is less than $t_{TIMEOUT(Min)}$.

If the HSCL clock input LOW time is between $t_{TIMEOUT(Min)}$ and $t_{TIMEOUT(Max)}$, the device does not guaranteed and it may or may not reset the I2C bus or I3C Basic bus.

When a SidebandBus Reset is detected, DDR5RCD01 devices:

1. Interface and any pending command or transaction cleared.
2. All internal register values are preserved unless noted otherwise in Item 3 below.
3. Device mode returns to power-on default conditions as follows: I3C Basic error interrupt disabled, I^2C mode enabled (RW25[5] cleared to '0'), I3C Basic parity checking enabled, I3C Basic PEC checking disabled, Parity and PEC Error Status bits (RW28[1:0]) cleared '00', and Device HID code set to '111'.
4. Device floats the SDA pin such that it gets pulled High by the external pull-up.
5. Device treats Bus Reset as STOP operation.

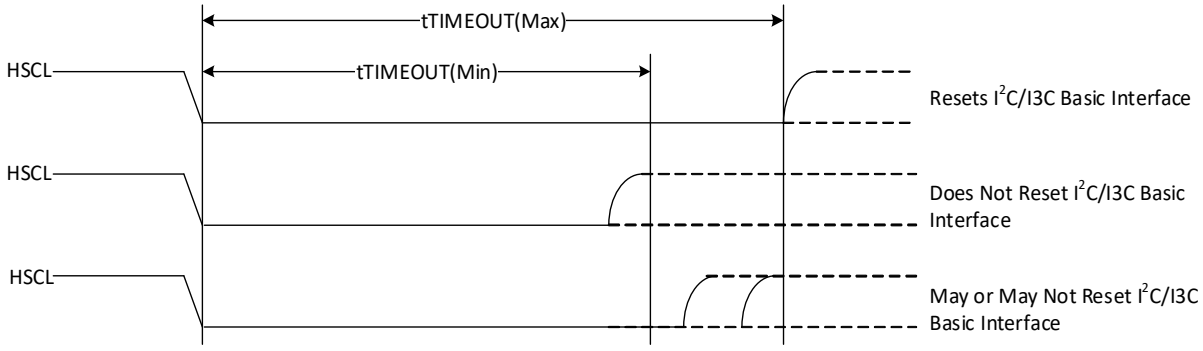


Figure 60 — I^2C or I3C Basic Reset

7.6.1 Sideband Interface and DRST_n RCD Reset Events

To maintain consistent configuration state with other devices in the DDR5 module, configuration settings and status registers pertaining to the Sideband Interface in the DDR5RCD01 device will not be affected by DRST_n Reset events. In particular:

1. I^2C or I3C Basic protocol selected before DRST_n event will continue in operation after DRST_n Reset event. RW25[5] shall be sticky.
2. I3C Basic error interrupt remains unchanged. IBI remains enabled or disabled after DRST_n Reset event.
3. I3C Basic parity checking and I3C Basic PEC checking remain unchanged after DRST_n Reset event.
4. Parity and PEC Error Status information retained after DRST_n Reset event. RW28 shall be sticky.
5. Device HID code configured before DRST_n event will remain unchanged after DRST_n Reset event.
6. When DRST_n is asserted, the DDR5RCD01 device is required to detect Timeout Reset and to execute I2C/I3C Basic Common Command Code (CCC) packets (excluding DEVCTRL with RegMod = 1).

7.7 I^2C Bus Clear

The DDR5RCD01 device supports the following described Bus Clear feature in I^2C mode only. Any attempt by host to perform I^2C Bus clear on a target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the target device is in the middle of outputting data for read operation. For these types of events, the SDA data line may appear as stuck LOW as the device is expecting to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck LOW on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

7.8 I²C Bus Error Handling

The I²C Bus target interface handles two types of errors: internal and PEC. These errors manifest as a Not-Acknowledge (NACK) for the read command (End bit is set). If an internal error occurs during a configuration write, the final write command receives a NACK just before the stop bit. If the controller receives a NACK, the entire configuration transaction should be reattempted.

If the controller supports packet error checking (PEC) and the PEC_en bit in the command is set, then the PEC byte is checked in the target interface. If the check indicates a failure, then the target will NACK the PEC packet.

7.9 Error Handling in I3C Basic

There are two types of error checking done by the DDR5RCD01 device. I3C Basic Parity error checking and Packet Error checking. By default, the parity error checking is always enabled (in I3C Basic mode) and packet error checking is disabled. The host may enable the packet error checking at any time. The parity error is calculated for each byte. The packet error is computed for the entire packet. The host sends parity error information in “T” bit.

I3C Basic defines TE0, TE1, TE2, TE3, TE4, TE5, TE6 & CE0, CE1, CE2 errors. Only TE1 and TE2 errors are supported by the DDR5RCD01 device. All other errors are not supported and not applicable. The DDR5RCD01 device will NACK unsupported CCCs.

7.9.1 Write Command Data Packet Error Handling - PEC Is Disabled

When I3C Basic mode is enabled, the DDR5RCD01 device checks for the parity error for each byte that it receives from the host in the Write Command Data Packet as shown in Table 60 through Table 62. The following description applies to I3C Basic mode only.

If no parity error detected in Write command:

- The DDR5RCD01 device executes the command.

If parity error in Write command:

- The DDR5RCD01 device discards the byte that had parity error.
- The DDR5RCD01 device discards all sub-sequent bytes in that packet until STOP operation. The DDR5RCD01 device may or may not check the parity for all sub-sequent bytes in that packet.
- Note that if the host write command was for two-byte write operation and if the parity error occurred in second byte of data, the RCD may or may not execute the first byte write operation but the second byte write operation is discarded.
- The DDR5RCD01 device sets registers RW28[0] and RW28[7]to ‘1’; sets P_Err to ‘1’ and Pending Interrupt Bits [3:0] to ‘0001’ in GETSTATUS CCC response; and waits for the next opportunity to send in band interrupt (if IBI is enabled by ENEC CCC).

7.9.2 Read Command Data Packet Error Handling - PEC Is Disabled

For Read Command Data Packet as shown in Table 51, the device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host.

The DDR5RCD01 device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the data bytes sent by the RCD. The device sends Continue (‘1’) or Stop (‘0’) information during T bit when device is sending the read data.

If no parity error detected in Read command:

- The DDR5RCD01 sends ACK back to the host when Host perform Repeat START operation.
- The DDR5RCD01 device executes the command and sends the data back to the host as shown in Table 51.

If parity error in Read command:

- The DDR5RCD01 device discards the byte that had parity error.
- The DDR5RCD01 device discards all sub-sequent bytes in that packet until STOP operation. The DDR5RCD01 device may or may not check the parity for all sub-sequent bytes in that packet.
- The DDR5RCD01 sends NACK back to the host when the host applies a Repeat START. This is shown in the RED color cell in Table 51. The NACK represents either a parity error in one of the six bytes or that DDR5RCD01 is not able to start the read operation. The host may re-try Repeat START again. The Host may do the Repeat START as many times as it may desire. If the RCD NACKs due to parity error in previous bytes from the host, it will always NACK regardless of how many times Host tries Repeat START.
- The DDR5RCD01 does not send Read data back to the host.
- The DDR5RCD01 device sets registers RW28[0] and RW28[7] to '1'; sets P_Err to '1' and Pending Interrupt Bits [3:0] to '0001' in GETSTATUS CCC response; and waits for the next opportunity to send in band interrupt (if IBI is enabled by ENEC CCC).

7.9.3 Write Command Data Packet Error Handling - PEC Is Enabled

When I3C Basic mode is enabled, the DDR5RCD01 device checks for the parity error for each byte and each packet that it receives from the host in the Write Command Data Packet as shown in Table 63. The following description applies to I3C Basic mode only.

If no parity error in Write command:

- The DDR5RCD01 device waits for the entire packet. If no error in packet, the DDR5RCD01 device executes the command. If there is an error in the packet, the DDR5RCD01 device discards the entire packet and does not execute that packet and waits for STOP, sets registers RW28[1] and RW28[7] to '1'; sets PEC_Err to '1' and Pending Interrupt Bits [3:0] to '0001' in GETSTATUS CCC response; and waits for the next opportunity to send in band interrupt (if IBI is enabled by ENEC CCC).

If parity error in Write command:

- The DDR5RCD01 device discards that byte and the entire packet until STOP operation.
- The DDR5RCD01 device sets registers RW28[0] and RW28[7] to '1'; sets P_Err to '1' and Pending Interrupt Bits [3:0] to '0001' in GETSTATUS CCC response; and waits for the next opportunity to send in band interrupt (if IBI is enabled by ENEC CCC).
- The DDR5RCD01 may or may not check the error for the packet. If the device checks for the packet error, likely it will detect an error in the packet and the device may also set the RW28[1] register and PEC_Err in GETSTATUS CCC response to '1' as well.

7.9.4 Read Command Data Packet Error Handling - PEC Is Enabled

For Read Command Data Packet as shown in Table 52, the DDR5RCD01 device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host (prior to Repeat Start).

The RCD does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes shown in Table 52. The device sends Continue ('1') or Stop ('0') information during "T" bit when the device is sending the Read data.

The RCD device checks for the PEC error for in a packet that it receives from the host from START condition to Repeat START condition (From first Device Select code followed by the Address Offset).

The device computes the packet error code for the entire packet starting with Repeat START (Device Select code and the data that device transmits back to the Host).

If no parity error and no PEC error in Read command:

- The DDR5RCD01 device sends ACK back to the host in response to Repeat START event.
- The DDR5RCD01 device executes the command and sends the Read data back to the host as shown in Table 52.
- The RCD computes PEC from Repeat START condition until STOP condition (Device Select code followed by the Data) the bytes shown in Table 52.

If parity error or PEC error in Read command:

- The DDR5RCD01 device discards the byte that had a parity error.
- The DDR5RCD01 device discards second byte in that packet if a parity error occurred in first byte. The DDR5RCD01 device may or may not check parity for the second byte in that packet.
- The DDR5RCD01 device sends NACK back to the host in response to Repeat START event. This is shown in the RED color cell in Table 52. The NACK represents either parity error in one of the seven bytes or that DDR5RCD01 is not able to start the read operation. The host may re-try Repeat START again. The Host may do the Repeat START as many times as it may desire. If the RCD NACKs due to parity error or PEC error in previous bytes from the host, it will always NACK regardless of how many times Host tries Repeat START.
- The device does not send Read data back to the host and instead expects the host to perform STOP operation.
- The DDR5RCD01 device sets RW28[0] register and P_Err bit in GETSTATUS CCC response to '1' for parity error and RW28[1] register and PEC_Err bit in GETSTATUS CCC response to '1' for PEC error. Further, the RCD sets RW28[7] register to '1' and Pending Interrupt Bits [3:0] to '0001' in GETSTATUS CCC response and waits for the next opportunity to send in band interrupt (if IBI is enabled by ENEC CCC).

7.9.5 CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled the same way as described for normal Read/Write operations.

7.10 Supported I3C Basic Common Command Codes (CCCs)

Table 68 lists all the I3C Basic Common Command Codes that must be supported by the DDR5RCD01 device. The RCD will NACK unsupported CCCs.

The DDR5RCD01 device requires STOP operation in between when switching from CCC operation to private device specific Write or Read operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read. Similarly, any device specific Write or Read operation must be followed by STOP operation before continuing to any CCC operation. The DDR5RCD01 device also requires STOP operation from any Direct CCC to Broadcast CCC.

The DDR5RCD01 device does allow Repeat Start operation between any Direct CCC to any other Direct CCC or between any Broadcast CCC to any other Broadcast CCC or between any private Write or Read operation to any other private Write or Read operation.

Table 68 — Supported I3C Basic Common Command Codes (CCCs)

Command	Mode	Code	Description	Note
ENEC	Broadcast	0x00	Enable Events Command	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable Events Command	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the Device in I^2C Mode (a.k.a. Reset Dynamic Address Assignment Command)	1
SETAASA	Broadcast	0x29	Put the Device in I3C Basic Mode (a.k.a. Set All Addresses to Static Address Command)	
GETSTATUS	Direct	0x90	Get Device Status Command	
DEVCAP	Direct	0xE0	Get Device Capability Command	2
SETHID	Broadcast	0x61	Update HID Code	2
DEVCTRL	Broadcast	0x62	Configure SPD Hub and All Devices Behind Hub	2

1. It is illegal for the host to send Direct RSTDAA CCC Code 0x86.
2. JEDEC specific CCC.

7.10.1 Enable/Disable Events Command (ENEC/DISEC) Operation

Refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of the ENEC/DISEC Command. This command is only supported by the RCD when it is operating in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. If host issues this CCC while the RCD is in I^2C mode, the response is undefined.

The only event types support by the DDR5RCD01 for ENEC/DISEC Command are **Target Interrupt Requests**. All other event types are not supported and ignored.

When ENEC/DISEC Command is received, it takes effect at the next START operation (i.e. after STOP condition).If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 69 — ENEC/DISEC CCC (I3C Basic, Broadcast, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x00 (Broadcast ENEC) or 0x01 (Broadcast DISEC)								T	
	0	0	0	0	0[2]	0	0[2]	ENINT/ DISINT	T	Sr[3] or P

1. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. DDR5RCD01 ignores HJ (Hot Join) and MR (Control Request) bits.
3. Repeat Start or Repeat Start with 7'h7E.

Table 70 — ENEC/DISEC CCC (I3C Basic, Broadcast, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x00 (Broadcast ENEC) or 0x01 (Broadcast DISEC)								T	
	0	0	0	0	0[2]	0	0[2]	ENINT/ DISINT	T	
	PEC(8)								T	Sr[3] or P

1. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. DDR5RCD01 ignores HJ (Hot Join) and MR (Control Request) bits.
3. Repeat Start or Repeat Start with 7'h7E.

Table 71 — ENEC/DISEC CCC (I3C Basic, Direct, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x80 (Direct ENEC) or 0x81 (Direct DISEC)								T	
Sr	1	0	1	1	HID			W = 0	A[1,2]	
	0	0	0	0	0[3]	0	0[3]	ENINT/ DISINT	T	Sr[4] or P

1.The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2.The DDR5RCD01 device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
3.DDR5RCD01 ignores HJ (Hot Join) and MR (Control Request) bits.
4.Repeat Start or Repeat Start with 7'h7E.

Table 72 — ENEC/DISEC CCC (I3C Basic, Direct, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x80 (Direct ENEC) or 0x81 (Direct DISEC)								T	
	PEC(8)								T	
Sr	1	0	1	1	HID			W = 0	A[1,2]	
	0	0	0	0	0[3]	0	0[3]	ENINT/ DISINT	T	
	PEC(8)								T	Sr[4] or P

1. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. The DDR5RCD01 device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The RCD device ignores the entire packet until STOP or next Repeat Start operation.
3. DDR5RCD01 ignores HJ (Hot Join) and MR (Control Request) bits.
4. Repeat Start or Repeat Start with 7'h7E.

7.10.2 Reset Dynamic Address Assignment Command (RSTDAA) Operation

Refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of the RSTDAA Command. This command is only supported by the RCD when it is operating in I3C Basic mode. In I^2C mode, this CCC is ignored (i.e., the RSTDAA command is not executed internally and any bytes arriving after the 0x86 RSTDAA Direct CCC are not acknowledged and they are ignored for all purposes, including parity checking, until the next STOP operation or Repeat START with 7'h7E is received).

The Host puts the DDR5RCD01 device in I^2C mode by issuing RSTDAA CCC. When RSTDAA CCC is registered by the device, the DDR5RCD01 updates RW25[5] to '0' and it takes effect at the next START operation (i.e. after STOP condition). Moreover, the RCD is allowed to disable IBI, disable PEC, and enable I3C Basic Parity Checking functions. The host is expected to send DISEC and DEVCTRL commands to disable IBI, disable PEC, and enable Parity Checking prior to issuing the RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 73 — RSTDAA CCC (I3C Basic, Broadcast, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x06 (Broadcast RSTDAA)								T	Sr[2] or P

1. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

Table 74 — RSTDAA CCC (I3C Basic, Broadcast, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x06 (Broadcast RSTDAA)								T	
	PEC(8)								T	Sr[2] or P

1. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Repeat Start or Repeat Start with 7'h7E.

7.10.3 Set All Addresses to Static Address Command (SETAASA) Operation

Refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of the SETAASA Command. This command is supported by the RCD only when it is operating in I^2C mode. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error and to avoid subsequent undesired effects, the host shall limit the maximum speed of operation for this CCC to 1 MHz. In I3C Basic mode, this CCC is ignored (i.e., the SETAASA command is not executed internally).

Upon receiving SETAASA Command, the DDR5RCD01 device will update the setting in RW25[5] to '1' and it takes effect at the next START operation (i.e. after STOP condition).

As the device is in I2C mode when SETAASA CCC is issued, SETAASA CCC does not support PEC function.

Table 75 — SETAASA CCC (I^2C, Broadcast)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A	
	0x29 (Broadcast SETAASA)								T	P

7.10.4 Get Device Status Command (GETSTATUS) Operation

Refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of the GETSTATUS Command. This command is only supported by the RCD when it is operating in I3C Basic mode. In I^2C mode, this CCC is ignored (i.e., the GETSTATUS command is not executed internally and GETSTATUS Direct CCC are not acknowledged and host must do STOP operation).

Table 76 shows the format of the MSb and LSb sent by the DDR5RCD01 device in response to a GETSTATUS command. When the DDR5RCD01 device completes a GETSTATUS CCC operation, it does not modify any of the status bits in Table 133, "RW28: I2C & I3C Basic Error Status Global Word".

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 76 — GETSTATUS MSb-LSb Format

Bits	Field	Description
15	PEC Error	DDR5RCD01 returns the value of RW28[1]. This bit is cleared when Host issues Clear Command to RW29[1]. 0 = No Error 1 = PEC Error Occurred
14:8	Vendor Reserved	Hard coded to all-zeros in DDR5RCD01.
7:6	Activity Mode	Hard coded to all-zeros in DDR5RCD01.
5	Protocol Error	DDR5RCD01 returns the value of RW28[0]. This bit is cleared when Host issues Clear Command to RW29[0]. 0 = No Error 1 = Protocol Error; Parity Error Occurred
4	Reserved	Hard coded to zero in DDR5RCD01.
3:0	Pending Interrupt	DDR5RCD01 returns the value of RW28[7] in Bit 0. Bit 0 is cleared when Host issues a Clear Command that causes the IBI Status register RW28[7] to get cleared. 0000 = No Pending Interrupt 0001 = Pending Interrupt All other encodings are reserved

Table 77 — GETSTATUS CCC (I3C Basic, Direct, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0x90 (Direct GETSTATUS)								T	
Sr	1	0	1	1	HID			R = 1	A[1]	
	PEC_Err	0	0	0	0	0	0	0	T = 1	
	0	0	Prot_Err	0	Pending Interrupt				T = 0[2]	Sr[3] or P

1. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.
3. Repeat Start or Repeat Start with 7'h7E.

Table 78 — GETSTATUS CCC (I3C Basic, Direct, PEC Enabled)[1]

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[2]	
	0x90 (Direct GETSTATUS)								T	
	PEC(8)								T	
Sr	1	0	1	1	HID			R = 1	A[2]	
	PEC_Err	0	0	0	0	0	0	0	T = 1	
	0	0	Prot_Err	0	Pending Interrupt				T = 1	
	PEC(8)								T = 0[3]	Sr[4] or P

1. GETSTATUS CCC with PEC check is only supported in I3C Basic mode.
2. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.
4. Repeat Start or Repeat Start with 7'h7E.

When the device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, Prot_Err, and Pending Interrupt Bits [3:0] do not automatically get cleared. The host must explicitly clear the appropriate status register through Clear command b writing '1' to corresponding register or by issuing Global Clear command. Once the DDR5RCD01 device clears the appropriate status register, only then PEC_Err, Prot_Err, and Pending Interrupt Bits [3:0] get cleared.

After the host issues a Clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001'.

7.10.5 Get Device Capability Command (DEVCAP) Operation

Refer to JESD403-1 for details on the encoding and usage of the DEVCAP Command. This command is only supported by the RCD when it is operating in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. If host issues this CCC while the RCD is in I^2C mode, the response is undefined.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 79 and Table 79 show the format of the DEVCAP CCC Packet.

Table 79 — DEVCAP CCC (I3C Basic, Direct, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0xE0 (Direct DEVCAP)								T	
Sr	1	0	1	1	HID			R = 1	A[1]	
	MSB (each bit defines capability); 1 = support; 0 = no support								T = 1	
	LSB (each bit defines capability); 1 = support; 0 = no support								T = 0[2]	Sr[3] or P

1. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.
3. Repeat Start or Repeat Start with 7'h7E.

Table 80 — DEVCAP CCC (I3C Basic, Direct, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0xE0 (Direct DEVCAP)								T	
	PEC(8)								T	
Sr	1	0	1	1	HID			R = 1	A[1]	
	MSB (each bit defines capability); 1 = support; 0 = no support								T = 1	
	LSB (each bit defines capability); 1 = support; 0 = no support								T = 1	
	PEC(8)								T = 0[2]	Sr[3] or P

1. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. Figure 116 shows how the RCD ends the operation followed by the Controller STOP bit.
3. Repeat Start or Repeat Start with 7'h7E.

Table 81 shows the format of the MSb and LSb sent by the DDR5RCD01 device in response to a DEVCAP command.

Table 81 — DEVCAP MSb-LSb Format

Bits	Field	Description
MSB[7]	Reserved	Hard coded to zero in DDR5RCD01.
MSB[6]	Reserved	Hard coded to zero in DDR5RCD01.
MSB[5]	Reserved	Hard coded to zero in DDR5RCD01.
MSB[4]	Reserved	Hard coded to zero in DDR5RCD01.
MSB[3]	Reserved	Hard coded to zero in DDR5RCD01.
MSB[2]	Timer Based Reset	Hard coded to one (yes support) in DDR5RCD01.
MSB[1:0]	Reserved	Hard coded to zero in DDR5RCD01.
LSB[7:0]	Reserved	Hard coded to zero in DDR5RCD01.

7.10.6 Set HID Command (SETHID) Operation

Refer to JESD403-1 for details on the encoding and usage of the SETHID Command. This command is supported by the RCD only when it is operating in I^2C mode. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error and to avoid subsequent undesired effects, the host shall limit the maximum speed of operation for this CCC to 1 MHz. In I3C Basic mode, it is illegal for host to issue this CCC. If host issues this CCC while the RCD is in I3C Basic mode, the response is undefined.

Upon receiving SETHID Command, the DDR5RCD01 device will update the HID code with the HID[2:0] bits it received in the SETHID command packet, and it takes effect at the next START operation (i.e. after STOP condition).

As the device is in I2C mode when SETHID CCC is issued, SETHID CCC does not support PEC function.

Table 82 — SETHID CCC (I^2C, Broadcast)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W = 0	A	
	0x61 (Broadcast SETHID)								T	
	0	0	0	0	HID[2:0]			0	T	P

7.10.7 Configure SPD Hub and All Devices Behind Hub Command (DEVCTRL) Operation

Refer to JESD403-1 for details on the encoding and usage of the DEVCTRL Command. This command is supported by the DDR5RCD01 device in both I^2C and in I3C Basic modes. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error and to avoid subsequent undesired effects, the host shall limit the maximum speed of operation for this CCC to 1 MHz.

On a typical I^2C or I3C Basic bus there can be up to 120 devices. For certain operation such as selecting the I3C Basic mode of operation or to enable or disable functions that are common to all devices such as Packet Error Check, the host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I3C Basic mode of operation. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error and to avoid subsequent undesired implication, the host shall limit the maximum speed of operation for this CCC to 1 MHz. Table 83 to Table 84 show examples of DEVCTRL CCC command packets.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

The host must pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (i.e. RegMod = '1'), the host must still follow any device specific register restriction. For instance, if any device specific register requires STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

Table 83 — DEVCTRL Command Operation (I^2C or I3C Basic, Broadcast, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[1]	
	0	1	1	0	0	0	1	0	T	
	AddrMask[2:0]			StartOffset[1:0]		0	0	RegMod	T	
	DevID[6:0]							0	T[2]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr[3] or P

1. The DDR5RCD01 NACKs if there was a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
2. As an exception, the DDR5RCD01 device will check parity in this byte even when the 7-bit Device ID code issued by the host does not match with its own device code. If the Device ID code is unmatched, the RCD will not check for Parity errors in subsequent bytes and it will ignore the entire packet until STOP or Repeat START operation.
3. Repeat Start or Repeat Start with 7'h7E.

Table 84 — DEVCTRL Command Operation (I3C Basic. Broadcast, PEC Enabled)[1]

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A[2]	
	0	1	1	0	0	0	1	0	T	
	AddrMask[2:0]			StartOffset[1:0]		PEC_BL		RegMod	T	
	DevID[6:0]							0	T[3]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC(8)								T	Sr[4] or P

1. DEVCTRL CCC with PEC check is only supported in I3C Basic mode.
2. The DDR5RCD01 NACKs if there was a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
3. As an exception, the DDR5RCD01 device will check parity in this byte even when the 7-bit Device ID code issued by the host does not match with its own device code. If the Device ID code is unmatched, the RCD will not check for Parity or PEC errors in subsequent bytes and it will ignore the entire packet until STOP or Repeat START operation.
4. Repeat Start or Repeat Start with 7'h7E.

Table 85 — DEVCTRL Command Definition

Parameter	Definition
AddrMask[2:0]	Broadcast, Uni-cast or Multi-cast Command Selection 000 = Uni-Cast Command; Target device responds if DevID[6:0] field matches with target device's own 7-bit address (4-bit LID + 3-bit HID) 011 = Multi-Cast Command; Target and possible other device responds if DevID[6:3] field matches with target's own 4-bit LID address 111 = Broadcast Command; All devices responds to this command All other encodings are reserved
StartOffset[1:0]	Only applicable if RegMod = '0' Identifies the starting Byte. (Byte 0 or Byte 1 or Byte 2 or Byte 3) in DEVCTRL command data packet. Host can start any Byte and can have continuous access to next byte until STOP operation. If Byte 3 is reached, the host is responsible for applying STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC_BL[1:0]	Only applicable if RegMod = '0' Identifies the burst length just for the DEVCTRL command data packet. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL command is going to be used for device specific offset register or general registers as identified in Byte 0 to Byte 3. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e. StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e. StartOffset[1:0] & PECBL[1:0] is a don't care and does not apply). The host shall not use RegMod = '1' with Broadcast Command for DDR5 DIMM because there are different types of devices on the I3C Basic bus. The DDR5RCD01 device is not required to support the RegMod = '1' option when the interface is running in I^2C mode.[1]
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL command data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.

1.This is a deviation from the JESD403-1 Specification for JEDEC Module SidebandBus.

Table 86 — DEVCTRL Command Definition

Byte	Bit	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable[1]	
	[6]	Parity Disable	0 = Enable 1 = Disable	
	[5]	RFU	RFU	
	[4:2]	RFU	RFU	
	[1]	RSVD - Reserved	X (0 or 1) = No action	This bit is used by other devices and must be ignored by the RCD.
	[0]	RFU	RFU	
Byte 1	[7:5]	RFU	RFU	
	[4]	RFU	RFU	
	[3]	Global and IBI Clear	0 = No action 1 = Clear All Event and pending IBI[1,2]	RW28[1:0] are updated
	[2]	RFU	RFU	RFU
	[1:0]	RFU	RFU	
Byte2	[7:0]	RFU	RFU	
Byte 3	[7:4]	RFU	RFU	
	[3:1]	RFU	RFU	
	[0]	RFU	RFU	

1. Global Clear and PEC Enable only applicable after device is configured in I3C Basic mode.
2. After DDR5RCD01 clears all events, the RCD can still have certain registers set to '1' if the event is still present in which case, the RCD will generate an IBI again at the next opportunity.

7.10.7.1 DEVCTRL Command Examples

The following DEVCTRL Command configures frequency information to 4560 MT/s (RW05 = 04h and RW06 = 0Ch) in all RCD devices simultaneously.

Table 87 — DEVCTRL Command Example (I3C Basic, Broadcast, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0	1	1	0	0	0	1	0	T	
	AddrMask[2:0] = '011' (Mcast)			StartOffset = xx		PEC_BL = xx		RegMod=1	T	
	DevID[6:0] = 1011_xxx (Match LID code for RCD Device)							0	T	
	SidebandBus Command = 11xx_11xx (Double Word Write)[1]								T	
	Byte Count = 08h								T	
	Reserved								T	
	Dev/Channel_Num = 00h (Channel A)								T	
	Page_Num [7:0] = 00h (Ignored for RW05 & RW06)								T	
	Reg_Num [7:0] = 04h (points at RW04)								T	
	Wr Data[31:24] = 00h (RW07 default)								T	
	Wr Data[23:16] = 0Ch (fbin - 240 MT/s)								T	
	Wr Data[15:8] = 04 h (4400 MT/s to 4800 MT/s)								T	
	Wr Data[7:0] = 00h (Command Space CMD 0 - NOP)								T	
	PEC(8)								T	P

1. In DEVCTRL, Bits [3:2] of SidebandBus Command can be set to 01 (Write Byte), 10 (Write Word), or 11 (Write DWord). In other words, all Write Internal Commands are supported in the DEVCTRL CCC packet.

8 Control Words

The DDR5RCD01 device features a set of 8-bit control words, which allow the optimization of the device properties for different raw card designs. DDR5RCD01 control word writes appear as MRW commands but with the CW bit HIGH. DRAMs will ignore MRW commands with the CW bit set HIGH. Each Register Word (RW) write generates an MRW command to the DRAMs behind the register, unless there is a parity error when parity checking is enabled or the DRAM interface Forward All Commands feature is disabled in RW01[1]. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for RW05 and RW06, the controller needs to wait t_{MRD} after the last control word access before further access to the DRAM can take place. For any changes to the clock timing (RW05 and RW06) this settling may take up to t_{STAB02} time. All chip select inputs for the accessed channel, DCS[1:0]_n, must be kept HIGH during that time.

The control words are independent between the two channels. Each channel has a separate control word space that is accessible via the input chip selects for that channel. Some control words are only accessible through Channel A. These are control words that pertain to the clock frequency, etc., that are global in nature. Control word writes may occur independently on the two channels, so it is possible that both channels will be processing control word accesses at the same time, possibly offset by any number of DCLKs from each other. The DDR5RCD01 must support control word access for any of the DDR5RCD01 specified frequency ranges.

RCD Control Word attributes can be:

- Reserved[1]
- Read Only
- Write Only
- RD/WR
- One Time Programmable
- Sticky - Cleared by power cycle not Reset

The control word space is divided as follows:

Table 88 — Control Word Addressing

CW bit	MRA7	Description
0	x	DRAM MR space.
1	0	RCD CW space. 128 registers decoded via MRA[6:0]
1	1	Data Buffer CW space. 128 registers decoded via MRA[6:0]

Within the RCD control word space, 96 registers are accessed directly, while 32 registers are addressed through an 8-bit paging system, providing 8192 registers. RW5F is the page register while addresses 60-7F are used to access the

1. Reserved control bits may not be physically implemented and they shall be written to zero to ensure forward compatibility.

registers within each page. Pages 00-7F are for JEDEC use while pages 80-FF are vendor specific.

Table 89 — RCD and DB Control Word Spaces

MRA[7:0]	Location	Page Pointer RW[1]	Page Pointer Value	Definition	Size (bytes)	Description
00h to 5Fh	RCD	RW5F	X	JEDEC	96	96 directly addressed registers
60h to 7Fh	RCD	RW5F	00h-7Fh	JEDEC	4096	32 paged registers
60h to 7Fh	RCD	RW5F	80h-FFh	Vendor	4096	32 paged registers
80h to DFh	Data Buffer	RWDF	X	JEDEC	96	96 directly addressed registers
E0h to FFh	Data Buffer	RWDF	00h-7Fh	JEDEC	4096	32 paged registers
E0h to FFh	Data Buffer	RWDF	80h-FFh	Vendor	4096	32 paged registers

1. RW5F is the Page Pointer located in the DDR5 Register and RWDF is the Page Pointer located in the DDR5 Data Buffer

All registers are 8-bit. If enabled in RCD, all MRW accesses are sent across the BCOM bus to the data buffers, allowing the data buffers to snoop values sent to the DRAM or RCD.

Control Word Naming Convention:

PG[x]RWyy[z:z]
x = Page
yy = RW Number
z = OP

8.1 Reading Control Words

Control words are read by passing the data onto the DRAM devices, where they are read by the host controller by doing an MRR (Mode Register Read). The sequence is as follows:

Table 90 — Control Word Read Sequence

Function	Cmd	CW bit	Address (hex)	Description
Select which control word to read	MRW	1	5Eh	MRW command to RCD control word RW5E which points to which RCD control word will be read[1].
Transfer the RCD control word content to the DRAMs	MRW	0	3Fh	MRW command to the DRAM MR63 (3Fh). When the RCD detects address MR63 in an MRW command in the 1st UI, it will substitute the data from the control word pointed to by RW5E onto CA[7:0] of the 2nd UI (replacing the data from the host)[2]. This data is written into the scratch pad register MR63 of the DRAM.
Read the data into the host controller	MRR	0	3Fh	MRR command to the DRAM MR63 to read the data from the DRAM.

1. If the RCD Control Word to be read is in the paged space, then the host must set the page register properly before issuing the MRW write to the DRAM scratch-pad register.
2. When the MR63 command is issued only CA[7:0] get replaced by the control word data and all other bits are forwarded to the DRAM.

Note: It is required that the DRAM has an 8-bit scratch-pad register at location MR63. MR63 is read and written in the same manner as all other mode registers. The RCD will check MRA[7:0] when determining whether to replace the host data with the selected RW register content.

8.2 Control Word Decoding

The control words are programmed by the host controller using the MRW command function. The DDR5RCD01 forwards the MRW command to the DRAM. The DRAM is required to ignore the MRW Command when CW = '1'.

Table 91 — DDR MRW Command to RCD[1]

MRW	DCS_n	CA Pins						
		CA0	CA1	CA2	CA3	CA4	CA5	CA6
UI1	L	H	L	H	L	L	MRA0	MRA1
UI2	H	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V
UI3	H	OP0	OP1	OP2	OP3	OP4	OP5	OP6
UI4	H	OP7	V	V	CW	V	V	V

1. V means H or L (a defined logic level).

The power-on reset default state of all control words is '0' unless specified otherwise. Every time the device is reset, its default state is restored with the exception of sticky RWs. Cycling the device in and out of low-power mode will not alter the control word settings.

8.3 Control Word Decoding

Table 92 — Control Word Decoding

Register Control Word	MRA [7:0] HEX[1]	Meaning	Global Only (Requires Channel A Access)[2]
RW00	0x00	Global Features	Yes
RW01	0x01	Parity, CMD Blocking, and Alert	Yes
RW02	0x02	Host Interface Training Mode	Yes
RW03	0x03	DRAM & DB Interface Training Mode	Yes
RW04	0x04	Command Space	Yes
RW05	0x05	DIMM Operating Speed	Yes
RW06	0x06	Fine Granularity DIMM Operating Speed	Yes
RW07	0x07	Validation Pass-Through and Lockout Protection	Yes
RW08	0x08	Clock Driver Enable	No
RW09	0x09	Output Address and Control Enable	No
RW0A	0x0A	QCK Signals Driver Characteristics	No
RW0B	0x0B	Reserved	No
RW0C	0x0C	QCA and QxCS_n Signals Characteristics	No
RW0D	0x0D	Data Buffer Interface Driver Characteristics	No
RW0E	0x0E	QCK, QCA and QCS Output Slew Rate	No
RW0F	0x0F	BCK, BCOM and BCS Output Slew Rate	No
RW10	0x10	IBT	Yes
RW11	0x11	Command Latency Adder	No
RW12	0x12	QACK Output Delay	No
RW13	0x13	QBCK Output Delay	No
RW14	0x14	QCCK Output Delay Control	No
RW15	0x15	QDCK Output Delay Control	No
RW16	0x16	Reserved	No
RW17	0x17	QACS0 Output Delay	No
RW18	0x18	QACS1 Output Delay	No
RW19	0x19	QBCS0 Output Delay	No
RW1A	0x1A	QBCS1 Output Delay	No
RW1B	0x1B	QACA Output Delay	No
RW1C	0x1C	QBCA Output Delay	No
RW1D	0x1D	BCS and BCOM Output Delay	No
RW1E	0x1E	BCK Output Delay	No
RW1F	0x1F	Reserved	No
RW20	0x20	Error Log Register	No
RW21	0x21	Error Log Register	No
RW22	0x22	Error Log Register	No
RW23	0x23	Error Log Register	No
RW24	0x24	Error Log Register	No
RW25	0x25	SidebandBus	Yes
RW26	0x26	Loopback	Yes
RW27	0x27	Loop-back I/O	Yes
RW28	0x28	I^2C & I3C Basic Error Status	Yes
RW29	0x29	I^2C & I3C Basic Clear Error Status	Yes
RW2A	0x2A	Vendor Specific	Yes
RW2B~RW2F	0x28~0x2F	Reserved	No
RW30	0x30	DFE_Vref Range Limit	Yes
RW31	0x31	DFE Configuration	No
RW32	0x32	DPAR and DCA[6:0] DFE Training Mode	No
RW33	0x33	Additional Filtering for DFE Training Mode	No
RW34	0x34	LFSR DFE Training Mode	No
RW35	0x35	LFSR State for DFE Training Mode	No
RW36	0x36	DFETM Inner Loop Start Value	No
RW37	0x37	DFETM Outer Loop Start Value	No
RW38	0x38	DFETM Inner Loop Current Value	No
RW39	0x39	DFETM Outer Loop Current Value	No
RW3A	0x3A	DFETM Inner and Outer Loop Step Size	No
RW3B	0x3B	DFETM Inner Loop Number of Increments	No
RW3C	0x3C	DFETM Outer Loop Number of Increments	No

Table 92 — Control Word Decoding

Register Control Word	MRA [7:0] HEX[1]	Meaning	Global Only (Requires Channel A Access)[2]
RW3D	0x3D	DFETM Inner Loop Current Increment	No
RW3E	0x3E	DFETM Outer Loop Current Increment	No
RW3F	0x3F	DFE Vref Range Selection	No
RW40	0x40	DCA0 Internal Vref	No
RW41	0x41	DCA1 Internal Vref	No
RW42	0x42	DCA2 Internal Vref	No
RW43	0x43	DCA3 Internal Vref	No
RW44	0x44	DCA4 Internal Vref	No
RW45	0x45	DCA5 Internal Vref	No
RW46	0x46	DCA6 Internal Vref	No
RW47	0x47	DPAR Internal Vref	No
RW48	0x48	DCS0 Internal Vref	No
RW49	0x49	DCS1 Internal Vref	No
RW4A	0x4A	DERROR_IN_n Vref	No
RW4B	0x4B	Loop-Back Vref	No
RW4C~RW5D	0x4C~0x5D	Reserved	No
RW5E	0x5E	CW Read Pointer	No
RW5F	0x5F	CW Page[3]	No

1. MRA7 must be 0 for RCD Control Word accesses and must be 1 for Data Buffer (DB) Control Words accesses.
2. This column indicates global Register Control Words that apply to both channels but are written and read from Channel A only. Any attempts to write to CH_B will do nothing.
3. All paged Control Words RW60 to RW7F are not global control words which means they are defined per sub channel and can be accessed through CH_A and CH_B unless otherwise stated.

8.4 Paged Control Word Decoding

8.4.1 Page 0 DFE Paged Control Word Decoding

Table 93 — Page 0 DFE Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x00	RW60	0x60	DCA0 Rx DFE Gain Coefficients
	RW61	0x61	DCA0 Rx DFE Tap 1 Coefficients
	RW62	0x62	DCA0 Rx DFE Tap 2 Coefficients
	RW63	0x63	DCA0 Rx DFE Tap 3 Coefficients
	RW64	0x64	DCA0 Rx DFE Tap 4 Coefficients
	RW65	0x65	RFU
	RW66	0x66	RFU
	RW67	0x67	RFU
	RW68	0x68	DCA1 Rx DFE Gain Coefficients
	RW69	0x69	DCA1 Rx DFE Tap 1 Coefficients
	RW6A	0x6A	DCA1 Rx DFE Tap 2 Coefficients
	RW6B	0x6B	DCA1 Rx DFE Tap 3 Coefficients
	RW6C	0x6C	DCA1 Rx DFE Tap 4 Coefficients
	RW6D	0x6D	RFU
	RW6E	0x6E	RFU
	RW6F	0x6F	RFU
	RW70	0x70	DCA2 Rx DFE Gain Coefficients
	RW71	0x71	DCA2 Rx DFE Tap 1 Coefficients
	RW72	0x72	DCA2 Rx DFE Tap 2 Coefficients
	RW73	0x73	DCA2 Rx DFE Tap 3 Coefficients
	RW74	0x74	DCA2 Rx DFE Tap 4 Coefficients
	RW75	0x75	RFU
	RW76	0x76	RFU
	RW77	0x77	RFU
	RW78	0x78	DCA3 Rx DFE Gain Coefficients
	RW79	0x79	DCA3 Rx DFE Tap 1 Coefficients
	RW7A	0x7A	DCA3 Rx DFE Tap 2 Coefficients
	RW7B	0x7B	DCA3 Rx DFE Tap 3 Coefficients
	RW7C	0x7C	DCA3 Rx DFE Tap 4 Coefficients
	RW7D	0x7D	RFU
	RW7E	0x7E	RFU
	RW7F	0x7F	RFU

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

8.4.2 Page 1 DFE Paged Control Word Decoding

Table 94 — Page 1 DFE Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x01	RW60	0x60	DCA4 Rx DFE Gain Coefficients
	RW61	0x61	DCA4 Rx DFE Tap 1 Coefficients
	RW62	0x62	DCA4 Rx DFE Tap 2 Coefficients
	RW63	0x63	DCA4 Rx DFE Tap 3 Coefficients
	RW64	0x64	DCA4Rx DFE Tap 4 Coefficients
	RW65	0x65	RFU
	RW66	0x66	RFU
	RW67	0x67	RFU
	RW68	0x68	DCA5 Rx DFE Gain Coefficients
	RW69	0x69	DCA5 Rx DFE Tap 1 Coefficients
	RW6A	0x6A	DCA5 Rx DFE Tap 2 Coefficients
	RW6B	0x6B	DCA5 Rx DFE Tap 3 Coefficients
	RW6C	0x6C	DCA5 Rx DFE Tap 4 Coefficients
	RW6D	0x6D	RFU
	RW6E	0x6E	RFU
	RW6F	0x6F	RFU
	RW70	0x70	DCA6 Rx DFE Gain Coefficients
	RW71	0x71	DCA6 Rx DFE Tap 1 Coefficients
	RW72	0x72	DCA6 Rx DFE Tap 2 Coefficients
	RW73	0x73	DCA6 Rx DFE Tap 3 Coefficients
	RW74	0x74	DCA6 Rx DFE Tap 4 Coefficients
	RW75	0x75	RFU
	RW76	0x76	RFU
	RW77	0x77	RFU
	RW78	0x78	DPAR Rx DFE Gain Coefficients
	RW79	0x79	DPAR Rx DFE Tap 1 Coefficients
	RW7A	0x7A	DPAR Rx DFE Tap 2 Coefficients
	RW7B	0x7B	DPAR Rx DFE Tap 3 Coefficients
	RW7C	0x7C	DPAR Rx DFE Tap 4 Coefficients
	RW7D	0x7D	RFU
	RW7E	0x7E	RFU
	RW7F	0x7F	RFU

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

8.4.3 Page 2 DFE Paged Control Word Decoding

Table 95 — Page 2 DFE Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x02	RW60	0x60	DCA0 Rx DFE Error Counter Lower 8 Bits
	RW61	0x61	DCA0 Rx DFE Error Counter Upper 8 Bits
	RW62	0x62	DCA0 DFE_Vref
	RW63	0x63	DCA0 LFSR Seed
	RW64	0x64	DCA1 Rx DFE Error Counter Lower 8 Bits
	RW65	0x65	DCA1 Rx DFE Error Counter Upper 8 Bits
	RW66	0x66	DCA1 DFE_Vref
	RW67	0x67	DCA1 LFSR Seed
	RW68	0x68	DCA2 Rx DFE Error Counter Lower 8 Bits
	RW69	0x69	DCA2 Rx DFE Error Counter Upper 8 Bits
	RW6A	0x6A	DCA2 DFE_Vref
	RW6B	0x6B	DCA2 LFSR Seed
	RW6C	0x6C	DCA3 Rx DFE Error Counter Lower 8 Bits
	RW6D	0x6D	DCA3 Rx DFE Error Counter Upper 8 Bits
	RW6E	0x6E	DCA3 DFE_Vref
	RW6F	0x6F	DCA3 LFSR Seed
	RW70	0x70	DCA4 Rx DFE Error Counter Lower 8 Bits
	RW71	0x71	DCA4 Rx DFE Error Counter Upper 8 Bits
	RW72	0x72	DCA4 DFE_Vref
	RW73	0x73	DCA4 LFSR Seed
	RW74	0x74	DCA5 Rx DFE Error Counter Lower 8 Bits
	RW75	0x75	DCA5 Rx DFE Error Counter Upper 8 Bits
	RW76	0x76	DCA5 DFE_Vref
	RW77	0x77	DCA5 LFSR Seed
	RW78	0x78	DCA6 Rx DFE Error Counter Lower 8 Bits
	RW79	0x79	DCA6 Rx DFE Error Counter Upper 8 Bits
	RW7A	0x7A	DCA6 DFE_Vref
	RW7B	0x7B	DCA6 LFSR Seed
	RW7C	0x7C	DPAR Rx DFE Error Counter Lower 8 Bits
	RW7D	0x7D	DPAR Rx DFE Error Counter Upper 8 Bits
	RW7E	0x7E	DPAR DFE_Vref
	RW7F	0x7F	DPAR LFSR Seed

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

8.4.4 Page 3 Manufacturing ID Control Word Decoding

Page 3 RW60 ~ RW6E control words in the DDR5RCD01 contain detailed RCD manufacturing information provided by RCD vendor. This information is programmed in OTP. The purpose is for improved manufacturing logistics management and not meant to be used by host platform to control normal operation. These registers must be accessible during run time.

Table 96 — Page 3 Manufacturing ID Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x03	RW60	0x60	Date Code Byte 0
	RW61	0x61	Date Code Byte 1
	RW62	0x62	Date Code Byte 2
	RW63	0x63	Vendor Specific Unique Unit Code Byte 0
	RW64	0x64	Vendor Specific Unique Unit Code Byte 1
	RW65	0x65	Vendor Specific Unique Unit Code Byte 2
	RW66	0x66	Vendor Specific Unique Unit Code Byte 3
	RW67	0x67	Vendor Specific Unique Unit Code Byte 4
	RW68	0x68	Vendor Specific Unique Unit Code Byte 5
	RW69	0x69	Vendor Specific Unique Unit Code Byte 6
	RW6A	0x6A	Vendor ID Byte 0
	RW6B	0x6B	Vendor ID Byte 1
	RW6C	0x6C	Vendor Device ID Byte 0
	RW6D	0x6D	Vendor Device ID Byte 1
	RW6E	0x6E	Revision ID
	RW6F	0x6F	Reserved
	RW70	0x70	Reserved
	RW71	0x71	Reserved
	RW72	0x72	Reserved
	RW73	0x73	Reserved
	RW74	0x74	Reserved
	RW75	0x75	Reserved
	RW76	0x76	Reserved
	RW77	0x77	Reserved
	RW78	0x78	Reserved
	RW79	0x79	Reserved
	RW7A	0x7A	Reserved
	RW7B	0x7B	Reserved
	RW7C	0x7C	Reserved
	RW7D	0x7D	Reserved
	RW7E	0x7E	Reserved
	RW7F	0x7F	Reserved

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

8.4.5 Page 4 VHost Paged Control Word Decoding

Table 97 — Page4 VHost Control Word Decoding[1,2,3]

Page	Register Control Word	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Encoding
0x04	RW60	cmd0a_CA07	cmd0a_CA06	cmd0a_CA05	cmd0a_CA04	cmd0a_CA03	cmd0a_CA02	cmd0a_CA01	cmd0a_CA00	cmd0 1st UI
	RW61	cmd0a_CS1	cmd0a_CS0	cmd0a_CA13	cmd0a_CA12	cmd0a_CA11	cmd0a_CA10	cmd0a_CA09	cmd0a_CA08	
	RW62	cmd0b_CA07	cmd0b_CA06	cmd0b_CA05	cmd0b_CA04	cmd0b_CA03	cmd0b_CA02	cmd0b_CA01	cmd0b_CA00	cmd0 2nd UI
	RW63	cmd0b_CS1	cmd0b_CS0	cmd0b_CA13	cmd0b_CA12	cmd0b_CA11	cmd0b_CA10	cmd0b_CA09	cmd0b_CA08	
	RW64	cmd1a_CA07	cmd1a_CA06	cmd1a_CA05	cmd1a_CA04	cmd1a_CA03	cmd1a_CA02	cmd1a_CA01	cmd1a_CA00	cmd1 1st UI
	RW65	cmd1a_CS1	cmd1a_CS0	cmd1a_CA13	cmd1a_CA12	cmd1a_CA11	cmd1a_CA10	cmd1a_CA09	cmd1a_CA08	
	RW66	cmd1b_CA07	cmd1b_CA06	cmd1b_CA05	cmd1b_CA04	cmd1b_CA03	cmd1b_CA02	cmd1b_CA01	cmd1b_CA00	cmd1 2nd UI
	RW67	cmd1b_CS1	cmd1b_CS0	cmd1b_CA13	cmd1b_CA12	cmd1b_CA11	cmd0a_CA10	cmd1b_CA09	cmd1b_CA08	
	RW68	cmd2a_CA07	cmd2a_CA06	cmd2a_CA05	cmd2a_CA04	cmd2a_CA03	cmd2a_CA02	cmd2a_CA01	cmd2a_CA00	cmd2 1st UI
	RW69	cmd2a_CS1	cmd2a_CS0	cmd2a_CA13	cmd2a_CA12	cmd2a_CA11	cmd2a_CA10	cmd2a_CA09	cmd2a_CA08	
	RW6A	cmd2b_CA07	cmd2b_CA06	cmd2b_CA05	cmd2b_CA04	cmd2b_CA03	cmd2b_CA02	cmd2b_CA01	cmd2b_CA00	cmd2 2nd UI
	RW6B	cmd2b_CS1	cmd2b_CS0	cmd2b_CA13	cmd2b_CA12	cmd2b_CA11	cmd2b_CA10	cmd2b_CA09	cmd2b_CA08	
	RW6C	cmd3a_CA07	cmd3a_CA06	cmd3a_CA05	cmd3a_CA04	cmd3a_CA03	cmd3a_CA02	cmd3a_CA01	cmd3a_CA00	cmd3 1st UI
	RW6D	cmd3a_CS1	cmd3a_CS0	cmd3a_CA13	cmd3a_CA12	cmd3a_CA11	cmd3a_CA10	cmd3a_CA09	cmd3a_CA08	
	RW6E	cmd3b_CA07	cmd3b_CA06	cmd3b_CA05	cmd3b_CA04	cmd3b_CA03	cmd3b_CA02	cmd3b_CA01	cmd3b_CA00	cmd3 2nd UI
	RW6F	cmd3b_CS1	cmd3b_CS0	cmd3b_CA13	cmd3b_CA12	cmd3b_CA11	cmd3b_CA10	cmd3b_CA09	cmd3b_CA08	
	RW70	Reserved	cmd1 to cmd2 Delay			Reserved	cmd0 to cmd1 Delay			Delay between commands
	RW71	Reserved	cmd3 to cmdn Delay			Reserved	cmd2 to cmd3 Delay			
	RW72	Reserved	Reserved	Reserved	Reserved	Reserved	Repeat Enable	Repeat Control		Repeat
	RW73	Reserved	Reserved	Reserved	Reserved	Reserved	VHost Start/Stop	VHost Selection		Start
	RW74	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW75	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW76	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW77	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW78	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW79	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW7A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW7B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW7C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW7D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW7E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	RW7F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

1. For LRDIMM, the BCOM interface interprets the relevant commands from VHost and sends them out as BCOM command sequences similar to the way it operates in normal mode. Irrelevant commands result in BCOM Deselect (idle) cycles.
2. For LRDIMM, the user is responsible for programming long enough command intervals in PG[4]RW70/PG[4]RW71 so that there is no chance of chopping any BCOM sequences or dropping commands that occur when the BCOM interface is busy transmitting the previous command. This includes avoiding sending another command requiring the BCOM bus one clock after a 1UI DRAM command which requires 2 clocks on the BCOM bus (PDE command).
3. For LRDIMM, the BCOM command sequences will be delayed one cycle with respect to the QCA commands similar to the way things work in normal operation.

8.5 Sticky Bits

8.5.1 Direct

1. RW00[1:0]: Command Address Rate & SDR Modes
2. RW05[3:0]: Operating Speed
3. RW05[6:5]: V_{DD} Operating Voltage & Frequency Context
4. RW06: Fine Granularity DIMM Operating Speed
5. RW08: Clock Driver Enable
6. RW09: Output Address and Control Enable
7. RW0A: QCK Signal Driver Characteristics
8. RW0C: QxCA and QxCS Signal Driver Characteristics

9. RW0D: Data Buffer Interface Driver Characteristics
10. RW0E: QCK, QCA and QCS Output Slew Rate
11. RW0F: BCK, BCOM and BCS Output Slew Rate
12. RW10: IBT
13. RW11: Command Latency Adder
14. RW12: QACK Output Delay
15. RW13: QBCK Output Delay
16. RW14: QCCK Output Delay
17. RW15: QDCK Output Delay
18. RW17: QACS0_n Output Delay
19. RW18: QACS1_n Output Delay
20. RW19: QBCS0_n Output Delay
21. RW1A: QBCS1_n Output Delay
22. RW1B: QACA Output Delay
23. RW1C: QBCA Output Delay
24. RW1D: BCS_n and BCOM[2:0] Output Delay
25. RW1E: BCK Output Delay
26. RW25[5]: SidebandBus Mode
27. RW28: I^2C & I3C Basic Error Status
28. RW31: DFE Configuration
29. RW[47:40]: Internal VrefCA
30. RW[49:48]: Internal VrefCS

8.5.2 Paged

1. PG[1:0]RW[61, 69, 71, 79]: DPAR and DCA[6:0] Receiver DFE Tap 1 Coefficients
2. PG[1:0]RW[62, 6A, 72, 7A]: DPAR and DCA[6:0] Receiver DFE Tap 2 Coefficients
3. PG[1:0]RW[63, 6B, 73, 7B]: DPAR and DCA[6:0] Receiver DFE Tap 3 Coefficients
4. PG[1:0]RW[64, 6C, 74, 7C]: DPAR and DCA[6:0] Receiver DFE Tap 4 Coefficients
5. PG[1:0]RW[60, 68, 70, 78]: DPAR and DCA[6:0] Receiver DFE Gain Offset Adjustment

8.6 Mode and Command Control Words

8.6.1 RW00 - Global Features Control Word

Table 98 — RW00 - Global Features Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Command Address Rate[1]	Single Data Rate (SDR)
x	x	x	x	x	x	x	1		Double Data Rate (DDR)
x	x	x	x	x	x	0	x	SDR Modes[1,2]	SDR1 (additional setup time)
x	x	x	x	x	x	1	x		SDR2
x	x	x	x	x	0	x	x	CA Pass Through mode Enable	Normal operation
x	x	x	x	x	1	x	x		Enabled - Rank selected in OP[3][3,4]
x	x	x	x	0	x	x	x	CA Pass Through mode Rank Selection	CA Pass Through Rank 0 [5]
x	x	x	x	1	x	x	x		CA Pass Through Rank 1[6]
x	x	x	0	x	x	x	x	BCOM Pass-Through mode	Normal operation
x	x	x	1	x	x	x	x		Enabled Pass-Through Mode
x	x	0	x	x	x	x	x	Output Inversion [7,8]	Enabled
x	x	1	x	x	x	x	x		Disabled
x	0	x	x	x	x	x	x	Power Down Mode[9]	Disabled
x	1	x	x	x	x	x	x		Enabled
0	x	x	x	x	x	x	x	Transparent Mode	Disabled
1	x	x	x	x	x	x	x		Enabled

1. RW00[1:0] will be sticky, cleared by power cycle not reset.
2. This bit does not apply for DDR CA when RW00[0] = 1.
3. Internal RCD logic is allowed to block command processing by the BCOM interface in this mode. However, the Host must write RW01[3] = 0 to ensure BCOM commands are being blocked when CA Pass Through mode is enabled in RW00[2].
4. If DRAM commands are blocked by RW01[1] = 0, DCSy_n pulses are not forwarded to QCSy_n outputs for any rank even if CA Pass Through Mode is enabled in RW00[2].
5. When Pass through mode is enable on Rank 0 the RCD will process MRW commands on Rank 1.
6. When Pass through mode is enable on Rank 1 the RCD will process MRW commands on Rank 0.
7. For normal operation, output inversion is always enabled. For DIMM vendor test purpose, output inversion can be disabled. When disabled, register tPDM is not guaranteed to be met.
8. Both output copies must be driven HIGH between CMD, regardless of the setting in RW00[5].
9. This bit will disable vendor specific circuitry if any, for power reduction during PDE mode.

8.6.2 RW01 - Parity, CMD Blocking, and Alert Control Word Global Control Word CA

Table 99 — RW01 - Parity, CMD Blocking, and Alert Global Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Parity Checking	Parity checking disabled[1]
x	x	x	x	x	x	x	1		Parity checking enabled
x	x	x	x	x	x	0	x	DRAM Interface Forward All CMDS	Block
x	x	x	x	x	x	1	x		Do not block
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Data Buffer Interface Forward All CMDs	Block
x	x	x	x	1	x	x	x		Do not block
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Host Interface Training Feedback[2]	Both Sub channels feedback on ALERT_n
x	x	1	x	x	x	x	x		Sub CH_A feedback on QLBD; Sub CH_B feedback on QLBS
x	0	x	x	x	x	x	x	ALERT_n Assertion[3,4]	Static ALERT_n Assertion Mode[5]
x	1	x	x	x	x	x	x		Pulsed ALERT_n Assertion Mode[6]
0	x	x	x	x	x	x	x	ALERT_n Re-enable[7]	Parity checking remains disabled after ALERT_n pulse
1	x	x	x	x	x	x	x		Parity checking is re-enabled after ALERT_n pulse

1. Register does not check for parity including control word programming.
2. Includes DCS, DCA, and DFE Training Mode
3. This bit only affects ALERT_n assertion that is a result of a CA parity error. In case of a LOW level on the DERROR_IN_n input, ALERT_n stays asserted as long as DERROR_IN_n remains LOW unless DRST_n is LOW or the device is in clock stopped power down mode.
4. For details on ALERT_n output driver strength settings, see Table 219, "Output Driver DC Electrical Characteristics, entire operating temperature range".
5. ALERT_n stays asserted until 'Clear CA Parity Error' command is sent.
6. ALERT_n pulse width according to Table 100.
7. CA Parity Error Status bit in Error Log Register remains set until cleared by sending a Clear CA Parity Error command.

Figure 61, "DxCSx_n Assertion during ALERT_n Pulse Width" shows DxCSx_n assertion are not permitted t_{CSALT} prior and after of ALERT_n de-assertion when RW01[0] = 1.

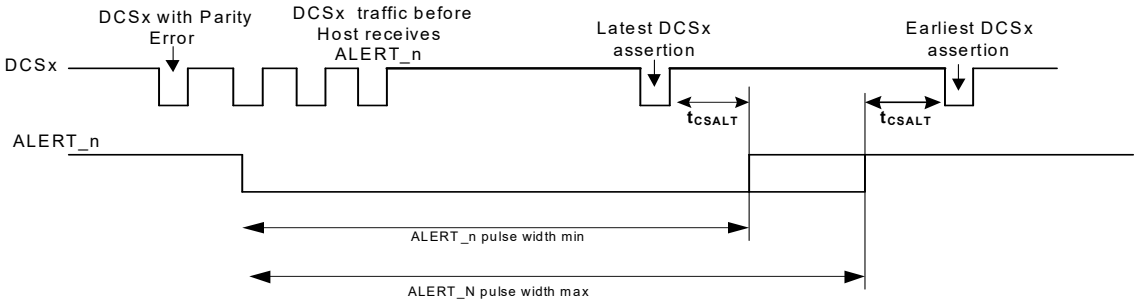


Figure 61 — DxCSx_n Assertion during ALERT_n Pulse Width

Table 100 — ALERT_n Pulse Width for Parity Error

ALERT_n Pulse Width[1]										
DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Units
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
96	192	108	216	120	240	132	264	144	288	nCK

1. The values in this table correspond to parity error in one of the channels. If parity errors occur in both CA channels, the resulting pulse width could be wider than the Maximum values shown in this table due to overlapping of the error pulse signals generated from each channel.

8.6.3 RW02 - Host Interface Training Mode Global Control Word

Table 101 — RW02: Host Interface Training Mode Global Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	Host Interface Training Mode selection CH_A	Normal operating mode
x	x	x	x	x	x	0	1		Clock-to-DCAy_A training mode
x	x	x	x	x	x	1	0		DCS0_A_n training mode
x	x	x	x	x	x	1	1		DCS1_A_n training mode
x	x	x	x	0	0	x	x	Host Interface Training Mode selection CH_B	Normal operating mode
x	x	x	x	0	1	x	x		Clock-to-DCAy_B training mode
x	x	x	x	1	0	x	x		DCS0_B_n training mode
x	x	x	x	1	1	x	x		DCS1_B_n training mode
x	x	0	0	x	x	x	x	DCA Training XOR sampling edge[1,2]	Both Rising and Falling Edges
x	x	0	1	x	x	x	x		Rising Edge
x	x	1	0	x	x	x	x		Falling Edge
x	x	1	1	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	VrefCA Broadcast[3]	Disabled
x	1	x	x	x	x	x	x		Enabled[4]
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. The DCA sampling edge bits only applies when Clock-to-DCAy_A or Clock-to-DCAy_B training modes are selected in RW02[3:2] or RW02[1:0].
2. When SDR mode is enabled (i.e., RW00[0] = 0), only code 01 'Rising Edge' is legal for this field.
3. The VrefCA Broadcast Enable mode bit is global and is enabled on both sub-channels by setting RW02[6] = 1 on channel A only. The actual broadcasting of the VrefCA control word writes is independent per sub-channel.
4. When VrefCA Broadcast mode is enabled, writes to RW[47:41] will be ignored by the RCD on both sub-channels. Vref DCA[6:0]_A and Vref DPAR_A are configured by writing to RW[40] on channel A. Vref DCA[6:0]_B and Vref DPAR_B are configured by writing to RW40 on channel B.

8.6.4 RW03 - DRAM & DB Interface Training Modes Global Control Word

Table 102 — RW03: DRAM & DB Interface Training Modes Global Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	QCS Training Mode Enable	Disabled
x	x	x	x	x	x	x	1		Enabled - Rank selected in OP[1]
x	x	x	x	x	x	0	x	QCS Training Rank Selection	[Rank 0] QACS0 and QBCS0 Training mode
x	x	x	x	x	x	1	x		[Rank 1] QACS1 and QBCS1 Training mode
x	x	x	x	x	0	x	x	Short MRR command for Data Buffer Training in SDR mode [1]	Disabled
x	x	x	x	x	1	x	x		Enable
x	x	x	x	0	x	x	x	Static Control Value for BCOM0[2]	Output driven statically Low
x	x	x	x	1	x	x	x		Output driven statically High
x	x	x	0	x	x	x	x	Static Control Value for BCOM1[2]	Output driven statically Low
x	x	x	1	x	x	x	x		Output driven statically High
x	x	0	x	x	x	x	x	Static Control Value for BCOM2[2]	Output driven statically Low
x	x	1	x	x	x	x	x		Output driven statically High
x	0	x	x	x	x	x	x	Static Control Value for BCS_n[2]	Output driven statically Low
x	1	x	x	x	x	x	x		Output driven statically High
0	x	x	x	x	x	x	x	Static BCOM Control Enable[3,4]	Normal
1	x	x	x	x	x	x	x		Enabled; BCOM and BCS driven statically according to OP[6:3]

1. When Enabled the DDR5RCD01 will forward a Short MRR Command on the BCOM Bus instead of normal MRR when it receives an MRR CMD from Host.
2. Static Control Value, when RW03[7] = 1
3. BCOM[2:0] and BCS_n outputs driven statically by the RCD with the values contained in RW03[6:3].
4. If RW03[7] = 1 the RCD will apply the static values selected in RW03[6:3] on BCS_n and BCOM[2:0] regardless of the setting in RW01[3] (Data Buffer Interface Block All Commands).

8.6.5 RW04 - Command Space Global Control Word

After issuing a register command via writes to RW04, t_{MRC} is the minimum waiting time required by the RCD before the next DRAM command or MRW write can be issued. Some of the commands in RW04 may require additional waiting times (longer than t_{MRC}) to meet timing parameters specified for the DRAM or Data Buffers.

Table 103 — RW04: Command Space Global Control Word definition

Command								Command No	Command Name	Result
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0			
0	0	0	0	0	0	0	0	CMD 0	NOP	NOP[1]
0	0	0	0	0	0	0	1	CMD 1	CH_A DB Reset[2]	Switches BRST_A_n to active which is LOW. Does NOT reset RCD.
0	0	0	0	0	0	1	0	CMD 2	Clear CH_A DB Reset[2]	Switches BRST_A_n to inactive which is HIGH.
0	0	0	0	0	0	1	1	CMD 3	CH_B DB Reset[2]	Switches BRST_B_n to active which is LOW. Does NOT reset RCD
0	0	0	0	0	1	0	0	CMD 4	Clear CH_B DB Reset[2]	Switches BRST_B_n to inactive which is HIGH
0	0	0	0	0	1	0	1	CMD 5	CH_A DRAM Reset	Switches QRST_A_n & QCSx_A_n to active which is LOW
0	0	0	0	0	1	1	0	CMD 6	Clear CH_A DRAM Reset	Switches QRST_A_n to inactive which is HIGH
0	0	0	0	0	1	1	1	CMD 7	CH_B DRAM Reset	Switches QRST_B_n & QCSx_B_n to active which is LOW
0	0	0	0	1	0	0	0	CMD 8	Clear CH_B DRAM Reset	Switches QRST_B_n to inactive which is HIGH
0	0	0	0	1	0	0	1	CMD 9	CH_A Clear parity Error	Clear 'CA Parity Error Status' bit and '> 1 Error' bit and re-enable parity checking (if not already enabled)
0	0	0	0	1	0	1	0	CMD 10	CH_B Clear parity Error	Clear 'CA Parity Error Status' bit and '> 1 Error' bit and re-enable parity checking (if not already enabled)
0	0	0	0	1	0	1	1	CMD 11	CH_A DFE ERROR Counter Reset	Resets All of CH_A DFE ERROR Counters to zero
0	0	0	0	1	1	0	0	CMD 12	CH_B DFE ERROR Counter Reset	Resets All of CH_B DFE ERROR Counters to zero
0	0	0	0	1	1	0	1	CMD 13	ALERT_n Toggle	Sends one 6 to 10-cycle LOW pulse on ALERT_n
0	0	0	0	1	1	1	0	CMD 14	CH_A QCS HIGH[3]	QCSx_A_n Released
0	0	0	0	1	1	1	1	CMD 15	CH_B QCS HIGH[4]	QCSx_B_n Released
1	1	1	1	0	0	0	0	Reserved	Reserved	Reserved
1	1	1	1	0	0	0	1	Reserved	Reserved	Reserved
1	1	1	1	0	0	1	0	Reserved	Reserved	Reserved
1	1	1	1	0	0	1	1	Reserved	Reserved	Reserved
1	1	1	1	0	1	0	0	Reserved	Reserved	Reserved
1	1	1	1	0	1	0	1	Reserved	Reserved	Reserved
1	1	1	1	0	1	1	0	Reserved	Reserved	Reserved
1	1	1	1	0	1	1	1	Reserved	Reserved	Reserved
1	1	1	1	1	0	0	0	Reserved	Reserved	Reserved
1	1	1	1	1	0	0	1	Reserved	Reserved	Reserved
1	1	1	1	1	0	1	0	Reserved	Reserved	Reserved
1	1	1	1	1	0	1	1	Reserved	Reserved	Reserved
1	1	1	1	1	1	0	0	Reserved	Reserved	Reserved
1	1	1	1	1	1	0	1	Reserved	Reserved	Reserved
1	1	1	1	1	1	1	0	Reserved	Reserved	Reserved
1	1	1	1	1	1	1	1	Reserved	Reserved	Reserved

1. This operation was added specifically for hosts that do not support byte writes over the SidebandBus, i.e. that have to write more than one CW at the same time.
2. The RCD is not responsible for blocking command traffic in the BCOM[2:0] and BCS_n outputs unless Static BCOM/BCS_n Control is enabled in RW03[7].
3. CMD 14 can be used during initialization sequences to start the QCK clocks and enable the QCA outputs in CH_A even when the RCD is not provided with the DCS input pulse shown in the Reset initialization timing diagram.

4. CMD 15 can be used during initialization sequences to start the QCK clocks and enable the QCA outputs in CH_B even when the RCD is not provided with the DCS input pulse shown in the Reset initialization timing diagram.

8.7 Clocking Control Words

8.7.1 RW05 - DIMM Operating Speed Global Control Word

Table 104 — RW05: DIMM Operating Speed Global Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Operating Speed[2]	DDR5-3200 (2800 MT/s < f ≤ 3200 MT/s)
x	x	x	x	0	0	0	1		DDR5-3600 (3200 MT/s < f ≤ 3600 MT/s)
x	x	x	x	0	0	1	0		DDR5-4000 (3600 MT/s < f ≤4000 MT/s)
x	x	x	x	0	0	1	1		DDR5-4400 (4000 MT/s < f ≤ 4400 MT/s)
x	x	x	x	0	1	0	0		DDR5-4800 (4400 MT/s < f ≤ 4800 MT/s)
x	x	x	x	0	1	0	1		Reserved for DDR5-5200(4800 MT/s < f ≤ 5200 MT/s)
x	x	x	x	0	1	1	0		Reserved for DDR5 5600 (5200 MT/s < f ≤ 5600 MT/s)
x	x	x	x	0	1	1	1		Reserved for DDR5 6000 (5600 MT/s < f ≤ 6000 MT/s)
x	x	x	x	1	0	0	0		Reserved for DDR5 6400 (6000 MT/s < f ≤ 6400 MT/s)
x	x	x	x	1	0	0	1		Reserved
x	x	x	x	1	0	1	0		Reserved
x	x	x	x	1	0	1	1		Reserved
x	x	x	x	1	1	0	0		Reserved
x	x	x	x	1	1	0	1		Reserved
x	x	x	x	1	1	1	0		Down-bin Data Rate (2000 MT/s < f ≤ 2100 MT/s)[3]
x	x	x	x	1	1	1	1		PLL bypass mode enabled
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Register V_{DD} Operating Voltage[4]	1.1 V
x	x	1	x	x	x	x	x		Reserved for lower voltage
x	0	x	x	x	x	x	x	Context for operation training	Default; Context 1 operation.
x	1	x	x	x	x	x	x		Context 2 operation.[5]
0	x	x	x	x	x	x	x	Frequency Band Select	Operation (Frequency Band 1)
1	x	x	x	x	x	x	x		Test Mode (Frequency Band 2)[6]

1. The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run.
2. RW05[6:5] and RW05[3:0] will be sticky, cleared by power cycle not Reset.
3. This setting may or may not support fractional delay settings, Fine Granularity DIMM Operating Speed Control, and will require a longer clock stabilization time.
4. RW05[5] will be used to inform DDR5RCD01 under what operating voltage V_{DD} will be used. The RCD can use the information to optimize their functionality and performance at low-voltage conditions.
5. The control words listed in Table 22 on page 59 are duplicated by the DDR5RCD01 for the 2nd frequency context.
6. RW05[7] shall be set to '1' in order to guarantee PLL Lock when DCK is running in the Band-2 frequency range (i.e., 140 MHz < f_{TEST} ≤ 1400 MHz).

8.7.2 RW06 - Fine Granularity DIMM Operating Speed Global Control Word

Table 105 — RW06: Fine Granularity DIMM Operating Speed Global Control Word[1]

Setting								Definition	Encoding[2]
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Fine Granularity Operating Speed in terms of f_{bin}, where f_{bin} is the top speed for the speed range selected in RW05 OP[3:0][3]	(f_{bin} - 20 MT/s) < f ≤ f_{bin}
x	x	x	0	0	0	0	1		(f_{bin} - 40 MT/s) < f ≤ (f_{bin} - 20 MT/s)
x	x	x	0	0	0	1	0		(f_{bin} - 60 MT/s) < f ≤ (f_{bin} - 40 MT/s)
x	x	x	0	0	0	1	1		(f_{bin} - 80 MT/s) < f ≤ (f_{bin} - 60 MT/s)
x	x	x	0	0	1	0	0		(f_{bin} - 100 MT/s) < f ≤ (f_{bin} - 80 MT/s)
x	x	x	0	0	1	0	1		(f_{bin} - 120 MT/s) < f ≤ (f_{bin} - 100 MT/s)
x	x	x	0	0	1	1	0		(f_{bin} - 140 MT/s) < f ≤ (f_{bin} - 120 MT/s)
x	x	x	0	0	1	1	1		(f_{bin} - 160 MT/s) < f ≤ (f_{bin} - 140 MT/s)
x	x	x	0	1	0	0	0		(f_{bin} - 180 MT/s) < f ≤ (f_{bin} - 160 MT/s)
x	x	x	0	1	0	0	1		(f_{bin} - 200 MT/s) < f ≤ (f_{bin} - 180 MT/s)
x	x	x	0	1	0	1	0		(f_{bin} - 220 MT/s) < f ≤ (f_{bin} - 200 MT/s)
x	x	x	0	1	0	1	1		(f_{bin} - 240 MT/s) < f ≤ (f_{bin} - 220 MT/s)
x	x	x	0	1	1	0	0		(f_{bin} - 260 MT/s) < f ≤ (f_{bin} - 240 MT/s)
x	x	x	0	1	1	0	1		(f_{bin} - 280 MT/s) < f ≤ (f_{bin} - 260 MT/s)
x	x	x	0	1	1	1	0		(f_{bin} - 300 MT/s) < f ≤ (f_{bin} - 280 MT/s)
x	x	x	0	1	1	1	1		(f_{bin} - 320 MT/s) < f ≤ (f_{bin} - 300 MT/s)
x	x	x	1	0	0	0	0		(f_{bin} - 340 MT/s) < f ≤ (f_{bin} - 320 MT/s)
x	x	x	1	0	0	0	1		(f_{bin} - 360 MT/s) < f ≤ (f_{bin} - 340 MT/s)
x	x	x	1	0	0	1	0		(f_{bin} - 380 MT/s) < f ≤ (f_{bin} - 360 MT/s)
x	x	x	1	0	0	1	1		(f_{bin} - 400 MT/s) < f ≤ (f_{bin} - 380 MT/s)
x	x	x	1	0	1	0	0		Reserved
x	x	x	...						Reserved
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. This control word defines the frequency of the DCK_t - DCK_c input reference clock during normal operation (i.e., when not in test frequency range) in units of 20 MT/s.
2. The frequency ranges shown in this column are for the base frequency of the input clock and they do not include SSC modulation effects. In some cases, due to SSC modulation, the actual frequency of the input clock can straddle two adjacent frequency ranges.
3. RW06[4:0] will be sticky, cleared by power cycle not Reset.

8.8 Validation and Lockout Control Words

8.8.1 RW07 - Validation Pass-Through and Lockout Protection Global Control Word

Table 106 — RW07: Validation Pass-Through and Lockout Protection Global Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Lockout Protection Enable[1]	No effect[2]
x	x	x	x	x	x	x	1		Protection enabled[3,4]
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Validation Pass-Through Feature Enable	Feature disabled
x	x	x	1	x	x	x	x		Feature enabled
x	x	0	x	x	x	x	x	Validation Pass-Through Mode Selection	Process MRW
x	x	1	x	x	x	x	x		Ignore MRW[5]
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. This feature is intended to protect the RCD against lockout state that is unrecoverable with DRST_n Reset and is caused by invalid DCA commands associated with incorrect input signal voltage levels or timing.
2. This control bit is type “Write-1 Only” and cannot be written to 0 by the user. It only gets cleared to zero by DRST_n Reset or by internal Power-On Reset.
3. When OP[0] = 1, the RCD prevents Writes to vendor specific CW pages (i.e., Pages 80h to FFh) triggered by commands received at the Host DCA interface of the RCD including MRW commands and CW in-band updates enabled when RW32[6] = 1.
4. This feature does not affect access performed through SMBus.
5. SMBus access to the RCD registers will not be blocked in Validation Pass-Through mode.

8.9 Output Enable Control Words

8.9.1 RW08 - Clock Driver Enable Control Word

Table 107 — RW08: Clock Driver Enable Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Disable QACK_t/QACK_c clock[1,2]	QACK_t/QACK_c clock enabled
x	x	x	x	x	x	x	1		QACK_t/QACK_c clock disabled
x	x	x	x	x	x	0	x	Disable QBCK_t/QBCK_c clock[1,2]	QBCK_t/QBCK_c clock enabled
x	x	x	x	x	x	1	x		QBCK_t/QBCK_c clock disabled
x	x	x	x	x	0	x	x	Disable QCCK_t/QCCK_c clock[1,2]	QCCK_t/QCCK_c clock enabled
x	x	x	x	x	1	x	x		QCCK_t/QDCK_c clock disabled
x	x	x	x	0	x	x	x	Disable QDCK_t/QDCK_c clock[1,2]	QDCK_t/QDCK_c clock enabled
x	x	x	x	1	x	x	x		QDCK_t/QDCK_c clock disabled
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	BCK_t/BCK_c [2]	BCK_t/BCK_c clock enabled
x	x	1	x	x	x	x	x		BCK_t/BCK_c clock disabled
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on DCK_t/DCK_c unless the system stops the clock inputs to the DDR5RCD01 to enter the lowest power mode.
2. RW08[5] and RW08[3:0] will be sticky, cleared by power cycle not Reset.

8.9.2 RW09 - Output Address and Control Enable Control Word

Table 108 — RW09: Output Address and Control Enable Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	QACA outputs	Enabled
x	x	x	x	x	x	x	1		Disabled
x	x	x	x	x	x	0	x	QBCA outputs	Enabled
x	x	x	x	x	x	1	x		Disabled
x	x	x	x	x	0	x	x	DCS1_n Input Buffer & QxCS1_n	DCS1_n & QxCS1_n pins Enabled
x	x	x	x	x	1	x	x	Outputs[1] (single rank)	DCS1_n & QxCS1_n pins Disabled[2]
x	x	x	x	0	x	x	x	BCS_n , BCOM[2:0] & BRST_n	Enabled (LRDIMM)
x	x	x	x	1	x	x	x	outputs[3]	Disabled (RDIMM)
x	x	x	0	x	x	x	x	Q[B:A]CA13 output driver disable	Enabled
x	x	x	1	x	x	x	x		Disabled
x	x	0	x	x	x	x	x	QACS[1:0]_n output	Enable
x	x	1	x	x	x	x	x		Disabled
x	0	x	x	x	x	x	x	QBCS[1:0]_n output	Enabled
x	1	x	x	x	x	x	x		Disabled
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. DCS1 is a required signal for training modes and must be routed even on single rank DIMMs. RW09[2] can be written to 1 to save power in single rank DIMMs during normal operation after initialization and training sequences have been completed.
2. The RCD will enter Power Down mode on a Single Rank DIMM when PDE command sent to Rank 0.
3. RW09[6:0] will be sticky, cleared by power cycle not Reset.

8.10 Output Driver Strengths

For details on RCD output driver strengths in this section, see Table 219, “Output Driver DC Electrical Characteristics, entire operating temperature range”.

8.10.1 RW0A - QCK Signals Driver Characteristics Control Word

Table 109 — RW0A: QCK Signals Driver Characteristics Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	QACK_t/QACK_c[1]	RZQ/12 (20 Ω)
x	x	x	x	x	x	0	1		RZQ/17 (14 Ω)
x	x	x	x	x	x	1	0		RZQ/24 (10 Ω)
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	QBCK_t/QBCK_c[1]	RZQ/12 (20 Ω)
x	x	x	x	0	1	x	x		RZQ/17 (14 Ω)
x	x	x	x	1	0	x	x		RZQ/24 (10 Ω)
x	x	x	x	1	1	x	x		Reserved
x	x	0	0	x	x	x	x	QCCK_t/QCCK_c[1]	RZQ/12 (20 Ω)
x	x	0	1	x	x	x	x		RZQ/17 (14 Ω)
x	x	1	0	x	x	x	x		RZQ/24 (10 Ω)
x	x	1	1	x	x	x	x		Reserved
0	0	x	x	x	x	x	x	QDCK_t/QDCK_c[1]	RZQ/12 (20 Ω)
0	1	x	x	x	x	x	x		RZQ/17 (14 Ω)
1	0	x	x	x	x	x	x		RZQ/24 (10 Ω)
1	1	x	x	x	x	x	x		Reserved

1. RW0A[7:0] will be sticky, cleared by power cycle not Reset.

8.10.2 RW0C - QxCA and QxCS_n Signals Driver Characteristics Control Word

Table 110 — RW0C: QxCA and QxCS_n Signals Driver Characteristics Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	Address/Command Address for both A&B copies[1]	RZQ/12 (20 Ω)
x	x	x	x	x	x	0	1		RZQ/17 (14 Ω)
x	x	x	x	x	x	1	0		RZQ/24 (10 Ω)
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	Reserved	Reserved
x	x	x	x	0	1	x	x		Reserved
x	x	x	x	1	0	x	x		Reserved
x	x	x	x	1	1	x	x		Reserved
x	x	0	0	x	x	x	x	QxCS0_n, QxCS1_n, Outputs[1]	RZQ/12 (20 Ω)
x	x	0	1	x	x	x	x		RZQ/17 (14 Ω)
x	x	1	0	x	x	x	x		RZQ/24 (10 Ω)
x	x	1	1	x	x	x	x		Reserved
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

1. RW0C[1:0] and RW0C[5:4] will be sticky, cleared by power cycle not Reset.

8.10.3 RW0D - Data Buffer Interface Driver Characteristics Control Word

Table 111 — RW0D: Data Buffer Interface Driver Characteristics Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	BCOM[2:0], BCS_n driver strength[1]	RZQ/12 (20 Ω)
x	x	x	x	x	x	0	1		RZQ/17 (14 Ω)
x	x	x	x	x	x	1	0		Reserved
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	0	0	x	x	x	BCK_t/BCK_c driver strength[1]	RZQ/12 (20 Ω)
x	x	x	0	1	x	x	x		RZQ/17 (14 Ω)
x	x	x	1	0	x	x	x		RZQ/24 (10 Ω)
x	x	x	1	1	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW0D[1:0] and RW0D[4:3] will be sticky, cleared by power cycle not Reset.

8.11 Output Slew Rate Control

The DDR5RCD01 will support output slew rate control, per channel, as describe in the following control words.

8.11.1 RW0E - QCK, QCA and QCS Output Slew Rate Control Word

Table 112 — RW0E - QCK, QCA and QCS Output Slew Rate Control Word[1]

Setting								Definition	Encoding	Range		Units
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0			Min	Max	
x	x	x	x	x	x	0	0	QCK[D:A]_t / QCK[D:A]_c Differential Slew Rate Setting[2]	Moderate	12	20	V/ns
x	x	x	x	x	x	0	1		Fast	14	27	V/ns
x	x	x	x	x	x	1	0		Reserved			
x	x	x	x	x	x	1	1		Reserved			
x	x	x	x	0	0	x	x	Q[B:A]CA[13:0] Single Ended Slew Rate setting[3]	Moderate	4.0	7.0	V/ns
x	x	x	x	0	1	x	x		Fast	6.0	10.0	V/ns
x	x	x	x	1	0	x	x		Slow	2.7	4.5	V/ns
x	x	x	x	1	1	x	x		Reserved			
x	x	0	0	x	x	x	x	Q[B:A]CS[1:0]_n Single Ended Slew Rate setting [3]	Moderate	4.0	7.0	V/ns
x	x	0	1	x	x	x	x		Fast	6.0	10.0	V/ns
x	x	1	0	x	x	x	x		Slow	2.7	4.5	V/ns
x	x	1	1	x	x	x	x		Reserved			
0	0	x	x	x	x	x	x	Reserved	Reserved			
0	1	x	x	x	x	x	x		Reserved			
1	0	x	x	x	x	x	x		Reserved			
1	1	x	x	x	x	x	x		Reserved			

1. RW0E[5:0] will be sticky, cleared by power cycle not reset.
2. Slew Rate Control encodings of Moderate and Fast apply to all driver strength settings. The base range values specified in Table 112 are applicable for only Ron = RZQ/24, VDD = 1.1 V, and 25 °C. Slew rates will be less for other Ron values. The Output slew rate is verified by design and characterization, and may not be subject to production test.
3. Slew Rate Control encodings of Moderate, Fast and Slow apply to all driver strength settings. The base range values specified in Table 112 are applicable for only Ron = RZQ/24, VDD = 1.1 V, and 25 °C. Slew rates will be less for other Ron values. The Output slew rate is verified by design and characterization, and may not be subject to production test

8.11.2 RW0F - BCK, BCOM and BCS Output Slew Rate Control Word

Table 113 — RW0F - BCK, BCOM and BCS Output Slew Rate Control Word[1]

Setting								Definition	Encoding	Range		Units
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0			Min	Max	
x	x	x	x	x	x	0	0	BCOM[2:0], BCS_n Single Ended Slew Rate setting [2]	Moderate	3.7	6.7	V/ns
x	x	x	x	x	x	0	1		Fast	5.2	9.2	V/ns
x	x	x	x	x	x	1	0		Slow	2.5	4.3	V/ns
x	x	x	x	x	x	1	1		Reserved			
x	x	x	x	0	0	x	x	BCK_t / BCK_c Differential Slew Rate Setting [3]	Moderate	12	20	V/ns
x	x	x	x	0	1	x	x		Fast	14	27	V/ns
x	x	x	x	1	0	x	x		Reserved			
x	x	x	x	1	1	x	x		Reserved			
x	x	0	0	x	x	x	x	Reserved	Reserved			
x	x	0	1	x	x	x	x		Reserved			
x	x	1	0	x	x	x	x		Reserved			
x	x	1	1	x	x	x	x		Reserved			
0	0	x	x	x	x	x	x	Reserved	Reserved			
0	1	x	x	x	x	x	x		Reserved			
1	0	x	x	x	x	x	x		Reserved			
1	1	x	x	x	x	x	x		Reserved			

1. RW0F[3:0] will be sticky, cleared by power cycle not reset.
2. Slew Rate Control encodings of Moderate, Fast and Slow apply to all driver strength settings. The base range values specified in Table 113 are applicable for only Ron = RZQ/17, VDD = 1.1 V, and 25 °C. Slew rates will be less for other Ron values. The Output slew rate is verified by design and characterization, and may not be subject to production test.
3. Slew Rate Control encodings of Moderate and Fast apply to all driver strength settings. The base range values specified in Table 113 are applicable for only Ron = RZQ/24, VDD = 1.1 V, and 25 °C. Slew rates will be less for other Ron values. The Output slew rate is verified by design and characterization, and may not be subject to production test.

8.12 Input Bus Termination Strengths

8.12.1 RW10 - IBT Global Control Word

Table 114 — RW10: IBT Global Control Word

Setting								Definition[1]	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	DCA[6:0]_[B:A] and DPAR_[B:A] Input Bus Termination[2]	60 Ω
x	x	x	x	x	x	0	1		TBD Ω
x	x	x	x	x	x	1	0		TBD Ω
x	x	x	x	x	x	1	1		OFF[3]
x	x	x	x	0	0	x	x	DCS[1:0]_[B:A]_n Input Bus[2] Termination	60 Ω
x	x	x	x	0	1	x	x		TBD Ω
x	x	x	x	1	0	x	x		TBD Ω
x	x	x	x	1	1	x	x		OFF[3]
x	x	0	0	x	x	x	x	DCK Input Bus Termination[2]	60 Ω
x	x	0	1	x	x	x	x		TBD Ω
x	x	1	0	x	x	x	x		TBD Ω
x	x	1	1	x	x	x	x		OFF[3]
0	0	x	x	x	x	x	x	DERROR_IN_[B:A]_n Input Bus Termination[2]	60 Ω
0	1	x	x	x	x	x	x		TBD Ω
1	0	x	x	x	x	x	x		TBD Ω
1	1	x	x	x	x	x	x		OFF[3]

1. These are target IBT values. Acceptable actual values are determined based on tolerances defined in electrical section.
2. RW10[7:0] will be sticky, cleared by power cycle not Reset.
3. Not intended for normal operation. For normal operation, Input Bus Termination is always enabled.

8.13 Timing Control Words

8.13.1 RW11 - Command Latency Adder Configuration Control Word

Table 115 — RW11: Command Latency Adder Configuration Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Latency adder nLadd to all DRAM commands[1]	0 nCK latency adder
x	x	x	x	0	0	0	1		1 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	0	0	1	0		2 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	0	0	1	1		3 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	0	1	0	0		4 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	0	1	0	1		Reserved for 5 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	0	1	1	0		Reserved for 6 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	0	1	1	1		Reserved for 7 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	1	0	0	0		Reserved for 8 nCK[2] latency adder to Qn[3], Bn[4]
x	x	x	x	1	0	0	1		Reserved
x	x	x	x	.....					Reserved
x	x	x	x	1	1	1	1		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW11[3:0] will be sticky, cleared by power cycle not Reset.
2. The correct frequency range has to be programmed in RW05 before any changes to RW11 from the power-on default are allowed
3. Qn = QxCA[13:0]. QxCS[1:0]_n.
4. Bn = BCOM[2:0]. BCS_n.

8.13.2 RW12 - QACK Output Delay Control Word

Table 116 — RW12: QACK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QACK_t/ QACK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64)* t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACK_t/QACK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW12[7] = 1.
2. RW12[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW12[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.3 RW13 - QBCK Output Delay Control Word

Table 117 — RW13: QBCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QBCK_t/ QBCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QBCK_t/QBCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW13[7] = 1.
2. RW13[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW13[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.4 RW14 - QCCK Output Delay Control Word

Table 118 — RW14: QCCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for QCCK_t/ QCCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QCCK_t/QCCK_c [2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW14[7] = 1.
2. RW14[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW14[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.5 RW15 - QDCK Output Delay Control Word

Table 119 — RW15: QDCK Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for QDCK_t/ QDCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QDCK_t/QDCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW15[7] = 1.
2. RW15[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW15[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.6 RW17 - QACS0_n Output Delay Control Word

Table 120 — RW17: QACS0_n Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for QACS0_n [1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Full cycle delay[1]	Disabled
x	1	x	x	x	x	x	x		Enabled adds 1tCK additional delay to OP[5:0]
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACS0_n [2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW17[7] = 1.
2. RW17[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW17[6:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.7 RW18 - QACS1_n Output Delay Control Word

Table 121 — RW18: QACS1_n Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for QACS1_n [1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Full cycle delay[1]	Disabled
x	1	x	x	x	x	x	x		Enabled adds 1tCK additional delay to OP[5:0]
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACS1_n[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW18[7] = 1.
2. RW18[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW18[6:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.8 RW19 - QBCS0_n Output Delay Control Word

Table 122 — RW19: QBCS0_n Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for QBCS0_n [1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Full cycle delay[1]	Disabled
x	1	x	x	x	x	x	x		Enabled adds 1tCK additional delay to OP[5:0]
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QBCS0_n output signals[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW19[7] = 1.
2. RW19[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW19[6:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.9 RW1A - QBCS1_n Output Delay Control Word

Table 123 — RW1A: QBCS1_n Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for QBCS1_n [1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Full cycle delay[1]	Disabled
x	1	x	x	x	x	x	x		Enabled adds 1tCK additional delay to OP[5:0]
0	x	x	x	x	x	x	x	Output Delay Feature Enable for	(Default) Feature Disabled
1	x	x	x	x	x	x	x	QBCS1_n output signals[2]	Feature Enabled[3]

1. These control bits do not have any effect unless RW1A[7] = 1.
2. RW1A[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW1A[6:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.10 RW1B - QACA Output Delay Control Word

Table 124 — RW1B: QACA Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for QACA	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1	Output Signals[1,2]	Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Full cycle delay[1]	Disabled
x	1	x	x	x	x	x	x		Enabled adds 1tCK additional delay to OP[5:0]
0	x	x	x	x	x	x	x	Output Delay Feature Enable for	(Default) Feature Disabled
1	x	x	x	x	x	x	x	QACA[2]	Feature Enabled[3]

1. These control bits do not have any effect unless RW1B[7] = 1
2. RW1B[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW1B[6:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.11 RW1C - QBCA Output Delay Control Word

Table 125 — RW1C: QBCA Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for QBCA Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Full cycle delay[1]	Disabled
x	1	x	x	x	x	x	x		Enabled adds 1tCK additional delay to OP[5:0]
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QBCA[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW1C[7] = 1
2. RW1C[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW1C[6:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.12 RW1D - BCS_n and BCOM[2:0] Output Delay Control Word

Table 126 — RW1D: BCS_n and BCOM[2:0] Output Delay Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	0	0	0	0	0	0	Output Delay Control for BCS_n and BCOM[2:0] Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Full cycle delay[1]	Disabled
x	1	x	x	x	x	x	x		Enabled adds 1tCK additional delay to OP[5:0]
0	x	x	x	x	x	x	x	Output Delay Feature Enable for BCS_n and BCOM[2:0][2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW1D[7] = 1.
2. RW1D[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW1D[6:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.13.13 RW1E - BCK Output Delay Control Word

Table 127 — RW1E: BCK Output Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Output Delay Control for BCK_t/BCK_c Output Signals[1,2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64)* t_{CK}
x	x	...							...
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for BCK_t/BCK_c[2]	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits do not have any effect unless RW1E[7] = 1.
2. RW1E[7:0] will be sticky, cleared by power cycle not Reset.
3. When feature is enabled the delay settings in RW1E[5:0] require a time of t_{ODU} for the delay to become stable on the outputs.

8.14 RW[24:20] - Error Log Register

Control word locations RW[24:20] function as a 32-bit error log register. Upon occurrence of a CA parity error, the device logs the following sampled command and address bits in the Error Log Register.

Table 128 — RW[24:20]: Error Log Register Encoding for DDR Mode[1,2]

Control Word	Setting (OP[7:0])							
RW20	CA13 2nd UI	CA12 2nd UI	CA11 2nd UI	CA10 2nd UI	CA9 2nd UI	CA8 2nd UI	CA7 2nd UI	DPAR 2nd UI
RW21	CA6 1st UI	CA5 1st UI	CA4 1st UI	CA3 1st UI	CA2 1st UI	CA1 1st UI	CA0 1st UI	DPAR 1st UI
RW22	CA13 4th UI	CA12 4th UI	CA11 4th UI	CA10 4th UI	CA9 4th UI	CA8 4th UI	CA7 4th UI	DPAR 4th UI
RW23	CA6 3rd UI	CA5 3rd UI	CA4 3rd UI	CA3 3rd UI	CA2 3rd UI	CA1 3rd UI	CA0 3rd UI	DPAR 3rd UI
RW24	> 1 Error[3,4]	CA Parity Error Status[3,5]	Reserved	CS1_n 1st cycle	CS0_n 1st cycle	CS1_n 2nd cycle	CS0_n 2nd Cycle	Reserved

1. The encoding shown in this table is valid when the DCA interface is operating in DDR mode (RW00[0] = 1).
2. When command and address bits are logged in the Error Log Register upon occurrence of a CA parity error, all bits in RW20 to RW24 are updated with the corresponding values from the offending command. Four consecutive UI's are always captured because, in some cases, it is not possible to distinguish between 1UI and 2UI commands due to the parity error. RW20 and RW21 always contain the start of the command (qualified by DCS_n assertion) regardless of the UI or cycle within the command where the parity error has been detected.
3. This bit will get reset to '0' when "Clear CA Parity Error" command is sent. The Clear CA Parity Error command does not affect any bits in RW[23:20] and RW24[4:1].
4. With RW01[7] = 1 and RW01[6] = 1, the device will forward commands and re-enable parity after the ALERT_n pulse. The CA Parity Error Status bit will remain set. If a subsequent parity error is detected, the device will re-enter the parity error state and set the '> 1 Error' bit.
5. The DDR5RCD01 will set this bit upon occurrence of a CA parity error.

Table 129 — RW[24:20]: Error Log Register Encoding for SDR Mode[1,2]

Control Word	Setting (OP[7:0])							
RW20	CA13 2nd Cycle	CA12 2nd Cycle	CA11 2nd Cycle	CA10 2nd Cycle	CA9 2nd Cycle	CA8 2nd Cycle	CA7 2nd Cycle	DPAR 2nd Cycle
RW21	CA6 1st Cycle	CA5 1st Cycle	CA4 1st Cycle	CA3 1st Cycle	CA2 1st Cycle	CA1 1st Cycle	CA0 1st Cycle	DPAR 1st Cycle
RW22	CA13 4th Cycle	CA12 4th Cycle	CA11 4th Cycle	CA10 4th Cycle	CA9 4th Cycle	CA8 4th Cycle	CA7 4th Cycle	DPAR 4th Cycle
RW23	CA6 3rd Cycle	CA5 3rd Cycle	CA4 3rd Cycle	CA3 3rd Cycle	CA2 3rd Cycle	CA1 3rd Cycle	CA0 3rd Cycle	DPAR 3rd Cycle
RW24	> 1 Error[3,4]	CA Parity Error Status[3,5]	Reserved	CS1_n 1st cycle	CS0_n 1st cycle	CS1_n 3rd cycle	CS0_n 3rd Cycle	Reserved

1. The encoding shown in this table is valid when the DCA interface is operating in SDR mode (RW00[0] = 0).
2. When command and address bits are logged in the Error Log Register upon occurrence of a CA parity error, all bits in RW20 to RW24 are updated with the corresponding values from the offending command. Four consecutive cycles are always captured because, in some cases, it is not possible to distinguish between 1UI and 2UI commands due to the parity error. RW20 and RW21 always contain the start of the command (qualified by DCS_n assertion) regardless of the cycle within the command where the parity error has been detected.
3. This bit will get reset to '0' when "Clear CA Parity Error" command is sent. The Clear CA Parity Error command does not affect any bits in RW[23:20] and RW24[4:1].
4. With RW01[7] = 1 and RW01[6] = 1, the device will forward commands and re-enable parity after the ALERT_n pulse. The CA Parity Error Status bit will remain set. If a subsequent parity error is detected, the device will re-enter the parity error state and set the '> 1 Error' bit.
5. The DDR5RCD01 will set this bit upon occurrence of a CA parity error.

8.15 SidebandBus

8.15.1 RW25 - SidebandBus Global Control Word

Table 130 — RW25: SidebandBus Global Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	SidebandBus Interface Disabled	SidebandBus interface is enabled
x	x	x	x	x	x	x	1		SidebandBus interface is disabled. DDR5RCD01 will not claim or acknowledge any access to its SidebandBus address space.
x	x	x	x	x	x	0	x	Vendor Specific[2]	Vendor Specific.
x	x	x	x	x	x	1	x		Vendor Specific.
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Vendor Specific[2]	Vendor Specific
x	x	x	1	x	x	x	x		Vendor Specific
x	x	0	x	x	x	x	x	SidebandBus Mode[3]	I^2C (Max speed of 1 MHz) Enabled
x	x	1	x	x	x	x	x		I3C Basic (Max speed of 12.5 MHz) Enabled
x	0	x	x	x	x	x	x	Vendor Specific[2]	Vendor Specific
x	1	x	x	x	x	x	x		Vendor Specific
0	x	x	x	x	x	x	x	Vendor Specific[2]	Vendor Specific
1	x	x	x	x	x	x	x		Vendor Specific

1. The write (or update) transaction to this register must be followed by STOP operation to allow the DDR5RCD01 device to update the setting.
2. This register is vendor specific and must be written to '0' by the host whenever RW25 is accessed for Writes.
3. This is a Read-Only Status register. This is a Sticky register (not cleared by DRST_n). This register is automatically updated to '1' or to '0', respectively, when SETAASA CCC or RSTDAA CCC is registered by the DDR5RCD01 device. This register is automatically cleared to '0' when the Timeout Reset condition described in Section 7.6, "I2C and I3C Basic Reset" is detected.

8.16 RX Loopback

8.16.1 RW26 - RX Loopback Global Control Word

Table 131 — RW26: RX Loopback Global Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	RCD RX Loopback Port Selection	Loopback Disabled[1]
x	x	x	x	x	0	0	1		Internal RCD CH_A Port[2]
x	x	x	x	x	0	1	0		Internal RCD CH_B Port[2]
x	x	x	x	x	0	1	1		External CH_A Port[3]
x	x	x	x	x	1	0	0		External CH_B Port[3]
x	x	x	x	x	1	0	1		Reserved
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved
x	x	0	0	0	x	x	x	Internal RCD bit selection[4]	DCA0
x	x	0	0	1	x	x	x		DCA1
x	x	0	1	0	x	x	x		DCA2
x	x	0	1	1	x	x	x		DCA3
x	x	1	0	0	x	x	x		DCA4
x	x	1	0	1	x	x	x		DCA5
x	x	1	1	0	x	x	x		DCA6
x	x	1	1	1	x	x	x		DPAR
x	0	x	x	x	x	x	x	External Loopback Data Rate[5,6]	Incoming and outgoing signals are 1/2 rate
x	1	x	x	x	x	x	x		Incoming and outgoing signals are 1/4 rate
0	x	x	x	x	x	x	x	Internal Loopback Select Phase[4]	Loopback Select Phase A
1	x	x	x	x	x	x	x		Loopback Select Phase B

1. Loopback circuitry is disabled.
2. Internal Port contains input Clock and CA. Fixed at 1/2 rate.
3. External Port contains input Strobe and Data. A waiting time $t_{Ext_LB_Entry}$ applies when External Loopback is enabled in RW26[2:0].
4. This field only applies when Internal RCD CH_A or Internal RCD CH_B ports are selected in RW26[2:0].
5. This bit only applies when External CH_A or External CH_B ports are selected in RW26[2:0].
6. The host must ensure this bit's setting is consistent with the Loopback signal rate received at the DLBD_N/DLBS_N pins selected in RW26[2:0]. The DDR5RCD01 device is allowed to use the information contained in this bit to configure its External Loopback circuitry.

8.16.2 RW27 - Loop-back I/O Global Control Word

Table 132 — RW27: Loop-back I/O Global Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	RX DLBS Termination	60 Ω
x	x	x	x	x	x	0	1		80 Ω
x	x	x	x	x	x	1	0		40 Ω
x	x	x	x	x	x	1	1		OFF
x	x	x	x	0	0	x	x	RX DLBD Termination	60 Ω
x	x	x	x	0	1	x	x		80 Ω
x	x	x	x	1	0	x	x		40 Ω
x	x	x	x	1	1	x	x		OFF
x	x	0	0	x	x	x	x	TX QLBS and QLBD Drive Strength	RZQ/5 (48 Ω)
x	x	0	1	x	x	x	x		RZQ/7 (34 Ω)
x	x	1	0	x	x	x	x		Reserved
x	x	1	1	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

8.17 SidebandBus Error Status

8.17.1 RW28: I²C & I3C Basic Error Status Global Word

Table 133 — RW28: I²C & I3C Basic Error Status Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Error in Parity Check[1,2,3]	No PARITY error has been detected
x	x	x	x	x	x	x	1		PARITY error has been detected[4]
x	x	x	x	x	x	0	x	Error in Packet Error Code Check[1,2,5]	No PEC error has been detected
x	x	x	x	x	x	1	x		PEC error has been detected[6]
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Device Event In-Band Interrupt Status[1]	No Pending IBI[7]
1	x	x	x	x	x	x	x		Pending IBI[8]

1. This is a Read-Only Status bit. This is a Sticky register (not cleared by DRST_n).
2. This register is automatically cleared to '0' when the Timeout Reset condition described in Section 7.8, "I2C Bus Error Handling" is detected.
3. This status bit only applies when I3C Basic mode is enabled or for CCC supported in I²C mode, provided that the Parity Checking function is not disabled.
4. The RCD device detected a PARITY error in one or more bytes received.
5. This status bit only applies when I3C Basic mode is enabled.
6. The RCD device detected a PEC error for one or more data packets received. When a PEC error is detected in I²C mode, this status field will not be updated.
7. The IBI status bit gets cleared to '0' when the RCD device processes a complete IBI operation (including uninterrupted IBI payload). This status bit also gets cleared when RW28[0] and RW28[1] become '00' after a Clear command in RW29.
8. The IBI status bit gets set to '1' when the RCD sets RW28[0] or RW28[1] to '1' after detecting a Parity Error or a PEC Error.

8.17.2 RW29: I²C & I3C Basic Clear Error Status Global Word

Table 134 — RW29: I²C & I3C Basic Clear Error Status Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Clear Parity Error Status[1]	No effect.
x	x	x	x	x	x	x	1		Clear RW28[0].
x	x	x	x	x	x	0	x	Clear Packet Error Status[1]	No effect.
x	x	x	x	x	x	1	x		Clear RW28[1].
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. This is a Write-1 Only register bit, and it self clears after the target status register has been cleared.

8.17.3 RW2A: Vendor Specific Global Word

Table 135 — RW2A: Vendor Specific Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Reserved	Reserved
x	x	x	x	x	x	x	1		Reserved
x	x	x	x	0	0	0	x	Vendor Specific	Vendor Specific
x	x	x	x	0	0	1	x		Vendor Specific
x	x	x	x	0	1	0	x		Vendor Specific
x	x	x	x	0	1	1	x		Vendor Specific
x	x	x	x	1	0	0	x		Vendor Specific
x	x	x	x	1	0	1	x		Vendor Specific
x	x	x	x	1	1	0	x		Vendor Specific
x	x	x	x	1	1	1	x		Vendor Specific
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

8.18 DFE Control Words

8.18.1 RW30 - DFE_Vref Range Limit Global Status Word

Table 136 — RW30: DFE_Vref Range Limit Global Status Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	DFE_Vref Configuration Limit[1,2]	Applies to 8 LSB portion of DFE Vref control in PG[2]RW[62,66,6A,6E,72,76,7A,7E] (Maximum Setting Supported by Device)
0	0	0	0	0	0	0	1		
0	0	0	0	0	0	1	0		
...									
1	1	1	1	1	1	0	1		
1	1	1	1	1	1	1	0		
1	1	1	1	1	1	1	1		

1. Read only register. Returns positive limit. DFE_Vref must have a symmetrical range.
2. This is a global status word. The status code can only be accessed from CH_A.

8.18.2 RW31 - DFE Configuration Control Word

Table 137 — RW31: DFE Configuration Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DFE Feature Enable Control[2]	(Default) DFE and gain features disabled
x	x	x	x	x	x	x	1		DFE and gain features enabled
x	x	x	x	x	x	0	x	DFE_Vref Enable[3]	DFE_Vref Circuitry Disabled
x	x	x	x	x	x	1	x		DFE_Vref Circuitry Enabled
x	x	x	x	x	0	x	x	ERROR Counter Enable[4]	All Error Counters Disabled
x	x	x	x	x	1	x	x		All Error Counters Enabled
x	x	x	x	0	x	x	x	RW Control Word Writes Broadcast	RW Write to selected DCAn or DPAR[5]
x	x	x	x	1	x	x	x		RW Writes Broadcast to DCA[6:0] and DPAR[6]
x	x	x	0	x	x	x	x	Tap 1 Enable[7]	(Default) Tap 1 disabled
x	x	x	1	x	x	x	x		Tap 1 enabled
x	x	0	x	x	x	x	x	Tap 2 Enable[7]	(Default) Tap 2 disabled
x	x	1	x	x	x	x	x		Tap 2 enabled
x	0	x	x	x	x	x	x	Tap 3 Enable[7]	(Default) Tap 3 disabled
x	1	x	x	x	x	x	x		Tap 3 enabled
0	x	x	x	x	x	x	x	Tap 4 Enable[7]	(Default) Tap 4 disabled
1	x	x	x	x	x	x	x		Tap 4 enabled

1. RW31[7:0] will be sticky, cleared by power cycle not Reset.
2. This control bit enables DFE circuitry in the RCD.
3. To save power, the host can keep DFE_VREF circuitry disabled when not in use.
4. Error Counter Reset is located RW04. CMD 11 for CH_A and CMD 12 for CH_B.
5. When RW31[3] = 0, RW Writes to PG[2:0] are written to a specific receiver selected in MRW command.
6. When RW31[3] = 1, RW Writes to any of the DCn Gain, Tap, and DFE_Vref registers in PG[2:0] are written to all DCA receivers DCA[6:0] and DPAR.
7. Enables Tap in DPAR and DCA[6:0] receivers.

8.18.3 RW32 - DPAR and DCA[6:0] DFE Training Mode Control Word

Table 138 — RW32 DPAR and DCA[6:0] DFE Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Global DFE Training Mode Enable [1]	DFE Training Mode disabled
x	x	x	x	x	x	x	1		DFE Training Mode enabled[2,3]
x	x	x	x	x	0	0	x	Training Source	Monitor
x	x	x	x	x	0	1	x		Monitor XOR Slicer Output
x	x	x	x	x	1	0	x		LFSR XOR
x	x	x	x	x	1	1	x		Reserved
x	x	0	0	0	x	x	x	DCn DFE pin selection[4]	DCA0
x	x	0	0	1	x	x	x		DCA1
x	x	0	1	0	x	x	x		DCA2
x	x	0	1	1	x	x	x		DCA3
x	x	1	0	0	x	x	x		DCA4
x	x	1	0	1	x	x	x		DCA5
x	x	1	1	0	x	x	x		DCA6
x	x	1	1	1	x	x	x		DPAR
x	0	x	x	x	x	x	x	RW In-Band Update Feature Enable[5]	(Default) Feature disabled.[6]
x	1	x	x	x	x	x	x		Feature enabled.[7]
0	x	x	x	x	x	x	x	Exit From RW In-Band Updated Mode[5]	No action.
1	x	x	x	x	x	x	x		(Default) Take the RCD out from RWUPD state.[8]

1. RW32[5:3] determines the target receiver for DFE training.
2. DFE circuits are configured into training mode for selected pin RW32[5:3].
3. Vref generator circuits are configured so that a DFE training reference voltage (DFE_Vref) is controlled by PG[2]RW[62, 66, 6A, 6E, 72, 76, 7A, 7E].
4. Logic in DDR5RCD01 device ensures that only one DCAn receiver is configured in training mode at any given time.
5. Default state of RW32[6] is 0, and the default state of RW32[7] is 1.
6. DCS1_n ignored during DFE training.
7. DCS1_n Low pulse received in idle state of DFE training triggers entry into RW Update Mode.
8. Writing a 1 in this bit location takes the RCD out from RWUPD state. The RCD hardware clears this register bit upon entry to RWUPD mode when DCS1_n Low pulse is received. Therefore, a setting RW32[7] = 1 indicates the channel is not in RWUPD mode.

8.18.4 RW33 - Additional Filtering for DFE Training Mode Control Word

Table 139 — RW33 Additional Filtering for DFE Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	UI Filtering Enable	UI Filter Disabled
x	x	x	x	x	x	0	1		Enable Per UI Filtering according to OP[4:2]
x	x	x	x	x	x	1	0		Enable Even UI Filtering[1]
x	x	x	x	x	x	1	1		Enable Odd UI Filtering[1]
x	x	x	0	0	0	x	x	Per-UI filtering[2]	UI 0
x	x	x	0	0	1	x	x		UI 1
x	x	x	0	1	0	x	x		UI 2
x	x	x	0	1	1	x	x		UI 3
x	x	x	1	0	0	x	x		UI 4
x	x	x	1	0	1	x	x		UI 5
x	x	x	1	1	0	x	x		UI 6
x	x	x	1	1	1	x	x		UI 7
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. When selected OP[4:2] is ignored by the DDR5RCD01.
2. UI filtering applies to the results in the error counter.

8.18.5 RW34 - LFSR DFE Training Mode Control Word

Table 140 — RW34 LFSR DFE Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DFE Training Accelerator	Stop DFE Training Accelerator
x	x	x	x	x	x	x	1		Start DFE Training Accelerator
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	0	0	x	x	Select Inner Loop Parameter	Select Inner Loop Parameter - NULL[1]
x	x	x	x	0	1	x	x		Select Inner Loop Parameter - DFE_Vref
x	x	x	x	1	0	x	x		Select Inner Loop Parameter - VrefCA
x	x	x	x	1	1	x	x		Reserved
x	0	0	0	x	x	x	x	Select Outer Loop Parameter	Select Outer Loop Parameter - NULL
x	0	0	1	x	x	x	x		Select Outer Loop Parameter - Tap 1
x	0	1	0	x	x	x	x		Select Outer Loop Parameter - Tap 2
x	0	1	1	x	x	x	x		Select Outer Loop Parameter - Tap 3
x	1	0	0	x	x	x	x		Select Outer Loop Parameter - Tap 4
x	1	0	1	x	x	x	x		Select Outer Loop Parameter - UI
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. NULL parameter choice means no change. NULL parameter loop can have multiple iterations.

8.18.6 RW35 - LFSR State for DFE Training Mode Control Word

Table 141 — RW35 LFSR State for DFE Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	LFSR State (Read Only)[1]	LFSR State = 0x00*
0	0	0	0	0	0	0	1		LFSR State = 0x01
0	0	0	0	0	0	1	0		LFSR State = 0x02
...									...
1	1	1	1	1	1	0	0		LFSR State = 0xFC
1	1	1	1	1	1	0	1		LFSR State = 0xFD
1	1	1	1	1	1	1	0		LFSR State= 0xFE
1	1	1	1	1	1	1	1		LFSR State = 0xFF

1. The LFSR State is the internal state of the Galois LFSR. This read only register is used for debug, and tracks the state of the LFSR associated with the selected DCA signal for training.

8.18.7 RW36 - DFETM Inner Loop Start Value Control Word

Table 142 — RW36 DFETM Inner Loop Start Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Start Value[1,2]	Inner Loop Start Value = 0x00
0	0	0	0	0	0	0	1		Inner Loop Start Value = 0x01
0	0	0	0	0	0	1	0		Inner Loop Start Value = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Start Value = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Start Value = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Start Value = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Start Value = 0xFF

1. Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.
2. Even though the tap setting parameter registers are defined as signed magnitude fields, this start value is a two's complement encoding. The RCD must convert this value to a signed magnitude format prior to updating the DFE_Vref when DFE_Vref is chosen for the Inner Loop Parameter.

8.18.8 RW37 - DFETM Outer Loop Start Value Control Word

Table 143 — RW37 DFETM Outer Loop Start Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Start Value[1,2]	Outer Loop Start Value = 0x00
x	0	0	0	0	0	0	1		Outer Loop Start Value = 0x01
x	0	0	0	0	0	1	0		Outer Loop Start Value = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Start Value = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Start Value = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Start Value = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Start Value = 0x7F
0	x	x	x	x	x	x	x	RW[36] Inner Loop Start Value[3,4]	Inner Loop Start Value[8] = 0
1	x	x	x	x	x	x	x		Inner Loop Start Value[8] = 1

1. Depending on the Outer Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Outer Loop Parameter.
2. Even though the tap setting parameter registers are defined as signed magnitude fields, this start value is a two's complement encoding. The RCD must convert this value to a signed magnitude format prior to updating the tap setting when Tap1, Tap2, Tap3, or Tap4 is chosen for the Outer Loop Parameter.
3. Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.
4. Even though the tap setting parameter registers are defined as signed magnitude fields, this start value is a two's complement encoding. The RCD must convert this value to a signed magnitude format prior to updating the DFE_Vref when DFE_Vref is chosen for the Inner Loop Parameter.

8.18.9 RW38 - DFETM Inner Loop Current Value Control Word

Table 144 — RW38 DFETM Inner Loop Current Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Current Value (Read Only)	Inner Loop Current Value = 0x00
0	0	0	0	0	0	0	1		Inner Loop Current Value = 0x01
0	0	0	0	0	0	1	0		Inner Loop Current Value = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Current Value = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Current Value = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Current Value = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Current Value = 0xFF

8.18.10 RW39 - DFETM Outer Loop Current Value Control Word

Table 145 — RW39 DFETM Outer Loop Current Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Current Value (Read Only)	Outer Loop Current Value = 0x00
x	0	0	0	0	0	0	1		Outer Loop Current Value = 0x01
x	0	0	0	0	0	1	0		Outer Loop Current Value = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Current Value = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Current Value = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Current Value = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Current Value = 0x7F
0	x	x	x	x	x	x	x	RW38[8] Inner Loop Current Value (Read Only)	Inner Loop Current Value[8] = 0
1	x	x	x	x	x	x	x		Inner Loop Current Value[8] = 1

8.18.11 RW3A - DFETM Inner and Outer Loop Step Size Control Word

Table 146 — RW3A DFETM Inner and Outer Loop Step Size Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Inner Loop Step Size[1]	Inner Loop Step Size = 1
x	x	x	x	0	0	0	1		Inner Loop Step Size = 2
x	x	x	x	0	0	1	0		Inner Loop Step Size = 3
x	x	x	x	0	0	1	1		Inner Loop Step Size = 4
x	x	x	x	0	1	0	0		Inner Loop Step Size = 5
x	x	x	x	0	1	0	1		Inner Loop Step Size = 6
x	x	x	x	0	1	1	0		Inner Loop Step Size = 7
x	x	x	x	0	1	1	1		Inner Loop Step Size = 8
x	x	x	x	1	0	0	0		Inner Loop Step Size = 9
x	x	x	x	1	0	0	1		Inner Loop Step Size = 10
x	x	x	x	1	0	1	0		Inner Loop Step Size = 11
x	x	x	x	1	0	1	1		Inner Loop Step Size = 12
x	x	x	x	1	1	0	0		Inner Loop Step Size = 13
x	x	x	x	1	1	0	1		Inner Loop Step Size = 14
x	x	x	x	1	1	1	0		Inner Loop Step Size = 15
x	x	x	x	1	1	1	1		Inner Loop Step Size = 16
0	0	0	0	x	x	x	x	Outer Loop Step Size[1]	Outer Loop Step Size = 1
0	0	0	1	x	x	x	x		Outer Loop Step Size = 2
0	0	1	0	x	x	x	x		Outer Loop Step Size = 3
0	0	1	1	x	x	x	x		Outer Loop Step Size = 4
0	1	0	0	x	x	x	x		Outer Loop Step Size = 5
0	1	0	1	x	x	x	x		Outer Loop Step Size = 6
0	1	1	0	x	x	x	x		Outer Loop Step Size = 7
0	1	1	1	x	x	x	x		Outer Loop Step Size = 8
1	0	0	0	x	x	x	x		Outer Loop Step Size = 9
1	0	0	1	x	x	x	x		Outer Loop Step Size = 10
1	0	1	0	x	x	x	x		Outer Loop Step Size = 11
1	0	1	1	x	x	x	x		Outer Loop Step Size = 12
1	1	0	0	x	x	x	x		Outer Loop Step Size = 13
1	1	0	1	x	x	x	x		Outer Loop Step Size = 14
1	1	1	0	x	x	x	x		Outer Loop Step Size = 15
1	1	1	1	x	x	x	x		Outer Loop Step Size = 16

1. The step size is always positive, and thus the increment is always from lowest to highest value in the sweep. Note that the actual field setting indicates the Step Size – 1. The RCD must account for this in the increment logic.

8.18.12 RW3B - DFETM Inner Loop Number of Increments Control Word

Table 147 — RW3B DFETM Inner Loop Number of Increments Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Number of Increments[1]	Inner Loop Number of Increments = 0x00
0	0	0	0	0	0	0	1		Inner Loop Number of Increments = 0x01
0	0	0	0	0	0	1	0		Inner Loop Number of Increments = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Number of Increments = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Number of Increments = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Number of Increments = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Number of Increments = 0xFF

1. Depending on the Inner Loop Parameter Selection and the Inner Loop Step Size, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter. When the Number of Increments = 0x00, the Start Value will be applied for a single iteration of the loop.

8.18.13 RW3C - DFETM Outer Loop Number of Increments Control Word

Table 148 — RW3C DFETM Outer Loop Number of Increments Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Number of Increments[1]	Outer Loop Number of Increments = 0x00
x	0	0	0	0	0	0	1		Outer Loop Number of Increments = 0x01
x	0	0	0	0	0	1	0		Outer Loop Number of Increments = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Number of Increments = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Number of Increments = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Number of Increments = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Number of Increments = 0x7F
0	x	x	x	x	x	x	x	RW3B[8] Inner Loop Number of Increments[2]	Inner Loop Number of Increments = 0
1	x	x	x	x	x	x	x		Inner Loop Number of Increments = 1

1. Depending on the Outer Loop Parameter Selection and the Outer Loop Step Size, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Outer Loop Parameter. When the Number of Increments = 0x00, the Start Value will be applied for a single iteration of the loop.
2. Depending on the Inner Loop Parameter Selection and the Inner Loop Step Size, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter. When the Number of Increments = 0x00, the Start Value will be applied for a single iteration of the loop.

8.18.14 RW3D - DFETM Inner Loop Current Increment Control Word

Table 149 — RW3D DFETM Inner Loop Current Increment Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Current Increment (Read Only)	Inner Loop Current Increment = 0x00
0	0	0	0	0	0	0	1		Inner Loop Current Increment = 0x01
0	0	0	0	0	0	1	0		Inner Loop Current Increment = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Current Increment = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Current Increment = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Current Increment = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Current Increment = 0xFF

8.18.15 RW3E - DFETM Outer Loop Current Increment Control Word

Table 150 — RW3E DFETM Outer Loop Current Increment Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Current Increment (Read Only)	Outer Loop Current Increment = 0x00
x	0	0	0	0	0	0	1		Outer Loop Current Increment = 0x01
x	0	0	0	0	0	1	0		Outer Loop Current Increment = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Current Increment = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Current Increment = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Current Increment = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Current Increment = 0x7F
0	x	x	x	x	x	x	x	RW3E[8] Inner Loop Current Increment (Read Only)	Inner Loop Current Increment = 0
1	x	x	x	x	x	x	x		Inner Loop Current Increment = 1

8.18.16 RW3F - DFE Vref Range Selection Control Word

Table 151 — RW3F DFE Vref Range Selection Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DCA0	Positive
x	x	x	x	x	x	x	1		Negative
x	x	x	x	x	x	0	x	DCA1	Positive
x	x	x	x	x	x	1	x		Negative
x	x	x	x	x	0	x	x	DCA2	Positive
x	x	x	x	x	1	x	x		Negative
x	x	x	x	0	x	x	x	DCA3	Positive
x	x	x	x	1	x	x	x		Negative
x	x	x	0	x	x	x	x	DCA4	Positive
x	x	x	1	x	x	x	x		Negative
x	x	0	x	x	x	x	x	DCA5	Positive
x	x	1	x	x	x	x	x		Negative
x	0	x	x	x	x	x	x	DCA6	Positive
x	1	x	x	x	x	x	x		Negative
0	x	x	x	x	x	x	x	DPAR	Positive
1	x	x	x	x	x	x	x		Negative

1. RW3F selects the sign for DFE_Vref registers located in PG[2]RW[62, 66, 6A, 6E, 72, 76, 7A, 7E].

8.19 Vref Control Words

8.19.1 RW[47:40] - Internal VrefCA Control Word

Table 152 — RW[47:40]: Internal VrefCA Control Word[1,2]

Setting								Definition	Encoding VrefCA as% of V_{DD}[3]
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Internal VrefCA Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	1	0		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x				...					...
x	0	1	0	1	1	0	1		75% (Default)
x				...					...
x	1	1	0	0	0	0	1		49.0%
x	1	1	0	0	0	1	0		48.5%
x	1	1	0	0	0	1	1		48.0%
x	1	1	0	0	1	0	0		47.5%
x	1	1	0	0	1	0	1		47.0%
x	1	1	0	0	1	1	0		46.5%
x	1	1	0	0	1	1	1		46.0%
x	1	1	0	1	0	0	0		45.5%
x	1	1	0	1	0	0	1		45.0%
x	1	1	0	1	0	1	0		Reserved
x	1	1	0	1	0	1	1		Reserved
x				...					Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW[47:40] OP[6:0] will be sticky, cleared by power cycle not Reset.
2. Table 92 illustrates the assignment of each control word in the RW[47:40] group to the corresponding input pin it controls.
3. These are target VrefCA values. Acceptable actual values are determined based on tolerances defined in electrical section.

8.19.2 RW[49:48] - Internal VrefCS Control Word

Table 153 — RW[49:48]: Internal VrefCS Control Word[1,2]

Setting								Definition	Encoding VrefCS as% of V_{DD}[3]
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Internal VrefCS Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	1	0		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x	...								...
x	0	1	0	1	1	0	1		75% (Default)
x	...								...
x	1	1	0	0	0	0	1		49.0%
x	1	1	0	0	0	1	0		48.5%
x	1	1	0	0	0	1	1		48.0%
x	1	1	0	0	1	0	0		47.5%
x	1	1	0	0	1	0	1		47.0%
x	1	1	0	0	1	1	0		46.5%
x	1	1	0	0	1	1	1		46.0%
x	1	1	0	1	0	0	0		45.5%
x	1	1	0	1	0	0	1		45.0%
x	1	1	0	1	0	1	0		Reserved
x	1	1	0	1	0	1	1		Reserved
x	...								Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW[49:48] OP[6:0] will be sticky, cleared by power cycle not Reset.
2. Table 92 illustrates the assignment of each control word in the RW[49:48] group to the corresponding input pin it controls.
3. These are target VrefCS values. Acceptable actual values are determined based on tolerances defined in electrical section.

8.19.3 RW4A - DERROR_IN_n Vref Control Word

Table 154 — RW4A: DERROR_IN_n Vref Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DERROR_IN_n Vref Control	0.80 x V_{DD} (Default)
x	x	x	x	x	0	0	1		0.75 x V_{DD}
x	x	x	x	x	0	1	0		0.70 x V_{DD}
x	x	x	x	x	0	1	1		0.60 x V_{DD}
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		Reserved
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

8.19.4 RW4B - Loop-Back Vref Control Word

Table 155 — RW4B: Loop-Back Vref Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DLBS Vref Control	0.80 x V_{DD} (Default)
x	x	x	x	x	0	0	1		0.75 x V_{DD}
x	x	x	x	x	0	1	0		0.70 x V_{DD}
x	x	x	x	x	0	1	1		0.60 x V_{DD}
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		Reserved
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	DLBD Vref Control	0.80 x V_{DD} (Default)
x	0	0	1	x	x	x	x		0.75 x V_{DD}
x	0	1	0	x	x	x	x		0.70 x V_{DD}
x	0	1	1	x	x	x	x		0.60 x V_{DD}
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

8.20 Read and Paging Control Words

8.20.1 RW5E - CW Read Pointer Control Word

Table 156 — RW5E - CW Read Pointer Control Word

Read Pointer[1]							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MRA7[2]	MRA6	MRA5	MRA4	MRA3	MRA2	MRA1	MRA0

1. Points to the RCD Register Control Word to be read.
2. MRA7 will always be '0' for RCD Reads.

8.20.2 RW5F - CW Page Control Word

Table 157 — RW5F - CW Page Control Word

Page Control Register[1,2]							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0

1. Power on Default is OP[7:0] = 0. This 8-bit control field uses binary encoding and it can be programmed with settings 0x00 (for CW Page 0) through 0xFF (for CW Page 255).
2. The host is responsible to set the page register properly before issuing the MRW write to the DRAM scratch-pad register.

8.21 DFE Paged Control Words

8.21.1 PG[1:0]RW[60, 68, 70, 78] - DPAR and DCA[6:0] Receiver DFE Gain Offset

Table 158 — PG[1:0]RW[60, 68, 70, 78]: DPAR and DCA[6:0] Receiver DFE Gain Offset Adjustment[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Flat-band (DC) gain adjustment [2, 3,4,5,6]	Gain Adjustment = 0 dB (default)
x	x	x	x	x	0	0	1		Gain Adjustment = +6 dB
x	x	x	x	x	0	1	0		Gain Adjustment = +4 dB
x	x	x	x	x	0	1	1		Gain Adjustment = +2 dB
x	x	x	x	x	1	0	0		Gain Adjustment = 0 dB (same as default)
x	x	x	x	x	1	0	1		Gain Adjustment = -2 dB
x	x	x	x	x	1	1	0		Gain Adjustment = -4 dB
x	x	x	x	x	1	1	1		Gain Adjustment = -6 dB
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x		Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x		Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x		Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x		Reserved
1	x	x	x	x	x	x	x		Reserved

1. Table 93 and Table 94 illustrate the assignment of each control word in the PG[1:0]RW[60, 68, 70, 78] group to the corresponding input pin it controls.
2. Flat-band (DC) gain adjustment (up to the Nyquist rate) adjustment control from I/O die pad to latching element in DCAn.
3. The Gain Adjustment is applied to the baseline (default) inherent gain implemented in the receiver.
4. Gain Adjustment values shown in Table 3 are verified by design and the measurement from device pins is defined in a separate specification.
5. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 12, “DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin,” on page 25.
6. PG[1:0]RW[60, 68, 70, 78] will be sticky, cleared by power cycle not reset.

8.21.2 PG[1:0]RW[61, 69, 71, 79] - DPAR and DCA[6:0] Receiver DFE Tap 1 Coefficients

Table 159 — PG[1:0]RW[61, 69, 71, 79]: DPAR and DCA[6:0] Receiver DFE Tap 1 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Tap 1 DFE Coefficient [2,3,4]	(Default) Tap 1 DFE bias = 0 mV
x	x	0	0	0	0	0	1		Tap 1 DFE bias +1 Tap Step
x	x	0	0	0	0	1	0		Tap 1 DFE bias +2 Tap Steps
x	x	0	0	0	0	1	1		Tap 1 DFE bias +3 Tap Step
x	x	0	0	0	1	0	0		Tap 1 DFE bias +4 Tap Steps
x	x	0	0	0	1	0	1		Tap 1 DFE bias +5 Tap Steps
x	x	0	0	0	1	1	0		Tap 1 DFE bias +6 Tap Steps
x	x	0	0	0	1	1	1		Tap 1 DFE bias +7 Tap Steps
x	x	0	0	1	0	0	0		Tap 1 DFE bias +8 Tap Steps
x	x	0	0	1	0	0	1		Tap 1 DFE bias +9 Tap Steps
x	x	0	0	1	0	1	0		Tap 1 DFE bias +10 Tap Steps
x	x	0	0	1	0	1	1		Tap 1 DFE bias +11 Tap Steps
x	x	0	0	1	1	0	0		Tap 1 DFE bias +12 Tap Steps
x	x	0	0	1	1	0	1		Tap 1 DFE bias +13 Tap Steps
x	x	0	0	1	1	1	0		Tap 1 DFE bias +14 Tap Steps
x	x	0	0	1	1	1	1		Tap 1 DFE bias +15 Tap Steps
x	x	0	1	0	0	0	0		Tap 1 DFE bias +16 Tap Steps
x	x	0	1	0	0	0	1		Tap 1 DFE bias +17 Tap Steps
x	x	0	1	0	0	1	0		Tap 1 DFE bias +18 Tap Steps
x	x	0	1	0	0	1	1		Tap 1 DFE bias +19 Tap Steps
x	x	0	1	0	1	0	0		Tap 1 DFE bias +20 Tap Steps
x	x	0	1	0	1	0	1		Tap 1 DFE bias +21 Tap Steps
x	x	0	1	0	1	1	0		Tap 1 DFE bias +22 Tap Steps
x	x	0	1	0	1	1	1		Tap 1 DFE bias +23 Tap Steps
x	x	0	1	1	0	0	0		Tap 1 DFE bias +24 Tap Steps
x	x	0	1	1	0	0	1		Tap 1 DFE bias +25 Tap Steps
x	x	0	1	1	0	1	0		Tap 1 DFE bias +26 Tap Steps
x	x	0	1	1	0	1	1		Tap 1 DFE bias +27 Tap Steps
x	x	0	1	1	1	0	0		Tap 1 DFE bias +28 Tap Steps
x	x	0	1	1	1	0	1		Tap 1 DFE bias +29 Tap Steps
x	x	0	1	1	1	1	0		Tap 1 DFE bias +30 Tap Steps
x	x	0	1	1	1	1	1		Tap 1 DFE bias +31 Tap Steps
x	x	1	0	0	0	0	0		Tap 1 DFE bias +32 Tap Steps
x	x	1	0	0	0	0	1		Tap 1 DFE bias +33 Tap Steps
x	x	1	0	0	0	1	0		Tap 1 DFE bias +34 Tap Steps
x	x	1	0	0	0	1	1		Tap 1 DFE bias +35 Tap Steps
x	x	1	0	0	1	0	0		Tap 1 DFE bias +36 Tap Steps
x	x	1	0	0	1	0	1		Tap 1 DFE bias +37 Tap Steps
x	x	1	0	0	1	1	0		Tap 1 DFE bias +38 Tap Steps
x	x	1	0	0	1	1	1		Tap 1 DFE bias +39 Tap Steps
x	x	1	0	1	0	0	0		Tap 1 DFE bias +40 Tap Steps
x	x	1	0	1	0	0	1		Tap 1 DFE bias +41 Tap Steps
x	x	1	0	1	0	1	0		Tap 1 DFE bias +42 Tap Steps
x	x	1	0	1	0	1	1		Tap 1 DFE bias +43 Tap Steps
x	x	1	0	1	1	0	0		Tap 1 DFE bias +44 Tap Steps
x	x	1	0	1	1	0	1		Tap 1 DFE bias +45 Tap Steps
x	x	1	0	1	1	1	0		Tap 1 DFE bias +46 Tap Steps
x	x	1	0	1	1	1	1		Tap 1 DFE bias +47 Tap Steps
x	x	1	1	0	0	0	0		Tap 1 DFE bias +48 Tap Steps
x	x	1	1	0	0	0	1		Tap 1 DFE bias +49 Tap Steps
x	x	1	1	0	0	1	0		Tap 1 DFE bias +50 Tap Steps
x	x	1	1	0	0	1	1		Reserved
x	x	1	1	0	1	0	0		Reserved
x	x	1	1	0	1	0	1		Reserved
x	x	1	1	0	1	1	0		Reserved

Table 159 — PG[1:0]RW[61, 69, 71, 79]: DPAR and DCA[6:0] Receiver DFE Tap 1 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	1	1	0	1	1	1	Tap 1 DFE Coefficient [1,2,3]	Reserved
x	x	1	1	1	0	0	0		Reserved
x	x	1	1	1	0	0	1		Reserved
x	x	1	1	1	0	1	0		Reserved
x	x	1	1	1	0	1	1		Reserved
x	x	1	1	1	1	0	0		Reserved
x	x	1	1	1	1	0	1		Reserved
x	x	1	1	1	1	1	0		Reserved
x	x	1	1	1	1	1	1		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 1 Coefficient Sign Bit	(Default) Positive Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 1 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 1 post-cursor)

1. Table 93 and Table 94 illustrate the assignment of each control word in the PG[1:0]RW[61, 69, 71, 79] group to the corresponding input pin it controls.
2. Tap coefficient values shown in Table 160 are verified by design and the measurement from device pins is defined in a separate specification.
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 12, “DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin,” on page 25.
4. PG[1:0]RW[61, 69, 71, 79]OP[7:0] will be sticky, cleared by power cycle not reset.

8.21.3 PG[1:0]RW[62, 6A, 72, 7A]- DPAR and DCA[6:0] Receiver DFE Tap 2 Coefficients

Table 160 — PG[1:0]RW[62, 6A, 72, 7A]: DPAR and DCA[6:0] Receiver DFE Tap 2 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Tap 2 DFE Coefficient [2,3,4]	(Default) Tap 2 DFE bias = 0 mV
x	x	0	0	0	0	0	1		Tap 2 DFE bias+1 Tap Step
x	x	0	0	0	0	1	0		Tap 2 DFE bias +2 Tap Steps
x	x	0	0	0	0	1	1		Tap 2 DFE bias +3 Tap Steps
x	x	0	0	0	1	0	0		Tap 2 DFE bias +4 Tap Steps
x	x	0	0	0	1	0	1		Tap 2 DFE bias +5 Tap Steps
x	x	0	0	0	1	1	0		Tap 2 DFE bias +6 Tap Steps
x	x	0	0	0	1	1	1		Tap 2 DFE bias +7 Tap Steps
x	x	0	0	1	0	0	0		Tap 2 DFE bias +8 Tap Steps
x	x	0	0	1	0	0	1		Tap 2 DFE bias +9 Tap Steps
x	x	0	0	1	0	1	0		Tap 2 DFE bias +10 Tap Steps
x	x	0	0	1	0	1	1		Tap 2 DFE bias +11 Tap Steps
x	x	0	0	1	1	0	0		Tap 2 DFE bias +12 Tap Steps
x	x	0	0	1	1	0	1		Tap 2 DFE bias +13 Tap Steps
x	x	0	0	1	1	1	0		Tap 2 DFE bias +14 Tap Steps
x	x	0	0	1	1	1	1		Tap 2 DFE bias +15 Tap Steps
x	x	0	1	0	0	0	0		Tap 2 DFE bias +16 Tap Steps
x	x	0	1	0	0	0	1		Tap 2 DFE bias +17 Tap Steps
x	x	0	1	0	0	1	0		Tap 2 DFE bias +18 Tap Steps
x	x	0	1	0	0	1	1		Tap 2 DFE bias +19 Tap Steps
x	x	0	1	0	1	0	0		Tap 2 DFE bias +20 Tap Steps
x	x	0	1	0	1	0	1		Reserved
x	x	0	1	0	1	1	0		Reserved
x	x	0	1	0	1	1	1		Reserved
x	x	0	1	1	0	0	0		Reserved
x	x	0	1	1	0	0	1		Reserved
x	x	0	1	1	0	1	0		Reserved
x	x	0	1	1	0	1	1		Reserved
x	x	0	1	1	1	0	0		Reserved
x	x	0	1	1	1	0	1		Reserved
x	x	0	1	1	1	1	0		Reserved
x	x	0	0	1	1	1	1		Reserved
x	x	1	0	0	0	0	1		Reserved
x	x	1	0	0	0	0	0		Reserved
x	x	1	0	0	0	1	1		Reserved
x	x	1	0	0	0	1	0		Reserved
x	x	1	0	0	1	0	1		Reserved
x	x	1	0	0	1	0	0		Reserved
x	x	1	0	0	1	1	1		Reserved
x	x	1	0	0	1	1	0		Reserved
x	x	1	0	1	0	0	1		Reserved
x	x	1	0	1	0	0	0		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 2 Coefficient Sign Bit	(Default) Positive Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 1 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 1 post-cursor)

1. Table 93 and Table 94 illustrate the assignment of each control word in the PG[1:0]RW[62, 6A, 72, 7A] group to the corresponding input pin it controls.
2. Tap coefficient values shown in Table 160 are verified by design and the measurement from device pins is defined in a separate specification.
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 12, “DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin,” on page 25.
4. PG[1:0]RW[62, 6A, 72, 7A] OP[7:0] will be sticky, cleared by power cycle not reset.

8.21.4 PG[1:0]RW[63, 6B, 73, 7B] - DPAR and DCA[6:0] Receiver DFE Tap 3 Coefficients

Table 161 — PG[1:0]RW[63, 6B, 73, 7B]: DPAR and DCA[6:0] Receiver DFE Tap 3 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 3 DFE Coefficient [2,3,4]	(Default) Tap 3 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 3 DFE bias +1 Tap Step
x	x	x	0	0	0	1	0		Tap 3 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 3 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 3DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 3 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 3 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 3 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 3 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 3 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 3 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 3 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 3 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 3 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 3 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 3 DFE bias +15 Tap Steps
x	x	x	1	0	0	0	0		Reserved
x	x	x	1	0	0	0	1		Reserved
x	x	x	1	0	0	1	0		Reserved
x	x	x	1	0	0	1	1		Reserved
x	x	x	1	0	1	0	0		Reserved
x	x	x	1	0	1	0	1		Reserved
x	x	x	1	0	1	1	0		Reserved
x	x	x	1	0	1	1	1		Reserved
x	x	x	1	1	0	0	0		Reserved
x	x	x	1	1	0	0	1		Reserved
x	x	x	1	1	0	1	0		Reserved
x	x	x	1	1	0	1	1		Reserved
x	x	x	1	1	1	0	0		Reserved
x	x	x	1	1	1	0	1		Reserved
x	x	x	1	1	1	1	0		Reserved
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 3 Coefficient Sign Bit	(Default) Positive Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 1 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 1 post-cursor)

1. Table 93 and Table 94 illustrate the assignment of each control word in the PG[1:0]RW[63, 6B, 73, 7B] group to the corresponding input pin it controls.
2. Tap coefficient values shown in Table 161 are verified by design and the measurement from device pins is defined in a separate specification.
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 12, “DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin,” on page 25.
4. PG[1:0]RW[63, 6B, 73, 7B] OP[7:0] will be sticky, cleared by power cycle not reset.

8.21.5 PG[1:0]RW[64, 6C, 74, 7C]- DPAR and DCA[6:0] Receiver DFE Tap 4 Coefficients

Table 162 — PG[1:0]RW[64, 6C, 74, 7C]: DPAR and DCA[6:0] Receiver DFE Tap 4 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 4 DFE Coefficient [2,3,4]	(Default) Tap 4 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 4 DFE bias +1 Tap Steps
x	x	x	0	0	0	1	0		Tap 4 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 4 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 4 DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 4 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 4 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 4 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 4 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 4 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 4 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 4 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 4 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 4 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 4 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 4 DFE bias +15 Tap Steps
x	x	x	1	0	0	0	0		Reserved
x	x	x	1	0	0	0	1		Reserved
x	x	x	1	0	0	1	0		Reserved
x	x	x	1	0	0	1	1		Reserved
x	x	x	1	0	1	0	0		Reserved
x	x	x	1	0	1	0	1		Reserved
x	x	x	1	0	1	1	0		Reserved
x	x	x	1	0	1	1	1		Reserved
x	x	x	1	1	0	0	0		Reserved
x	x	x	1	1	0	0	1		Reserved
x	x	x	1	1	0	1	0		Reserved
x	x	x	1	1	0	1	1		Reserved
x	x	x	1	1	1	0	0		Reserved
x	x	x	1	1	1	0	1		Reserved
x	x	x	1	1	1	1	0		Reserved
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 4 Coefficient Sign Bit	(Default) Positive Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 1 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 1 post-cursor)

1. Table 93 and Table 94 illustrate the assignment of each control word in the PG[1:0]RW[64, 6C, 74, 7C] group to the corresponding input pin it controls.
2. Tap coefficient values shown in Table 162 are verified by design and the measurement from device pins is defined in a separate specification.
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 12, “DFE Gain and Tap Coefficient Step Parameters Required per Speed Bin,” on page 25.
4. PG[1:0]RW[64, 6C, 74, 7C] OP[7:0] will be sticky, cleared by power cycle not reset.

8.21.6 PG[2]RW[60, 64, 68, 6C, 70, 74, 78, 7C] DFE Error Counter Lower 8 Bits

Table 163 — PG[2][60, 64, 68, 6C, 70, 74, 78, 7C]- DFE Error Counter Lower 8 Bit

DFE Error Counter Lower 8 Bit Register[1,2,3,4]							
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

1. Table 95 illustrates the assignment of each control word in the PG[2]RW[60, 64, 68, 6C, 70, 74, 78, 7C] group to the corresponding input pin it controls.
2. Power on Default is OP[7:0] = 0.
3. Read Only Register.
4. ERROR counters will run regardless of DCn selection.

8.21.7 PG[2]RW[61, 65, 69, 6D, 71, 75, 79, 7D] - DFE Error Counter Upper 8 Bits

Table 164 — PG[2][61, 65, 69, 6D, 71, 75, 79, 7D] DFE Error Counter Upper 8 Bit

DFE Error Counter Upper 8 Bit Register[1,2,3,4]							
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**
EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC 9	EC 8

1. Table 95 illustrates the assignment of each control word in the PG[2]RW[61, 65, 69, 6D, 71, 75, 79, 7D] group to the corresponding input pin it controls.
2. Power on Default is OP[7:0] = 0.
3. Read Only Register.
4. ERROR counters will run regardless of DCn selection.

8.21.8 PG[2]RW[62, 66, 6A, 6E, 72, 76,7A, 7E] - DFE Vref

Table 165 — PG[2]RW[62, 66, 6A, 6E, 72, 76,7A, 7E]: DFE Vref

PG02RW[62, 66 .. 7E]						DFE Training VREF in mV[1,2,3,4,5]							
						RW3F[x6]= 1 (NEG Range)				RW3F[x4] = 0 (POS Range)			
OP7	OP6	OP5	OP4	OP3	OP2	OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11	OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11
0	0	0	0	0	0	0.0	- 2.5	- 5.0	- 7.5	0.0	+ 2.5	+ 5.0	+ 7.5
0	0	0	0	0	1	- 10.0	- 12.5	- 15.0	- 17.5	+ 10.0	+ 12.5	+ 15.0	+ 17.5
0	0	0	0	1	0	- 20.0	- 22.5	- 25.0	- 27.5	+ 20.0	+ 22.5	+ 25.0	+ 27.5
0	0	0	0	1	1	- 30.0	- 32.5	- 35.0	- 37.5	+ 30.0	+ 32.5	+ 35.0	+ 37.5
0	0	0	1	0	0	- 40.0	- 42.5	- 45.0	- 47.5	+ 40.0	+ 42.5	+ 45.0	+ 47.5
0	0	0	1	0	1	- 50.0	- 52.5	- 55.0	- 57.5	+ 50.0	+ 52.5	+ 55.0	+ 57.5
0	0	0	1	1	0	- 60.0	- 62.5	- 65.0	- 67.5	+ 60.0	+ 62.5	+ 65.0	+ 67.5
0	0	0	1	1	1	- 70.0	- 72.5	- 75.0	- 77.5	+ 70.0	+ 72.5	+ 75.0	+ 77.5
0	0	1	0	0	0	- 80.0	- 82.5	- 85.0	- 87.5	+ 80.0	+ 82.5	+ 85.0	+ 87.5
0	0	1	0	0	1	- 90.0	- 92.5	- 95.0	- 97.5	+ 90.0	+ 92.5	+ 95.0	+ 97.5
0	0	1	0	1	0	- 100.0	- 102.5	- 105.0	- 107.5	+ 100.0	+ 102.5	+ 105.0	+ 107.5
0	0	1	0	1	1	- 110.0	- 112.5	- 115.0	- 117.5	+ 110.0	+ 112.5	+ 115.0	+ 117.5
0	0	1	1	0	0	- 120.0	- 122.5	- 125.0	- 127.5	+ 120.0	+ 122.5	+ 125.0	+ 127.5
0	0	1	1	0	1	- 130.0	- 132.5	- 135.0	- 137.5	+ 130.0	+ 132.5	+ 135.0	+ 137.5
0	0	1	1	1	0	- 140.0	- 142.5	- 145.0	- 147.5	+ 140.0	+ 142.5	+ 145.0	+ 147.5
0	0	1	1	1	1	- 150.0	- 152.5	- 155.0	- 157.5	+ 150.0	+ 152.5	+ 155.0	+ 157.5
0	1	0	0	0	0	- 160.0	- 162.5	- 165.0	- 167.5	+ 160.0	+ 162.5	+ 165.0	+ 167.5
0	1	0	0	0	1	- 170.0	- 172.5	- 175.0	- 177.5	+ 170.0	+ 172.5	+ 175.0	+ 177.5
0	1	0	0	1	0	- 180.0	- 182.5	- 185.0	- 187.5	+ 180.0	+ 182.5	+ 185.0	+ 187.5
0	1	0	0	1	1	- 190.0	- 192.5	- 195.0	- 197.5	+ 190.0	+ 192.5	+ 195.0	+ 197.5
0	1	0	1	0	0	- 200.0	- 202.5	- 205.0	- 207.5	+ 200.0	+ 202.5	+ 205.0	+ 207.5
0	1	0	1	0	1	- 210.0	- 212.5	- 215.0	- 217.5	+ 210.0	+ 212.5	+ 215.0	+ 217.5
0	1	0	1	1	0	- 220.0	- 222.5	- 225.0	- 227.5	+ 220.0	+ 222.5	+ 225.0	+ 227.5
0	1	0	1	1	1	- 230.0	- 232.5	- 235.0	- 237.5	+ 230.0	+ 232.5	+ 235.0	+ 237.5
0	1	1	0	0	0	- 240.0	- 242.5	- 245.0	- 247.5	+ 240.0	+ 242.5	+ 245.0	+ 247.5
0	1	1	0	0	1	- 250.0	- 252.5	- 255.0	- 257.5	+ 250.0	+ 252.5	+ 255.0	+ 257.5
0	1	1	0	1	0	- 260.0	- 262.5	- 265.0	- 267.5	+ 260.0	+ 262.5	+ 265.0	+ 267.5
0	1	1	0	1	1	- 270.0	- 272.5	- 275.0	- 277.5	+ 270.0	+ 272.5	+ 275.0	+ 277.5
0	1	1	1	0	0	- 280.0	- 282.5	- 285.0	- 287.5	+ 280.0	+ 282.5	+ 285.0	+ 287.5
0	1	1	1	0	1	- 290.0	- 292.5	- 295.0	- 297.5	+ 290.0	+ 292.5	+ 295.0	+ 297.5
0	1	1	1	1	0	- 300.0	- 302.5	- 305.0	- 307.5	+ 300.0	+ 302.5	+ 305.0	+ 307.5
0	1	1	1	1	1	- 310.0	- 312.5	- 315.0	- 317.5	+ 310.0	+ 312.5	+ 315.0	+ 317.5
1	0	0	0	0	0	- 320.0	- 322.5	- 325.0	- 327.5	+ 320.0	+ 322.5	+ 325.0	+ 327.5
1	0	0	0	0	1	- 330.0	- 332.5	- 335.0	- 337.5	+ 330.0	+ 332.5	+ 335.0	+ 337.5
1	0	0	0	1	0	- 340.0	- 342.5	- 345.0	- 347.5	+ 340.0	+ 342.5	+ 345.0	+ 347.5
1	0	0	0	1	1	- 350.0	- 352.5	- 355.0	- 357.5	+ 350.0	+ 352.5	+ 355.0	+ 357.5
1	0	0	1	0	0	- 360.0	- 362.5	- 365.0	- 367.5	+ 360.0	+ 362.5	+ 365.0	+ 367.5
1	0	0	1	0	1	- 370.0	- 372.5	- 375.0	- 377.5	+ 370.0	+ 372.5	+ 375.0	+ 377.5
1	0	0	1	1	0	- 380.0	- 382.5	- 385.0	- 387.5	+ 380.0	+ 382.5	+ 385.0	+ 387.5
1	0	0	1	1	1	- 390.0	- 392.5	- 395.0	- 397.5	+ 390.0	+ 392.5	+ 395.0	+ 397.5
1	0	1	0	0	0	- 400.0	- 402.5	- 405.0	- 407.5	+ 400.0	+ 402.5	+ 405.0	+ 407.5
1	0	1	0	0	1	- 410.0	- 412.5	- 415.0	- 417.5	+ 410.0	+ 412.5	+ 415.0	+ 417.5
1	0	1	0	1	0	- 420.0	- 422.5	- 425.0	- 427.5	+ 420.0	+ 422.5	+ 425.0	+ 427.5
1	0	1	0	1	1	- 430.0	- 432.5	- 435.0	- 437.5	+ 430.0	+ 432.5	+ 435.0	+ 437.5
1	0	1	1	0	0	- 440.0	- 442.5	- 445.0	- 447.5	+ 440.0	+ 442.5	+ 445.0	+ 447.5
1	0	1	1	0	1	- 450.0	- 452.5	- 455.0	- 457.5	+ 450.0	+ 452.5	+ 455.0	+ 457.5
1	0	1	1	1	0	- 460.0	- 462.5	- 465.0	- 467.5	+ 460.0	+ 462.5	+ 465.0	+ 467.5
1	0	1	1	1	1	- 470.0	- 472.5	- 475.0	- 477.5	+ 470.0	+ 472.5	+ 475.0	+ 477.5
1	1	0	0	0	0	- 480.0	- 482.5	- 485.0	- 487.5	+ 480.0	+ 482.5	+ 485.0	+ 487.5
1	1	0	0	0	1	- 490.0	- 492.5	- 495.0	- 497.5	+ 490.0	+ 492.5	+ 495.0	+ 497.5
1	1	0	0	1	0	- 500.0	Reserved	Reserved	Reserved	+ 500.0	Reserved	Reserved	Reserved
1	1	0	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

1. Table 95 illustrates the assignment of each control word in the PG[2]RW[62, 66, 6A, 6E, 72, 76, 7A 7E] group to the corresponding input pin it controls.
2. These are target DFE_Vref values. Acceptable actual values are determined based on tolerances defined in electrical section.
3. The target DFE_Vref values shown in this table are input referred.
4. Even though each input receiver has a dedicated DFE_Vref control word, only one DFE Vref monitor is allowed to be enabled at the same time in each sub-channel.
5. VrefCA and DFE_Vref are independent. External VrefCA must be adjusted for large input swings.
6. The range selection per Dx is controlled by writing to RW3F.

8.21.9 PG[2]RW[63, 67, 6B, 6F, 73, 77, 7B, 7F] - LFSR Seed for DFE Training Mode Control Word

Table 166 — PG[2]RW[63, 67, 6B, 6F, 73, 77, 7B, 7F] LFSR Seed for DFE Training Mode Control Word[1,]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	LFSR Seed	LFSR Seed = 0x00*
0	0	0	0	0	0	0	1		LFSR Seed = 0x01
0	0	0	0	0	0	1	0		LFSR Seed = 0x02
...									...
1	1	1	1	1	1	0	0		LFSR Seed = 0xFC
1	1	1	1	1	1	0	1		LFSR Seed = 0xFD
1	1	1	1	1	1	1	0		LFSR Seed = 0xFE
1	1	1	1	1	1	1	1		LFSR Seed = 0xFF

1. Table 95 illustrates the assignment of each control word in the PG[2]RW[63, 67, 6B, 6F, 73, 77, 7B, 7F] group to the corresponding input pin it controls.

8.22 OTP Paged Global Control Words

Page 3 contains Global Read-Only Words that must be accessed through Channel A only.

8.22.1 PG[3]RW60 - Date Code Byte 0 Global Word

Table 167 — PG[3]RW60: Date Code Byte 0 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 0[1,2] Year Information - Ones Digit (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 1[1, 2] Year Information - Tens Digit (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.
2. This is year date code byte for RCD. It must be represented in Binary Coded Decimal (BCD). For example, year 2015 would be coded as 0x15 (0001 0101).

8.22.2 PG[3]RW61 - Date Code Byte 1 Global Word

Table 168 — PG[3]RW61: Date Code Byte 1 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 2[1,2] Work Week Information - Ones Digit ISO 8601 compliant (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 3[1, 2] Work Week Information - Tens Digit ISO 8601 compliant (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.
2. This is work week date code byte for RCD. It must be represented in Binary Coded Decimal (BCD). For example, week 47 would be coded as 0x47 (0100 0111).

8.22.3 PG[3]RW62 - Date Code Byte 2 Global Word

Table 169 — PG[3]RW62: Date Code Byte 2 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 4[1] Reserved (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 5[1] Reserved (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.4 PG[3]RW63 - Vendor Specific Unique Unit Code Byte 0 Global Word

Table 170 — PG[3]RW63: Vendor Specific Unique Unit Code Byte 0 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 0 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.5 PG[3]RW64 - Vendor Specific Unique Unit Code Byte 1 Global Word

Table 171 — PG[3]RW64: Vendor Specific Unique Unit Code Byte 1 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 1 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.6 PG[3]RW65 - Vendor Specific Unique Unit Code Byte 2 Global Word

Table 172 — PG[3]RW65: Vendor Specific Unique Unit Code Byte 2 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 2 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.7 PG[3]RW66 - Vendor Specific Unique Unit Code Byte 3 Global Word

Table 173 — PG[3]RW66: Vendor Specific Unique Unit Code Byte 3 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 3 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.8 PG[3]RW67 - Vendor Specific Unique Unit Code Byte 4 Global Word

Table 174 — PG[3]RW67: Vendor Specific Unique Unit Code Byte 4 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 4 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.9 PG[3]RW68 - Vendor Specific Unique Unit Code Byte 5 Global Word

Table 175 — PG[3]RW68: Vendor Specific Unique Unit Code Byte 5 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 5 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.10 PG[3]RW69 - Vendor Specific Unique Unit Code Byte 6 Global Word

Table 176 — PG[3]RW69: Vendor Specific Unique Unit Code Byte 6 Global Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
0	0	0	0	0	0	0	0	Byte 6 of Unique Unit Code[1] (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR5RCD01 vendor.

8.22.11 PG[3]RW6A - Vendor ID Byte 0 Global Word

Table 177 — PG[3]RW6A: Vendor ID Byte 0 Global Word[1]

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
0	0	0	0	0	0	0	0	Byte 0 of Vendor ID (Read Only)	VID[7:0] = 0x00h
0	0	0	0	0	0	0	1		VID[7:0] = 0x01h
0	0	0	0	0	0	1	0		VID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		VID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		VID[7:0] = 0xFFh

1. Each vendor will have a specific Vendor ID value assigned by JEDEC.

8.22.12 PG[3]RW6B - Vendor ID Byte 1 Global Word

Table 178 — PG[3]RW6B: Vendor ID Byte 1 Global Word[1]

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
0	0	0	0	0	0	0	0	Byte 1 of Vendor ID (Read Only)	VID[15:8] = 0x00h
0	0	0	0	0	0	0	1		VID[15:8] = 0x01h
0	0	0	0	0	0	1	0		VID[15:8] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[15:8] = 0xFDh
1	1	1	1	1	1	1	0		VID[15:8] = 0xFEh
1	1	1	1	1	1	1	1		VID[15:8] = 0xFFh

1. Each vendor will have a specific Vendor ID value assigned by JEDEC.

8.22.13 PG[3]RW6C - Device ID Byte 0 Global Word

Table 179 — PG[3]RW6C: Device ID Byte 0 Global Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 0 of Device ID (Read Only)	DID[7:0] = 0x00h
0	0	0	0	0	0	0	1		DID[7:0] = 0x01h
0	0	0	0	0	0	1	0		DID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		DID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		DID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		DID[7:0] = 0xFFh

1. The device ID value is 0x0051.

8.22.14 PG[3]RW6D - Device ID Byte 1 Global Word

Table 180 — PG[3]RW6D: Device ID Byte 1 Global Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 1 of Device ID (Read Only)	DID[15:8] = 0x00h
0	0	0	0	0	0	0	1		DID[15:8] = 0x01h
0	0	0	0	0	0	1	0		DID[15:8] = 0x02h
...									...
1	1	1	1	1	1	0	1		DID[15:8] = 0xFDh
1	1	1	1	1	1	1	0		DID[15:8] = 0xFEh
1	1	1	1	1	1	1	1		DID[15:8] = 0xFFh

1. The device ID value is 0x0051.

8.22.15 PG[3]RW6E - Revision ID Global Word

Table 181 — PG[3]RW6E: Revision ID Global Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Revision ID (Read Only)	RID[7:0] = 0x00h
0	0	0	0	0	0	0	1		RID[7:0] = 0x01h
0	0	0	0	0	0	1	0		RID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		RID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		RID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		RID[7:0] = 0xFFh

1. This is a fixed vendor specific register.

8.23 VHost Paged Control Words

8.23.1 PG[4]RW[6E,6C,6A,68,66,64,62,60] - VHost Cmd[3:0] CA[7:0] Control Word

Table 182 — PG[4]RW[6E,6C,6A,68,66,64,62,60] - VHost Cmd[3:0] CA[7:0] Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Cmd[3:0] 1st/2nd UI CA0	QCA0 = 0
x	x	x	x	x	x	x	1		QCA0 = 1
x	x	x	x	x	x	0	x	Cmd[3:0] 1st/2nd UI CA1	QCA1 = 0
x	x	x	x	x	x	1	x		QCA1 = 1
x	x	x	x	x	0	x	x	Cmd[3:0] 1st/2nd UI CA2	QCA2 = 0
x	x	x	x	x	1	x	x		QCA2 = 1
x	x	x	x	0	x	x	x	Cmd[3:0] 1st/2nd UI CA3	QCA3 = 0
x	x	x	x	1	x	x	x		QCA3 = 1
x	x	x	0	x	x	x	x	Cmd[3:0] 1st/2nd UI CA4	QCA4 = 0
x	x	x	1	x	x	x	x		QCA4 = 1
x	x	0	x	x	x	x	x	Cmd[3:0] 1st/2nd UI CA5	QCA5 = 0
x	x	1	x	x	x	x	x		QCA5 = 1
x	0	x	x	x	x	x	x	Cmd[3:0] 1st/2nd UI CA6	QCA6 = 0
x	1	x	x	x	x	x	x		QCA6 = 1
0	x	x	x	x	x	x	x	Cmd[3:0] 1st/2nd UI CA7	QCA7 = 0
1	x	x	x	x	x	x	x		QCA7 = 1

1. Table 97 illustrates the assignment of each control word in the PG[4]RW[6E, 6C, 6A, 68, 66, 64, 62, 60] group to the corresponding input pin it controls.

8.23.2 PG[4]RW[6F,6D,6B,69,67,65,63,61] - VHost Cmd[3:0] CS[1:0]/CA[13:8] Control Word

Table 183 — PG[4]RW[6F,6D,6B,69,67,65,63,61] - VHost Cmd[3:0] CA[7:0] Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Cmd[3:0] 1st/2nd UI CA8	QCA8 = 0
x	x	x	x	x	x	x	1		QCA8 = 1
x	x	x	x	x	x	0	x	Cmd[3:0] 1st/2nd UI CA9	QCA9 = 0
x	x	x	x	x	x	1	x		QCA9 = 1
x	x	x	x	x	0	x	x	Cmd[3:0] 1st/2nd UI CA10	QCA10 = 0
x	x	x	x	x	1	x	x		QCA10 = 1
x	x	x	x	0	x	x	x	Cmd[3:0] 1st/2nd UI CA11	QCA11 = 0
x	x	x	x	1	x	x	x		QCA11 = 1
x	x	x	0	x	x	x	x	Cmd[3:0] 1st/2nd UI CA12	QCA12 = 0
x	x	x	1	x	x	x	x		QCA12 = 1
x	x	0	x	x	x	x	x	Cmd[3:0] 1st/2nd UI CA13	QCA13 = 0
x	x	1	x	x	x	x	x		QCA13 = 1
x	0	x	x	x	x	x	x	Cmd[3:0] 1st/2nd UI CS0_n	QCS0_n = 0
x	1	x	x	x	x	x	x		QCS0_n = 1
0	x	x	x	x	x	x	x	Cmd[3:0] 1st/2nd UI CS1_n	QCS1_n = 0
1	x	x	x	x	x	x	x		QCS1_n = 1

1. Table 97 illustrates the assignment of each control word in the PG[4]RW[6F, 6D, 6B, 69, 67, 65, 63, 61] group to the corresponding input pin it controls.

8.23.3 PG[4]RW70 - VHost [1:0] Cmd to Cmd Delay Control Word

Table 184 — PG[4]RW70 - VHost [1:0] Cmd to Cmd Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	cmd0 to cmd1 Delay	2 nCK
x	x	x	x	x	0	0	1		4 nCK
x	x	x	x	x	0	1	0		8 nCK
x	x	x	x	x	0	1	1		16 nCK
x	x	x	x	x	1	0	0		64 nCK
x	x	x	x	x	1	0	1		256 nCK
x	x	x	x	x	1	1	0		1024 nCK
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	cmd1 to cmd2 Delay	2 nCK
x	0	0	1	x	x	x	x		4 nCK
x	0	1	0	x	x	x	x		8 nCK
x	0	1	1	x	x	x	x		16 nCK
x	1	0	0	x	x	x	x		64 nCK
x	1	0	1	x	x	x	x		256 nCK
x	1	1	0	x	x	x	x		1024 nCK
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

8.23.4 PG[4]RW71 - VHost [3:2]Cmd to Cmd Delay Control Word

Table 185 — PG[4]RW71 - VHost [3:2] Cmd to Cmd Delay Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	cmd2 to cmd3 Delay	2 nCK
x	x	x	x	x	0	0	1		4 nCK
x	x	x	x	x	0	1	0		8 nCK
x	x	x	x	x	0	1	1		16 nCK
x	x	x	x	x	1	0	0		64 nCK
x	x	x	x	x	1	0	1		256 nCK
x	x	x	x	x	1	1	0		1024 nCK
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	cmd3 to cmdn Delay	2 nCK
x	0	0	1	x	x	x	x		4 nCK
x	0	1	0	x	x	x	x		8 nCK
x	0	1	1	x	x	x	x		16 nCK
x	1	0	0	x	x	x	x		64 nCK
x	1	0	1	x	x	x	x		256 nCK
x	1	1	0	x	x	x	x		1024 nCK
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

8.23.5 PG[4]RW72 - VHost Repeat Mode Control Word

Table 186 — PG[4]RW72 - VHost Repeat Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	Repeat Control	Repeat to cmd0 (repeat all 4)
x	x	x	x	x	x	0	1		Repeat to cmd1 (repeat last 3)
x	x	x	x	x	x	1	0		Repeat to cmd2 (repeat last 2)
x	x	x	x	x	x	1	1		Repeat to cmd3 (repeat last 1)
x	x	x	x	x	0	x	x	Repeat Enable	Do not repeat
x	x	x	x	x	1	x	x		Repeat as defined in RW72[1:0]
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

8.23.6 PG[4]RW73 - VHost Start and Stop Global Control Word

Table 187 — PG[4]RW73 - VHost Start and Stop Global Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	VHost Selection	CH_A only
x	x	x	x	x	x	0	1		CH_B only
x	x	x	x	x	x	1	0		CH_A and CH_B Start and Stop at the same time
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	x	0	x	x	VHost Start/Stop[1]	Stop VHost
x	x	x	x	x	1	x	x		Start VHost
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[4]RW73 is only accessible from CH_A.

9 Absolute maximum ratings

Table 188 — Absolute maximum ratings over operating free-air temperature range[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.3	1.4	V
V_{IN}	Receiver input voltage[2]	See Note 4 and 5	–0.3	V_{DD} + 0.5	V
V_{OUT}	Driver output voltage[3]	See Note 4 and 5	–0.3	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_{IN} < 0$ or $V_{IN} > V_{DD}$	-	-50	mA
I_{OK}	Output clamp current	$V_{OUT} < 0$ or $V_{OUT} > V_{DD}$	-	±50	mA
I_{OUT}	Continuous output current	$0 < V_{OUT} < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or V_{ss} pin		-	±100	mA
T_{stg}	Storage temperature		–55	+100	°C

NOTE(S):

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. This parameter does not apply to SCL. See Management Bus Interface chapter for voltage specifications for these inputs.
3. This parameter does not apply to SDA. See Management Bus Interface chapter for voltage specifications for these inputs.
4. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
5. This value is limited to 1.4 V maximum.

10 Electrical - Timing Requirements

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V
T_j	Junction temperature[2]		0	-	125	°C
T_{case}	Case temperature	Measurement procedure JESD51-2	-	-	103[3]	°C

1. DC bandwidth limited to 20 MHz.
2. For operation beyond Tj min and max datasheet values are not guaranteed and may de-rate. For operation above Tj max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C and 95 °C.
3. This spec is meant to guarantee a Tj of 125 °C by the DDR5RCD01. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a DDR5RCD01 shall not be higher than 125 °C.

10.2 Input Timing Requirements

Table 190 — Input Timing requirements

Symbol	Parameter	Conditions	DDR5-3200/ 3600/4000		DDR5-4400		DDR5-4800		
			Min	Max	Min	Max	Min	Max	Unit
f_{CLOCK}	Input clock frequency[1]	Application frequency[2]	1400	2030	1400	2233	1400	2436	MHz
f_{TEST}	Input clock frequency	Test frequency[3]	140	1400	140	1400	140	1400	MHz
t_{MRD}	Control word to control word delay	Number of clock cycles between two control word accesses or one control word access and any DRAM command.	8	-	8	-	8	-	t_{CK}
t_{MRD_L}	Control word to control word delay	Number of clock cycles between an access to RW0A, RW0B, RW0C, RW0D[4], RW10, RW25, RW26, RW27, RW31[7:2], RW[4B:40][5], RW5E[6], RW5F[6], PG[1:0]RW[7C:61] (i.e., any receiver DFE tap coefficient value) and the next control word access or DRAM command.	16	-	16	-	16	-	t_{CK}
t_{MRD_L2}	Control word to control word delay	Number of clock cycles between an access to RW00[7], RW01, RW02, RW03, RW05[7], RW06[7], RW07, RW09, RW0E, RW0F, RW11[2:0], RW32[7:6, 2:1][8] and the next control word access or DRAM command[9]	32	-	32	-	32	-	t_{CK}
t_{MRD_L3}	Control word to control word delay for DFE Gain Adjustment	Waiting time between an access to RW32[5:3, 0], PG[1:0]RW[60, 68, 70, 78] and the next input DCS_n assertion.	300	-	300	-	300	-	ns
t_{MRD_L4}	Control word to control word delay for DFE Vref Settling Time	Waiting time between an access to RW31[1:0], RW3F, PG02RW[62, 66, 6A, 6E, 72, 76, 7A, 7E] and the next input DCS_n assertion.	300	-	300	-	300	-	ns
t_{MRC}	Register command word to CW or DRAM command delay	Number of clock cycles between register command word (RW04) and CW or any DRAM command	32	-	32	-	32	-	t_{CK}
$t_{Ext_LB_Entry}$	External Loopback Entry Time	Delay from MRW (RW26) that enables External Loopback and start of valid QLBD/QLBS forwarded from selected DLBD/DLBS.	-	300	-	300	-	300	ns
t_{MRD2N}	Control word to control word delay in SDR/2N mode.	Number of clock cycles between two control word accesses or one control word access and any DRAM command.	16	-	16	-	16	-	
t_{MRD2N_L}	Control word to control word delay in SDR/2N mode	Number of clock cycles between an access to RW0A, RW0B, RW0C, RW0D[4], RW10, RW25, RW26, RW27, RW[4B:40][5], RW5E[6], RW5F[6] and the next control word access or DRAM command.	24	-	24	-	24	-	t_{CK}
t_{MRD2N_L2}	Control word to control word delay in SDR/2N mode	Number of clock cycles between an access to RW00[7], RW01, RW02, RW03, RW05[7], RW06[7], RW07, RW09, RW0E, RW0F, RW11[2:0], RW32[7:6, 2:1][8] and the next control word access or DRAM command[9]	50	-	50	-	50	-	t_{CK}
t_{MRC2N}	Register command word to CW or DRAM command delay in SDR/ 2N mode	Number of clock cycles between register command word (RW04) and CW or any DRAM command	40	-	40	-	40	-	t_{CK}
$t_{RWUPDInit}$	Time needed from enter into RWUPD to being able to receive in band RW updates		500	-	500	-	500	-	ns
$t_{RWUPDA2D}$	Time between address transfer and data transfer		8	-	8	-	8	-	t_{CK}

Table 190 — Input Timing requirements

Symbol	Parameter	Conditions	DDR5-3200/ 3600/4000		DDR5-4400		DDR5-4800		
			Min	Max	Min	Max	Min	Max	Unit
$t_{RWUPDD2A}$	Time between data transfer and next operation address transfer		8	-	8	-	8	-	t_{CK}
$t_{RWUPDExit}$	Time needed between last RWUPD CS1_n de-assertion and the first CS0_n assertion of DFE training mode or any other operation.[10]		500	-	500	-	500	-	ns
t_{DCSTM_Entry}	Registration of DCSTM entry from SMBus RW command to start of training samples time		-	250	-	250	-	250	ns
t_{DCSTM_Exit}	Registration of DCSTM exit from SMBus RW command to end of training mode		-	250	-	250	-	250	ns
t_{DCSTM_Valid}	Time from sample evaluation to output on ALERT_n or QLBx		-	20	-	20	-	20	t_{CK}
$t_{DCSTM_ALERT_Window}$	Time output is available[11] on ALERT_n or QLBx		2	-	2	-	2	-	t_{CK}
t_{QCSTM_Entry}	Registration of QCSTM entry from MRW command to start of QCS training pattern		-	72	-	72	-	72	t_{CK}
t_{QCSTM_Exit}	Registration of QCSTM exit from SMBus RW command to end of QCS training pattern		-	72	-	72	-	72	t_{CK}
t_{DCATM_Entry}	Registration of DCATM entry from SMBus RW command to start of training samples time		-	250	-	250	-	250	ns
t_{DCATM_Exit}[12]	Registration of DCATM exit from SMBus RW command to end of training mode		-	250	-	250	-	250	ns
$t_{DCATM_CS_Exit}$[12]	Time DCS0_n must be held LOW to exit from DCATM training mode		2	8	2	8	2	8	t_{CK}
t_{DCATM_Valid}	Time from sample evaluation to output on ALERT_n or QLBx		-	20	-	20	-	20	t_{CK}
$t_{DCATM_ALERT_Window}$	Time output is available[11] on ALERT_n or QLBx		2	-	2	-	2	-	t_{CK}
$t_{DFETM_Interval}$	Number of cycles for CA DFE Training data comparison for each output result.		4	4	4	4	4	4	t_{CK}
t_{DFETM_Valid}	Time from end of CA DFE Training data comparison to valid result output.		-	20	-	20	-	20	t_{CK}
$t_{DFETM_RSP_Window}$	Duration of CA DFE Training output result signal pulse.		2	-	2	-	2	-	t_{CK}
$t_{DFETM_Pattern_Wait_Accel}$[13]	Time between de-assertion of DCS0_n for one pattern to DCS0_n assertion of the next pattern.	DFE Training Accelerator enabled.	64	-	64	-	64	-	t_{CK}
$t_{DFETM_Pattern_Wait}$[14]	Time between de-assertion of DCS0_n for one pattern to DCS0_n assertion of the next pattern.	DFE Training Accelerator disabled.	16	-	16	-	16	-	t_{CK}
t_{CSALT}	Chip select assertion before and after ALERT_n Pulse Width deassertion	Number of clock cycles between DCSx assertion and rising edge of ALERT_n when RW01[6] =1	8	-	8	-	8	-	t_{CK}
t_{CPDED}	Minimum time between SRE and DCS pulse to drive QCS LOW.	DCS[1:0]_n = HIGH; DRST_n = HIGH; DCK_t/DCK_c = Toggling.	Min: max(8 nCK, 5 ns); Max: (-)						t_{CK}

Table 190 — Input Timing requirements

Symbol	Parameter	Conditions	DDR5-3200/ 3600/4000		DDR5-4400		DDR5-4800		Unit
			Min	Max	Min	Max	Min	Max	
t_{PDEX}	Minimum time between PDE and PDX in the same rank.		Min: max(16 nCK, 10 ns); Max: (-)						t_{CK}
t_{RPDX}	Minimum time between RCD PDX and the next valid command other than DRAM Exit from PD.[15]		Min: max(16 nCK, 10 ns); Max: (-)						t_{CK}
$t_{CPDED2SRX}$	Minimum time from single DCS LOW pulse following SRE command to NOP (SRX) command	DCS[1:0]_n = LOW; DRST_n = HIGH.	Min: max(16 nCK, 10 ns); Max: (-)						t_{CK}
t_{CSSR}	Minimum DCS[1:0]_n LOW time (after SRE) when entering DCK stop.	DCS[1:0]_n = LOW; DRST_n = HIGH; DCK_t/DCK_c invalid.	Min: max(24 nCK, 15 ns); Max: (-)						ns
t_{CKoff}	Minimum time required after DCS[1:0]_n goes LOW following SRE command to DCK stop	DCS[1:0]_n = LOW; DRST_n = HIGH; DCK_t/DCK_c = Toggling.	Min: max(24 nCK, 15 ns); Max: (-)						ns
$t_{SRX2SRX}$	Minimum number of valid input clock cycles between SRX command to release QCS and SRX to take DRAM out of Self Refresh	DB control interface disabled (RW09[3] = 0).	Min: max(16 nCK, 10 ns); Max: (-)						t_{CK}
t_{DFE_PRD}	Minimum time from static HIGH or Valid DCA[6:0]/DPAR before initial DCS_n assertion	DFE Enabled during Reset with Stable Power (Figure 24) or Self Refresh Exit (Figure 26).	Min: max(8 nCK, 5 ns); Max: (-)						t_{CK}
$t_{DCSLHSK1}$	Maximum delay between any DCSx_n in LOW-to-HIGH transition from Initialization or Exit from Self Refresh With Clock Stop		200						ns
$t_{DCSLHSK2}$	Maximum delay between DCS0_n and DCS1_n (within the same sub-channel) in LOW-to-HIGH transition from Initialization or Exit from Self Refresh With Clock Stop		500						ps
t_{XS}	DRAM Exit Self Refresh to next valid command not requiring DLL		See DDR5 DRAM Specification						
t_{RINIT1}	Minimum DRST_n LOW time after completion of voltage ramp.		200	-	200	-	200	-	µs
	Minimum DRST_n LOW time with stable power.		1	-	1	-	1	-	µs
t_{RINIT2}	Min DCS_n LOW time to DRST_n HIGH.		20	-	20	-	20	-	ns
t_{RINIT3}	Minimum DCS LOW time after DRST_n HIGH.		20	-	20	-	20	-	ns
t_{CKACT}	Maximum time from DCS_n transition HIGH to start of valid DCK.		-	16	-	16	-	16	t_{CK}
t_{XPR}	DRAM minimum time from Exit Reset to first valid Configuration Command		Min: max(5 nCK, t_{RFC}(min) + 10 ns); Max: (-), See DDR5 DRAM Specification						ns
t_{ZQCAL}	ZQ Calibration Time		1	-	1	-	1	-	µs
t_{ZQLAT}	ZQ Calibration Latch Time		Min: max(30 ns, 8 nCK); Max: (-)						ns

1. Including SSC according Table 197, "SSC and PLL Loop Filter Characteristics".
2. All specified timing parameters apply
3. Timing parameters specified for frequency band 2 apply
4. Since RW0A, RW0B, RW0C, RW0D affect output driver operation, it is necessary for these settings to be updated during initialization when Bits OP[1] and OP[3] in RCD control word RW01 are still configured to block all commands at the DRAM and Data Buffer interfaces, respectively.
5. When Vref settings for DLBD, DLBS, DERROR_IN_n, DCA[6:0], DPAR, and DCS[1:0]_n are updated, it is necessary to meet the Vref settling times defined in Table 192 in addition to meeting t_{MRD_L}.

6. Applies to the timing between MRW to RW5E or RW5F in RCD space and MRW to MR63 in DRAM space only during an RCD Control Word Read sequence, otherwise this parameter does not apply to RW5E or RW5F.
7. A t_{STAB} waiting time is required when changing the setting in RW00[0] (Command Address SDR/DDR Rate selection), RW05[3:0] (RDIMM Operating Speed), RW05[7] (Frequency Band Select), and RW06 (Fine Granularity Operating Speed).
8. When exiting from RW In-Band Update mode (i.e., when writing a 1 to RW32[7]), it is necessary to meet the $t_{RWUPDExit}$ timing parameter defined in Table 190 in addition to meeting t_{MRD_L2}.
9. This parameter also applies to control words inside the DDR5DB01 device. Refer to JESD82-521 for details.
10. This parameter also covers the exit latency if exit is triggered through SMBus operation.
11. As shown in Figure 121 on page 247, this is the minimum guaranteed LOW pulse (i.e., below $[V_{OH} + V_{OL}]/2$, where V_{OH} and V_{OL} are the measured Logic HIGH and LOW DC voltage levels) into the test load. Logically, the minimum pulse width out of the RCD in DCS or DCA training modes is four DCK clock cycles wide.
12. For the double CS Exit the corresponding Host Interface TM selection in RW02 will be reset to default (Normal Operating Mode).
13. When the DFE Training Acceleration is enabled, the minimum waiting time between de-assertion of DCS0_n for one pattern and assertion of DCS0_n of the next pattern is determined by the larger of tDFETM_Pattern_Wait_Accel [min] specified in this table and the minimum settling time for the parameter setting updated by the Training Accelerator logic (e.g. for DFE_Vref or VrefCA, the minimum settlingtime could be much larger than tDFETM_Pattern_Wait_Accel [min]).
14. When the DFE Training Acceleration is disabled, there is a different minimum spacing between patterns, since there is no need to account for automated parameter changes.
15. During the t_{RPDX} window, the logic levels for QACA[13:0] and QBCA[13:0] outputs are not deterministic as the RCD transitions from disabled DCA[6:0] & DPAR receivers to normal operation. During this time, the host is allowed to take a memory rank still in PDE out of power-down state using one DCS_n pulse, but it must refrain from sending any additional commands to any memory rank that has already received its first PDX CS_n pulse. By the end of the t_{RPDX} window, the DDR5RCD01 device is required to forward any legal command from the DCA[6:0] inputs to the QxCA[13:0] and BCOM[2:0] outputs as defined in normal operation requirements.

10.3 Output Timing Requirements

Table 191 — Output timing requirements[1]

Symbol	Parameter	Conditions	DDR5-3200 to 4800		Unit	Note
			Min	Max		
t_{PDM}	Propagation delay, single bit switching; DCK_t/DCK_c falling edge crosspoint to output	1.1 V Operation, DDR Mode (RW00[0] = 1)	0.95	1.25	ns	2
t_{PDM2N}	Propagation delay, single bit switching; DCK_t/DCK_c rising edge crosspoint to output	1.1 V Operation, SDR Mode (RW00[0] = 0)	0.95	1.25	ns	3
t_{PDM_LB}	Propagation delay; External Loopback signals	1.1 V Operation	-	2	ns	4
tQLBSL	Loopback QLBS Output Low Time	1.1 V Operation, DDR Mode (RW00[0] = 1)	TBD	-	t_{CK}	5
tQLBSH	Loopback QLBS Output High Time	1.1 V Operation, DDR Mode (RW00[0] = 1)	TBD	-	t_{CK}	5
tQLBS2Q	Loopback QLBS to QLBD Skew	1.1 V Operation	-	0.15	t_{CK}	
tQLBDH	Loopback QLBD Output Hold Time	1.1 V Operation, DDR Mode (RW00[0] = 1)	TBD	-	t_{CK}	5
tQLBDVW	Loopback QLBD Valid Window (tQLBDH - tQLBS2Q)	1.1 V Operation, DDR Mode (RW00[0] = 1)	TBD	-	t_{CK}	5
tDCK2QLBS	Internal Loopback Propagation Delay from Rising (RW26[7] = 0) or Falling (RW26[7] = 1) DCK crossing point to the Corresponding QLBS Rising Edge	1.1 V Operation, DDR Mode (RW00[0] = 1)	-	10	t_{CK}	5
t_{QSK}	Total magnitude of Qn Output to Output Clock tolerance within the same A or B group (in the same unit) $t_{QSK} = t_{QSK_static} + t_{QSK_dynamic}$	Across the supported voltage-temperature range and with SSO conditions and pattern dependence included	0	0.385	t_{CK}	6,7
t_{QSK_static}	Magnitude of Qn Output to Output Clock tolerance within the same A or B group (in the same unit) under **quiet conditions**	Measured with quiet conditions, only one output switching, and nominal V-T conditions of V_{DD} = 1.1 V and 25°C	0	0.3	t_{CK}	7,8
$t_{QSK_dynamic}$	Magnitude of t_{QSK} change (additive to t_{QSK_static}) under **noisy conditions**	Across the supported voltage-temperature range and with SSO conditions and pattern dependence included	0	0.085	t_{CK}	7,9,10
t_{Q2Q}	Earliest Qn Output to Latest Qn Output Skew Tolerance, using the DCK differential signal at 0.0 V as the common reference, within the same A or B group (in the same unit)	Measured with quiet conditions, only one output switching, and nominal V-T conditions of V_{DD} = 1.1 V and 25°C	0	0.15	t_{CK}	7,10,11
t_{Qerr}	Total magnitude of t_{QSK} error $t_{Qerr} = 2 \times t_{QSK_dynamic} + t_{Q2Q}$	Across the supported voltage-temperature range and with SSO conditions and pattern dependence included	0	0.25	t_{CK}	7,10
t_{ALERT}	ALERT_n propagation delay	DERROR_IN_n LOW to ALERT_n LOW	-	2	ns	12
t_{ALERT_HL}	ALERT_n assertion delay from DCK_t/ DCK_c	DCK_t/DCK_c to ALERT_n LOW	-	1.5	ns	13
t_{RST}	RESET propagation delay	DRST_n LOW to QRST_n LOW	-	20	ns	
t_{QDIS}	Output buffers (except for QxCK_t/QxCK_c, QxCSn) hi-z after QCS[1:0]_n goes LOW following SRE command.	QCS[1:0]_n = LOW; DRST_n = HIGH; DCK_t/DCK_c = toggling.	2	-	t_{CK}	
$t_{SRX2QCK}$	Number of cycles from NOP command to release QCS to QCK clocks running and QCS driven HIGH.	DRST_n = HIGH; DCK_t/DCK_c = Toggling	-	16 + t_{PDM}	t_{CK}	
t_{CASRX}	QCA HIGH to QCS HIGH when exiting Self-Refresh		0	-	ns	
t_{ODU}	Output Delay Update time	OP7 = 1 for RW12 to RW1E	-	100	ns	14

1. See diagram (Figure 122, "Test Load," on page 248).
2. See diagram (Figure 7, "One UI DRAM Command Timing Diagram" on page 15). t_{PDM} is defined for 0 nCK command latency adder (RW11[2:0] = '000'), default (Moderate) output slew rate control settings in RW0E and RW0F, and output delay features are all enabled in RW12 - RW1A but set to zero delay.
3. t_{PDM} for SDR mode is measured from DCK_t/DCK_c rising edge cross point to output.
4. Applies to External Loopback Only (RW26[2:0] = '011' or '100').
5. Applies to Internal Loopback Only (RW26[2:0] = '001' or '010').

6. This skew represents the absolute Qn skew compared to the output clock QxCK and contains the register pad skew, clock skew, package routing skew and SSO noise (See Figure 10, “Qn Output Skew,” on page 16). The output clock jitter is not included in this skew. The measurement is averaged. The Qn output can be either early or late relative to the output clocks in the channel. For outputs QxCA[13:0]_N, QxCS[1:0]_N_n, this parameter applies to each of the two A/B output groups independently per channel. This parameter also applies to the BCOM[2:0]_N and BCS_N_n outputs w.r.t. to the output clock BCK_N.
7. The values for this parameter are defined for default settings in the output delay control words RW12 to RW1E and default settings in the driver characteristics and slew rate control words RW0A through RW0F.
8. This skew represents the absolute Qn skew compared to the output clock QxCK and contains the register pad skew, clock skew, and package routing skew at nominal V-T conditions of VDD = 1.1 V and 25°C (See Figure 10, “Qn Output Skew,” on page 16). The output clock jitter is not included in this skew. The measurement is averaged. The Qn output can be either early or late relative to the output clocks in the channel. For outputs QxCA[13:0]_N, QxCS[1:0]_N_n, this parameter applies to each of the two A/B output groups independently per channel. This parameter also applies to the BCOM[2:0]_N and BCS_N_n outputs w.r.t. to the output clock BCK_N. In this test, a single output signal switches with clock-like pattern of repeating 6 “1s” and 6 “0s” while all other outputs remaining stable (HIGH).
9. $t_{QSK_dynamic}$ represents the largest change in output skew (relative to t_{QSK_static}) within an output signal group in either direction (i.e., Early signals moving to an earlier time or Late signals moving to a later time). The output clock jitter is not included in this skew. The measurement is averaged. In this test, all outputs send patterns simultaneously to excite realistic on-die noise and crosstalk.
10. t_{Qerr} imposes an additional constraint on the maximum value for the total of 2 x $t_{QSK_dynamic}$ + t_{Q2Q} measured per individual unit. The device shall meet t_{Qerr}(max) in addition to meeting $t_{QSK_dynamic}$(max) and t_{Q2Q}(max).
11. This parameter represents the absolute Qn skew between earliest and latest signals within the same A/B group and contains the register pad skew and package routing skew (See Figure 10, “Qn Output Skew,” on page 16). The measurement is averaged. For outputs QxCA[13:0]_N, this parameter applies to each of the two A/B output groups independently per channel. Similarly, for outputs QxCS[1:0]_N_n, this parameter applies to each of the two A/B output groups independently per channel. This parameter also applies to the {BCOM[2:0]_N, BCS_N_n} output groups independently per channel. In this test, a single output signal switches with clock-like pattern of repeating 6 “1s” and 6 “0s” while all other outputs remaining stable (HIGH).
12. See Figure 119, “Voltage waveforms, tALERT Measurement,” on page 247.
13. See Figure 122, “Test Load,” on page 248 and .Figure 120, “Voltage waveforms, tALERT_HL Measurement,” on page 247
14. This is the time the RCD requires to update delay timing setting to the output after it receives RW write.

11 VrefCA and Vref CS Specifications

The internal VrefCA and VrefCS specifications parameters are Vref operating range, Vref step size, Vref set tolerance, Vref step time and Vref valid tolerance.

The Vref operating range specifies the minimum required Vref setting range for DDR5RCD01 devices and is specific by a Vref min operating point and a Vref max operating point, as depicted in Figure 62 below.

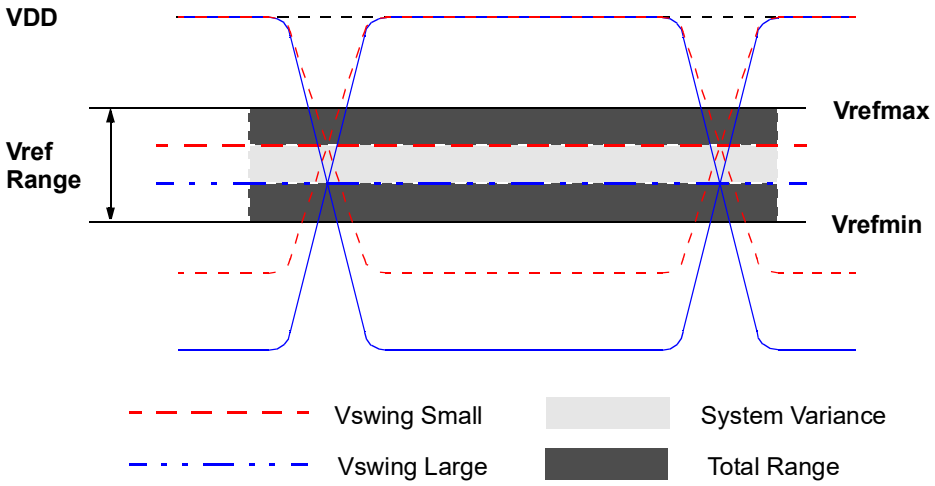


Figure 62 — Vref operating range (Vrefmin, Vrefmax)

The Vref step size is defined as the target voltage between adjacent steps. For a given design, the DDR5RCD01 VrefCA and VrefCS step size must be within the range specified.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two parameters for Vref set tolerance uncertainty for different numbers of steps n. The Vref set tolerance is measured with respect to the ideal line which is based on two endpoints, where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the step size and Vref set tolerance is shown in Figure 63

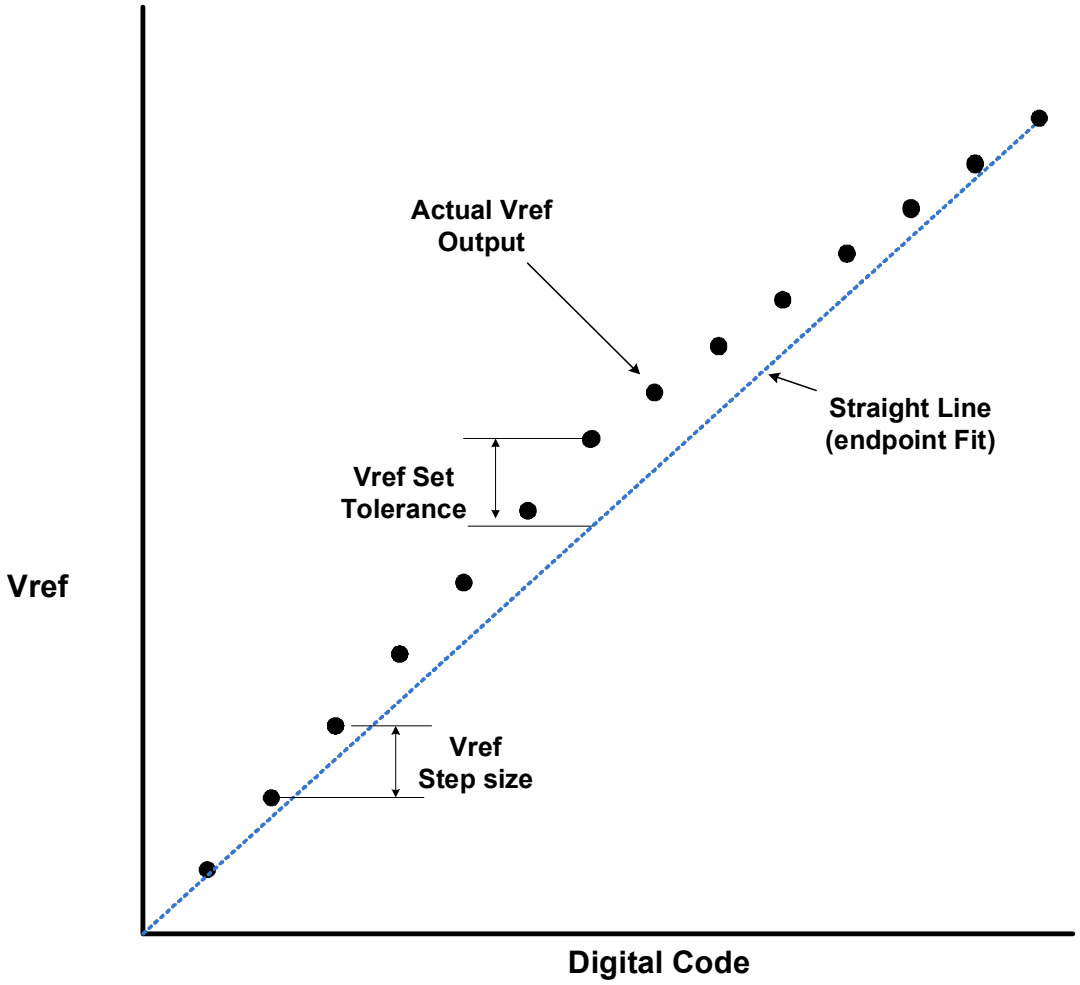


Figure 63 — Example of Vref set tolerance (max case only shown) and step size

The Vref increment/decrement step times are defined by Vref_time. Vref_time is defined from t0 to t1 as shown in Figure 64 below where t0 is referenced to when the RW write occurs and t1 is referenced to when the Vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val_tol to qualify the step time t1 as shown in Figure 65. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for component level validation/characterization.

Vref_time is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to RW write command clock

t1 - is referenced to the Vref_val_tol

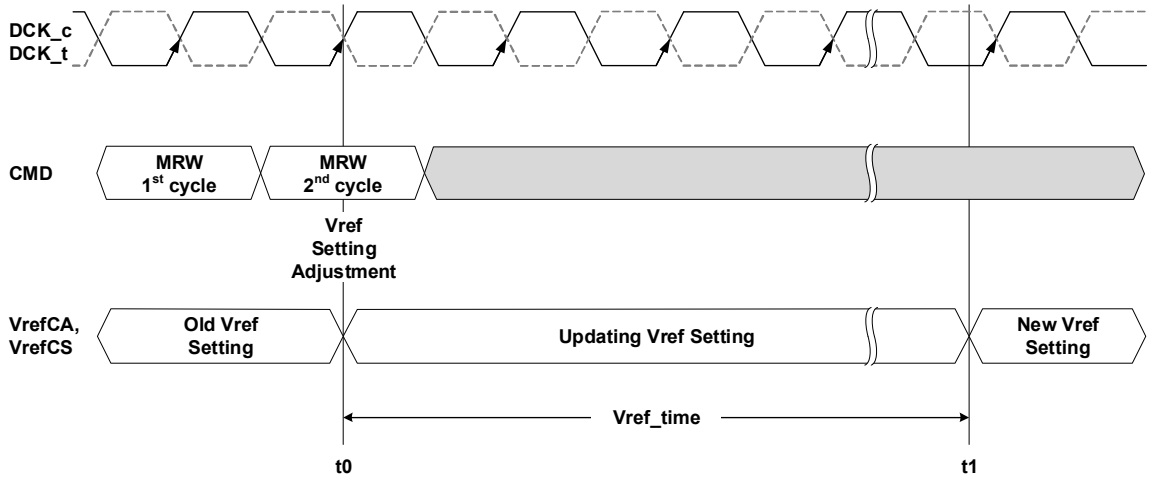


Figure 64 — Vref_time timing diagram

An MRW write to the (Internal Vref Control Word) is used to program the Vref value.

The minimum time required between two Vref MRW commands is Vref_time for single step and Vref_time for a full voltage range step.

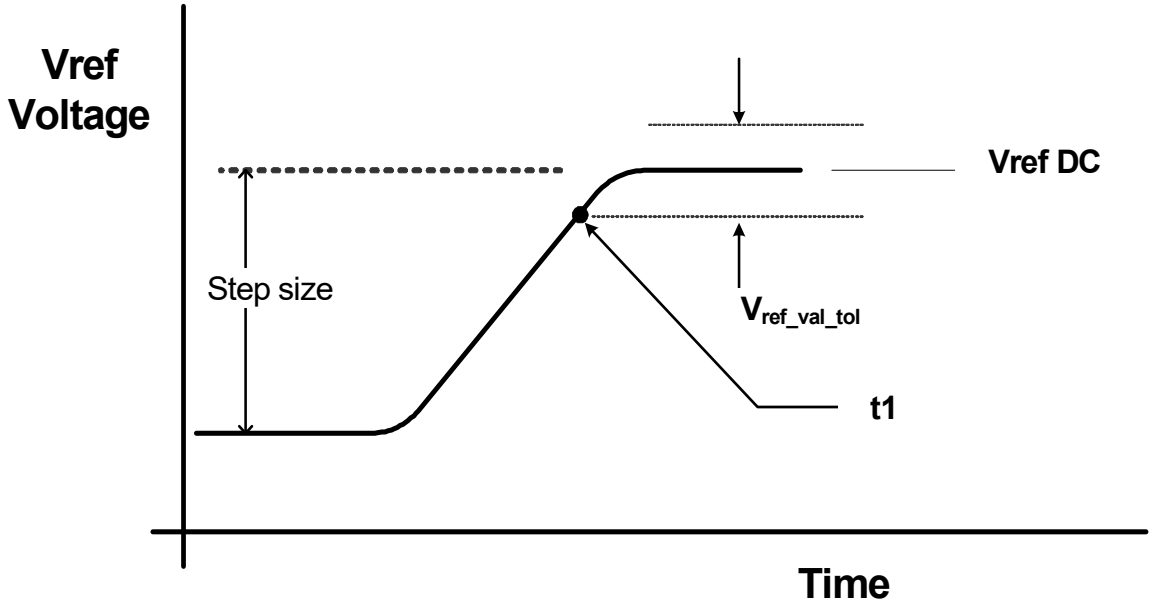


Figure 65 — Vref step single step size increment case

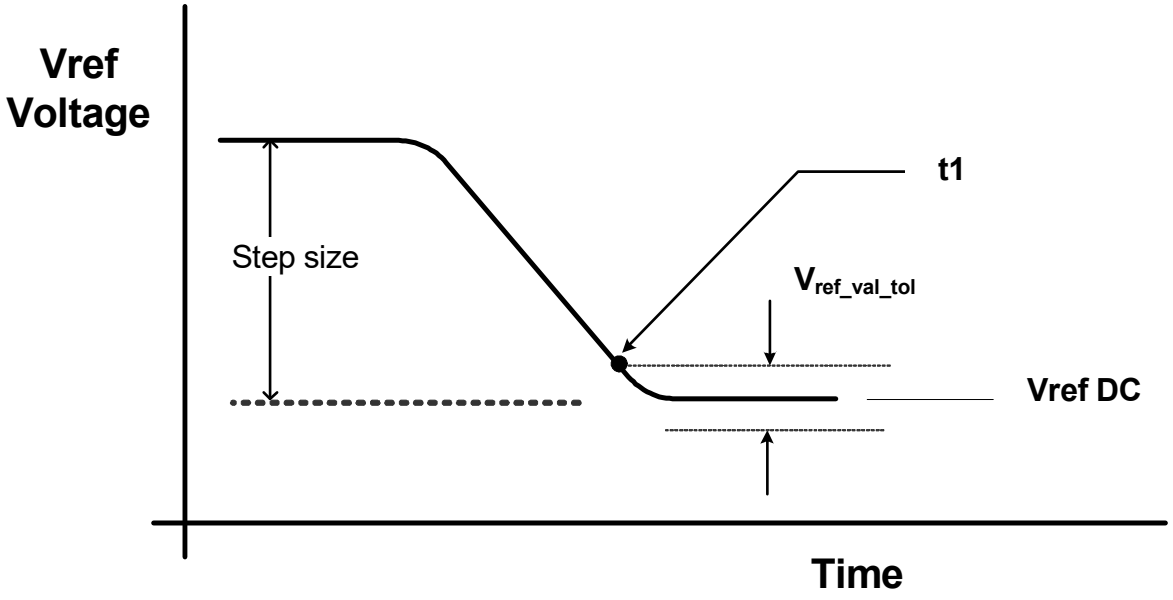


Figure 66 — Vref step single step size decrement case

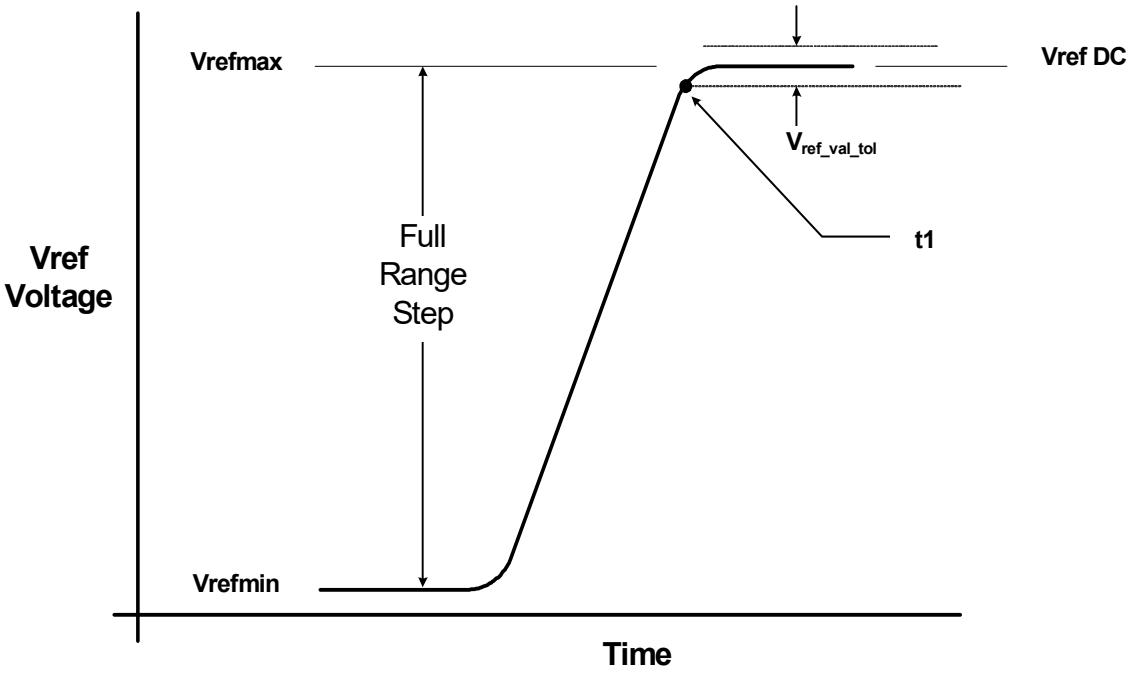


Figure 67 — Vref full step from Vrefmin to Vrefmax case

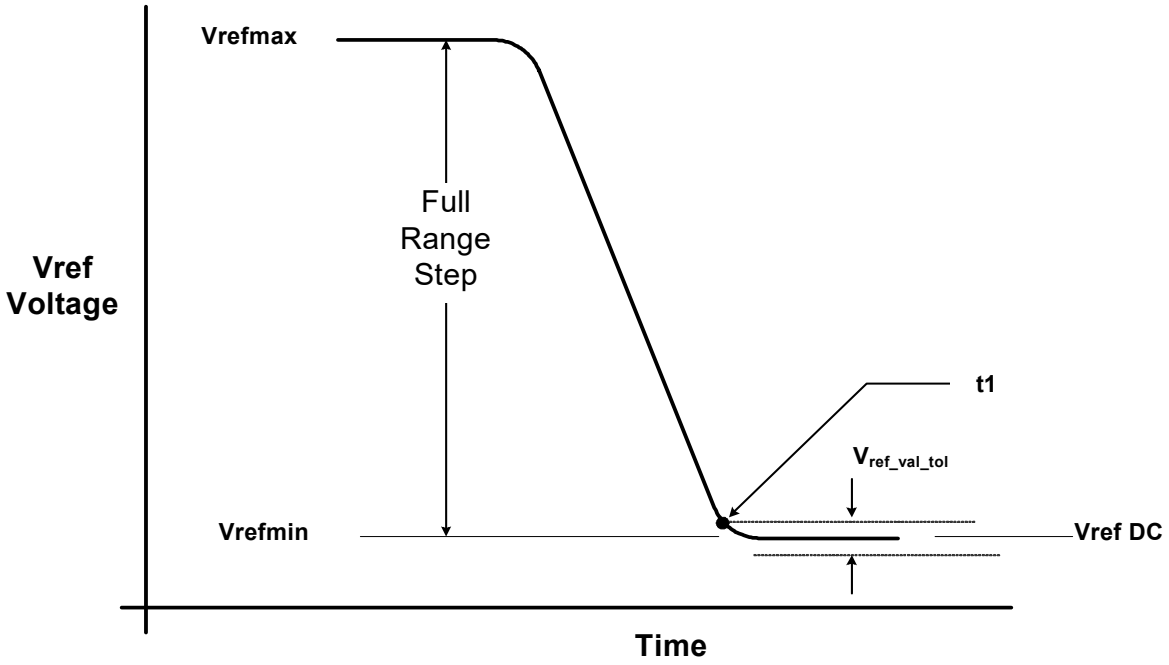


Figure 68 — Vref full step from Vrefmax to Vrefmin case

Table 192, "Internal VrefCA & VrefCS Specifications" below contains the internal VrefCA specifications that will be characterized at the component level for compliance. The characterization method is defined in a separate specification.

Table 192 — Internal VrefCA & VrefCS Specifications

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Vref Max Operating Point	Vref_max	97.5%	-	-	V_{DD}	1
Vref Min Operating Point	Vref_min	-	-	45%	V_{DD}	1
Vref Step size	Vref_step	0.41%	0.50%	0.59%	V_{DD}	2
Vref Set Tolerance	Vref_set_tol_long	-1.625%	0.0%	1.625%	V_{DD}	3, 4, 6
	Vref_set_tol_short	- 0.15%	0.0%	0.15%	V_{DD}	3, 5, 7
Vref Step Time	Vref_time_short	-	-	300	ns	8, 9
	Vref_time_long	-	-	500	ns	8, 9
Vref Valid Tolerance	Vref_val_tol	- 0.15%	0.0%	0.15%	V_{DD}	

NOTE 1 Vref DC voltage referenced to VDD.
NOTE 2 Vref step size increment/decrement range. Vref at DC level. Vref_step(avg) = (Vref_max - Vref_min)/ 105.
NOTE 3 Vref_new = Vref_old + n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-".
NOTE 4 The minimum value of Vref setting tolerance = Vref_new - 1.625%*VDD. The maximum value of Vref setting tolerance = Vref_new + 1.625%*VDD. For n>4.
NOTE 5 The minimum value of Vref setting tolerance = Vref_new - 0.15%*VDD. The maximum value of Vref setting tolerance = Vref_new + 0.15%*VDD. For n< 4.
NOTE 6 Measured by recording the min and max values of the Vref output over the full range, drawing a straight line between those points and comparing all other Vref output settings to that line
NOTE 7 Measured by recording the min and max values of the Vref output across 4 consecutive steps (n=4), drawing a straight line between those points and comparing all other Vref output settings to that line
NOTE 8 Time from MRW command to Vref stable. Applicable for component level test/characterization purposes. Vref valid is to qualify the step times which will be characterized at the component level.
NOTE 9 The maximum value of VrefCA or VrefCS step time = 300 ns for n < 16 and 500 ns for n ≥ 16, where n = number of steps.

11.1 DFE_Vref INL Tolerance

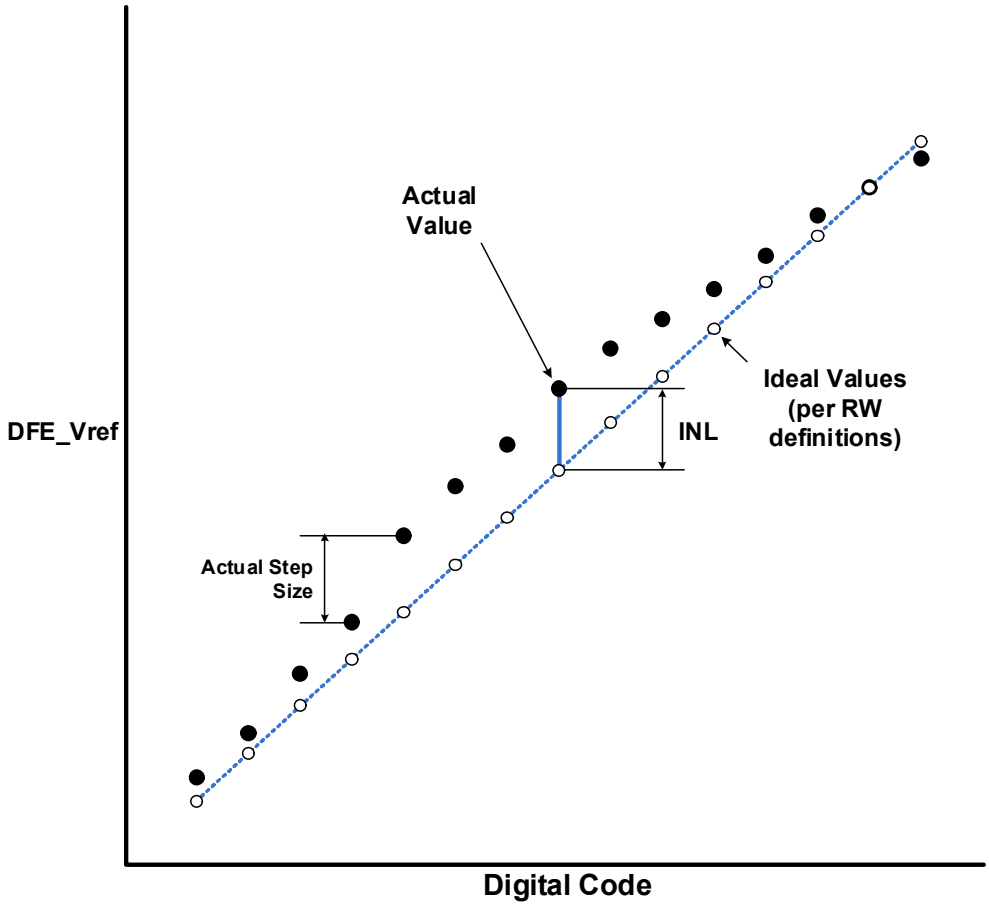


Figure 69 — Example of DFE_Vref INL Tolerance

Integral nonlinearity (INL) is the deviation between effective analog values and expected ideal values for the corresponding settings in Receiver DFE_Vref Control words as defined in RW3F and PG02RW[62, 66, 6A,6E, 72, 76,7A, 7E].

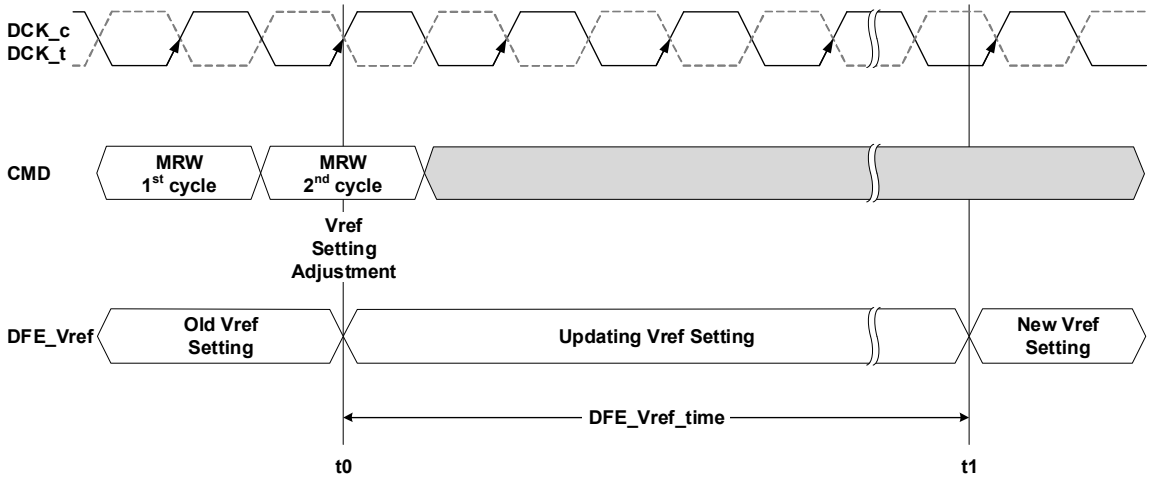


Figure 70 — DFE_Vref_step time timing diagram

An MRW write to the (Internal Vref Control Word) is used to program the Vref value.

The minimum time required between two DFE_Vref MRW commands is DFE_Vref Step Time.

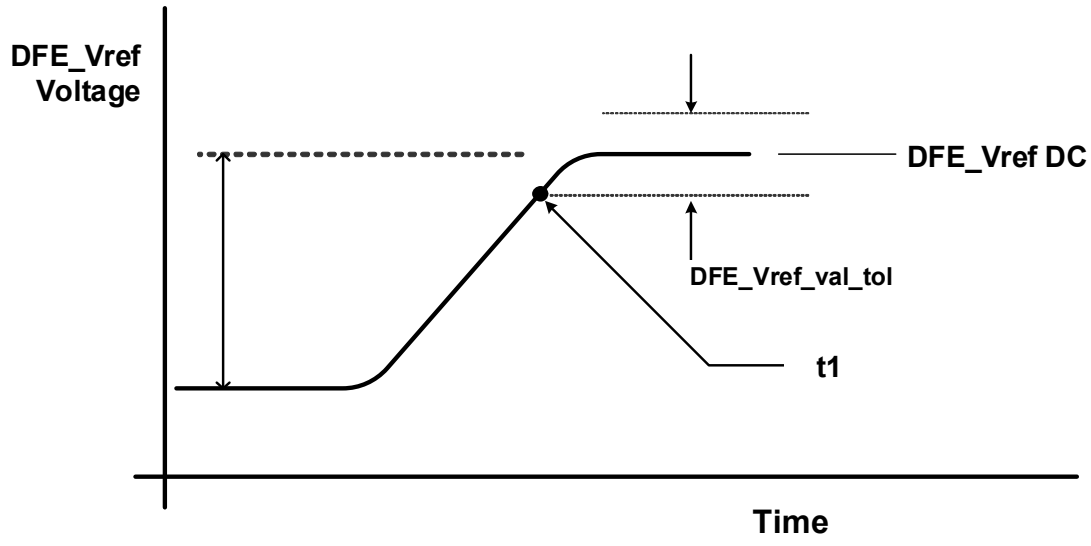


Figure 71 — DFE_Vref Increment Case

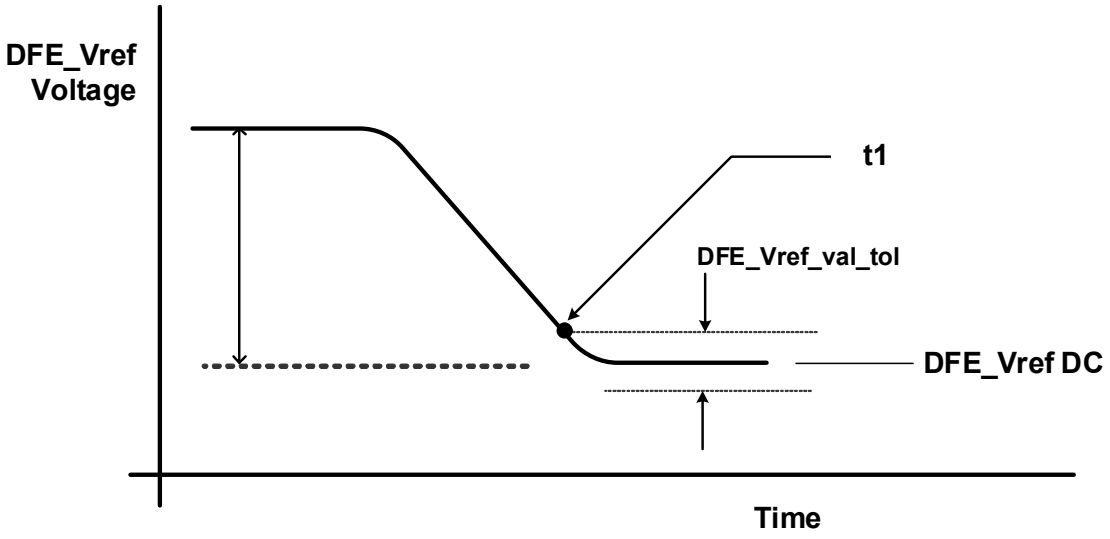


Figure 72 — DFE_Vref Decrement Case

Table 193 below contains the DFE Training Vref specifications that will be characterized at the component level for compliance. The characterization method is defined in a separate specification.

Table 193 — DFE_Vref Specification

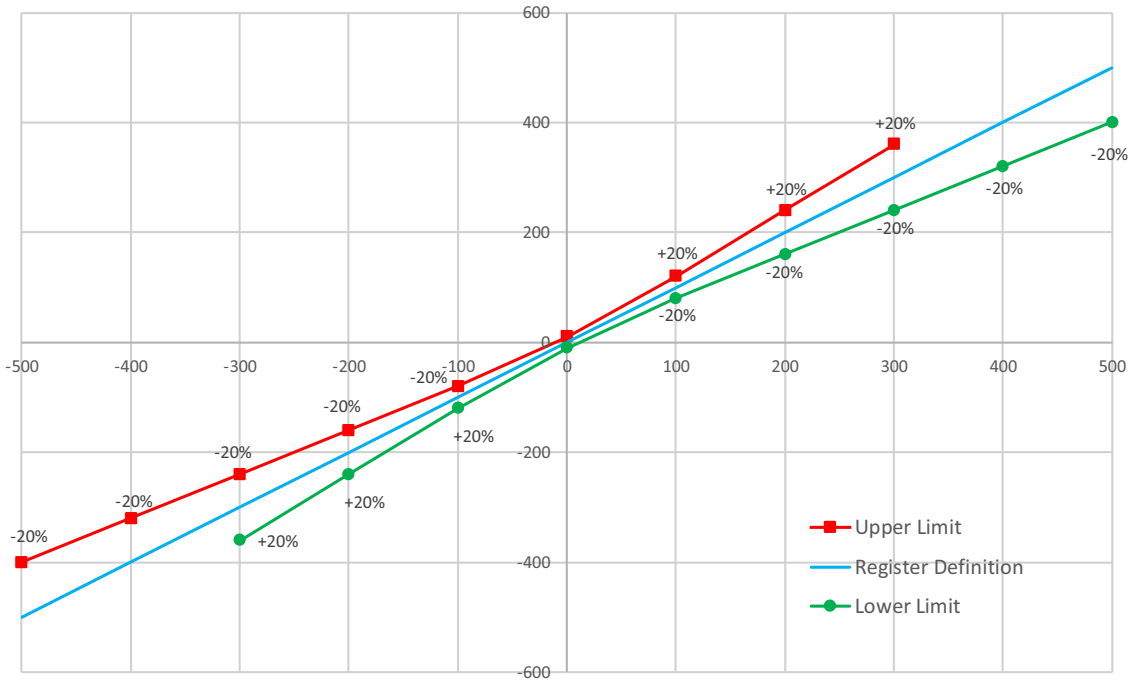
Parameter	Symbol	Min	Typ	Max	Unit	NOTE
DFE_Vref Step Time Short	DFE_Vref_Short_16	-	-	200	ns	1, 2
	DFE_Vref_Short_32	-	-	300	ns	1, 3
DFE_Vref Step Time Long	DFE_Vref_Long	-	-	600	ns	1, 4
DFE_Vref Valid Tolerance	DFE_Vref_val_tol	-1.65	0	1.65	mV	1

NOTE 1 Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is used to qualify the step times which will be characterized at the component level.
NOTE 2 The maximum value of DFE_Vref step time = 200 ns for n < 16, where n = number of steps.
NOTE 3 The maximum value of DFE_Vref step time = 300 ns for 16 ≤ n < 32, where n = number of steps.
NOTE 4 The maximum value of DFE_Vref step time = 600 ns for n ≥ 32, where n = number of steps.

Table 194 — DFE_Vref INL Tolerance

DFE_Vref Setting	Lower Limit	Upper Limit	NOTE
- 500 mV ~ 300 mV	-	V_ideal * 80%	1,3,4
- 300 mV ~ 0 mV	Min(V_ideal * 120%, V_ideal – 4 * LSB)	Max(V_ideal * 80%, V_ideal + 4 * LSB)	1,2,3,4
0 mV ~ + 300 mV	Min(V_ideal * 80%, V_ideal – 4 * LSB)	Max(V_ideal * 120%, V_ideal + 4 * LSB)	1,2,3,4
+300 mV ~ + 500 mV	V_ideal * 80%	-	1,3,4

NOTE 1 V_ideal refers to the ideal DFE_Vref value based on the setting.
NOTE 2 LSB is 2.5mV.
NOTE 3 DFE_Vref must be monotonic.
NOTE 4 The range values specified in the table are applicable for default VrefCA and DFE Gain Offset setting, under VDD = 1.1V and 25°C ambient temperature.



X axis = ideal control word setting value
Y axis = actual implementation value

Figure 73 — Illustration Example of DFE_Vref INL Tolerance

11.2 Measurement Steps

1. Make sure VrefCA are at default setting, DFE_Vref setting is 0, power supply is 1.1V. Configure Margin Monitor RW32[2:0] to 3'b001.
2. Sweep input signal from 1.1 V to 0 V to find the lowest level for HIGH and record this input signal HIGH level as V1 when HIGH-to-LOW transition starts.
3. Sweep input signal from 0 V to 1.1 V to find the highest level for LOW and record this input signal LOW level as V2 when LOW-to-HIGH transition starts.
4. Transition level V = (V1 + V2)/2.
5. Set DFE_Vref, wait for DFE_Vref_Step_Time to let the new setting settle.
6. Repeat steps 2 ~ 4, to get a new transition level V'.
7. Validate (V' - V) is within specification.
8. Repeat steps 2 ~ 7 until all the settings of DFE_Vref are measured.

11.3 DFE Tap Coefficient and Gain Adjustment tolerances (DNL and INL)

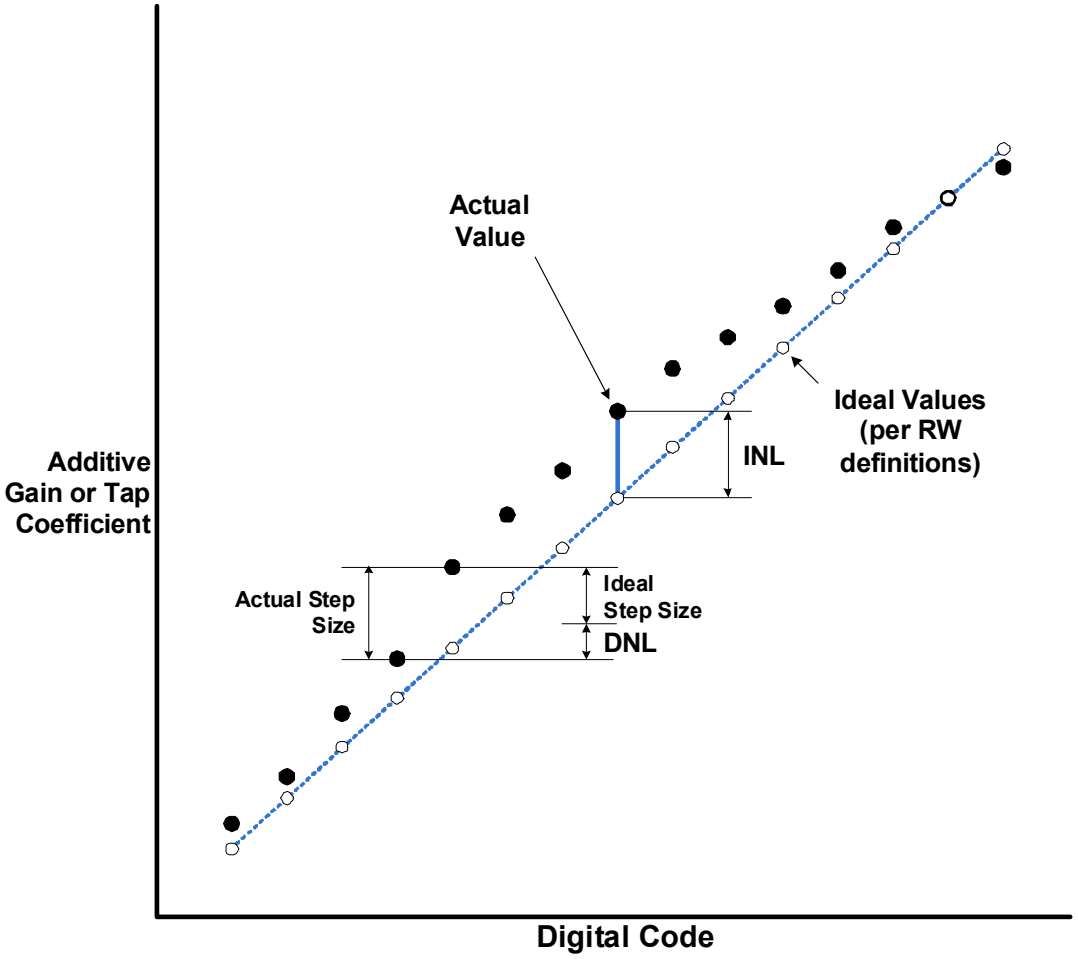


Figure 74 — Example of Tap Coefficient and Gain Adjustment tolerances (DNL and INL)

Differential nonlinearity (DNL) is the deviation between effective and ideal control step sizes for any pair of analog values resulting from adjacent settings in Receiver DFE Tap Coefficient and Gain Adjustment control words as defined in PG[1:0]RW[7F:60].

Integral nonlinearity (INL) is the deviation between effective analog values and expected ideal values for the corresponding settings in Receiver DFE Tap Coefficient and Gain Adjustment control words as defined in PG[1:0]RW[7F:60].

12 AC & DC Global Definitions

12.1 Transmitter (Tx), Receiver (Rx) and Channel Definitions

Transmitter (Tx): Input to the transmitter is the DCA from the logical portion of the RCD Core and output is at the package pins. The normal components contained in the transmitter are, but not limited to, the pre-driver and the output driver with the transmitter package.

The DDR5 RCD uses a differential re driven clock-source, and single-ended CA.

The transmitter for a forwarded clock based source synchronous system must include specification and test methodology for low and high frequency random and deterministic jitter and duty cycle error and must take into account Bounded Uncorrelated Jitter (BUJ), Duty cycle error etc.

For single ended signaling cases, crosstalk and Simultaneous switching noise often impact the measurement of the Transmitter. Therefore, the Transmitter's decimated jitter component parameters and the BER must be specified.

Receiver (Rx): The normal components contained in the clock receiver are: (1) receiver package, (2) input amplifier (to receive the clock), and (3) optionally, a PLL and time adjustment circuitry. The data input receives the single ended data and measures it against a reference voltage. The difference between the received signal and reference voltage is then sampled. However, the link may need some form of receiver equalization at the speeds that the DDR5 link needs to operate. Since there may be no input eye margin at the receiver pin, the receiver equalization specification may be defined based on a virtual receive sampler/slicer. This means that components of the receiver, which have nothing to do with inter symbol interference (ISI), will have to be specified in such a way as to avoid the impact of ISI. Hence items like receiver jitter, receiver jitter sensitivity, receiver amplitude sensitivity, which are typically orthogonal to ISI, will have to be specified in an ISI free environment. Either the infrastructure, or the test methodology will ensure that the correct amount of ISI, or no ISI, as the case might be, for that specific Rx parameter is used. The validation of the receiver is also dependent on either loop-back of data being enabled or restricting to receiver testing to be dependent on a pre-specified set of patterns and the accompanying pattern checker and error counters. The Receiver equalization will be evaluated in the presence of a set of pre-specified receiver testing golden channels. These receiver testing golden channels will attempt to span the ISI range to which the receiver needs to be designed. The key measurement parameter in this test is the stressed eye and the receiver's error sensitivity to the stressed eye.

Channel: The channel is defined from the transmitter package pin to the receiver package pin and includes all the interconnect topology components included in the channel definition (connectors, sockets, and so on).However, this spec will not specify system platform level channel models, but restrict itself to specifying the Golden Reference Transmitter and Receiver evaluation channels.

Applicability:

The parameters defined in this section apply to the appropriate sections of the RCD irrespective of the system, platform or the topology of the system where the RCD is situated. The parameters, however, are defined separately for each of the speeds that the DDR5RCD01 is expected to operate at.

12.1.1 Bit Error Rate

Introduction

This section provides an overview of the Bit Error Rate (BER) and the desired Statistical Level of Confidence.

12.1.2 General Equation

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1-SLC) + \ln\left(\sum_{k=0}^{N}\frac{(n\cdot BER)^{k}}{k!}\right)\right]$$

Where:

n = number of bits in a trial

SLC = statistical level of confidence

BER = Bit Error Rate

k = intermediate number of specific errors found in trial

N = number of errors recorded during trial

If no errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER}\right)[-\ln(1-SLC)]$$

Testing to 99.5% confidence levels is recommended; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N = 0), using $BER = 10^{-9}$ and confidence level SLC = 99.5%, the result is $n = (1/BER)(-\ln(1 - 0.995)) = 5.298 \times 10^{9}$.

Results for commonly used confidence levels of 99.5% down to 70% are shown in Table 195.

Table 195 — Estimated Number of Transmitted Bits (n) for confidence level of 70% to 99.5%

Number of Error	$n = \ln(1 - SLC)/BER$							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/*BER*	4.61/*BER*	2.99/*BER*	2.3/*BER*	1.90/*BER*	1.61/*BER*	1.39/*BER*	1.20/*BER*

12.1.3 Minimum Bit Error Rate (BER) Requirements

Table 196 specifies the UI_{AVG} and Bit Error Rate requirements over which certain receiver timing and voltage specifications need to be validated assuming a 99.5% confidence level at $BER = 10^{-9}$.

Table 196 — Minimum BER Requirements for RX and TX Timing and Voltage Tests

Symbol	Parameter	DDR5-3200 - 4800			Unit	NOTE
		Min	Nom	Max		
UI_{AVG}	Average UI	0.999* nominal	1.000/f	1.001* nominal	ps	1
$N_{MIN_UI_Validation}$	Number of UI (min)	5.3×10^9		-	UI	2
BER_{Lane}	Bit Error Rate	-		10^{-16}	Events	3, 4, 5, 6

NOTES:
1. Average UI size, "f" is data rate.
2. # of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER = 10^{-9}.
3. This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link layer based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.
4. Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5. This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx CA Voltage Sensitivity, Rx Clock Jitter Sensitivity, Rx CA Stressed Eye, Tx Clock Jitter, Tx QCA Jitter, and Tx QCA Stressed EH/EW specifications.
6. The BER for DDR5 during normal operation is 10^{-16}. For validation purposes, the BER used is 10^{-9}.

12.1.4 Unit Interval and Jitter Definitions

This document describes the UI and NUI Jitter definitions associated with the Jitter parameters specified in Rx Stressed Eye, Tx QCK Jitter, and Input Clock Jitter specifications.

12.1.5 Unit Interval

The times at which the differential crossing points of the clock occur are defined at $t_1, t_2, \ldots, t_{n-1}, t_n, \ldots, t_K$.

The UI at index "n" is defined as shown in Figure 75 (with $n = 1, 2, \ldots$) from an arbitrary time in steady state, where $n = 0$ is chosen as the starting crossing point.

Mathematical definition of UI is shown in Figure 75 and Figure 76.

$$UI_n = t_n - t_{n-1}$$

Figure 75 — UI Definition in Terms of Adjacent Edge Timings

For the Single-Ended data, the unit interval time starts when the signal crosses a pre-specified reference voltage. For the differential clock, the unit interval time starts when the DCK_t and DCK_c intersect (see Figure 76).

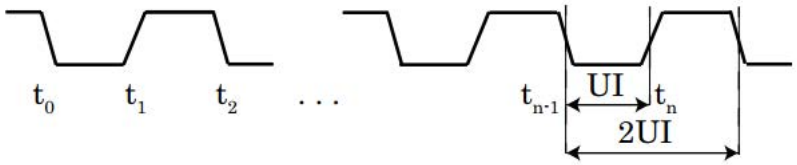


Figure 76 — UI definition Using Clock Waveforms

12.1.6 UI Jitter Definition

If a number of UI edges are computed or measured at times t_1, t_2, …, t_{n-1}, t_n, ... , t_K, where K is the maximum number of samples, then the UI jitter at any instance "n" is defined in Figure 77, where T = the ideal UI size.

$$\mathrm{UI}_{(jit)n} = (t_n - t_{n-1}) - T;\ n = 1, 2, 3, ..., K$$

Figure 77 — UI Jitter of the "nth" UI Definition (in terms of ideal UI)

In a large sample with random Gaussian-like jitter (therefore very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described in Figure 77 assumes starting from an instant of steady state, where $n = 0$ is chosen as the starting point. 1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded clock.

Example: For 6.4 GT/s signaling, the forwarded clock frequency is 3.2 GHz, or 1 UI = 156.25 ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (*BER*) for the link.

12.1.7 UI-UI Jitter Definition

UI-UI (read as "UI to UI") jitter is defined to be the jitter between two consecutive UI as shown in Figure 78.

$$\mathrm{UI}_n = \mathrm{UI}_n - \mathrm{UI}_{n-1};\ n = 2, 3, ..., K$$

Figure 78 — UI - UI Jitter Definitions

12.1.8 Accumulated Jitter (Over "N" UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive "N" UI as shown in Figure 79.

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1} (UI_p - \overline{UI}), \text{ where } m = 1, 2, ..., K\text{-}N$$

Figure 79 — Definition of Accumulated Jitter (over "N" UI)

where UI is defined in the equation shown in Figure 80.

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K}, \text{ where } p = 1, 2, ..., N, ..., K$$

Figure 80 — Definition of UI

13 Electrical - Input AC and DC Specifications

13.1 Input Clock Architecture

The RCD is provided a clock by the entity that is controlling it, i.e., memory controller, or any test equipment. This clock is used by the RCD to generate all the IO specific timing, and is the same clock used by the controlling entity as the one and only deterministic source of all the response timings to and from the RCD. This allows the memory controller to have a deterministic control of every event in the RCD. Spread Spectrum Clocking (SSC) Capability

13.1.1 Input Clock SSC and PLL Loop Filter

The system platform uses a reference clock, which is used to synthesize the RCD clock. Spread Spectrum Clock (SSC) with up to 0.5% down-spread in frequency must be supported by the clocking system. The frequency of the reference clock, and therefore bit rate, can be modulated from 0% to –0.5% of the nominal data rate/frequency at a modulation rate in the range of 30 KHz to 33 KHz. The modulation profile of SSC must provide optimal or close to optimal EMI reduction. Typical profiles include a triangular profile. The RCD must ensure that it functions normally even in the presence of SSC and truthfully lets SSC related components pass through to its output signals.

Table 197 — SSC and PLL Loop Filter Characteristics

Symbol	Parameter	Conditions	DDR5-3200 to 4800		Unit
			Min	Max	
f_{SSC}	SSC modulation frequency[1]		30	33	KHz
a_{SSC}	SSC amplitude[1]		0	-0.5	%
f_{band}	PLL loop bandwidth[2]	-3dB bandwidth[3]	0.01 x f_{clock}	-	MHz

1. The DDR5RCD01 must meet all parameters defined in this specification while supporting input clock SSC requirements described in this table
2. The DDR5RCD01 PLL must fulfill this loop filter requirement in order to track typical system clock synthesizer output clock signals
3. Implies a jitter peaking of <3 dB

13.1.2 Input Single-ended Swing Requirements for Differential Clock

TBD

13.1.3 Input Slew Rate for Differential Clock

Input slew rate for differential signals DCK_t/DCK_c are defined and measured as shown below.

Table 198 — Differential Input Slew Rate Definition for DCK_t/DCK_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
V_{IHdiff_CK}	Differential Input High	0.75 * V_{DIFFpp}	-	mV	1, 2, 3, 4
V_{ILdiff_CK}	Differential input Low	-	0.25 * V_{DIFFpp}	mV	1, 2, 3, 4

NOTE 1 Clock V_{DIFFpp}, V_{ILdiff_CK} and V_{IHdiff_CK} are defined in Figure 81.
NOTE 2 V_{DIFFpp} is the mean HIGH voltage minus the mean LOW voltage over 1e6 samples.
NOTE 3 Differential signal rising edge from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic slope.
NOTE 4 Differential signal falling edge from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic slope.

Table 199 — Differential Input Slew Rate DCK_t/DCK_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
SRIdiff	Differential Input Slew Rate	2	18	V/ns	1

NOTE 1 All parameters are defined over the entire clock common mode range.

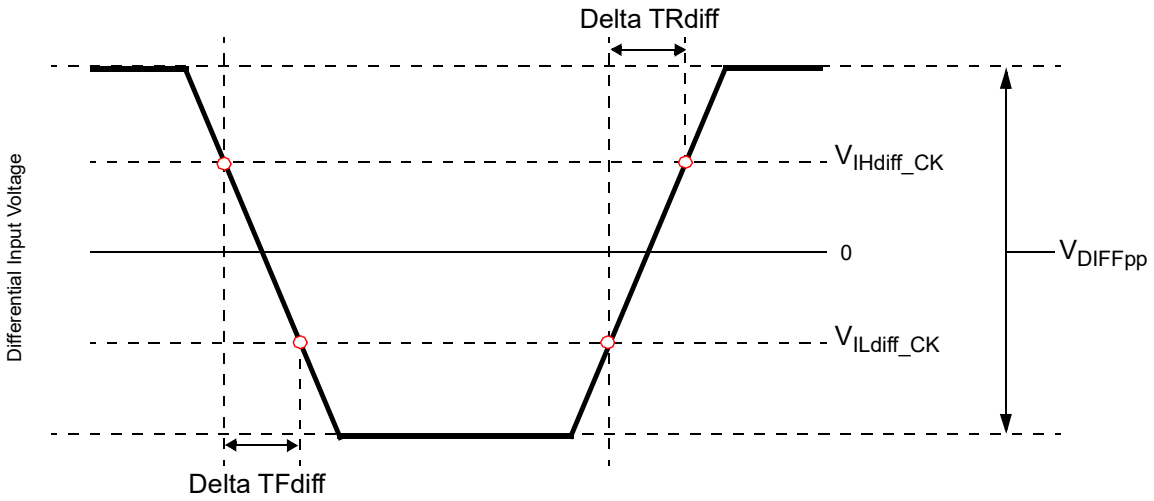


Figure 81 — Differential Input Slew Rate Definition for DCK_t/DCK_c

13.1.4 Input Clock Differential Cross point voltage

To achieve tight CA Rx Mask input requirements as well as output skew parameters with respect to clock, the cross point voltage of differential input clock signals (DCK_t, DCK_c) must meet the requirements in Figure 82. The differential input cross point voltage VIX_CK (VIX_CK_FR and VIX_CK_RF) is measured from the actual cross point of DCK_t, DCK_c relative to the Vswing/2 of the DCK_t and DCK_c signals.

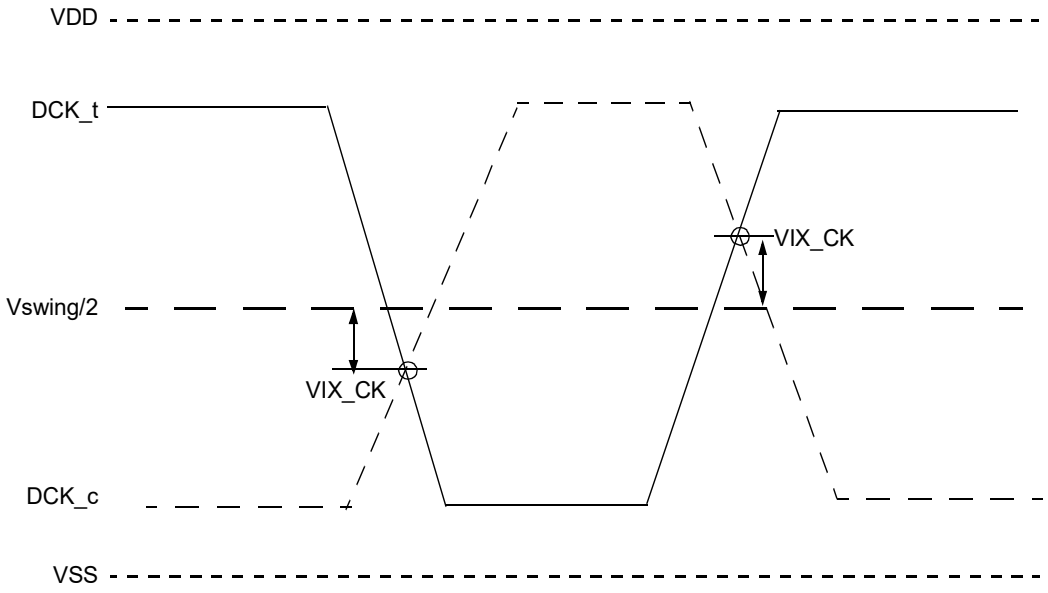


Figure 82 — Vix Definition (DCK)

Table 200 — Cross point voltage (VIX) for differential input signals (DCK)

Symbol	Parameter	DDR5-3200		DDR5-3600		DDR5-4000/4400/4800		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
VIX_CK_Ratio	Clock differential input crosspoint voltage ratio	-	25	tbd	tbd	tbd	tbd	%	1, 2

NOTE 1 The VIX_CK voltage is referenced to V_{swing}/2(mean) = (DCK_t voltage + DCK_c voltage) / 2, where the mean is over 1e6 UI.

NOTE 2 VIX_CK_Ratio = (VIX_CK / Vdiff) * 100%, where Vdiff = |DCK_t voltage – DCK_c voltage|.

13.2 Input Voltage Levels for DERROR_IN_n Signals

Table 201 — Input Voltage Levels for DERROR_IN_n Signals

Symbol	Parameter	Min	Max	Unit	NOTE
$V_{IH.ERROR}$	HIGH-level input voltage	Vref + 75	-	mV	1
$V_{IL.ERROR}$	LOW-level input voltage	-	Vref - 75	mV	1

NOTE 1 Vref refers to the target setting selected in Table 154, “RW4A: DERROR_IN_n Vref Control Word,” on page 155.

13.3 Overshoot and Undershoot Specifications

TBD

13.4 Input Bus Termination (IBT) Characteristics for DCA, DPAR, DCS, and DERROR_IN_n

A functional representation of the input bus termination is shown in Figure 83.

$$RTT = \frac{V_{DD} - V_{IN}}{|I_{IN}|}$$

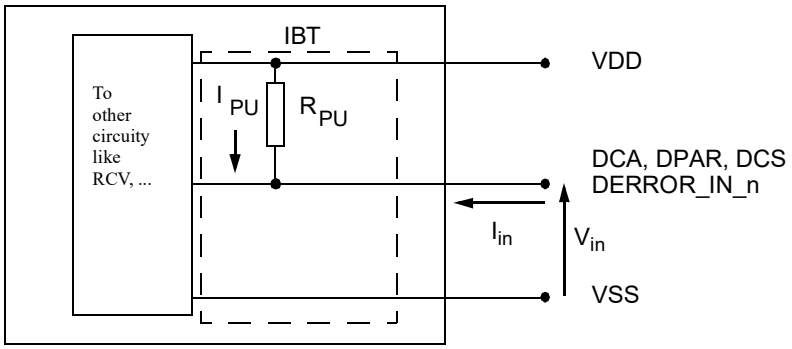


Figure 83 — Input Bus Termination: Definition of Voltages and Currents

The DDR5RCD01 device supports an effective Input Bus Termination Rtt value of 60 ohms (in addition to RTT_OFF).

Table 202 — IBT Electrical Characteristics for DCA, DPAR, DCS, and DERROR_IN_n

RTT	Vout	Min	Nom	Max	Unit	NOTE
60 Ω	VILdc= 0.5 * VDD	0.9	1	1.25	RZQ/4	1,2
	VIMdc= 0.8 * VDD	0.9	1	1.1	RZQ/4	1,2
	VIHdc= 0.95 * VDD	0.8	1	1.1	RZQ/4	1,2
DCA-DCA Mismatch within sub-channel	VIMdc = 0.8 * VDD	0	-	8	%	1,3,4

NOTE 1 For the behavior of the tolerance limits if temperature or voltage changes, see Section 14.5, “Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity,” on page 223.
NOTE 2 Applies to DCA[6:0]_[B:A], DPAR_[B:A], DCS[1:0]_[B:A]_n, and DERROR_IN_[B:A]_n.
NOTE 3 DCA to DCA mismatch within sub-channel variation for a given component including DCA[6:0], DPAR, and DCS[1:0]_n but excluding DERROR_IN_n (characterized).
NOTE 4 RTT variance range ratio to RTT Nominal value in a given component, including DCA[6:0], DPAR, and DCS[1:0]_n but excluding DERROR_IN_n.

$$\text{DCA-DCA Mismatch in a Sub-channel} = \frac{RTT_{MAX} - RTT_{MIN}}{RTT_{NOM}} \times 100$$

13.5 DLBD and DLBS Loopback Input Termination

The DDR5RCD01 device includes On-Die termination resistance for DLBD and DLBS Loopback inputs.

A functional representation of the on-die termination is shown in Figure 84.

$$RTT = \frac{V_{DD} - V_{IN}}{|I_{IN}|}$$

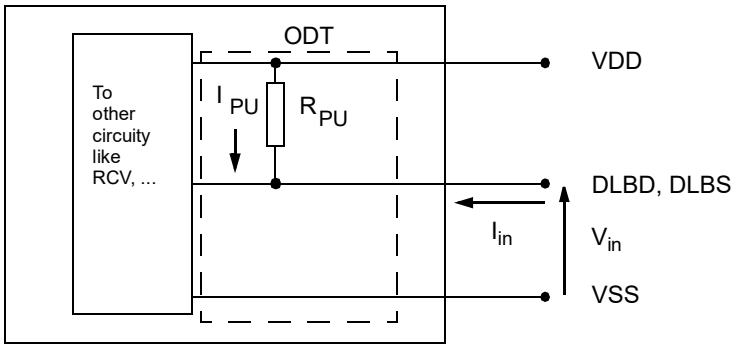


Figure 84 — DLBD and DLBS Termination: Definition of Voltages and Currents

The DDR5RCD01 device supports effective On-Die Termination Rtt values of 80, 60, and 40 ohms (in addition to RTT_OFF).

Table 203 — Electrical Characteristics for DLBD and DLBS Input Termination

RTT	Vout	Min	Nom	Max	Unit	NOTE
80 Ω	VILdc= 0.5 * VDD	0.9	1	1.25	RZQ/3	1,2
	VIMdc= 0.8 * VDD	0.9	1	1.1	RZQ/3	1,2
	VIHdc= 0.95 * VDD	0.8	1	1.1	RZQ/3	1,2
60 Ω	VILdc= 0.5 * VDD	0.9	1	1.25	RZQ/4	1,2
	VIMdc= 0.8 * VDD	0.9	1	1.1	RZQ/4	1,2
	VIHdc= 0.95 * VDD	0.8	1	1.1	RZQ/4	1,2
40 Ω	VILdc= 0.5 * VDD	0.9	1	1.25	RZQ/6	1,2
	VIMdc= 0.8 * VDD	0.9	1	1.1	RZQ/6	1,2
	VIHdc= 0.95 * VDD	0.8	1	1.1	RZQ/6	1,2
DLBD-DLBS Mismatch within sub-channel	VIMdc = 0.8 * VDD	0	-	8	%	1,2,3

NOTE 1 For the behavior of the tolerance limits if temperature or voltage changes, see Section 14.5, “Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity,” on page 223.
NOTE 2 DLBD to DLBS mismatch within sub-channel for a given component (characterized).
NOTE 3 RTT variance range ratio to RTT Nominal value in a given component.

$$\text{DLBD-DLBS Mismatch in a Sub-channel} = \frac{RTT_{MAX} - RTT_{MIN}}{RTT_{NOM}} \times 100$$

13.6 Input CMOS Rail-to-Rail Levels for DRST_n

Table 204 — CMOS Rail-to-Rail Input Levels for DRST_n

Symbol	Parameter	Min	Max	Unit	NOTE
VIH(AC)_RESET	AC Input High Voltage	0.8 * V_{DD}	V_{DD}	V	6
VIH(DC)_RESET	DC Input HIGH Voltage	0.7 * V_{DD}	VDD	V	2
VIL(DC)_RESET	DC Input LOW Voltage	VSS	0.3*VDD	V	1
VIL(AC)_RESET	AC Input LOW Voltage	VSS	0.2*VDD	V	7
TR_RESET	Rise Time	-	1.0	µs	4
t_{PW_RESET}	RESET pulse width	1.0	-	µs	3, 5, 8

NOTE 1 After DRST_n is registered LOW, DRST_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, the RCD may not be reset.
NOTE 2 Once DRST_n is registered HIGH, DRST_n level must be maintained above VIH(DC)_RESET, otherwise, RCD operation will not be guaranteed until it is reset asserting DRST_n signal LOW.
NOTE 3 DRST_n will clear all register settings to their default values with the exception of sticky registers listed in Section 8.5.
NOTE 4 No slope reversal (ringback) requirement during its level transition from Low to High.
NOTE 5 This definition is applied only “Reset Procedure with Power Stable.”
NOTE 6 Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 7 Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.
NOTE 8 t_{PW_RESET} is equivalent to parameter t_{RINIT1} (see Table 190 on page 177).

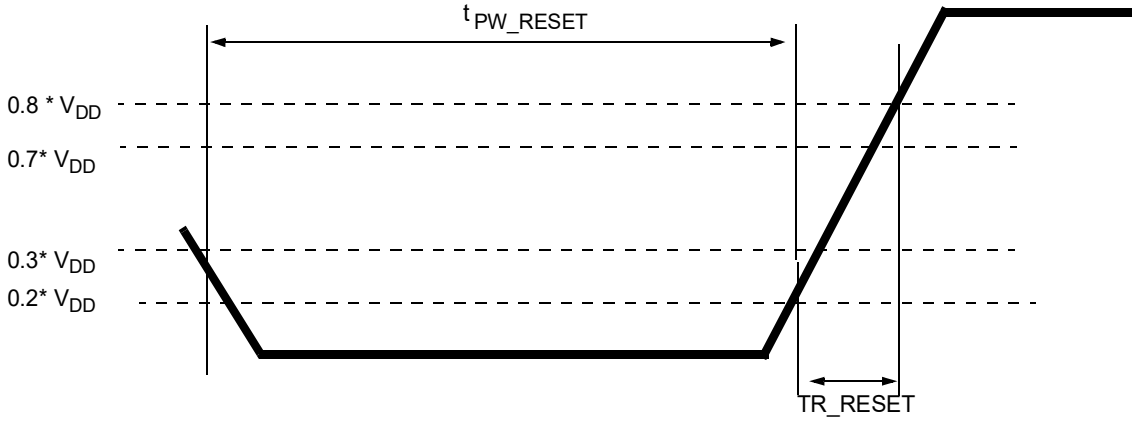


Figure 85 — DRST_n Input Slew Rate Definition

13.7 Differential Input Clock and DCA Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

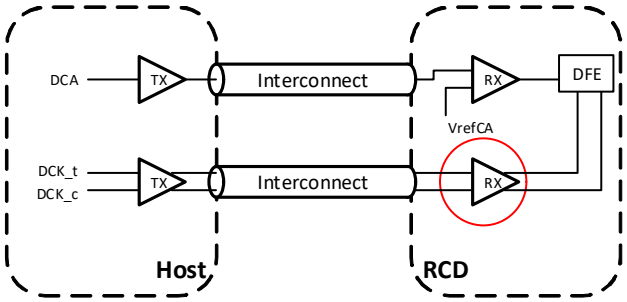


Figure 86 — Example of DDR5 Memory Interconnect

13.7.1 Differential Input Clock and DCA Voltage Sensitivity Parameter

Differential input clock (DCK_t, DCK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

Table 205 — Rx Input Voltage Sensitivity Parameters for DDR5-3200 to 4800

Symbol	Parameter	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VRx_CK_1	Differential DCK_t/DCK_c Rx input voltage sensitivity (differential p-p).	-	130	-	115	-	105	-	100	-	100	mV	1, 3, 4, 5, 7, 8
VRx_CK_2	Differential DCK_t/DCK_c Rx input voltage sensitivity (differential p-p).	-	100	-	90	-	85	-	80		75	mV	1, 3, 4, 6, 7, 8
VRx_DCA_V	Minimum Voltage Amplitude (p-p) that needs to be applied around VrefCA.	-	75	-	70	-	65	-	60	-	55	mV	1, 2, 3, 7, 8
VRx_DLBS	Minimum Voltage Amplitude (p-p) that needs to be applied around DLBS Vref.	-	100	-	100	-	100	-	100	-	100	mV	1, 3, 7

NOTE(S):

1. Refer to the minimum BER 1e-9 requirements for DDR5.
2. This Parameter applies to DCA[6:0]_[B:A] and DPAR_[B:A].
3. Test using clock-like pattern of repeating 3 "1s" and 3 "0s" without applying cross-talk or SSO conditions.
4. The DDR5RCD01 device is required to meet either VRx_CK_1 or VRx_CK_2.
5. VRx_CK_1 only applies to devices that meet Option-1 Rx Clock Jitter Sensitivity specification defined in Table 207.
6. VRx_CK_2 only applies to devices that meet Option-2 Rx Clock Jitter Sensitivity specification defined in Table 208.
7. This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C).
8. tRx_DCA_tMargin condition does not need to be met.

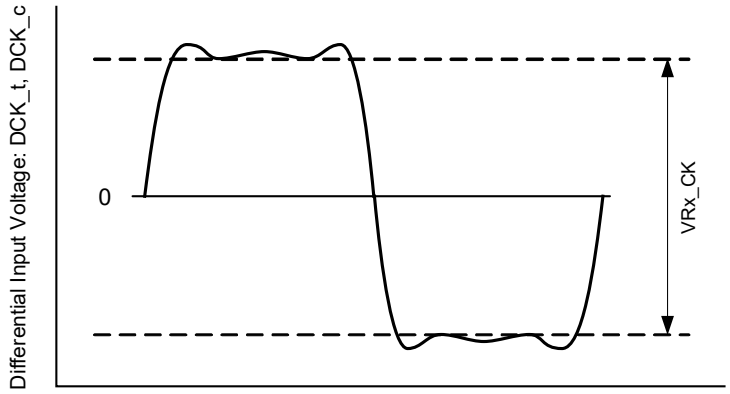


Figure 87 — VRx_CK

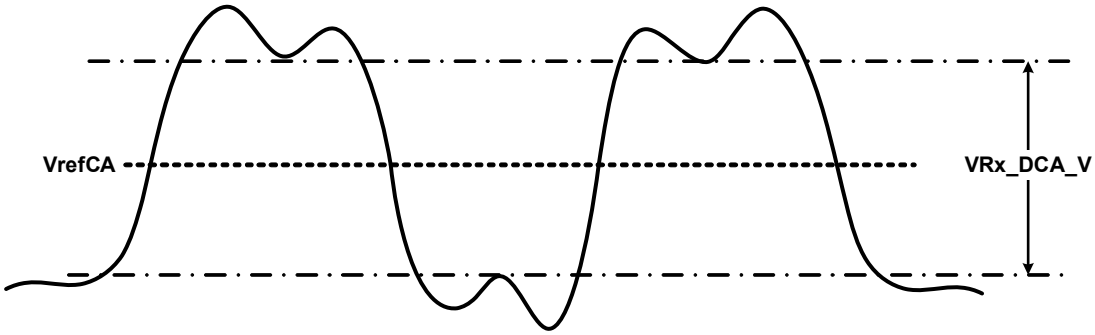


Figure 88 — VRx_DCA_V

13.8 Input Clock Jitter

13.8.1 Overview

The clock is being driven to the RCD for L/RDIMM modules, Figure 89.

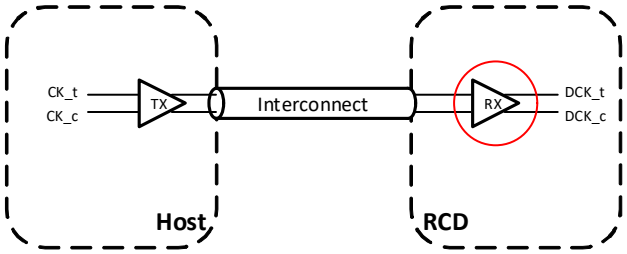


Figure 89 — Host driving clock signals to the RCD

13.8.2 Specification for RCD Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5RCD01 device.

Table 206 — Input Clock Differential Jitter

[BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; Tj = Total jitter; pp = Peak-to-Peak]

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tCK	RCD Reference clock frequency	0.9999*f0	1.0001*f0	MHz	1, 12
tCK_Duty_UI	Duty Cycle	0.45	0.55	UI	4, 12
tCK_Duty_UI_Error	Duty Cycle Error	-	0.05	UI	1, 5, 12
tCK_1UI_Rj_NoBUJ	Rj value of 1-UI Jitter	-	0.0037	UI (RMS)	3, 6, 12
tCK_1UI_Dj_NoBUJ	Dj pp value of 1-UI Jitter	-	0.030	UI	3, 7, 12
tCK_1UI_Tj_NoBUJ	Tj value of 1-UI Jitter	-	0.090	UI	3, 7, 12
tCK_NUI_Rj_NoBUJ, where N=2,3	Rj value of N-UI Jitter, where N=2,3	-	0.004	UI (RMS)	3, 8, 12
tCK_NUI_Dj_NoBUJ, where N=2,3	Dj pp value of N-UI Jitter, where N=2,3	-	0.074	UI	3, 9, 12
tCK_NUI_Tj_NoBUJ, where N=2,3	Tj value of N-UI Jitter, where N=2,3	-	0.140	UI	3, 9, 12
tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	Rj value of N-UI Jitter, where N=4,5,6,...,30	-	TBD	UI (RMS)	3, 10, 12, 13
tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	Dj pp value of N-UI Jitter, N=4,5,6,...,30	-	TBD	UI	3, 11, 12, 13
tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	Tj value of N-UI Jitter, N=4,5,6,...,30	-	TBD	UI	3, 11, 12, 13

Unit UI = tCK(avg).min/2

Note(s):

1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600
2. Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock
3. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility
4. Duty Cycle defined as the ratio between any even UI and tCK.
5. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
6. Rj RMS value of 1-UI jitter without BUJ. This extraction is to be done after software correction of DCD
7. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
8. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD
9. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
10. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD
11. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
12. The validation methodology for these parameters will be covered in future ballots
13. If the clock meets total jitter Tj at BER of 1E-16, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of 1E-16

13.9 RX Clock Jitter Sensitivity

The receiver clock jitter sensitivity test provides the methodology for testing the receiver's clock sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded clock input while keeping the data input jitter free, noise free and ISI free. The receiver must pass the appropriate BER rate when the equivalent cross-talk pattern is applied through the combination of applied DCD and Rj.

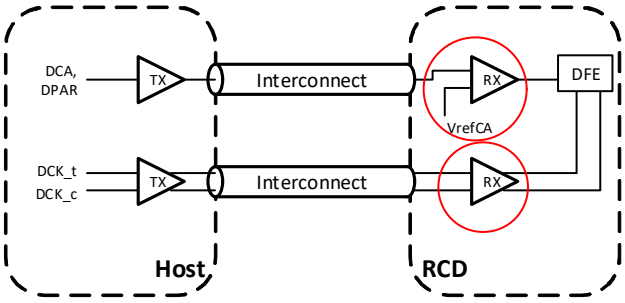


Figure 90 — RCD RX Forward Clock for Jitter Sensitivity

13.9.1 Rx Clock Jitter Sensitivity Specification

The following tables provide Rx DCK Jitter Sensitivity Specification for the DDR5RCD01 receivers when operating at various possible transfer rates. These parameters are tested with neither additive gain nor Rx Equalization set. The DDR5RCD01 device is required to meet only one of the following two options: the Option-1 requirements defined in Table 207 or the Option-2 requirements defined in Table 208 (as applicable for the implemented receiver architecture).

Table 207 — Rx Clock Jitter Sensitivity Option-1 Specification for DDR5-3200 to 4800

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tRx_DCA_tMargin	DCA Timing Width	0.75	-	UI	1, 2, 3, 8, 9, 10
ΔtRx_DCA_tMargin_DCD_DCK	Degradation of timing width compared to tRx_DCA_tMargin, with DCD injection in DCK	-	0.03	UI	1, 4, 8, 9, 10
ΔtRx_DCA_tMargin_Rj_DCK	Degradation of timing width compared to tRx_DCA _tMargin, with Rj injection in DCK	-	0.03	UI	1, 5, 8, 9, 10
ΔtRx_DCA_tMargin_DCD_Rj_DCK	Degradation of timing width compared to tRx_DCA_tMargin with both DCD and Rj injection in DCK	-	0.05	UI	1, 2, 6, 8, 9, 10
tRx_DCK2DCA_Skew	Delay of any DCA or DCS lane relative to the DCK_t/DCK_c crossing within a sub-channel.	- 0.25	0.25	UI	1, 7, 8, 9, 10

Unit UI = tCK(avg).min/2

NOTE(S):
1. Validation methodology will be defined in future ballots.
2. Each of ΔtRx_DCA_tMargin_DCD_DCK, ΔtRx_DCA_tMargin_DCD_Rj_DCK, and ΔtRx_DCA_tMargin_DCD_Rj_DCK can be relaxed by up to 5% if tRx_DCA_tMargin exceeds the spec by at least by 5%.
3. DCA Timing Width - timing width for any data lane using repetitive patterns (check notes 4 to 6 for the pattern) measured at BER=E-9.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded clock compared to tRx-_DCA_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx clock Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded clock measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx Clock Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
6. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded clock measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx Clock Jitter Sensitivity Testing.
7. Delay of any data lane relative to the clock lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
8. All measurements at BER=E-9.
9. This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C) with default VrefCA settings.
10. The user has the freedom to set the voltage swing and slew rates for clock and DCA signals as long as they meet the specification.

Table 208 — Rx Clock Jitter Sensitivity Option-2 Specification for DDR5-3200 to 4800

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tRx_DCA_tMargin	DCA Timing Width	0.9	-	UI	1, 2, 3, 8, 9, 10
ΔtRx_DCA_tMargin_DCD_DCK	Degradation of timing width compared to tRx_DCA_tMargin, with DCD injection in DCK	-	0.05	UI	1, 4, 8, 9, 10
ΔtRx_DCA_tMargin_Rj_DCK	Degradation of timing width compared to tRx_DCA _tMargin, with Rj injection in DCK	-	0.075	UI	1, 5, 8, 9, 10
ΔtRx_DCA_tMargin_DCD_Rj_DCK	Degradation of timing width compared to tRx_DCA_tMargin with both DCD and Rj injection in DCK	-	0.1	UI	1, 2, 6, 8, 9, 10
tRx_DCK2DCA_Skew	Delay of any DCA or DCS lane relative to the DCK_t/DCK_c crossing within a sub-channel.	0	1	UI	1, 7, 8, 9, 10

Unit UI = tCK(avg).min/2

NOTE(S):
1. Validation methodology will be defined in future ballots.
2. Each of ΔtRx_DCA_tMargin_DCD_DCK, ΔtRx_DCA_tMargin_DCD_Rj_DCK, and ΔtRx_DCA_tMargin_DCD_Rj_DCK can be relaxed by up to 5% if tRx_DCA_tMargin exceeds the spec by at least by 5%.
3. DCA Timing Width - timing width for any data lane using repetitive patterns (check notes 4 to 6 for the pattern) measured at BER=E-9.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded clock compared to tRx-_DCA_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx clock Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded clock measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx Clock Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
6. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded clock measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx Clock Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
7. Delay of any data lane relative to the clock lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8. All measurements at BER=E-9.
9. This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C) with default VrefCA settings.
10. The user has the freedom to set the voltage swing and slew rates for clock and DCA signals as long as they meet the specification.

13.9.2 Test Conditions for RX Clock Jitter Sensitivity Tests

Table 209 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded clock when measuring the Rx Clock Jitter Sensitivity parameters specified in Table 208.

Table 209 — Rx Clock Jitter Sensitivity Specification for DDR5-3200 to 4800

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tRx_DCK_DCD	Applied DCD to the DCK	-	0.045	UI	1, 2, 3, 6, 7, 10
tRx_DCK_Rj	Applied Rj RMS to the DCK	-	0.00625	UI (RMS)	1, 2, 4, 6, 8, 10
tRx_DCK_DCD_Rj	Applied DCD and Rj RMS to the DCK	-	0.045 UI DCD + 0.00625 UI (RMS) Rj	UI	1, 2, 5, 6, 7, 9, 10

Unit UI = tCK(avg).min/2

NOTE(S):

1. While imposing this spec, the clock lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DCK and DCA input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2. The jitter response of the forwarded clock channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin.
3. Various DCD values should be tested, complying within the maximum limits.
4. Various Rj values should be tested, complying within the maximum limits.
5. Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table.
6. Although DDR5 has bursty traffic, in order to ensure that current available BERTs can be used for this test, a continuous clock and continuous DCA are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7. Duty Cycle Distortion (in UI DCD) as applied to the input forwarded clock from BERT (UI).
8. RMS value of Rj (specified as Edge jitter) applied to the input forwarded clock from BERT (values of the edge jitter RMS values specified as % of UI).
9. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded clock from BERT (values of the edge jitter RMS values specified as % of UI).
10. The user has the freedom to set the voltage swing and slew rates for clock and DCA signals as long as they meet the specification.

13.10 Input Stressed Eye

13.10.1 Overview

The stressed eye tests provide the methodology for creating the appropriate stress for the RCD's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

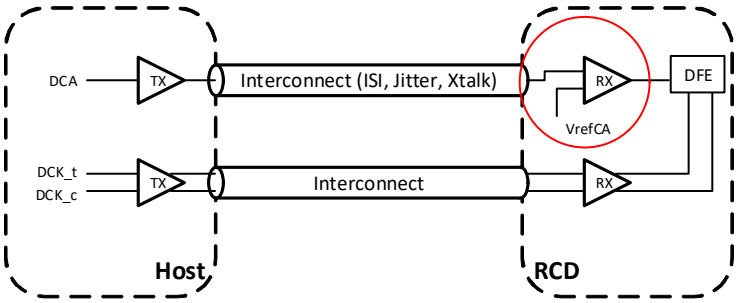


Figure 91 — Example of Rx Stressed Test Setup in Presence of ISI, Jitter and Crosstalk

13.10.2 Input Stressed Eye Parameters

Table 210 — Test Conditions for Rx Stressed Eye Tests for DDR5-3200 to 4800
[BER = Bit Error Rate; DCD = Duty Cycle Distortion; Rj = Random Jitter; Sj = Sinusoidal Jitter; p-p = peak to peak]

Symbol	Parameter	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
RxEH_Stressed_Eye	Eye height of stressed eye	-	65	-	65	-	65	-	55	-	55	mV	1, 2, 3, 4, 5, 6, 7
RxEW_Stressed_Eye	Eye width of stressed eye	-	0.20	-	0.20	-	0.20	-	0.20	-	0.20	UI	1, 2, 3, 4, 5, 6, 7
VSwing_Stressed_Eye	Vswing stress to meet above data eye	0	600	0	600	0	600	0	600	0	600	mV	1, 2
Sj_Stressed_Eye	Injected sinusoidal jitter at 200 MHz to meet above data eye	0	0.45	0	0.45	0	0.45	0	0.45	0	0.45	UI (p-p)	1, 2
Rj_Stressed_Eye	Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	0	0.04	0	0.04	0	0.04	0	0.04	0	0.04	ps RMS	1, 2
V_Noise_Stressed_Eye	Injected voltage noise at 2.1 GHz to meet above eye	0	125	0	125	0	125	0	125	0	125	mV (p-p)	1, 2

Unit UI = tCK(avg).min/2

NOTE(S):
1. Must meet minimum BER 1e-9 requirement with eye measured at the input of CA Slicer (i.e., node CA_Sum_p/n in Figure 40, “DFE Training Circuitry” on page 52).
2. These parameters are applied on the reference channel (TBD).
3. Evaluated with no DC supply voltage drift.
4. Evaluated with no temperature drift.
5. Supply voltage noise limited according to DC bandwidth spec, see Recommended DC Operating Conditions.
6. The stressed eye is to be assumed to have a diamond shape.
7. The VrefCA, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test.

13.11 DCS Input Receiver Specification

The DCS input receiver mask for voltage and timing is shown in Figure 92. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR5RCD01 input receiver to successfully capture a valid input signal. The mask is a receiver property for each pin and it is not the valid data eye.

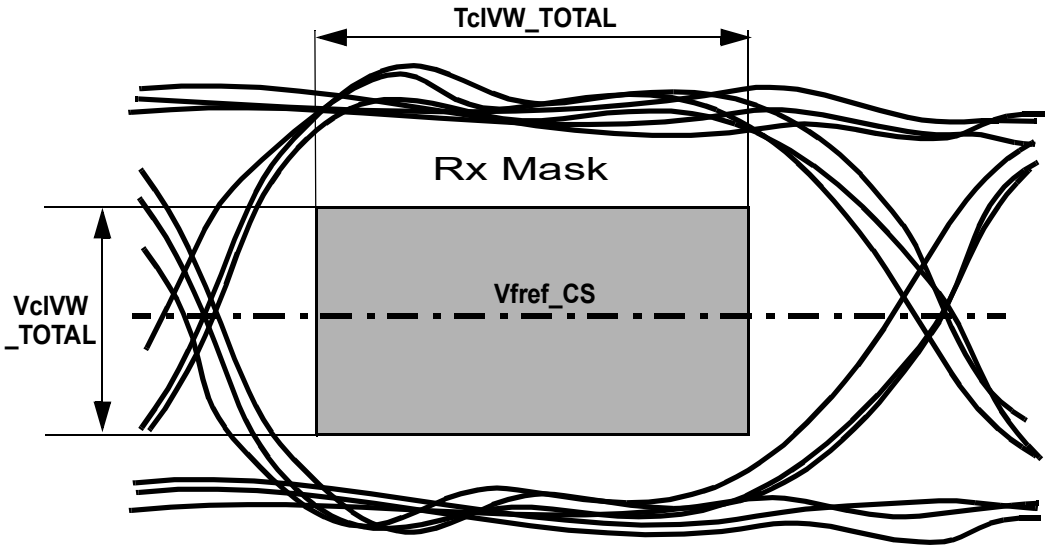


Figure 92 — DCS Receiver (RX) Mask

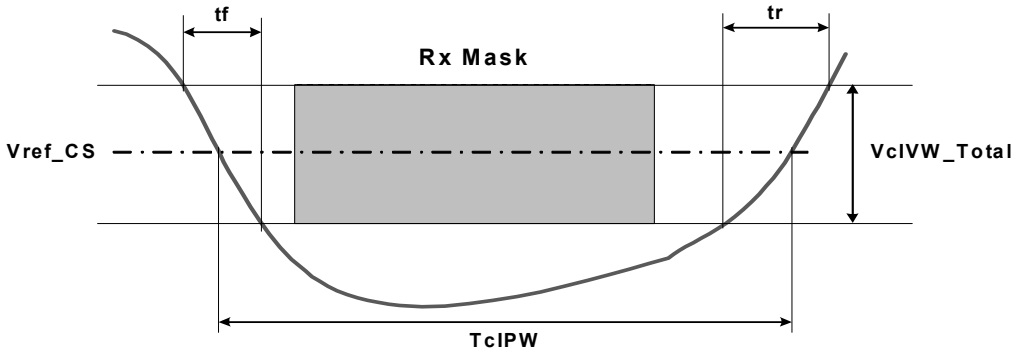


Figure 93 — DCS TcIPW and SRIN_clVW definition (for each input pulse)

13.11.1 DCS Input Receiver Voltage Margin and AC Timing by Speed Bin

Table 211 — DCS Input Receiver Voltage Margin and AC Timing by Speed Bin

Speed		DDR5- 3200		DDR5- 3600		DDR5- 4000		DDR5- 4400		DDR5- 4800		Unit	NOTE
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VcIVW_TOTAL	Rx Mask p-p voltage total	-	100	-	95	-	95	-	90	-	90	mV	1,2,3,4
TcIVW_TOTAL	Rx timing window total	-	0.135	-	0.130	-	0.130	-	0.125	-	0.125	UI	1,4
VIHL_AC	DCS AC input pulse amplitude pk-pk	120	-	115	-	115	-	110	-	110	-	mV	5
TcIPW	DCS input pulse width	0.3	-	0.29	-	0.29	-	0.28	-	0.28	-	UI	6
SRIN_cIVW	Input Slew Rate over VcIVW_TOTAL	1	5	1	5	1	5	1	5	1	5	V/ns	7

Unit UI = tCK(avg).min

NOTE 1 DCS Rx mask voltage and timing total input valid window where VcIVW is centered around Vref CS). The data Rx mask is applied per bit and includes voltage and temperature drift terms.
NOTE 2 Rx mask voltage AC swing peak-peak requirement over TcIVW_TOTAL with at least half of VcIVW_TOTAL(max) above VrefCS and at least half of VcIVW_TOTAL(max) below VrefCS.
NOTE 3 The VcIVW voltage levels are centered around VrefCS.
NOTE 4 Overshoot and Undershoot Specifications see Section 13.3 on page 200.
NOTE 5 DCS input pulse signal swing into the receiver must meet or exceed VIHL_AC for at least one point over the duration of TcIPW for any UI during which there is a signal transition. No timing requirement above level. VIHL_AC is the peak to peak voltage centered around VrefCS, which is defined in Figure 92.
NOTE 6 DCS minimum input pulse width defined at the VrefCS).
NOTE 7 Input slew rate over VcIVW Mask centered at VrefCS. For a given measurement, under the same conditions, the applied slew rate for all transition edges (slowest to fastest) must be within tbd V/ns of each other. This single-ended slew rate also applies to DCK_t and DCK_c.

13.12 DLBD Input Receiver Specification

The Loopback input receiver mask for voltage and timing is shown in Figure 94. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR5RCD01 input receiver to successfully capture a valid input signal. The mask is a receiver property for each pin and it is not the valid data eye.

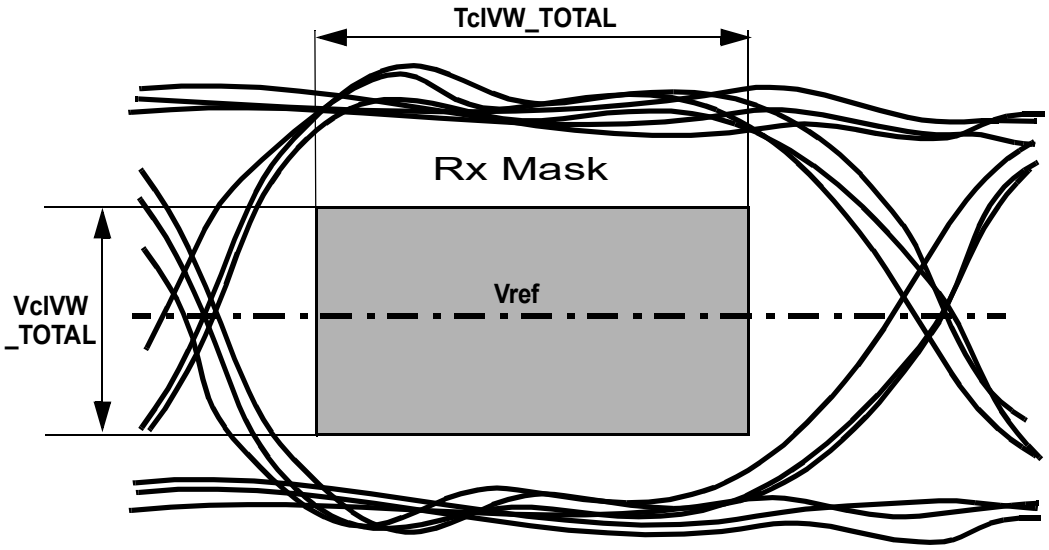
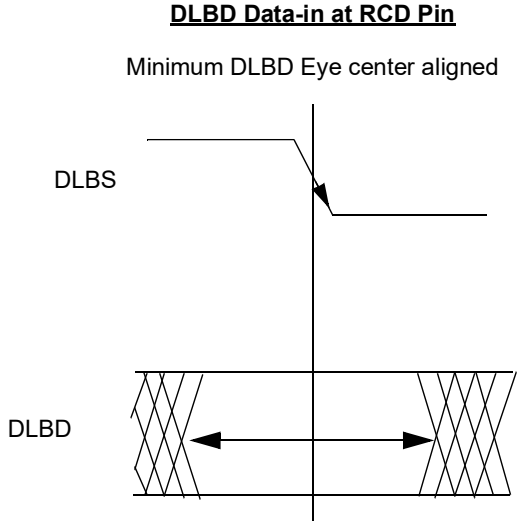


Figure 94 — DLBD Receiver (RX) Mask



TcIVW for DLBD is defined as centered on the DLBS falling edge at the RCD pin

Figure 95 — DLBD Timings at the RCD

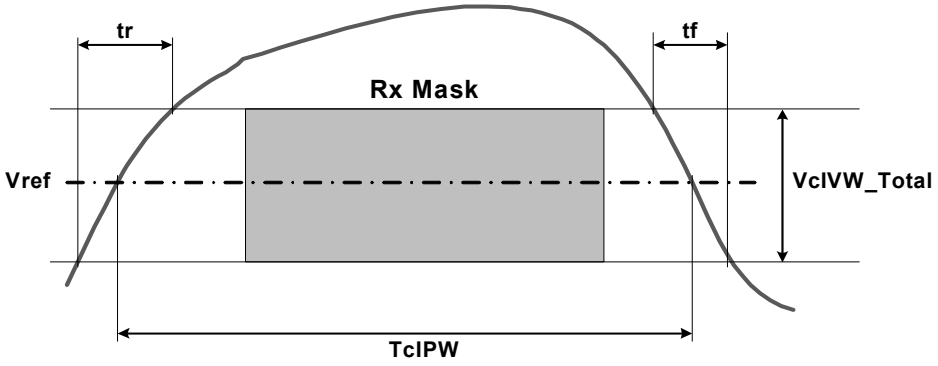


Figure 96 — DLBD TcIPW definition (for each input pulse)

Table 212 — Loopback RX Receiver Voltage Margin and AC Timing by Speed Bin for DDR5 3200 - 4800

Speed	Parameter	DDR5-3200-4800		Unit	Note
Symbol		Min	Max		
Data Voltage and Timing					
VcIVW_TOTAL	DLBD Rx Mask p-p voltage total	-	TBD	mV	1,2,3,4
TcIVW_TOTAL	DLBD Rx timing window total	-	0.3	UI	1,4
tDLBS2DLBD	DLBS to DLBD offset	-	0.1	UI	5
TdlbsIPW	DLBS input pulse width	0.25	-	UI	6

* UI=tck(avg)min

NOTE 1 Loopback Rx mask voltage and timing total input valid window where VcIVW is centered around the effective Vref level. The Loopback Rx mask is applied per bit and includes voltage and temperature drift terms.

NOTE 2 Rx mask voltage AC swing peak-peak requirement over TcIVW_TOTAL with at least half of VcIVW_TOTAL(max) above effective Vref and at least half of VcIVW_TOTAL(max) below effective Vref.

NOTE 3 The VcIVW voltage levels are centered around the effective Vref level.

NOTE 4 DLBD minimum input pulse width defined at the effective Vref level.

NOTE 5 DLBS to DLBD is defined as the input offset for each Loopback input in the DDR5RCD01 device measured at the package balls. Includes all DDR5RCD01 process, voltage and temperature variation. Measured from the falling edge of DLBS to the center (midpoint) of the DLBD TcIVW_TOTAL window. SeeFigure 95 on page 215.

NOTE 6 DLBS minimum input pulse width defined at the effective Vref level.

14 Electrical - Output AC and DC Specifications

14.1 Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between 75% and 25% of the Total swing as shown in Table 213 and Figure 97.

Table 213 — Output Single-ended Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	25%	75%	[|25% - 75%|] / DeltaTRse
Single-ended output slew rate for falling edge	75%	25%	[|75% - 25%|] / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

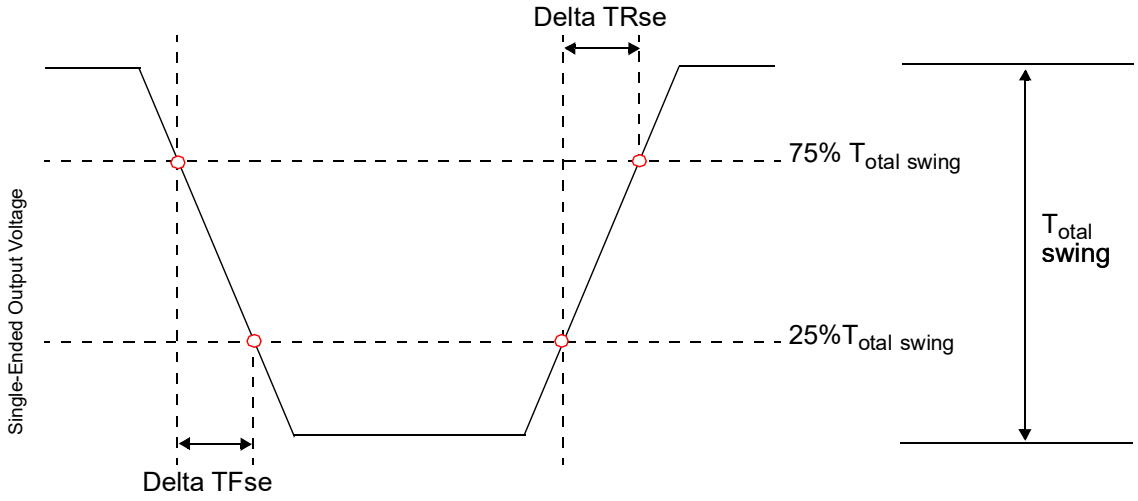


Figure 97 — Output Single-Ended Slew Rate Definition

Table 214 — Output Single-Ended Edge Rates Over Specified Operating Temperature Range

Symbol	Parameter	Conditions	DDR5-3200 - 4800		Unit
			Min	Max	
dV/dt_r_{QCA}	QCA rising edge slew rate[1,2]	1.1V operation	2.7	10	V/ns
dV/dt_f_{QCA}	QCA falling edge slew rate[1,2]	1.1V operation	2.7	10	V/ns
dV/dt_r_{QCS}	QCS rising edge slew rate[2]	1.1V operation	2.7	10	V/ns
dV/dt_f_{QCS}	QCS falling edge slew rate[2]	1.1V operation	2.7	10	V/ns
$dV/dt_f_{Alert_n}$	Alert_n falling edge slew rate[2]	1.1V operation	2.7	10	V/ns
$dV/dt_r_{QRST_n}$	QRST_n rising edge slew rate[2]	1.1V operation	0.1	3.0	V/ns
$dV/dt_f_{QRST_n}$	QRST_n falling edge slew rate[2]	1.1V operation	0.1	1.0	V/ns
$dV/dt_r_{BRST_n}$	BRST_n rising edge slew rate[2]	1.1V operation	0.1	3.0	V/ns
$dV/dt_f_{BRST_n}$	BRST_n falling edge slew rate[2]	1.1V operation	0.1	1.0	V/ns
dV/dt_D[3]	absolute difference between dV/dt_r and dV/dt_f	1.1V operation	-	2	V/ns

1. These parameters are for the QCAn, BCOM, and BCS_n outputs.
2. Measured into 50-Ω reference load terminated to V_{DD}, as shown in Figure 122.
3. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

14.2 Output Clock Differential Slew Rate

Output slew rates for differential signals QnCKx_t / QnCKx_c and BnCK_t / BnCK_c are defined and measured as shown in Table 215 and Figure 98.

Table 215 — Output Clock Differential Slew Rate Definition for QnCK_t / QnCK_c and BnCK_t / BnCK_c

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge (QnCK_t / QnCK_c and BnCK_t /BnCK_c).	25%	75%	[|25% - 75%|] / DeltaTRdiff
Differential output slew rate for falling edge (QnCK_t / QnCK_c and BnCKn_t /BnCK_c).	75%	25%	[|75% - 25%|] / DeltaTFdiff
NOTE Differential output slew rate is verified by design and characterization, and may not be subject to production test.			

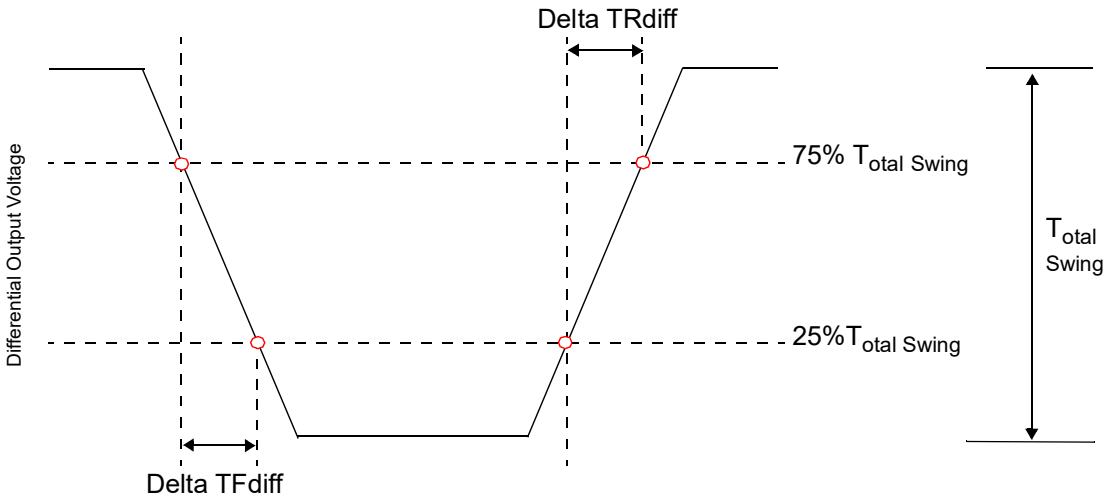


Figure 98 — Differential Output Slew Rate Definition for QnCK_t / QnCK_c and BnCK_t / BnCK_c

Table 216 — Output Differential Edge Rates[1]

Symbol	Parameter	Conditions	DDR5-3200 - 4800		Unit
			Min	Max	
dV/dt_r	QCK rising edge differential Slew Rate	1.1V operation	12	27	V/ns
dV/dt_f	QCK falling edge differential Slew Rate	1.1V operation	12	27	V/ns

1. Note: There are two selectable output slew rate ranges defined for QCK and BCK in RW0E and RW0F, respectively. See Table 112 on page 134 and Table 113 on page 135, for operating conditions.

14.3 Output Differential Clock Cross Point Voltage

The differential cross point output voltage is defined as the max to min cross point measured on the differential signals QnCK_t / QnCK_c and BnCK_t/BnCK_c with respect to the output common mode voltage (V_{OCM}).

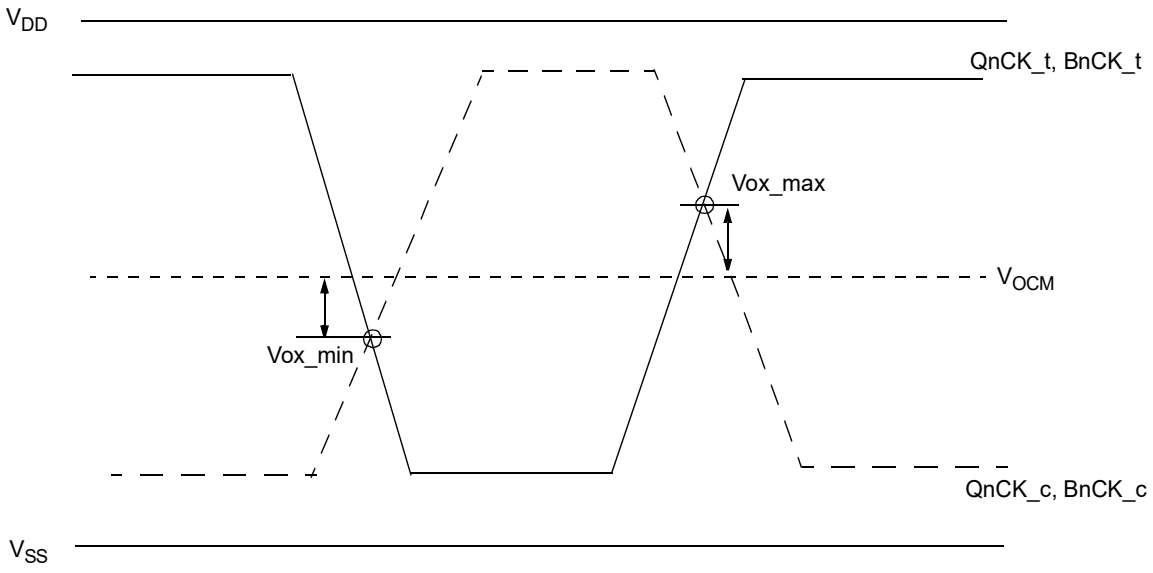


Figure 99 — Vox Definition (QnCKx and BnCK)

Table 217 — Output Cross Point Voltage for QnCK_t/QnCK_c and BnCK_t/BnCK_c

Symbol	Parameter	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400/ 4800		Unit	NOTE
		min	max	min	max	min	max	min	max		
Vox(clock)	QnCK and BnCK Differential Output Cross-Point Voltage	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mV	1

NOTE 1 Referenced to V_{OCM} = avg (QCK_t + QCK_c)/2 where the average is over 1e6 UI.

14.4 Output R-on Drive Specifications per Drive Strength Setting

Table 218 — Output Ron Drive

Symbol	Parameter	DDR5-3200 to 4800			Unit
		Min	Nom	Max	
ALERT_n					
$R_{on(ALERT)Pd}$	ALERT_n Pull-down Impedance	see Table 219	$R_{ZQ}/17$	see Table 219	Ω
$R_{on(ALERT)Pu}$	ALERT_n Pull-up Impedance		R_{ZQ}		Ω
QLBS, QLBD					
R_{on48}	48-Ω Drive Impedance	see Table 219	$R_{ZQ}/5$	see Table 219	Ω
R_{on34}	34-Ω Drive Impedance		$R_{ZQ}/7$		Ω
BCOM[2:0]/BCS_n					
R_{on20}	20-Ω Drive Impedance	see Table 219	$R_{ZQ}/12$	see Table 219	Ω
R_{on14}	14-Ω Drive Impedance		$R_{ZQ}/17$		Ω
QxCA[13:0]/QxCS[1:0]_n/QnCK_t/QnCK_c/BCK_t/BCK_c					
R_{on20}	20-Ω Drive Impedance	see Table 219	$R_{ZQ}/12$	see Table 219	Ω
R_{on14}	14-Ω Drive Impedance		$R_{ZQ}/17$		Ω
R_{on10}	10-Ω Drive Impedance		$R_{ZQ}/24$		Ω

NOTE 1 A functional representation of the output buffer is shown in Figure 100. Output impedance RON is defined by the value of the external reference resistor R_{ZQ} as defined in Table 219.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|} \quad \text{under the condition that } RON_{Pd} \text{ is turned off.} \tag{1}$$

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|} \quad \text{under the condition that } RON_{Pu} \text{ is turned off.}$$

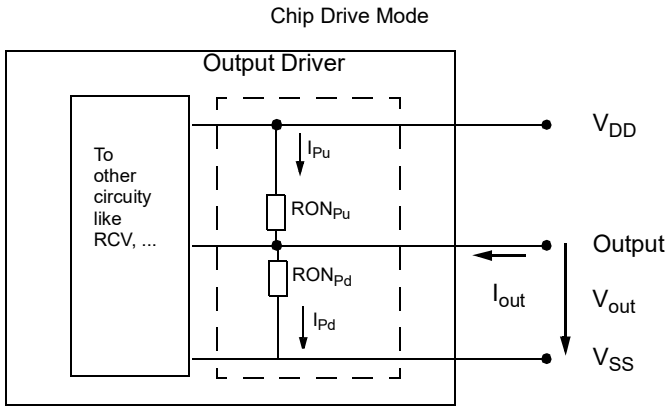


Figure 100 — Output Driver: Definition of Voltages and Currents

NOTE 2: Assuming R_{ZQ} = 240 Ω +/- 1%

Table 219 — Output Driver DC Electrical Characteristics, entire operating temperature range

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	NOTE
48 Ω	RON_{48Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/5	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/5	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/5	1, 2
	RON_{48Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/5	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/5	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/5	1, 2
34 Ω	RON_{34Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/7	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/7	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/7	1, 2
	RON_{34Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/7	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/7	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/7	1, 2
20 Ω	RON_{20Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/12	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/12	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/12	1, 2
	RON_{20Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/12	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/12	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/12	1, 2
14 Ω	RON_{14Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/17	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/17	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/17	1, 2
	RON_{14Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/17	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/17	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/17	1, 2
10 Ω	RON_{10Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/24	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/24	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/24	1, 2
	RON_{10Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/24	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/24	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/24	1, 2
14 Ω (for ALERT_n pulldown only)	$RON_{ALERTPd}$	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/17	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/17	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/17	1, 2
240 Ω (for ALERT_n pullup only)	$RON_{ALERTPu}$	V_{OLdc} = 0.5 x V_{DD}	0.85	1.0	1.25	R_{ZQ}	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.85	1.0	1.1	R_{ZQ}	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.6	1.0	1.1	R_{ZQ}	1, 2
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} = 0.8 x V_{DD}	-10		10	%	1, 2, 3
Mismatch within component variation pull-up, MM_{Pudd}		V_{OMdc} = 0.8 x V_{DD}	0		10	%	1, 2, 4
Mismatch within component variation pull-down, MM_{Pddd}		V_{OMdc} = 0.8 x V_{DD}	0		10	%	1, 2, 4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Section 14.5, “Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity,” on page 223.

NOTE 2 Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.8 * V_{DD}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * V_{DD} and 0.95 * V_{DD}.RON variance range ratio to RON nominal value in a given component.

NOTE 3 Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
Measure RON_{Pu} and RON_{Pd}, both at 0.8 * V_{DD} separately. Ron-nom is the nominal Ron value:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

NOTE 4 RON variance range ratio to RON nominal value in a given component:

$$MM_{Pudd} = \frac{RON_{PuMax} - RON_{PuMin}}{RON_{Nom}} x100$$

$$MM_{Pddd} = \frac{RON_{PdMax} - RON_{PdMin}}{RON_{Nom}} x100$$

14.5 Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the tables shown below.

Table 220 — Output Driver and Termination Resistor Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Note
R_{ONPD}	0.8 x VDD	90 - ($dR_{ONPD}dT$ x |ΔT|) - ($dR_{ONPD}dV$ x |ΔV|)	110+($dR_{ONPD}dT$ x |ΔT|) + ($dR_{ONPD}dV$ x |ΔV|)	%	1,2
R_{ONPU}	0.8 x VDD	90 - (dR_{ONPU} x |ΔT|) - (dR_{ONPU} x |ΔV|)	110 +(dR_{ONPU} x |ΔT|) + (dR_{ONPU} x |ΔV|)	%	1,2
R_{IBT}	0.8 x VDD	90 - ($dR_{IBT}dT$ x |ΔT|) - ($dR_{IBT}dV$ x |ΔV|)	110 + ($dR_{IBT}dT$ x |ΔT|) + ($dR_{IBT}dV$ x |ΔV|)	%	1,2,3

Notes:
1. ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration)
2. $dR_{ONPD}dT$, $dR_{ONPD}dV$, $dR_{ONPU}dT$, $dR_{ONPU}dV$, $dR_{IBT}dV$, and $dR_{IBT}dT$ are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input pins such as DCA[6:0], DPAR, DCS[1:0]_n,DCK_t/DCK_c, DERROR_IN_n, DLBD, and DLBS.

.

Table 221 — Output Driver and Termination Resistor Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ONPD}dT$	R_{ONPD} Temperature Sensitivity	0.00	0.1	%/°C
$dR_{ONPD}dV$	R_{ONPD} Voltage Sensitivity	0.00	0.1	%/mV
$dR_{ONPU}dT$	R_{ONPU} Temperature Sensitivity	0.00	0.1	%/°C
$dR_{ONPU}dV$	R_{ONPU} Voltage Sensitivity	0.00	0.1	%/mV
$dR_{IBT}T$	R_{IBT} Temperature Sensitivity	0.00	0.1	%/°C
$dR_{IBT}dV$	R_{IBT} Voltage Sensitivity	0.00	0.1	%/mV

14.6 Output Clock Driver Characteristics

Table 222 — Output Clock Driver Characteristics at Application Mode (Frequency Band 1)

Symbol	Parameter	Conditions	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400/ 4800		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{STAB01}	RCD Stabilization time from start of DCK toggle to PLL lock	DCK_t/DCK_c stable	-	3.5	-	3.5	-	3.5	-	3.5	µs
t_{STAB02}	RCD Stabilization time from control word write to PLL lock[1]	DCK_t/DCK_c stable	-	25.0	-	25.0	-	25.0	-	25.0	µs
t_{STAB_DB}	Data Buffer Stabilization time	BCK_t/BCK_c stable	See DDR5DB01 Specification								µs
t_{STAB_DBCMD}	LRDIMM stabilization time for commands **not** requiring use of data path[2,3]	DCK_t/DCK_c stable	-	3.5	-	3.5	-	3.5	-	3.5	µs
t_{STAB_DBDATA}	LRDIMM stabilization time for commands requiring use of data path[4,3]	DCK_t/DCK_c stable	-	4.14	-	4.14	-	4.14	-	4.14	µs
t_{CKsk}	Fractional Clock Output Skew[5]		-	20	-	20	-	20	-	20	ps
t_{staoff}[6]	Clock delay through the register between the input clock and output clock[7]		Min:(t_{PDM}(min) + 1/2 tCK); Max: (t_{PDM}(max) + 1/2 tCK)								ps
t_{dynoff}[8]	Maximum re-driven dynamic clock offset[9]		-	40	-	35	-	35	-	35	ps

1. This parameter applies to control word writes to RW05/RW06 and Bit OP0 in RW00. Since application of RW05/RW06 is postponed in the frequency change sequence defined in Section 5.4.2, a t_{STAB01} waiting time is always sufficient after exit from Self Refresh with Clock Stop (i.e., t_{STAB02} is not required). See timing diagrams in Figure 26 on page 37 and Figure 27 on page 38.
2. Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does not require the use of data path (e.g., SRX, NOP, etc.).
3. Applies only to Self Refresh Exit without frequency change.
4. Measured from start of DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and requires the use of data path (e.g., WR, RD).
5. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 103). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between QACK_A_t/QACK_A_c and QCCK_A_t/QCCK_A_c, as well as left side of the clock pairs between QACK_B_t/QACK_B_c and QCCK_B_t/QCCK_B_c. Similarly, to right side clock pairs between QBCK_A_t/QBCK_A_c and QDCK_A_t/QDCK_A_c, as well as left side of the clock pairs between QBCK_B_t/QBCK_B_c and QDCK_B_t/QDCK_B_c. This is not a tested parameter and has to be considered as a design goal only.
6. RW05/RW06 must be set to correct speed and the device must run at one of the speed nodes defined in Table 190 on page 177. See Figure 101 and Figure 102.
7. This measures the delay from the rising differential input clock which samples incoming DCA to the rising differential output clock that will be used to sample the same QCA data. The parameter describes the maximum and minimum QxCK clock t_{PD}.
8. V_{DD} measurement DC bandwidth is limited to 20 MHz.
9. See Figure 101 and Figure 102.

Table 223 — Output Clock Driver Characteristics at Test Mode (Frequency Band 2)

Symbol	Parameter	Conditions	Test Frequency (140 to 1400 MHz)		Unit
			Min	Max	
t_{STAB01}	RCD Stabilization time from start of DCK toggle to PLL lock	DCK_t/DCK_c stable	-	15	µs
t_{STAB02}	RCD Stabilization time from control word write to PLL lock[1]	DCK_t/DCK_c stable	-	25	µs
t_{CKsk}	Fractional Clock Output Skew[2]		-	100	ps
t_{staoff}[3]	Clock delay through the register between the input clock and output clock[4]		Min:(t_{PDM}(min) + 1/2 tCK); Max: (t_{PDM}(max) + 1/2 tCK)		ps
t_{dynoff}[5]	Maximum re-driven dynamic clock offset[6]		-	500	ps

1. This parameter applies to control word writes to RW05 and Bit OP0 in RW00.
2. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 103). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between QACK_A_t/QACK_A_c and QCCK_A_t/QCCK_A_c, as well as left side of the clock pairs between QACK_B_t/QACK_B_c and QCCK_B_t/QCCK_B_c. Similarly, to right side clock pairs between QBCK_A_t/QBCK_A_c and QDCK_A_t/QDCK_A_c, as well as left side of the clock pairs between QBCK_B_t/QBCK_B_c and QDCK_B_t/QDCK_B_c. This is not a tested parameter and has to be considered as a design goal only.
3. RW05 must not be set to enable PLL bypass mode and the device must run within the Test Frequency range defined in Table 190 on page 177. See Figure 101 and Figure 102.
4. This measures the delay from the rising differential input clock which samples incoming DCA to the rising differential output clock that will be used to sample the same QCA data. The parameter describes the maximum and minimum QxCK clock t_{PD}.
5. V_{DD} measurement DC bandwidth is limited to 20 MHz.
6. See Figure 101 and Figure 102.

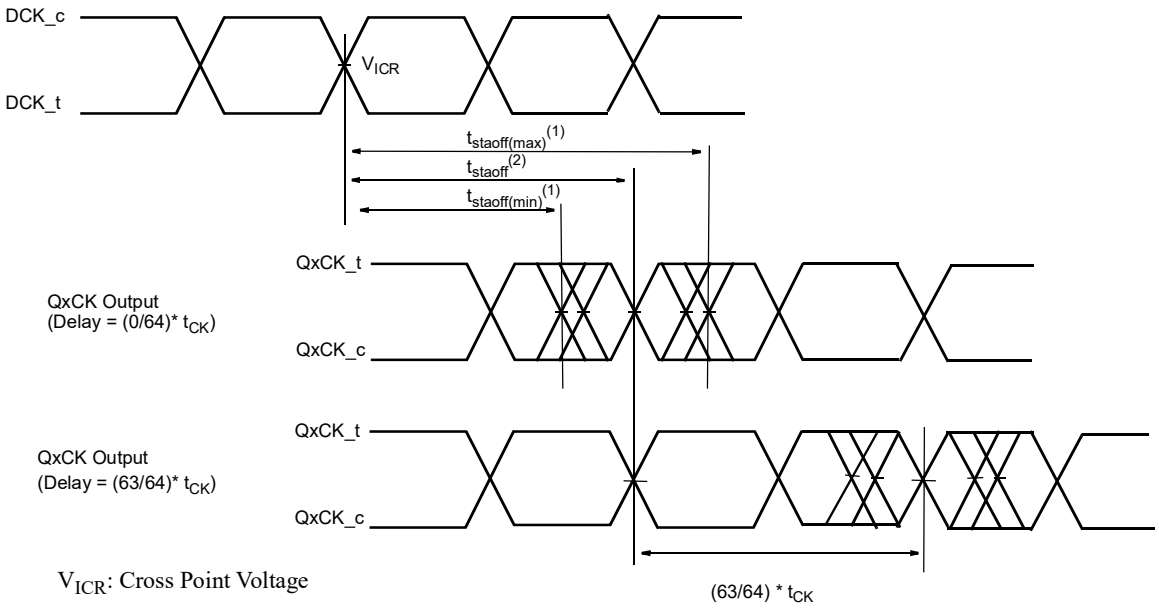


Figure 101 — Definition for tstaoff and tdynoff in DDR Mode

1. $t_{staoff(max/min)}$ = propagation delay specification limits for clock signal (falling DCK input clock edge to rising QxCK output clock edge for corresponding data cycles) over process, voltage and temperature.
2. t_{staoff} = measured propagation delay for clock signal (falling DCK input clock edge to rising QxCK output clock edge for corresponding data cycles).
3. t_{dynoff} = maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g. thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc.) except reference clock noise.

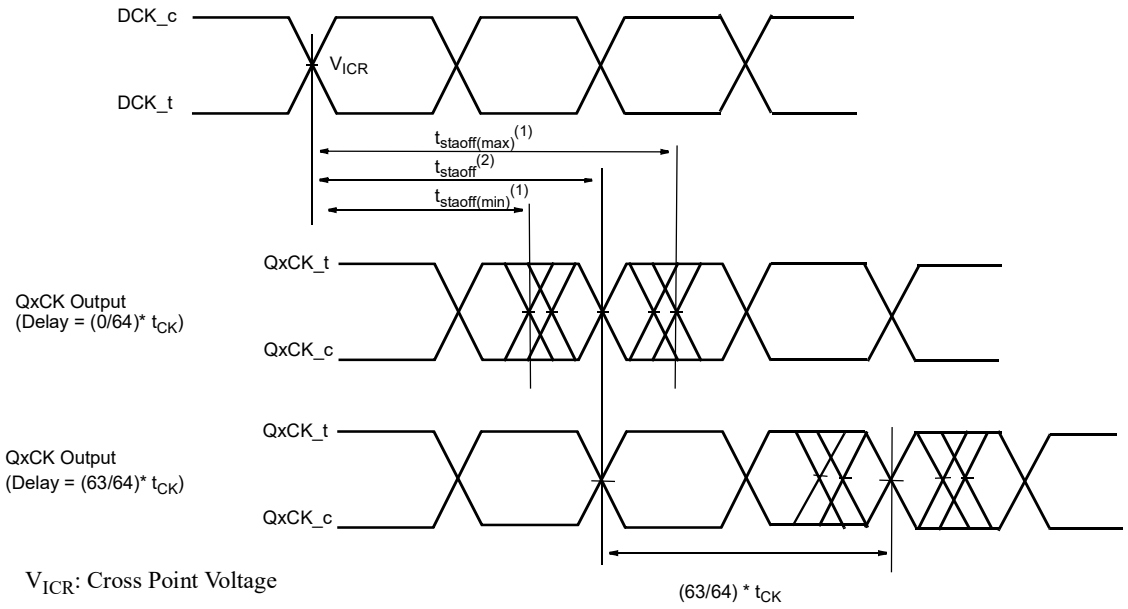


Figure 102 — Definition for tstaoff and tdynoff in SDR Mode

1. $t_{staoff(max/min)}$ = propagation delay specification limits for clock signal (rising DCK input clock edge to rising QxCK output clock edge for corresponding data cycles) over process, voltage and temperature.
2. t_{staoff} = measured propagation delay for clock signal (rising DCK input clock edge to rising QxCK output clock edge for corresponding data cycles).
3. t_{dynoff} = maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g. thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc.) except reference clock noise.

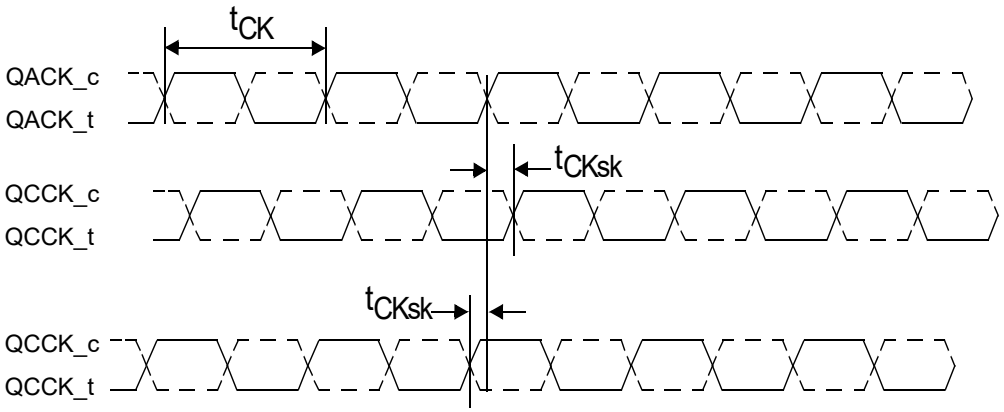


Figure 103 — Clock Output (QxCK) Skew

14.7 Differential Output Clock Driver Jitter Characteristics

14.7.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 206.

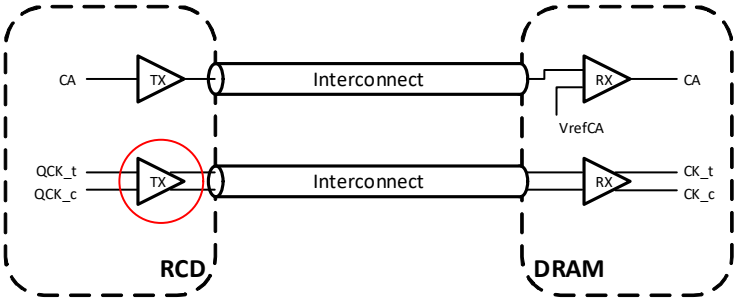


Figure 104 — Example of QCK TX Interconnect

14.7.2 Output Clock Jitter Parameters

Table 224 — Tx QCK Jitter Specifications for DDR5-3200 to 4800

[BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; pp = Peak-to-Peak]

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tTx_QCK_1UI_Rj_NoBUJ	Rj value of 1-UI Jitter without BUJ	-	0.0035	UI (RMS)	1, 2, 3
tTx_QCK_1UI_Dj_NoBUJ	Dj pp value of 1-UI Jitter without BUJ	-	0.025	UI	1, 3, 4
tTx_QCK_NUI_Rj_NoBUJ, where 1 < N < 4	Rj value of N-UI Jitter without BUJ, where 1 < N < 4	-	0.0035	UI (RMS)	1, 3, 5
tTx_QCK_NUI_Dj_NoBUJ, where 1 < N < 4	Dj pp value of N-UI Jitter without BUJ, where 1 < N < 4	-	0.07	UI	1, 3, 6
tTx_QCK_NUI_Rj_NoBUJ, where 3 < N < 31	Rj value of N-UI Jitter without BUJ, where 3 < N < 31	-	TBD	UI (RMS)	1, 3, 7
tTx_QCK_NUI_Dj_NoBUJ, where 3 < N < 31	Dj pp value of N-UI Jitter without BUJ, where 3 < N < 31	-	TBD	UI	1, 3, 8

Unit UI = tCK(avg).min/2

Note(s):

1. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DRAM component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. Rj RMS value of 1-UI jitter without BUJ. This extraction is to be done after software correction of DCD.
3. This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C).
4. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ. Dj indicates Djdd of dual-Dirac fitting.
5. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD.
6. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD.
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.

14.8 ALERT_n Output Driver DC Electrical Characteristic

Table 225 — ALERT_n Output Driver DC Electrical Characteristics

Symbol	Parameter	Applicable Signals	Condition	Min	Nom	Max	Unit
I_{OL}	LOW-level output current ALERT_n	Measured at V_{OL} of 0.4 V	-	25	-	-	mA
V_{OL}	Output LOW voltage ALERT_n	Measured at I_{OL} = 25 mA	-	-	-	0.4	V

15 IDD Specification Parameters

15.1 IDD Specification Parameters and Test Conditions

In this chapter, IDD measurement conditions such as test load and patterns are defined. Figure 105 shows the setup and test load for IDD measurements.

- IDD currents (such as IDD3NA, IDD3NB, IDD3P1, IDD3P2, IDD4A, IDD4B, IDD6R and IDD6S) are measured as time-averaged currents with all V_{DD} balls of the DDR5RCD01 under test tied together.
- IDD currents can be measured for each speed bin. Each measurement shall use the minimum tCK (avg) for each speed bin.
- **ATTENTION:** IDD values cannot be directly used to calculate IO power of the DDR5RCD01. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 106.

For IDD measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} <= V_{IL(AC)}$.max.
- "1" and "HIGH" is defined as $V_{IN} >= V_{IH(AC)}$.min.
- Basic IDD Measurement Conditions are described in Table 226.
- Detailed IDD Measurement-Loop Patterns are described in Table 227 and Table 228.

IDD Measurements are done after properly initializing the DDR5RCD01. This includes but is not limited to setting

- All four clock outputs enabled per channel in RW08;
- IBT enabled in RW10
- All output driver strength set to RZQ/17;
- Parity checking disabled in RW01[0];
- SidebandBus interface enabled;
- QCA13 enabled;
- 60 Ω IBT enabled for DCA[6:0], DPAR, DCS[1:0].

ATTENTION: The IDD Measurement-Loop Patterns need to be executed at least one time before actual IDD measurement is started.

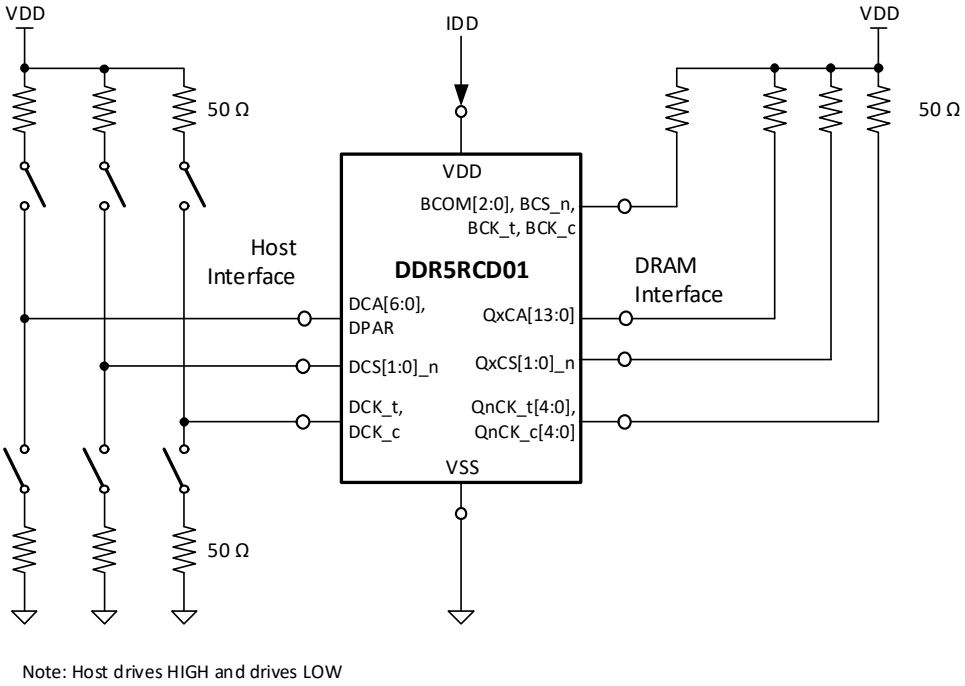


Figure 105 — Measurement Setup and Test Load for IDD Measurements

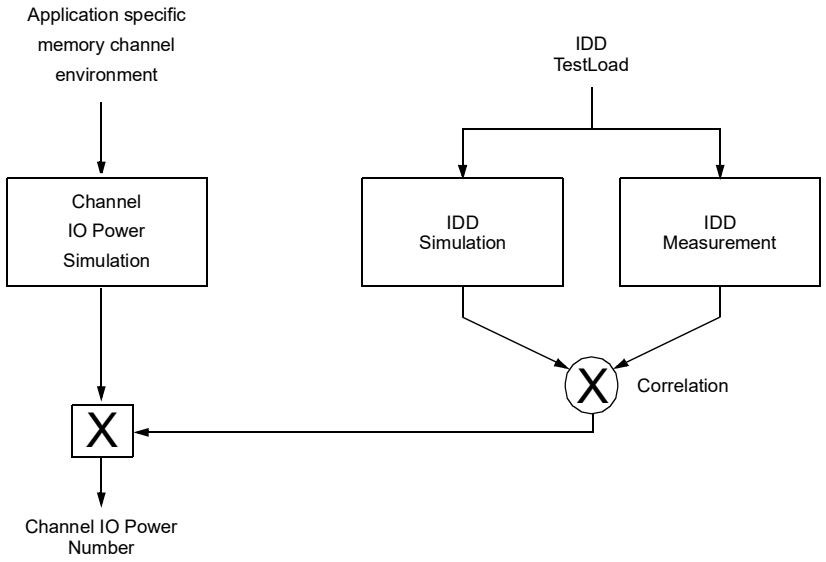


Figure 106 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDD Measurement

Table 226 — Basic IDD Measurement Conditions[1]

Symbol	Description
IDD3NA	Active Idle Current DB interface: Disabled; Q[D:A]CK: Enabled; Data IO & Pattern Details: see Table 227
IDD3NB	Active Idle Current DB interface: Enabled; Q[D:A]CK: Enabled; Data IO & Pattern Details: see Table 227 on page 233
IDD3P1	Power Down with ODT Control DB interface: Enabled; Q[D:A]CK: Enabled; Data IO & Pattern Details: see Table 227 on page 233
IDD3P2	Power Down without ODT Control DB interface: Enabled; Q[D:A]CK: Enabled; Data IO & Pattern Details: see Table 227 on page 233
IDD4A	Active Current DB interface: Disabled; Q[D:A]CK: Enabled; Data IO & Pattern Details: see Table 228 on page 234
IDD4B	Active Current DB interface: Enabled; Q[D:A]CK: Enabled; Data IO & Pattern Details: see Table 228 on page 234
IDD6R	Static Reset Current DRST_n: LOW; DCK_t and DCK_c: LOW; DCS: LOW; Outputs Hi-Z (except QRST, BRST, QCS)
IDD6S	Clock Stopped Power Down Current DRST_n: HIGH after being LOW for t_{RINIT1} with described input conditions (i.e., DCK_t = DCK_c = DCS_n = LOW) applied; DCK_t and DCK_c: LOW; DCS: LOW; Outputs Hi-Z (except QCS: LOW, BCK:HIGH or HI-Z[2], BCS & BCOM: HIGH)

1. All tests use termination setup depicted in Figure 105.
2. BCK output is HIGH or HI-Z depending on vendor implementation.

Table 227 — IDD3NA. IDD3NB, IDD3P1, and IDD3P2 Measurement-Loop Pattern

DCK_t, DCK_c	Cycle Number	UI Number	Command	DCS[0]_n	DCS[1]_n	DCA0	DCA1	DCA2	DCA3	DCA4	DCA5	DCA6	DPAR
Toggling	0	0	None	1	1	1	1	1	1	1	1	1	1
		1		1	1	1	1	1	1	1	1	1	1

Table 228 — IDD4A, IDD4B Measurement-Loop Pattern

DCK_t,DCK_c	Sub-Loop	Cycle Number	UI Number	Command	DCS[0]_n	DCS[1]_n	DCA0	DCA1	DCA2	DCA3	DCA4	DCA5	DCA6	DPAR
Toggling	0	0	0	RD	0	1	1	0	1	1	1	1	0	1
			1		1	1	1	0	1	0	0	0	0	0
		1	0		1	1	1	0	1	0	1	0	1	0
			1		1	1	1	0	1	1	1	1	0	1
		2	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1
		3	0	ACT	0	1	0	0	0	1	0	1	0	0
			1		1	1	1	0	1	0	0	0	0	0
		4	0		1	1	1	0	1	0	1	0	1	0
			1		1	1	0	1	0	1	0	1	0	1
		5	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1
		6	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1
		7	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1
	1	8	0	RD	1	0	1	0	1	1	1	1	0	1
			1		1	1	1	0	1	0	0	0	0	0
		9	0		1	1	1	0	1	0	1	0	1	0
			1		1	1	1	0	1	1	1	1	0	1
		10	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1
		11	0	ACT	1	0	0	0	0	1	0	1	0	0
			1		1	1	1	0	1	0	0	0	0	0
		12	0		1	1	1	0	1	0	1	0	1	0
			1		1	1	0	1	0	1	0	1	0	1
		13	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1
		14	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1
		15	0		1	1	1	1	1	1	1	1	1	1
			1		1	1	1	1	1	1	1	1	1	1

16 Input/Output Capacitance

Table 229 — Silicon pad I/O Capacitance values

Symbol	Parameter	DDR5 - 3200-4800		Unit	Notes
		Min	Max		
C_I	Input capacitance, Data inputs	0.2	0.95	pF	1, 2
C_O	Output capacitance	0.45	2.5	pF	1,3
C_{CK}	Input capacitance, DCK_t, DCK_c	0.2	0.95	pF	1
C_{DCK}	Input capacitance delta DCK_t and DCK_c	-	0.1	pF	1, 4
C_{IDCA}	Delta capacitance over all DCA inputs, per sub-channel	-	0.2	pF	1
C_{IDCS}	Delta capacitance over all DCS inputs, per sub-channel	-	0.2	pF	1
C_{ILB}	Input capacitance DLB	0.2	1.0	pF	1
C_{OLB}	Output capacitance QLB	0.45	2.0	pF	1
C_{IR}	Input capacitance, DRST_n	0.5	2	pF	1, 5
C_{OR}	Output Capacitance of QRST_n & BRST_n	0.4	2.0	pF	1
C_{ALERT}	Output capacitance of ALERT_n	0.4	2.5	pF	1
C_{DERROR_IN}	Input capacitance of DERROR_IN_n	0.4	1.5	pF	1

NOTE 1 This parameter does not include package capacitance.

NOTE 2 Data inputs are DCAy_N, DPAR_N, DCSy_N_n.

NOTE 3 Applies to QxCAy_N, QxCSy_N_n,, BCS_N_n, BCOMy_N, BCK_N_t, BCK_N_c, QxCKy_N_t, and QxCKy_N_c.

NOTE 4 Absolute value of DCK_t - DCK_c

NOTE 5 Parameter specified at VI = VDD or VSS; VDD = 1.1 V

Table 230 — Package Electrical Parameters

Symbol	Parameter	DDR5 - 3200 to 4800		Unit	Notes
		Min	Max		
ZI_{DCS}	Input DCS pins Zpkg	40	70	Ω	1, 2, 4
TdI_{DCS}	Input DCS pins Pkg Delay	14	55	ps	1, 3, 4
DZI_{DCS}	Delta DCS pins Zpkg	-	15	Ω	1, 2, 4, 5
$DTdI_{DCS}$	Delta DCS pins Pkg Delay	-	20	ps	1,3, 4, 6
ZI_{DCA}	Input DCA pins Zpkg	40	70	Ω	1, 2, 7
TdI_{DCA}	Input DCA pins Pkg Delay	14	55	ps	1, 3, 7
DZI_{DCA}	Delta DCA pins Zpkg	-	15	Ω	1, 2, 7, 8
$DTdI_{DCA}$	Delta DCA input pins Pkg Delay	-	20	ps	1, 3, 7, 9
ZO_{QCS}	Output QCS pins Zpkg	40	70	Ω	1, 2, 10
TdO_{QCS}	Output QCS pins Pkg Delay	14	65	ps	1, 3, 10
DZO_{QCS}	Delta QCS pins Zpkg	-	15	Ω	1, 2, 10, 11
$DTdO_{QCS}$	Delta QCS input pins Pkg Delay	-	20	ps	1, 3, 10, 12
ZO_{QCA}	Output QCA pins Zpkg	40	70	Ω	1, 2, 13
TdO_{QCA}	Output QCA pins Pkg Delay	14	65	ps	1, 3, 13
DZO_{QCA}	Delta QCA pins Zpkg	-	15	Ω	1, 3, 13, 14
$DTdO_{QCA}$	Delta QCA output pins Pkg Delay	-	20	ps	1, 3, 13, 15
ZO_{BC}	Output QBC pins Zpkg	40	70	Ω	1, 3, 16
TdO_{BC}	Output BC pins Pkg Delay	14	65	ps	1, 3, 16
DZO_{BC}	Delta BC pins Zpkg	-	15	Ω	1, 3, 16, 17
$DTdO_{BC}$	Delta BC output pins Pkg Delay	-	20	ps	1, 3, 16, 18
ZI_{DCK}	Input DCK pins Zpkg	40	70	Ω	1, 2, 19
TdI_{DCK}	Input DCK pins Pkg Delay	14	55	ps	1, 3
ZO_{QCK}	Output QnCK pins Zpkg	40	70	Ω	1, 2, 19
TdO_{QCK}	Output QnCK pins Pkg Delay	14	65	ps	1, 3
$DTdO_{QBCK}$	Delta Delay between all QxCKy_N and BCK_N for a sub-channel	-	20	ps	12,14
DZI_{DCK}	Delta Zpkg DCK_t and DCK_c	-	10	Ω	1, 2, 19, 20
$DTdI_{DCK}$	Delta Delay DCK_t and DCK_c	-	5	ps	1, 3, 21
DZO_{QCK}	Delta Zpkg QxCK_t and QxCK_c	-	10	Ω	1, 2, 10, 19,22
$DTdO_{QCK}$	Delta Delay QxCK_t and QxCKn_c	-	5	ps	1, 3, 11, 23
ZO_{BCK}	Output BCK pins Zpkg	40	70	Ω	1, 2
TdO_{BCK}	Output BCK pins Pkg Delay	14	65	ps	1, 3
DZO_{BCK}	Delta Zpkg BCK_t and BCK_c	-	10	Ω	1, 2
$DTdO_{BCK}$	Delta Delay BCK_t and BCK_c	-	5	ps	1, 3
ZO_{ZQ}	Output ZQCAL Zpkg	30	70	Ω	1, 2
ZI_{DLB}	Input DLB pins Zpkg	40	70	Ω	1, 2
TdI_{DLB}	Input DLB pins Pkg Delay	14	75	ps	1, 3
ZO_{QLB}	Output QLB pins Zpkg	40	70	Ω	1, 2
TdO_{QLB}	Output QLB pins Pkg Delay	14	50	ps	1, 3
ZO_{ALERT}	Output ALERT_n Zpkg	40	70	Ω	1, 2
TdO_{ALERT}	Output ALERT_n Pkg Delay	14	75	ps	1, 3

Table 230 — Package Electrical Parameters

Symbol	Parameter	DDR5 - 3200 to 4800		Unit	Notes
		Min	Max		
ZI_{DERROR_IN}	Input Error in Zpkg	40	70	Ω	1,2
TdI_{DERROR_IN}	Input Error in Pkg Delay	14	55	ps	1,3
ZO_{QRST}	Output QRST Zpkg	40	70	Ω	1,2
TdO_{QRST}	Output QRST Pkg Delay	14	55	ps	1,3
ZI_{DRST}	Input DRST Zpkg	40	70	Ω	1,2
TdI_{DRST}	Input DRST Pkg Delay	14	55	ps	1,3
ZI_{SDA_SCL}	Input SDA/SCL Zpkg	40	70	Ω	1,2
TdI_{SDA_SCL}	Input SDA/SCL Pkg Delay	14	55	ps	1,3

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The package parasitics (L &C) are determined using package only samples. Package capacitance and inductance are computed from S-parameters. The capacitance is derived with V_{DD}, V_{SS} shorted and all other signals floating. The inductance is derived with V_{DD}, V_{SS} shorted and all other signals shorted at the die side (not pin).

NOTE 2 Package only impedance (Zpkg) is calculated based on the computed Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT(Lpkg/Cpkg) (Lpkg and Cpkg for trace only, i.e. without including the ball).

NOTE 3 Package only delay (Tdpkg) is calculated based on computed Lpkg and Zpkg total for a given pin where: Tdpkg (total per pin) = SQRT(Lpkg*Cpkg) (Lpkg and Cpkg for trace only, i.e. without including the ball).

NOTE 4 This value applies to DCS.

NOTE 5 Absolute value of MAX(ZI_{DCS})-MIN(ZI_{DCS}) per sub-channel.

NOTE 6 Absolute value of MAX(TdI_{DCS})-MIN(TdI_{DCS}) per sub-channel.

NOTE 7 This value applies to DCA and DPAR.

NOTE 8 Absolute value of MAX(ZI_{DCA})-MIN(ZI_{DCA}) per sub-channel.

NOTE 9 Absolute value of MAX(TdI_{DCA})-MIN(TdI_{DCA}) per sub-channel.

NOTE 10 This value applies to QxCS.

NOTE 11 Absolute value of MAX(ZI_{QCS})-MIN(ZI_{QCS}) per sub-channel.

NOTE 12 Absolute value of MAX(TdI_{QCS})-MIN(TdI_{QCS}) within A or B output group in sub-channel.

NOTE 13 This value applies to QxCA.

NOTE 14 Absolute value of MAX(ZI_{QCA})-MIN(ZI_{QCA}) per sub-channel.

NOTE 15 Absolute value of MAX(TdI_{QCA})-MIN(TdI_{QCA}) within A or B output group in sub-channel.

NOTE 16 This value applies to BCOM, BCS, and BRST.

NOTE 17 Absolute value of MAX(ZI_{BC})-MIN(ZI_{BC}) per sub-channel.

NOTE 18 Absolute value of MAX(TdI_{BC})-MIN(TdI_{BC}) per sub-channel.

NOTE 19 Single-ended impedance.

NOTE 20 Absolute value of ZIDCK_t - ZIDCK_c.

NOTE 21 Absolute value of TdIDCK_t - TdIDCK_c.

NOTE 22 Absolute value of ZOQxCK_N_t - ZOQxCK_N_c.

NOTE 23 Absolute value of TdIQxCK_N_t - TdIQxCK_N_c.

16.1 Electrostatic Discharge Sensitivity Characteristics

Table 231 — Electrostatic Discharge Sensitivity Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Human body model (HBM)	ESD_{HBM}	1000	-	V	1, 2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	1, 3

NOTE 1 State-of-the-art basic ESD control measures have to be in place when handling devices.
NOTE 2 Refer to JEDEC / ESDA Joint Standard JS-001 for measurement procedures.
NOTE 3 Refer to ANSI / ESDA / JEDEC Joint Standard JS-002 f for measurement procedures.

17 SidebandBus Interface Electrical and Timing Specifications

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the DDR5RCD01 SidebandBus interface. The parameter in the DC and AC Characteristics tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuits match the measurement conditions when relying on the quoted parameters.

17.1 Operating Conditions

Table 232 — Operating Conditions for the SidebandBus Interface

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage	0.95	1.0	1.05	V

17.2 Measurement Test Conditions

Table 233 — AC Measurement Conditions for SidebandBus interface

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	40		pF
	Input rise and fall times (Open Drain)	--	120	ns
	Input rise and fall times (Push-Pull)	--	5	ns
	Input Signal (Swing) Levels	0.2 to 0.8		V
	Input Levels for Timing Reference	0.3 to 0.7		V

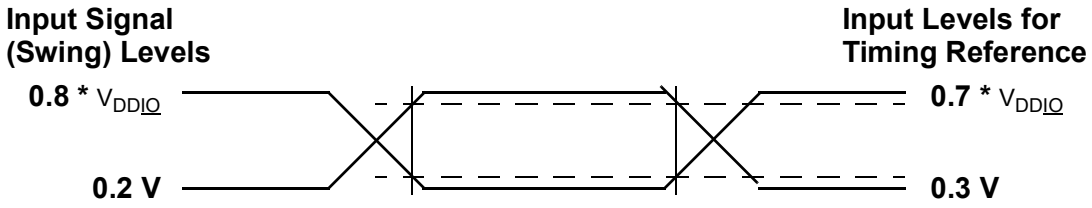


Figure 107 — AC Measurement I/O Waveform

17.3 DC Electrical Characteristics

Table 234 — Output Ron Spec

Symbol	Parameter	Min	Max	Unit	Notes
R_{ON}	SDA Output Pullup and Pulldown Driver Impedance	20	100	Ω	1
NOTE 1 Pull-down R_{on} = Vout/Iout; Pull-up R_{on} = (V_{DDIO} - Vout)/Iout					

Table 235 — Input Parameters for SidebandBus interface

Symbol	Parameter[1,2]	Test Condition	Min	Max	Unit
C_{IN}	Input capacitance (SDA)	--	--	5	pF
C_{IN}	Input capacitance (SCL)	--	--	5	pF
NOTE 1 TA = 25 °C, f = 1000 kHz NOTE 2 Verified by design and characterization, not necessarily tested on all devices					

Table 236 — DC Characteristics for SidebandBus Interface

Symbol	Parameter	Test Condition (in addition to those in Table 232 on page 239)	Min	Max	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{DDIO}	--	±5	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{DDIO}, SDA in Hi-Z	--	±5	µA
I_{DDIO}	Supply current	V_{DDIO} = 1.0 V, f_C = 12.5 MHz (rise/ fall time < 5 ns)	--	5	mA
V_{IL}	Input LOW voltage (SCL, SDA)	--	-0.35	0.3	V
V_{IH}	Input HIGH voltage (SCL, SDA)	--	0.7	1.3	V
V_{OL}	Output LOW voltage (SDA)	3-mA sink current	--	0.3	V
V_{OH}	Output HIGH voltage (SDA)	3-mA source current	V_{DDIO} - 0.3	--	V
I_{OL}	LOW-level output current	V_{OL} = 0.3 V	--	3	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DDIO}$ - 0.3	-3	--	mA
Slew_Rate	Output Slew Rate (SDA)	See Note 3	0.1	1.0	V/ns
NOTE 1 Undershoot might occur. It should be limited by the Absolute Maximum DC Ratings. NOTE 2 Overshoot might occur. It should be limited by Absolute Maximum DC Ratings NOTE 3 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 113 and Figure 112 shows the timing measurement points.					

17.4 AC Electrical Characteristics

Table 237 — AC Characteristics for SidebandBus interface

Symbol	Parameter	I²C Mode (Open Drain)[1]		I3C Basic Push-Pull[2] (12.5 MHz)		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency	0.01	1	0.01	12.5	MHz
t_{HIGH}	Clock pulse width HIGH time	260	--	35	--	ns
t_{LOW}[3]	Clock pulse width LOW time	500	--	35	--	ns
$t_{TIMEOUT}$[4,5]	Detect clock LOW timeout	10	50	10	50	ms
t_R[6,7,8]	SDA rise time	--	120	--	5	ns
t_F[6,7,8]	SDA fall time	--	120	--	5	ns
$t_{SU:DAT}$[6,9]	Data in setup time	50	--	8	--	ns
$t_{HD:DI}$[6,9]	Data in hold time	0	--	3	--	ns
$t_{SU:STA}$[6,10]	START condition setup time	260	--	12	--	ns
$t_{HD:STA}$[6]	START condition hold time	260	--	30	--	ns
$t_{SU:STO}$[6]	STOP condition setup time	260	--	12	--	ns
t_{BUF}[6]	Time between STOP Condition and next START Condition	500	--	500	--	ns
$t_{HD:DAT}$[11]	Data out hold time	0.5	350	N/A	N/A	ns
t_{DOUT}[12,13]	SCL Falling Clock In to Valid SDA Data Out Time	N/A	N/A	0.5	12	ns
t_{DOFFT}[12,14]	SCL Rising Clock In to Target SDA Output Off	N/A	N/A	0.5	12	ns
t_{DOFFC}[12,15]	SCL Rising Clock In to Controller SDA Output Off	N/A	N/A	0.5	12	ns
$t_{CL_r_DAT_f}$[16]	SCL Rising Clock In to Controller Driving Data Signal LOW	N/A	N/A	40	--	ns
t_{AVAL}	Bus Available Time (no edges seen on SDA and SCL)	N/A	N/A	1	--	µs
t_{IBI_Issue}	Time to issue IBI after an event is detected when Bus is available	-	-	-	15	µs
$t_{CLR_I3C_CMD_Delay}$	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation (PEC Disabled)	-	-	4	-	µs
	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation (PEC Enabled)	-	-	15	-	µs
$t_{DEVCTRLCCC_DELAY_PEC_DIS}$	DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay[17,18,19]	3	--	3	--	µs
$t_{WR_RD_DELAY_PEC_EN}$	Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode[18,19,20]	N/A	N/A	8	--	µs
$t_{I2C_CCC_Update_Delay}$	Minimum delay from SETHID CCC or SETAASA CCC to any other CCC or Read/Write Command	2.5	-	N/A	N/A	µs
$t_{I3C_CCC_Update_Delay}$	Minimum delay from ENEC/DISEC CCC or RSTDAA CCC to any other CCC or Read/Write Command	N/A	N/A	2.5	-	µs
t_{CCC_Delay}	Delay from any CCC to RSTDAA CCC	N/A	N/A	2.5	-	µs

NOTE 1 The timing parameters listed under this column correspond to Fast-mode Plus from the I²C specification. The DDR5RCD01 device must also support the values and conditions corresponding to the other (lower) speed modes supported by I²C specification. Namely, Standard-mode and Fast-mode.

NOTE 2 I3C Basic mode with Open Drain operation follows timing values as shown in I²C Mode - Open Drain column.

NOTE 3 The DDR5RCD01 I²C/I3C Basic interface logic shall not initiate clock stretching.

NOTE 4 The DDR5RCD01 must support bus timeout on I²C/I3C Basic access.

NOTE 5 Devices participating in a transfer can abort the transfer in progress and release the bus by forcing SCL LOW. A timeout condition can only be ensured if the device forcing the timeout holds SCL LOW for $t_{TIMEOUT,MAX}$ or longer. After the controller in a transaction detects this condition, it must generate a STOP condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 10ms after the controller generates the STOP condition.
NOTE 6 See Figure 108 for input timing definitions.
NOTE 7 See Figure 111 for voltage threshold definitions for rise and fall times.
NOTE 8 Guaranteed by design and characterization, not necessarily tested.
NOTE 9 The input setup time is referenced from SDA V_{IL} or V_{IH} threshold to SCL V_{IL} threshold as shown in Figure 108. The input hold time is referenced from SCL V_{IL} threshold to SDA V_{IL} or V_{IH} threshold as shown in Figure 108.
NOTE 10 For a reSTART condition, or following a write cycle.
NOTE 11 The DDR5RCD01 device guarantees $t_{HD:DAT}$ value in I^2C mode of operation. See Figure 109 for I^2C output timing definitions as well as SCL clock input threshold level and SDA data output threshold levels.
NOTE 12 This timing parameter is guaranteed into output timing reference load as shown in Figure 113.
NOTE 13 The DDR5RCD01 must be configured in I3C Basic mode to guarantee t_{DOUT} value. See Figure 110 for I3C Basic output timing definition as well as SCL clock input threshold level and SDA data output threshold levels. See Figure 113 for output timing parameter measurement reference load.
NOTE 14 The DDR5RCD01 must be configured in I3C Basic mode to guarantee t_{DOFFT} value. See Figure 114. See Figure 113 for output timing parameter measurement reference load.
NOTE 15 The DDR5RCD01 must be configured in I3C Basic mode to guarantee t_{DOFFC} value. See Figure 115. See Figure 113 for output timing parameter measurement reference load.
NOTE 16 The DDR5RCD01 must be configured in I3C Basic mode to guarantee $t_{CL_r_DAT_f}$ value. See Figure 117.
NOTE 17 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.
NOTE 18 The device sends NACK if Host does not satisfy this timing parameter.
NOTE 19 This timing constraint is only applicable when PEC is disabled. If PEC is enabled, this timing parameter does not apply.
NOTE 20 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.

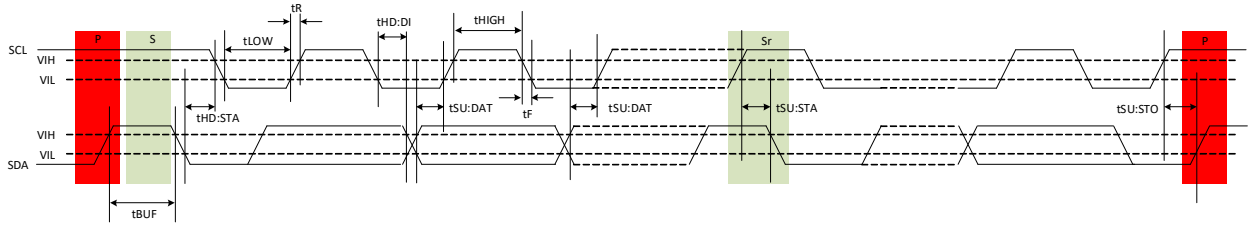


Figure 108 — I^2C and I3C Basic AC Input Timing Parameter Definitions

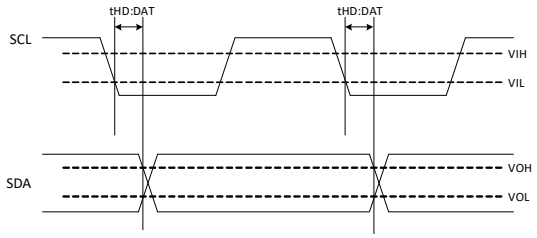


Figure 109 — I^2C Bus AC Output Timing Parameter Definitions

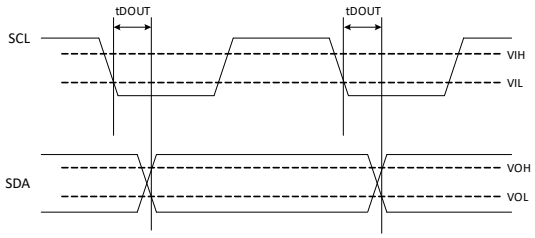


Figure 110 — I3C Basic AC Output Timing Parameter Definitions

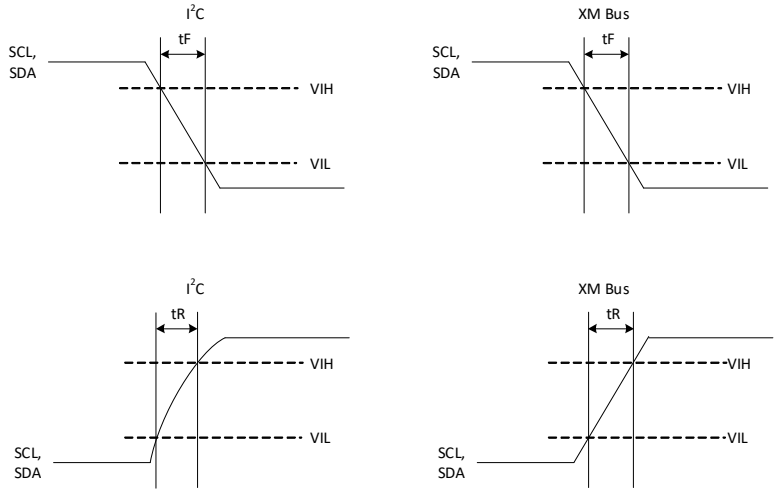


Figure 111 — Rise and Fall Timing Parameter Definitions

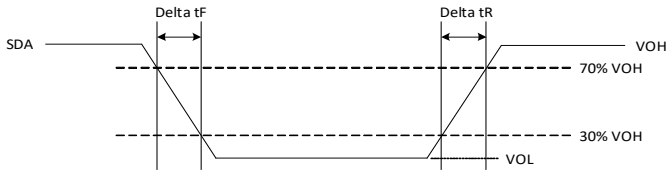


Figure 112 — Output Slew Rate Measurement Points

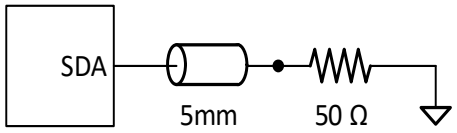


Figure 113 — Test Load for Output Slew Rate and Output Timing Measurement

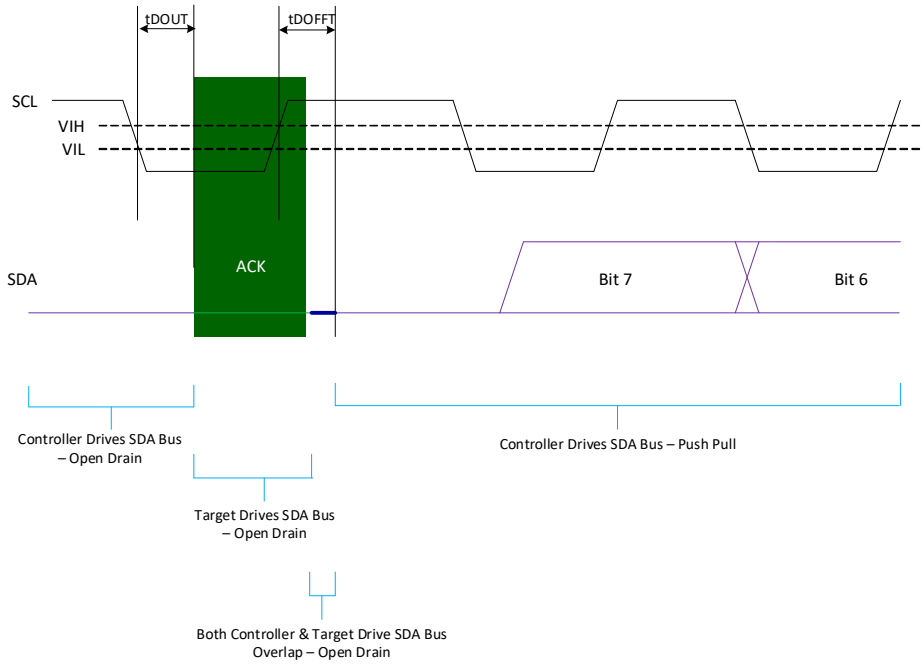


Figure 114 — I3C Basic Hand-off Operation - RCD Open Drain (ACK) to Controller Push-Pull

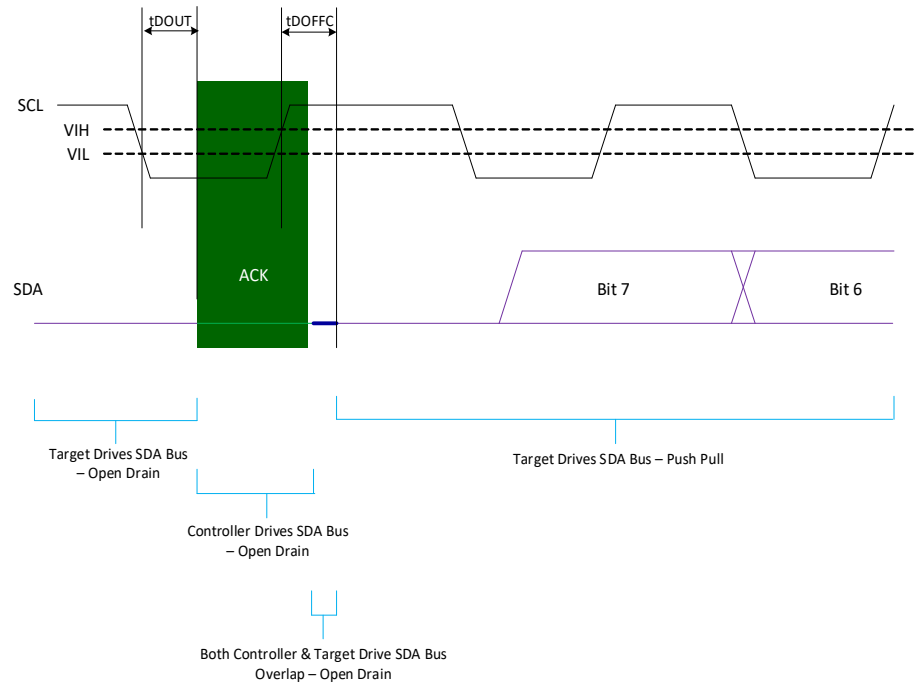


Figure 115 — I3C Basic Hand-off Operation - Controller Open Drain (ACK) to RCD Push-Pull

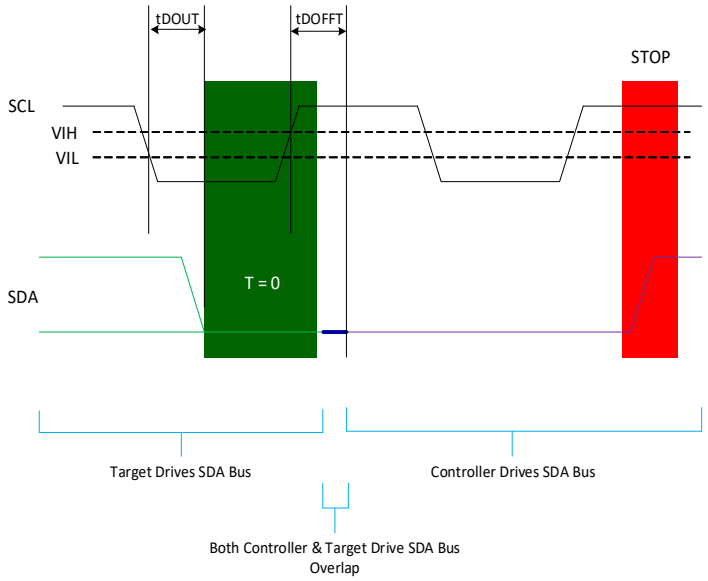


Figure 116 — I3C Basic T=0 Transition from RCD Read Operation to Controller STOP bit

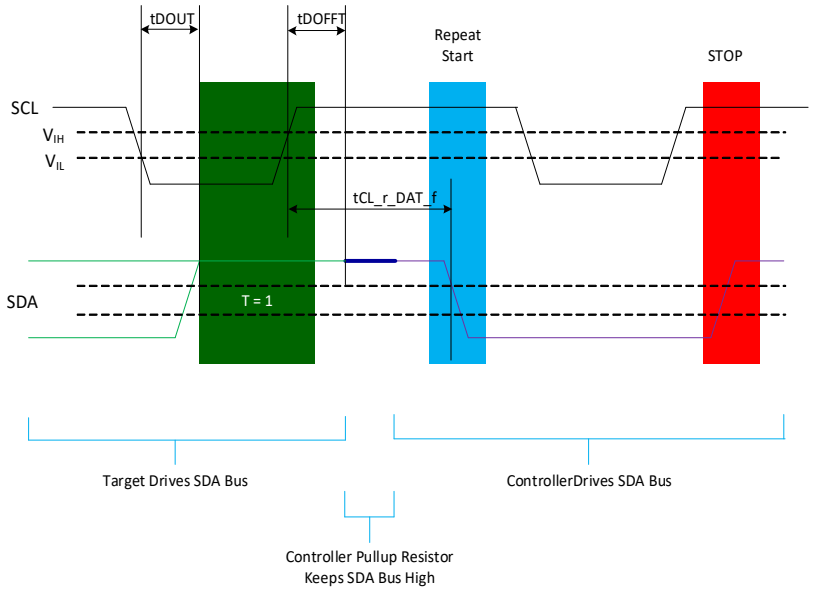


Figure 117 — I3C Basic T = 1 Transition from RCD Read Operation Interrupted by Controller Repeated START and STOP bit

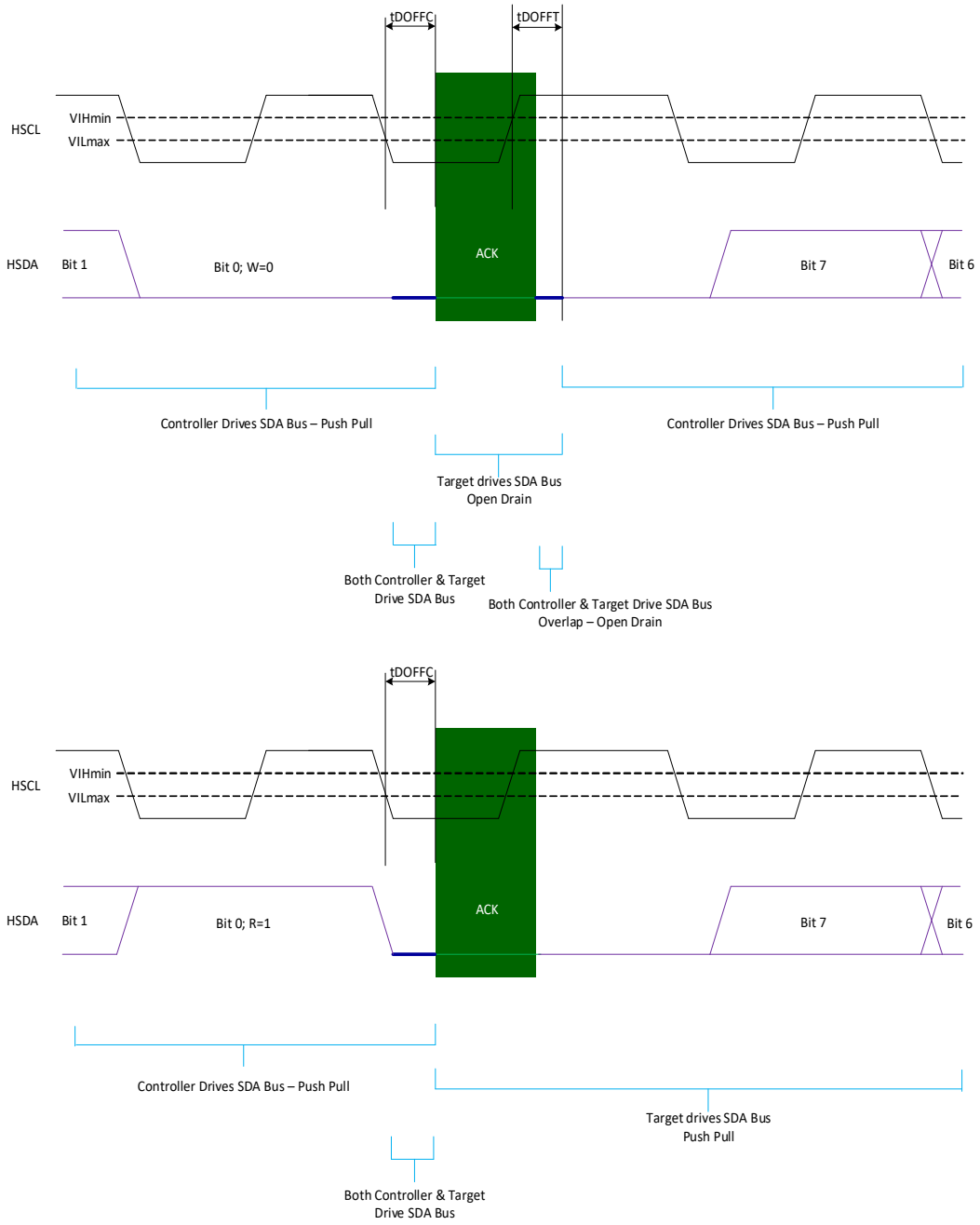
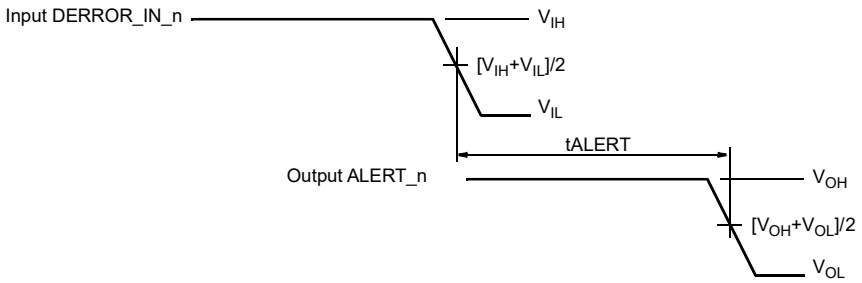


Figure 118 — Controller Push Pull to Target Open Drain Hand Off Operation

18 Test Circuits and Switching Waveforms

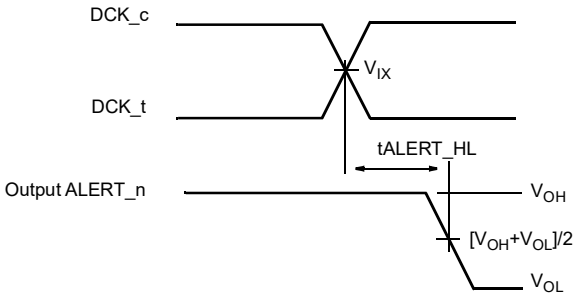
18.1 Alert Output Voltage Measurement Information

All input pulses are supplied by generators having the following characteristics: 1000 MHz ≤ PRR (Pulse Repetition Rate) ≤ 2436 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



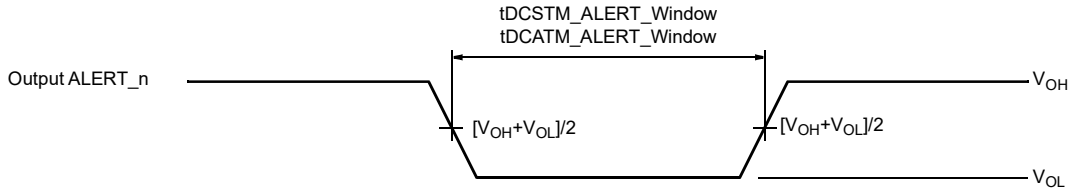
NOTE 1 V_{IH} and V_{IL} represent the applied Logic HIGH and LOW input DC voltage levels resulting from 50-Ω driver into the default on-die termination (60 Ω).
NOTE 2 V_{OH} and V_{OL} represent the measured Logic HIGH and LOW output DC voltage levels into the test load (50 Ω).

Figure 119 — Voltage waveforms, tALERT Measurement



NOTE 1 V_{OH} and V_{OL} represent the measured Logic HIGH and LOW output DC voltage levels into the test load (50 Ω).

Figure 120 — Voltage waveforms, tALERT_HL Measurement



NOTE 1 V_{OH} and V_{OL} represent the measured Logic HIGH and LOW output DC voltage levels into the test load (50 Ω).

Figure 121 — Voltage waveforms, tDCSTM_ALERT_Window and tDCATM_ALERT_Window Measurements

18.2 DDR5RCD01 Reference Load

The following circuit represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

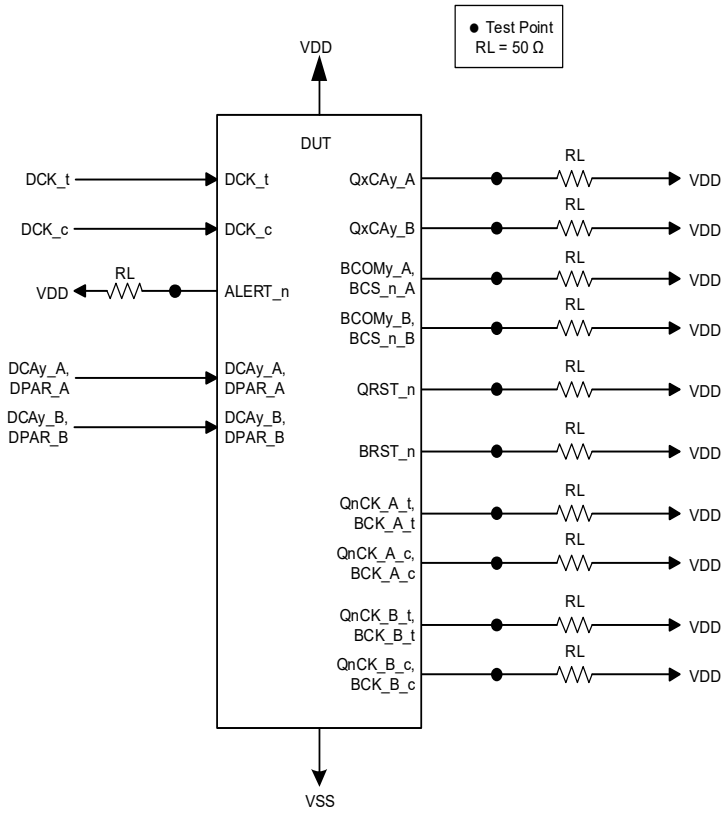


Figure 122 — Test Load

19 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*

JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*

JESD21-C, *Configuration for Solid State Memories.*

JESD8-11A, *Definition of wide range non-terminated logic.*

JESD79-5, *DDR5 SDRAM Specification.*

JESD82-521*, DDR5DB01 Specification.*

MO-330A, *Package Mechanical Outline.*

I3C Basic, *Specification for I3C Basic Version 1.0 – 19 July 2018.*

JESD403-1, *Specification for JEDEC Module SidebandBus.*

JS-001-2017, *Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test – Human Body Model (HBM) – Component Level.*

JS-002-2018, *ANSI/ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.*

Standard Improvement Form JEDEC _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

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