JEDEC STANDARD

Definition of CDCV857 PLL Clock Driver for Registered DDR DIMM Applications

JESD82

JULY 2000

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

Electronic Industries Alliance

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the EIA General Counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby an JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7560/7559 or www.jedec.org

Published by
JEDEC Solid State Technology Association 2000
2500 Wilson Boulevard
Arlington, VA 22201-3834

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering Documents, USA and Canada (1-800-854-7179), International (303-397-7956)

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS

(Formerly JEDEC Council Ballot JCB-00-22, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Background

1.1 Purpose

The purpose is to provide a standard for a CDCV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

1.2 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of a CDCV857 PLL clock device for registered DDR DIMM applications.

2 Definitions for the purpose of this document

$C_{I(\Delta)}$ – Delta input capacitance.

3 Device standard

3.1 Description

This PLL Clock Buffer is designed for 2.5 V_{DD} and 2.5 AV_{DD} operation and differential data input and output levels. Package options include plastic Thin Shrink Small-Outline Package (TSSOP).

The device is a zero delay buffer that distributes a differential clock input pair (CK, $\overline{CK}$) to ten differential pair of clock outputs (Y[0:9], $\overline{Y[0:9]}$) and one differential pair feedback clock outputs (FBOUT, $\overline{FBOUT}$). The clock outputs are controlled by the input clocks (CK, $\overline{CK}$), the feedback clocks (FBIN, $\overline{FBIN}$), the 2.5-V LVCMOS input ($\overline{PWRDWN}$) and the Analog Power input (AV_{DD}). When input $\overline{PWRDWN}$ is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are 3-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than approximately 20 MHz, which is below the operating frequency of the PLL, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the $\overline{PWRDWN}$ input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FBIN, $\overline{FBIN}$) and the input clock pair (CK, $\overline{CK}$).

The PLL in the CDCV857 clock driver uses the input clocks (CK, $\overline{CK}$) and the feedback clocks (FBIN, $\overline{FBIN}$) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], $\overline{Y[0:9]}$). The CDCV857 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

The CDCV857 is characterized for operation from 0 ^{o}C to 70 ^{o}C.

3.2 Pinout figure

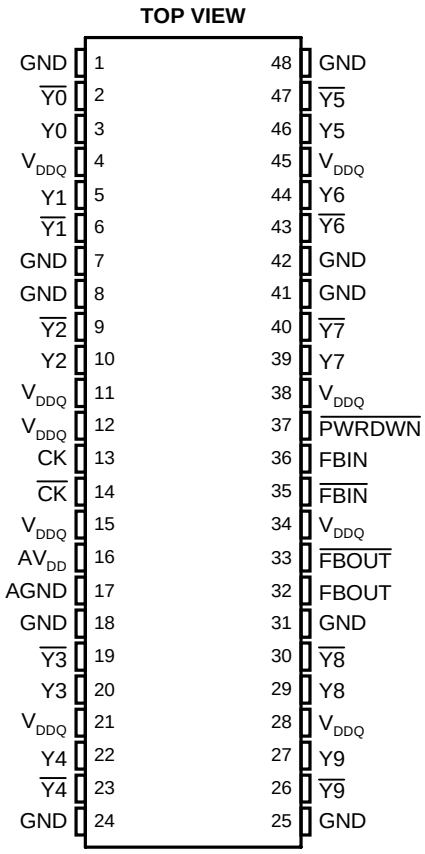


Figure 1 — 48-Pin dual inline package pinout

3.3 Terminal functions

Table 1 — Thermal functions

Terminal Name	Description	Electrical Characteristics
AGND	Analog Ground	Ground
AV_{DD}	Analog power	2.5 V nominal
CK	Clock input	Differential input
$\overline{CK}$	Complementary clock input	Differential input
FBIN	Feedback clock input	Differential input
$\overline{FBIN}$	Complementary feedback clock input	Differential input
FBOUT	Feedback clock output	Differential input
$\overline{FBOUT}$	Complementary feedback clock output	Differential input
$\overline{PWRDWN}$	Power down	LVCMOS input
GND	Ground	Ground
V_{DDQ}	Logic and output power	2.5 V nominal
Y[0:9]	Clock outputs	Differential outputs
$\overline{Y[0:9]}$	Complementary clock outputs	Differential outputs

3.4 Function table

Table 2 — Function table

Inputs				Outputs				PLL
AV_{DD}	$\overline{PWRDWN}$	CK	$\overline{CK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5V(nom)	H	L	H	L	H	L	H	On
2.5V(nom)	H	H	L	H	L	H	L	On
2.5V(nom)	X	<20MHz	<20MHz	Z	Z	Z	Z	Off

3.5 Logic diagram

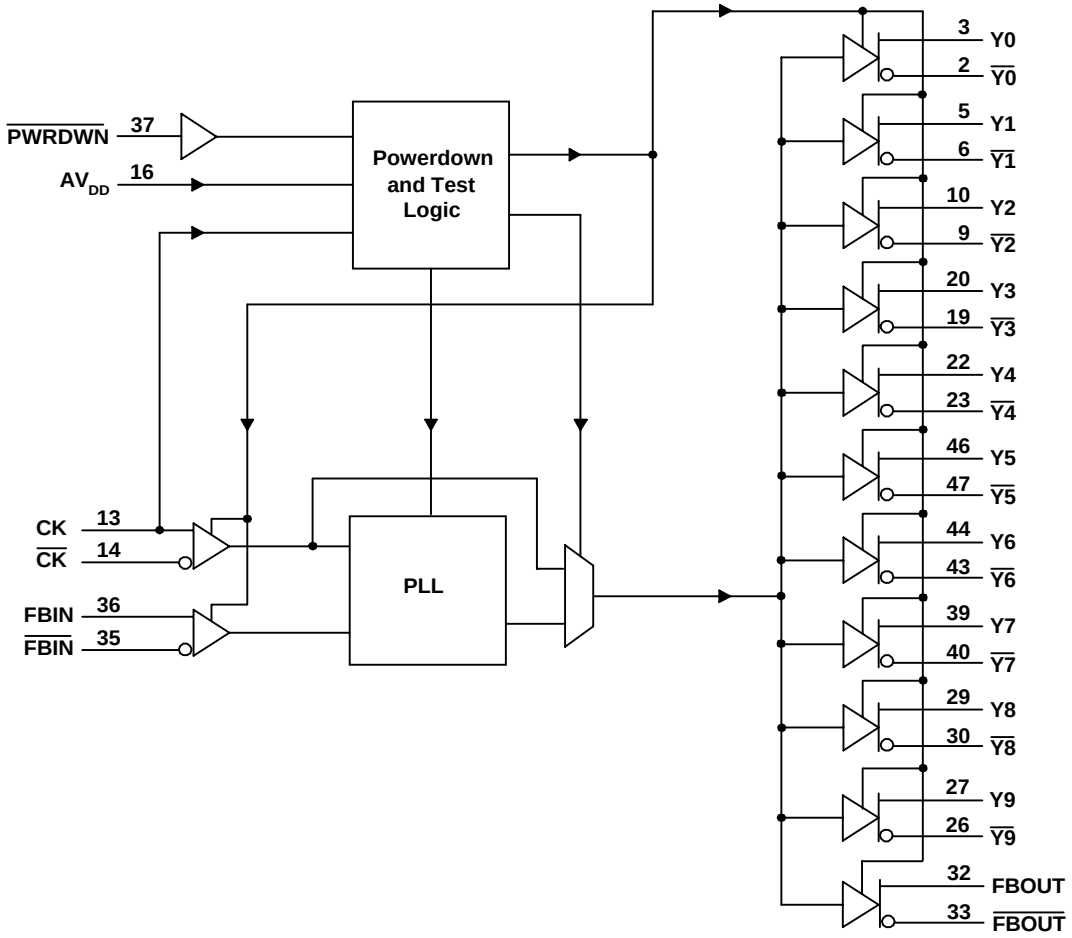


Figure 2 — Logic diagram (positive logic)

3.6 Absolute maximum ratings

Table 3 — Absolute maximum ratings over operating free-air temperature range (see Note 1)

Supply voltage range, V_{DDQ} or AV_{DD} . . . . . –0.5 V to 3.6 V
Input voltage range, V_I (see Notes 2 and 3) . . . . . –0.5 to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 2 and 3). . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ}) . . . . . ±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}). . . . . ±50 mA
Continuous current through each V_{DD}, V_{DDQ} or GND . . . . . ±100 mA
Storage temperature range, T_{STG}. . . . . –65 °C to 150 °C

NOTES

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

3. This value is limited to 3.6 V maximum.

3.7 Recommended operating conditions

Table 4 — Recommended operating conditions (see Note 4)

			Min	Nom	Max	Unit
V_{DDQ}	Output supply voltage		2.3	2.5	2.7	V
AV_{DD}	Supply voltage	See Note 4		V_{DDQ}		
V_{IL}	Low-level input voltage	$\overline{PWRDWN}$	–0.3		0.7	V
V_{IH}	High-level input voltage	$\overline{PWRDWN}$	1.7		V_{DDQ} + 0.3	V
V_I	Input voltage		0		V_{DDQ}	V
I_{OH}	High-level output current				12	mA
I_{OL}	Low-level output current				–12	mA
V_{IX}	Input differential-pair cross voltage		(V_{DDQ}/2) – 0.2		(V_{DDQ}/2) + 0.2	V
V_{OX}	Output differential-pair cross-voltage	See Note 5	(V_{DDQ}/2) – 0.2		(V_{DDQ}/2) + 0.2	V
V_{IN}	Input voltage level		–0.3		V_{DDQ} + 0.3	V
V_{ID}	Input differential voltage	See Note 6	0.36		V_{DDQ} + 0.6	V
V_{OD}	Output differential voltage	See Note 7	0.70		V_{DDQ} + 0.6	V
T_A	Operating free-air temperature		0		70	°C

NOTES

4. The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operationing conditions and no timing parameters are guaranteed.

5. V_{OX} specified at the DRAM clock input or the test load.

6. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

7. V_{OD} is the magnitude of the difference of the output level between Y[n] and $\overline{Y[n]}$, and FBOUT and $\overline{FBOUT}$.

3.8 DC specifications

Table 5 — Electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	AV_{DD}, V_{DDQ}	MIN	TYP	MAX	UNIT
V_{IK}	All inputs	I_I = –18 mA	2.3 V			–1.2	V
V_{OH}	High output voltage	I_{OH} = –100 µA	2.3 to 2.7 V	V_{DDQ}–0.1			V
		I_{OH} = –12 mA	2.3 V	1.7			
V_{OL}	Low output voltage	I_{OL} = 100 µA	2.3 to 2.7 V			0.1	V
		I_{OL} = 12 mA	2.3 V			0.6	
I_I	CK, FBIN	$V_I = V_{DD}$ or GND	2.7 V			±10	µA
	$\overline{PWRDWN}$	$V_I = V_{DD}$ or GND	2.7 V			±10	
I_{DDQ}	Dynamic supply current	CK and $\overline{CK}$ = 170 MHz	2.7 V		200	300	mA
	Static supply current	CK and $\overline{CK}$ < 20 MHz or $\overline{PWRDWN}$ = Low				100	µA
I_{ADD}	Dynamic supply current	CK and $\overline{CK}$ = 170 MHz	2.7 V		9	12	mA
	Static supply current	CK and $\overline{CK}$ < 20 MHz or $\overline{PWRDWN}$ = Low				100	µA
C_I	CK and $\overline{CK}$	$V_I = V_{DD}$ or GND	2.5 V	2.5		3.5	pF
	FBIN and $\overline{FBIN}$	$V_I = V_{DD}$ or GND		2.5		3.5	
$C_{I(\Delta)}$	CK and $\overline{CK}$	$V_I = V_{DD}$ or GND		–0.25		0.25	
	FBIN and $\overline{FBIN}$	$V_I = V_{DD}$ or GND		–0.25		0.25	

3.9 Timing requirements

Table 6 — Timing requirements over recommended operating free-air temperature range

		AV_{DD}, V_{DD} = 2.5 V ± 0.2 V		UNIT
		MIN	MAX	
f_{CK}	Operating clock frequency (see Notes 8 and 9)	60	170	MHz
	Application clock frequency (see Notes 8 and 10)	95	170	MHz
t_{DC}	Input clock duty cycle	40	60	%
t_{STAB}	Stabilization time (see Note 11)		100	μsec

NOTES

8. The PLL must be able to handle spread spectrum induced skew.

9. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)

10. Application clock frequency indicates a range over which the PLL must meet all timing parameters.

11. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal when the input clock frequency falls below 20 MHz, entered the power-down mode and later increased above 20 MHz.

3.10 AC specifications

Table 7 — Switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	DESCRIPTION	Diagram	AV_{DD}, V_{DD} = 2.5 V ± 0.2 V			UNIT
			MIN	Nom	MAX	
*t*jit(cc)	Cycle-to-cycle jitter	see Figure 5	–75		75	ps
t(∅)	Static phase offset (see Note 12)	see Figure 6	–50	0	50	ps
*t*sk(o)	Output clock skew	see Figure 7			100	ps
*t*jit(per)	Period jitter (see Note 13)	see Figure 8	–75		75	ps
*t*jit(hper)	Half-period jitter (see Note 13)	see Figure 9	–100		100	ps
*t*sl(i)	Input clock slew rate	see Figure 10	1.0		4.0	V/ns
*t*sl(o)	Output clock slew rate (see Note 14)	see Figure 10	1.0		2.0	V/ns
The PLL on the CDCV857 must be capable of meeting all the above test parameters while supporting SSC synthesizers (see Note 15) with the following parameters:						
	SSC modulation frequency		30.00		50.00	KHz
	SSC clock input frequency deviation		0.00		–0.50	%
CDCV857 PLL designs should target the values below to meet the 200 ps maximum of SSC induced skew:						
	PLL loop bandwidth (see Note 16)		2.0			MHz
	Phase angle				–0.031	degrees

NOTES

12. Static Phase Offset does not include Jitter.

13. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.

14. The Output Slew Rate is determined from the IBIS model into the load shown in Figure 3.

15. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

16. Each Individual vendor must supply a plot (Gain vs. Frequency) of the PLL's closed loop bandwidth.

4 Output Buffer Characteristics

4.1 Purpose

The following table describes output-buffer Voltage vs. Current (V/I) characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these curves is not mandatory if it can be adequately demonstrated that alternate characteristics meet the requirements of the registered DDR DIMM application.

Table 8 — Output buffer voltage vs. current (V/I) characteristics

Voltage (V)	Pull-Down			Pull-Up		
	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)
	TYP	MIN	MAX	TYP	MIN	MAX
–2.7	–91.7	–79.2	–112	127	100	169
–2.6	–88.2	–76.2	–108	122	96.6	162
–2.5	–84.8	–73.2	–104	117	92.8	156
–2.4	–81.3	–70.2	–99.4	112	88.9	150
–2.3	–77.9	–67.2	–95.3	108	85.1	143
–2.2	–74.4	–64.1	–91.1	103	81.3	137
–2.1	–71.0	–61.1	–86.9	98.2	77.4	131
–2.0	–67.5	–58.1	–82.7	93.5	73.6	124
–1.9	–64.1	–55.1	–78.6	88.7	69.8	118
–1.8	–60.6	–52.1	–74.4	83.9	65.9	112
–1.7	–57.2	–49.0	–70.2	79.2	62.1	106
–1.6	–53.8	–46.0	–66.1	74.4	58.2	99.2
–1.5	–50.3	–43.0	–61.9	69.7	54.4	92.9
–1.4	–46.9	–40.0	–57.7	64.9	50.6	86.6
–1.3	–43.4	–37.0	–53.6	60.1	46.7	80.3
–1.2	–40.0	–33.9	–49.4	55.4	42.9	74.0
–1.1	–36.5	–30.9	–45.2	50.6	39.1	67.7
–1.0	–33.1	–27.9	–41.0	45.9	35.2	61.4
–0.9	–29.6	–24.9	–36.9	41.1	31.4	55.1
–0.8	–26.2	–21.9	–32.7	36.3	27.6	48.8
–0.7	–22.8	–18.9	–28.5	31.6	23.8	42.5
–0.6	–19.4	–16.0	–24.4	26.8	19.7	36.2
–0.5	–15.7	–12.5	–20.1	22.1	16.2	29.9
–0.4	–12.5	–9.9	–16.1	17.5	12.7	23.8
–0.3	–9.4	–7.4	–12.1	12.9	9.4	17.7
–0.2	–6.3	–4.9	–8.1	8.5	6.1	11.7
–0.1	–3.1	–2.5	–4.0	4.2	3.0	5.8
0	0	0	0	0	0	0
0.1	3.1	2.4	4.0	–4.0	–2.8	–5.6
0.2	6.2	4.8	8.0	–7.8	–5.4	–10.9
0.3	9.2	7.2	11.9	–11.3	–7.9	–16.0
0.4	12.2	9.5	15.8	–14.7	–10.2	–20.8

Table 8 — Output buffer voltage vs. current (V/I) characteristics

Voltage (V)	Pull-Down			Pull-Up		
	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)
	TYP	MIN	MAX	TYP	MIN	MAX
0.5	15.1	11.8	19.6	–17.8	–12.3	–25.3
0.6	17.9	14.0	23.3	–20.7	–14.2	–29.5
0.7	20.7	16.1	27.0	–23.4	–15.9	–33.5
0.8	23.4	18.2	30.5	–25.8	–17.4	–37.1
0.9	26.1	20.2	34.0	–28.0	–18.8	–40.5
1.0	28.7	22.1	37.4	–29.9	–19.9	–43.6
1.1	31.2	24.0	40.8	–31.6	–20.8	–46.4
1.2	33.6	25.7	44.0	–33.1	–21.6	–48.9
1.3	35.9	27.4	47.1	–34.3	–22.1	–51.1
1.4	38.1	29.0	50.1	–35.3	–22.6	–53.0
1.5	40.2	30.4	53.0	–36.1	–22.9	–54.6
1.6	42.2	31.8	55.7	–36.7	–23.1	–55.9
1.7	44.0	32.9	58.3	–37.3	–23.3	–57.1
1.8	45.7	34.0	60.8	–37.7	–23.5	–58.0
1.9	47.2	34.8	63.0	–38.1	–23.7	–58.8
2.0	48.6	35.5	65.0	–38.5	–23.9	–59.6
2.1	49.6	36.0	66.7	–38.9	–24.1	–60.2
2.2	50.5	36.4	68.1	–39.2	–24.2	–60.8
2.3	51.1	36.7	69.1	–39.5	–24.3	–61.3
2.4	51.6	37.0	69.8	–39.7	–24.5	–61.8
2.5	52.0	37.2	70.4	–40.0	–24.6	–62.3
2.6	52.3	37.4	70.8	–40.3	–24.7	–62.7
2.7	52.6	37.6	71.1	–40.5	–24.9	–63.1
2.8	52.8	37.8	71.4	–40.7	–25.0	–63.5
2.9	53.0	38.0	71.7	–40.9	–25.1	–63.9
3.0	53.2	38.2	71.9	–41.2	–25.2	–64.2
3.1	53.5	38.3	72.1	–41.4	–25.4	–64.6
3.2	53.7	38.5	72.4	–41.6	–25.5	–64.9
3.3	53.9	38.7	72.6	–41.8	–25.6	–65.2
3.4	54.1	38.9	72.9	–42.1	–25.7	–65.6
3.5	54.3	39.1	73.1	–42.3	–25.9	–65.9
3.6	54.6	39.2	73.4	–42.5	–26.0	–66.3
3.7	54.8	39.4	73.6	–42.7	–26.1	–66.6
3.8	55.0	39.6	73.9	–43.0	–26.2	–66.9
3.9	55.2	39.8	74.1	–43.2	–26.4	–67.3
4.0	55.4	40.0	74.4	–43.4	–26.5	–67.6
4.1	55.7	40.1	74.6	–43.6	–26.6	–68.0
4.2	55.9	40.3	74.8	–43.9	–26.7	–68.3
4.3	56.1	40.5	75.1	–44.1	–26.9	–68.6

Table 8 — Output buffer voltage vs. current (V/I) characteristics

Voltage (V)	Pull-Down			Pull-Up		
	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)
	TYP	MIN	MAX	TYP	MIN	MAX
4.4	56.3	40.7	75.3	–44.3	–27.0	–69.0
4.5	56.5	40.9	75.6	–44.5	–27.1	–69.3
4.6	56.8	41.0	75.8	–44.8	–27.2	–69.7
4.7	57.0	41.2	76.1	–45.0	–27.4	–70.0
4.8	57.2	41.4	76.3	–45.2	–27.5	–70.3
4.9	57.4	41.6	76.6	–45.4	–27.6	–70.7
5.0	57.6	41.8	76.8	–45.7	–27.7	–71.0
5.1	57.9	41.9	77.1	–45.9	–27.9	–71.4
5.2	58.1	42.1	77.3	–46.1	–28.0	–71.7
5.3	58.3	42.3	77.5	–46.3	–28.1	–72.0
5.4	58.5	42.5	77.8	–46.6	–28.2	–72.4

5 Test circuit and switching waveforms

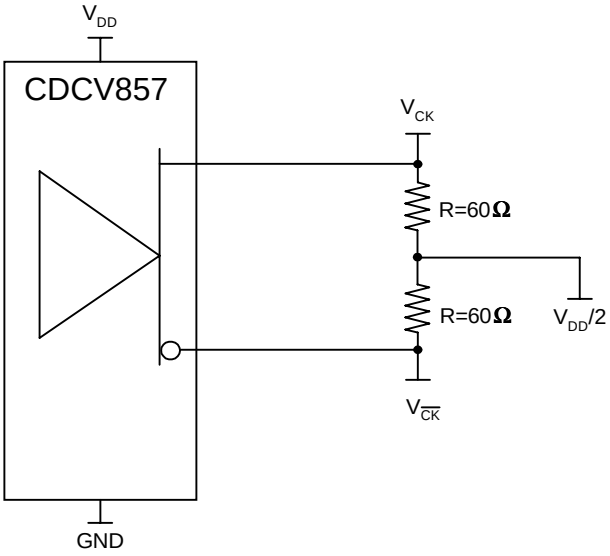


Figure 3 — IBIS model output load

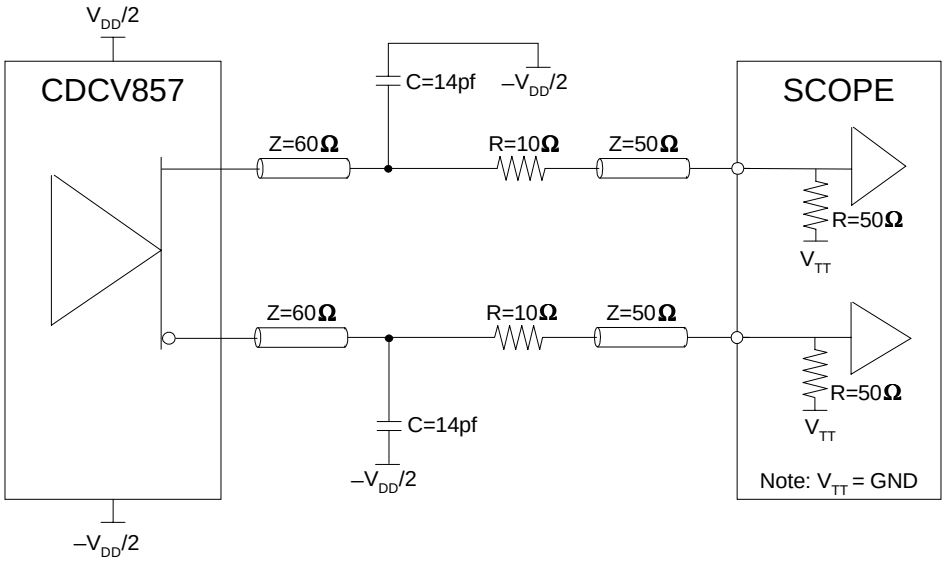


Figure 4 — Output load test circuit

5 Test circuit and switching waveforms (cont'd)

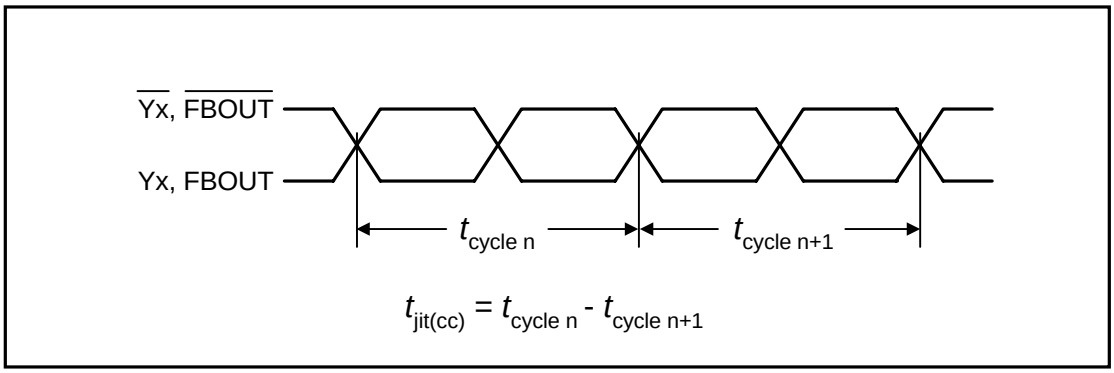


Figure 5 — Cycle-to-cycle jitter

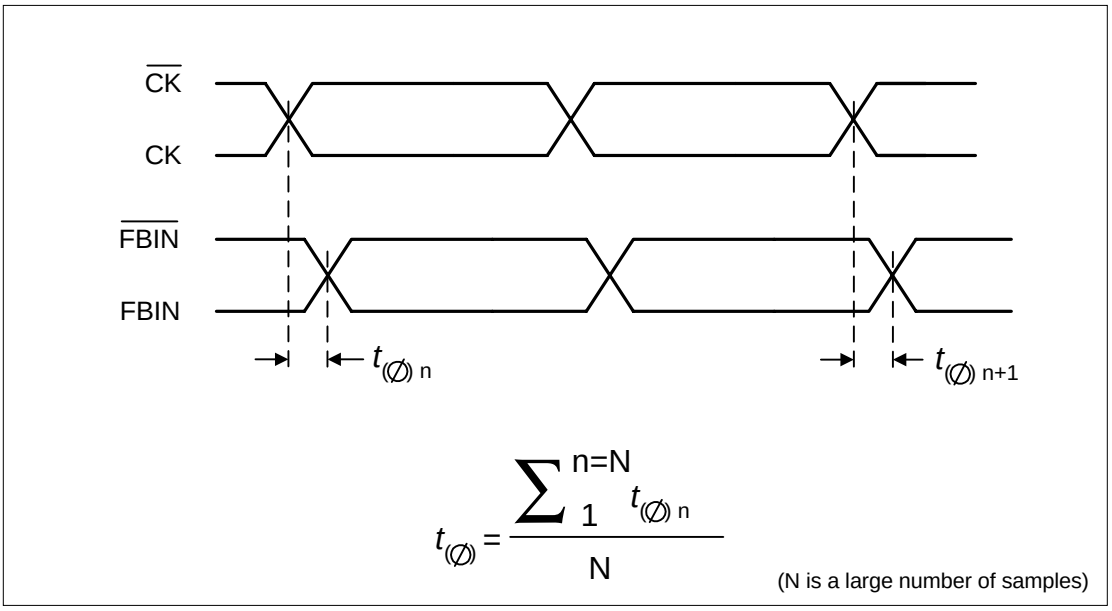


Figure 6 — Static phase offset

5 Test circuit and switching waveforms (cont'd)

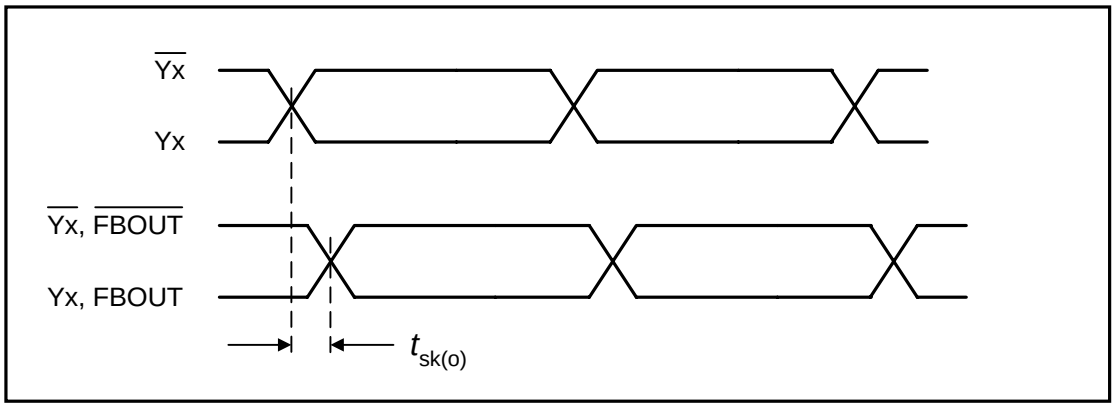


Figure 7 — Output skew

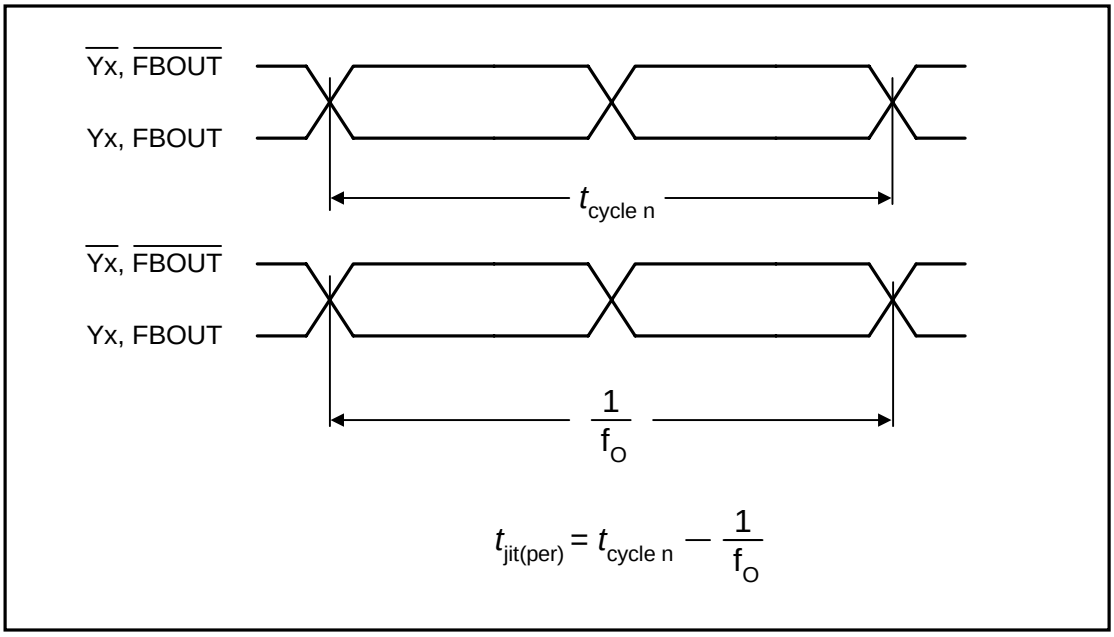


Figure 8 — Period jitter

5 Test circuit and switching waveforms (cont'd)

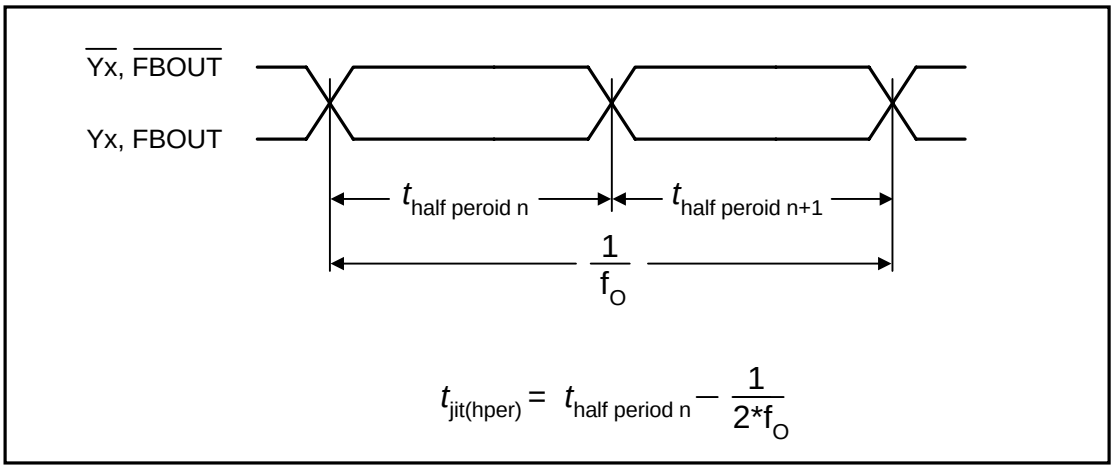


Figure 9 — Half-period jitter

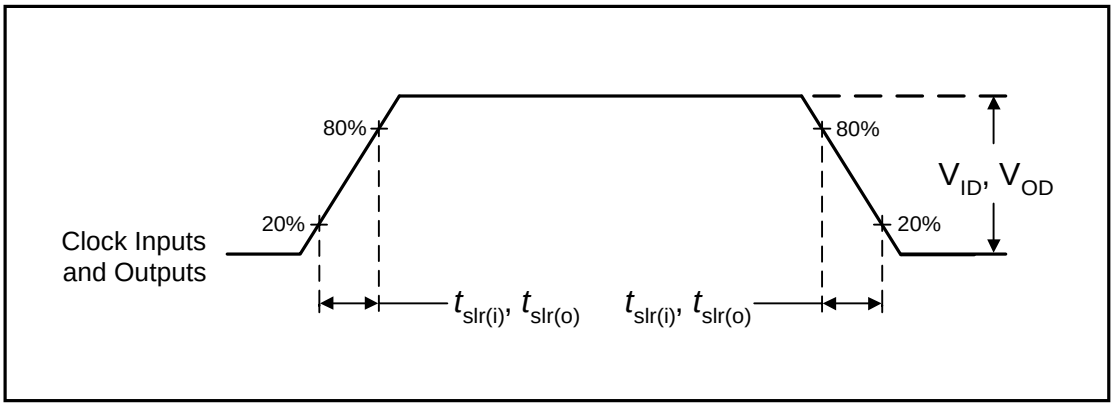


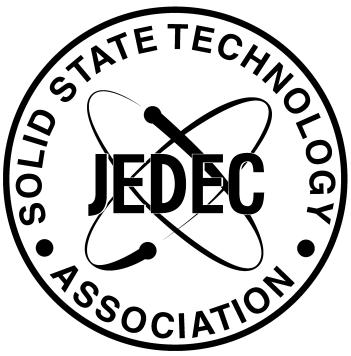
Figure 10 — Input and output slew rates

6 Reference to other applicable JEDEC standards and publications

JESD65: *Definition of Skew Specification for Standard Logic Devices*

JESD8-5: *2.5 Volt ± 0.2 V (Normal Range) and 1.8 V to 2.7 V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits.*

JESD21-C: *Configuration for Solid State Memories*


SOLID STATE TECHNOLOGY
JEDEC
ASSOCIATION