# JEDEC PUBLICATION

# Chip-Package Interaction Understanding, Identification, and Evaluation

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# CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION, AND EVALUATION

## Introduction

The present solid state component level test structures or procedures do not always ensure that problems associated with chip-package interactions (CPI) are discovered in standard device level qualifications. As component structures integrate ultra low-k (ULK) chip level dielectrics to increase performance, the interaction between the device and the package increases, though these interactions can be found in prior technologies. This document discusses identification and evaluation methods to evaluate the effect of chip package interactions on product reliability.

# CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION AND EVALUATION GUIDELINE

(From JEDEC Board Ballot JCB-18-12, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualification and Monitoring.)

## 1 Scope

This publication references a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products. CPI test structures may not be a prerequisite for device qualification dependent on the device technology; however, if the effect of CPI on a device technology placed in a specific packaging scheme is not known, there could be reliability concerns for that component that are not evident with standard component level test structures. Therefore, it is recommended that CPI test structures are used and the associated testing and failure analysis be performed to determine if there are any adverse effects on that component due to packaging. Chip sizes and packages should be used that are representative of the product family to allow investigation of failure mechanisms for those products.

NOTE This publication covers only interaction between the semiconductor package stresses and the semiconductor device. Interactions between the assembled component and a second level assembly are not covered. See JEP 150 for information regarding assembled component reliability. Interactions resulting from package interconnect electromigration are also not covered. See JEP 154 regarding Package interconnect electromigration. . See JEP158 for the effects on chip reliability due to through-silicon vias (TSVs).

NOTE CPI tests should be performed in addition to process and package qualification typically performed on new products.

These reliability stress tests have been found capable of stimulating and precipitating failures in components in an accelerated manner, but these tests should not be used indiscriminately. Each qualification should be examined for:

a) Any potential new and unique failure mechanism
b) Any situations where these tests/conditions may induce invalid or overstress failures.

In either case the set of reliability requirements, tests and/or conditions should be appropriately modified to properly include the new failure mechanisms and modes.

This document does not relieve the supplier of the responsibility to meet internal or customer specified qualification programs.

## 2 Terms and definitions

**assembled state (of a component):** The state of a component that has been attached to a second-level assembly.

**back-end-of-line (BEOL)(adj):** Pertaining to the portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

**back end of line (BEOL)(noun):** The portion of the semiconductor processing line that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

**bond and assembly processes (B&A):** The processes associated with connecting chips (dice) to other package elements and assembling semiconductor-device packages.

**chip-package interaction (CPI):** The interaction between the semiconductor package stresses and the semiconductor device.

NOTE Package stresses are cause by thermal, mechanical, or chemical mechanisms.

**chip-to-substrate-interconnect; level 1 (L1) interconnect:** The structure that connects the chip to the substrate.

NOTE 1 For the purpose of this document chip-to-substrate-interconnect will be referred to as “interconnect”.

NOTE 2 Examples of this structure include, but are not limited to, solder bumps or copper columns.

NOTE 3 Level 1 (L1) interconnect is not associated with JP 001 Foundry Level 1 Qualification (L1).

**failure mechanism:** The physical, chemical, electrical, or other process that has led to a nonconformance.

NOTE 1 See JESD671, Component Quality Problem Analysis and Corrective Action Requirements.

NOTE 2 A failure mechanism may be characterized by how a degradation process proceeds including the driving force, e.g., oxidation, diffusion, electric field, current density.

**failure mode (general):** The way in which a failure mechanism manifests itself in a failing component.

NOTE Examples of failure modes are a visual blemish, a bent lead, a foreign particle or material, an incorrect dopant profile or grain size, a scratch, an electrical fault (open, short, leakage, inadequate slew rate or noise margin, stuck at high or low, etc.).

**far-back-end-of-line (FBEOL)(adj):** Pertaining to the portion of the semiconductor processing line that creates the metal layers (including the under-bump metal UBM or redistribution layer) and associated interconnect structures forming the connection between the chip and the outside world by conductors, e.g., bond wires, bumps, balls, via.

## 2 Terms and definitions (cont'd)

**far back end of line (FBEOL)(noun):** The portion of the semiconductor processing line that creates the metal layers (including the under-bump metal UBM or redistribution layer) and associated interconnect structures forming the connection between the chip and the outside world by conductors, e.g., bond wires, bumps, balls, via.

**free-standing state (of a component):** The state of a component that is not attached to the next level of assembly packaging.

**front-end-of-line (FEOL)(adj):** Pertaining to the portion of the semiconductor processing line that creates active devices, ending with the gate oxide conductors.

**front end of line (FEOL)(noun):** The portion of the semiconductor processing line that creates active devices, ending with the gate oxide conductors.

**packaged device:** A semiconductor device within an enclosure that allows electrical connection to, and provides mechanical and environmental protection for, that device.

**second-level assembly:** The attachment of a component to the next level of assembly packaging.

**substrate (of a semiconductor device) (general):** The supporting material upon which or within which the elements of a semiconductor device are fabricated or attached.

**under-bump metal (UBM):** The metal layers located between the solder bump or column and the die.

## 3 Reference documents

JEP122, *"Failure Mechanisms and Models for Silicon Semiconductor Devices"*

JEP131, "*Process Failure Modes and Effect Analysis (FMEA)"*

JEP150, *"Stress-test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components"*

JEP154, "*Guideline for Characterizing Solder Bump Electromigration under Constant Current and Temperature Stress"*

JESD22, *"Reliability Test Methods for Packaged Devices"*

JESD47, *"Stress-Test-Driven Qualification of Integrated Circuits"*

JESD74, "*Early Life Failure Rate Calculation Procedure for Electronic Components"*

JESD85, "*Methods for Calculating Failure Rate in Units of FITs"*

JESD91, *"Method for Developing Acceleration Models for Electronic Component Failure Mechanisms"*

JESD94, *"Application Specific Qualification using Knowledge Based Test Methodology"*

JP001, *"Foundry Process Qualification Guidelines"*

JEP158, *"3d Chip Stack with Through-Silicon Vias (TSVS): Identifying, Evaluating and Understanding Reliability Interactions"*

## 4 Understanding CPI

CPI stresses arise from the processes and materials used in attaching and encapsulating a chip forming a functional module. Thermal excursions, either alone, or in combination with mismatches in material properties, such as coefficient of thermal expansion (CTE), are a major source of mechanical stress on the chip. With increasing chip size, CTE mismatch and associated stress increase, that can result in CPI concerns. Processing defects, such as dicing cracks or chip backside flaws, can serve as initiation points for CPI failure. Material defects such as particles in a thermal conduction adhesive can serve as stress concentrators to promote CPI fails. Material interactions such as alloy or intermetallic formation can cause volume changes which concentrate stress. Low-k dielectric materials in the chip are mechanically weak and tend to form weak interfaces with other materials. An improper cooling rate during chip attach to substrate can cause CPI failures. And solder bump solidification, particularly on lead-free flip chip modules, if not uniform, can also concentrate CTE stress.

Bond and assembly processes include solder bump attach, wafer dice, chip reflow, underfill and cure, thermal enhancement apply, encapsulation, module test, burn-in, module card attach, and rework of any of these processes for flip chip plastic ball grid arrays (FCPBGA) and similar module types. The critical materials are the substrate, interconnect, underfill, and thermal enhancement on the back of the chip, heat spreader, heatsink, if any, and card. Wire bond processes include wafer dice, chip attach, wire bond, mold compound dispense and cure, card attach, and reworks. The critical materials are the package, wire, mold, and card.

It is worth examining a few examples of potential CPI failures to highlight the critical contributors to the failures:

Underfill can crack during simulated or actual on/off cycles, either in stress testing or in the field. The CTE mismatch between chip and package concentrates strain at the corner of the chip during the cold portion of the thermal cycle, causing a crack which propagates out from the corner. As the crack propagates, it opens up either the chip-underfill interface, or at another weak interface, causing either interconnect fatigue, or an electrical fail in the chip dielectric.

Particles in a material used to provide a good cooling path between the top of the chip and the cap can initiate a crack that, during on/off cycles, can propagate through the chip to the active devices and chip wiring. Care is needed to ensure that the maximum particle size does not exceed the intended chip-to cap-gap.

Flip chip solder ball interconnects solidify after chip join reflow as individuals. If fast cool down causes, for example, outer balls to solidify first, the strain from CTE mismatch is concentrated at their contact pads, and can cause cracking of the dielectric, providing a crack which can propagate, and also serve as an opening for humidity and corrosive contaminants to enter the chip.

Saw dicing or laser grooving can introduce flaws in BEOL structures. These flaws can develop into cracks during reliability stressing (especially in thermal cycle stresses) and further grow and propagate to the crackstop along weak interfaces in the BEOL structures. The crackstop can then be breached by the cracks which gained energy in propagation particularly at chip corners. These cracks can then fail the chip once they reach the active chip area within crackstop. Such cracks can also set up moisture degradation mechanisms (like TDDB). Without special protection, the cracks may also dive into the silicon and fail the FEOL devices. In those cases, FEOL monitoring is also recommended.

## 4 Understanding CPI (cont'd)

These mechanisms may not show up in standard device stress testing due to the insensitivity of common test structures, even though the stress levels in the test may be much higher than those that can cause CPI fails. Mechanical stresses, which can scale with size, and defects introduced by the far back end of the wafer line and bond and assembly processes, can only be addressed through representative test structure design and processing, followed by stress testing and appropriate electrical, physical and physio-chemical characterization, see 5.

Through-silicon vias (TSVs) are used to enable 3D chip stacking. A chip containing TSVs is subject to experiencing a variety of reliability effects on BEOL and FEOL structures. For more detail on this area, refer to JEP158.

## 5 CPI failure concerns and associated hardware design considerations

### 5.1 Primary CPI reliability fail types requiring test vehicle evaluation

CPI failure mechanisms predominantly initiate due to thermal and mechanical stresses, and normally affect the chip or the chip-to-package interconnection structure, but generally not the package laminate or substrate itself. It should be noted that physio-chemical interactions can also play a role in CPI failure mechanisms. For discussion purposes, the interconnect itself (e.g., solder bump) is considered part of the chip structure. The design of the CPI test vehicle must account for worst-case attributes with respect to chip-level or interconnect structure type, dimension and physical placement, in order for the reliability testing to adequately stress the subject technology. Accordingly, the process sequence for back end of line (BEOL), wafer finishing, and bond and assembly (B&A) must include the representative conditions that production parts might experience during fabrication.

Beginning with the 90nm technology node, the chip BEOL wiring levels generally employ advanced low-k dielectrics which have inherently less mechanical strength than pure silicon dioxide. However, it should be noted that CPI concerns are not limited to those technology nodes.

With the solder bump structure and a flip-chip plastic ball grid array (FPBGA) or flip chip scale package (FCSP), which have organic laminate packaging substrates, chip to package CTE mismatch gives rise to potentially damaging stresses during thermal cycling. The introduction of Pb-free interconnect materials increases the overall rigidity of the chip-interconnect-substrate connection, which together with the correspondingly higher chip to package join temperature, results in higher stress transfer into the chip than for the case of leaded bumps. For the case of a ceramic substrate with a CTE close to that of the chip, the risk of chip damage is reduced.

A wire bond chip to package configuration with a low-k BEOL chip must also be evaluated for CPI reliability, but the risk of CPI failure due to thermal stresses is lower than it is for a solder bump package, primarily because of the inherently flexible nature of the wire bond itself and because wire bond chip die sizes tend to be relatively small in size, consistent with relatively low DNP even at chip corners. Wire bond chip CPI fails may be a function of the BEOL layer stack, particularly in cases for which there is minimal thin-layer oxide or fluorinated silica glass (FSG) coverage of the underlying low-k or ultra low-k (ULK) advanced dielectric layers.

### 5.1 Primary CPI reliability fail types requiring test vehicle evaluation (cont'd)

As an example, a typical worst case chip to package situation would generally comprise a very large die size with low-k BEOL wiring and passivation levels, that are interconnected with a Pb-free fine-pitch solder bump to a package with CTE mismatch to the die; e.g. organic laminate or ceramic high CTE substrate. Once CPI reliability testing is done for the worst-case configuration, it may be possible that the CPI testing coverage for lower risk options has been covered. This, however, needs to be reviewed for the specific case.

A CPI test vehicle must be devised to evaluate the CPI integrity for any new chip to package type built with any new process or material in the BEOL, FBEOL, wafer backside grinding and polishing, wafer dicing or B&A sectors. A set of primary CPI reliability fail mechanism types are described below, followed by test vehicle design considerations.

#### 5.1.1 Chip-side BEOL and chip edge integrity failure

Structural interruption of the BEOL wiring can occur due to thermal treatment of chip to package and appears as either interfacial delamination (adhesive failure) or physical film cracking (cohesive failure).

Examples of the specific mechanisms which may lead to failure include, but are not limited to:

1. Weakening or loss of dielectric film adhesion
2. Reduction of dielectric mechanical strength
3. Dielectric breakage beneath the interconnection (e.g., solder bump structure)
4. Crack propagation from dicing imperfections (Chip edge seal & crack stop integrity)
5. High DNP location cracking
6. Stress migration
7. Bump non-wet in flip chip
8. Metal peel-off in wire bond applications
9. Wire bond displacement
10. Passivation cracks

Annex A lists the failure mechanisms and some reasons for their occurrence.

#### 5.1.2 Chip to package interconnection integrity failure

Failure of the UBM to the interconnect structure itself can be seen in a packaged device.

Examples of these specific mechanisms include, but are not limited to:

1. Interconnect fatigue during thermal cycling
2. Interconnect process defects, e.g., excessive UBM undercut
3. Process residues from plating or UBM fabrication
4. Interconnect nonplanarity resulting in marginal contact, especially at high DNP locations
5. Too fast a cooling rate during chip attach to the substrate can cause bump cracking or UBM peeling.

### 5.2 Test vehicle design considerations

If feasible, use of a test vehicle is suggested since actual product may not have the electrical test sensitivity to adequately isolate or detect CPI concerns or failures. Validation of results on actual product is also recommended. Failure analysis of a test vehicle can be easier, if properly designed.

#### 5.2.1 CPI chip, substrate and interconnect

The CPI test chip and substrate should be carefully designed so as to provide adequate representation of worst-case structural and process integration attributes relating to BEOL chip side wiring, chip-to-package interconnect structure and laminate configuration. These structures should be included in the final reliability stress activity.

##### 5.2.1.1 CPI die

The chip size should be maximized for reliability coverage that is representative of a product family, preferably to the worst case design. It is acceptable for the CPI test chip to be comprised primarily of BEOL levels. Inclusion of ESD protection structures is suggested for ease of parts handling and elimination of non-CPI test failure modes. If ESD structures are not included, care must be taken in handling, stressing and testing operations. ESD protection structures provide the ultimate protection of the finished module from electrostatic charges that can create electrical fails independently of a CPI reliability mechanism. The BEOL film stack does not need to include every possible discrete build level available in a subject technology, but should be designed such that every possible BEOL interface is represented, and so as to capture a worst-case configuration of advanced low-k dielectric layers. Establishing the worst case configuration can be a difficult task because it depends on more than one variable. The specific materials and processes used to create the wafer level wiring structure (BEOL processes) and the individual finished die (wafer finishing processes) all should be included in the simulation build. This includes, but is not limited to, special features such as crack stop or seal ring (if they are present in the product or the technology being tested). The dicing channel width of the CPI test chip on the wafer does not need to be exactly the same as the product chip; however, the distance from the diced edge to the crackstop should be the same as the product. Fill areas of the dicing channel and active chip area should mimic that used in the product chip.

##### 5.2.1.2 CPI substrate

The packaged device substrate is matched to the test vehicle chip size and representative of the product or technology being tested. The CPI substrate should be designed with a stress profile that is consistent with worst-case for the technology requiring reliability coverage. Particular consideration should be afforded to laminate core thickness, number of wiring levels, laminate materials, die-to-substrate interconnections, copper loading, and overall laminate size.

### 5.2.1 CPI chip, substrate and interconnect (cont'd)

#### 5.2.1.3 Die to substrate interconnect

The interconnection structure for the CPI Reliability exercise should be an interconnect type chosen as representative of the qualifying technology, and a worst-case with respect to transfer of stresses between the chip and the packaging substrate. This applies particularly to the solder alloy material, solder bump pitch, solder bump process, and underfill material. The solder bump layout should be uniform and should include inactive solder bumps if necessary in order to create a product representative array configuration. Other types of interconnects include, but are not limited to, die attach and down bonds. Use of modeling analysis may also be used to gain a better understanding of product interconnect configurations. The specific materials and processes used to create the UBM, the interconnect bump structure, and other relevant parts of the device should all be included in the simulation build.

#### 5.2.1.4 Thermal solution

The thermal solution for the test vehicle should be matched to the test vehicle chip size and representative of the product or technology being tested. The package thermal solution should be consistent with the worst-case for the technology requiring reliability coverage. Particular consideration should be afforded to the lid material, lid configuration/dimensions, and the lid to substrate attach material.

### 5.3 CPI chip-level test structures

Individual CPI test structures should be placed at multiple locations across the chip, with particular emphasis at high DNP locations, especially in the corner or close to the crack stop or seal ring, so that worst case stress effects are adequately covered by the reliability stress. Table 1 gives a listing of potential failure modes and some examples of basic CPI structure types and stress tests that can be used to discover the specific failure modes in the application. Other structures are possible based on experience and product design. The number of test structures used on a test die may be limited based on test capability and substrate wiring limitations.

### 5.3.1 Examples of CPI test structure type

#### 5.3.1.1 Corner sensor (within die)

Relatively short length continuity or chain structure that includes BEOL via to metal connections at all levels in the BEOL build stack, are wired out through level 1 interconnect (bumps, wire bonds, copper pillars, etc.) at either end. Structures are generally built to minimum line and space (pitch) rules for each metal layer.

#### 5.3.1.2 Perimeter lines (within die)

Single line or parallel line pair are placed as close to chip perimeter as possible, extending around the entire periphery of the chip at each metal layer. They are wired out through a single interconnect at each end (or an interconnect pair if a double line is used). The double line allows for detection of shorts, as well as, opens. If possible, it is recommended that there be one perimeter line structure at each BEOL metal layer. If using perimeter line(s), it is recommended that there be intermediate test points to help isolate failure locations.

### 5.3.1 Examples of CPI test structure type (cont'd)

#### 5.3.1.3 Perimeter stitch (within die)

BEOL via stacks are placed along the chip perimeter and neighboring traditional perimeter lines. The via stacks are serially connected to each other by short metal lines at the bottom and top BEOL metal layers associated with the via stacks. The perimeter stitch is sensitive to detect corner and peripheral BEOL delamination and via breakage. It is recommended to cover all BEOL metal and via levels in the perimeter stitch design. Intermediate or tap test points are also recommended for failure location isolation.

#### 5.3.1.4 Under-bump sensor (within die)

BEOL via stacks are placed underneath an array of bumps. There is at least one via stack under each bump. All these via stacks are serially connected to each other for resistance measurement. The under-bump sensor allows for detection of under bump crack. The bumps close to die corners and edges typically have higher stress to the BEOL structures underneath them; therefore these locations are of most interest for the under-bump sensor design.

#### 5.3.1.5 Interconnect stitch chains (die to substrate)

Daisy-chain vertically wired repeating interconnect to via structures are connected by wire lengths at one or more of the BEOL wiring layers. Several individually wired test chain structures should be placed on the chip at multiple distance to neutral point (DNP) locations, including chip center and along chip edges.

#### 5.3.1.6 BEOL serpentines (within die)

Within BEOL level metal wiring with interleaved comb and serpentine structures, built at minimum ground rule pitch may be included. Several individually wired structures may be placed on chip in multiple locations. It allows for resistance measurements on serpentines and leakage measurements between serpentines and combs.

A design with serpentines at each metal level can enable interlevel leakage measurements between serpentines. Consider alternating the orientation of serpentines on consecutive levels to enhance risk area for interlevel leakage.

#### 5.3.1.7 BEOL via chains (within die)

Vertically wired, repeating via chain lengths, wired between two or more BEOL wiring levels that use tight line and space pitch, consistent with product being tested, should also be included. Several individually wired structures may be placed on the chip at multiple DNP locations, including chip center and along chip edges.

The primary design objective is to detect BEOL cracking with CPI test structures arranged so that the test chip appears similar to a typical product chip with respect to critical layout parameters and interconnect density. It is recommended that 4-point probe structures be used wherever possible in the design.

# 6 CPI test requirements

## 6.1 CPI test regimen

Table 1 shows a number of CPI structure types, the failure modes they are designed to detect, the reliability stress that should be used and the recommended method of detection. Other structures are possible based on the particular technology test needs

**Table 1 — General CPI Structure Types and Associated Failure Mode**

| CPI Structure Type | CPI Failure Mode | Reliability Stress | Detection Method |
|---|---|---|---|
| 1. Corner Sensor | Interconnect Resistance Increase/ Open<br>Chip Corner Crack<br>Corner Delamination<br>Dicing Related Defects | Thermal Cycle | Electrical Test (opens)<br>Acoustic microscopy<br>Optical inspection |
| 2. Perimeter Lines | Dicing Related Defects<br>Edge/Corner<br>Shifted perimeter line | Thermal Cycle<br>THB<br>uHAST<br>HTS | Electrical Test (opens)<br>Acoustic microscopy<br>Optical inspection |
| 3. Perimeter Stitch | Chip Corner/Edge Crack<br>Corner/Edge Delamination<br>Dicing Related Defects | Thermal Cycle<br>THB<br>uHAST<br>HTS | Electrical Test (opens)<br>Acoustic microscopy<br>Optical inspection |
| 4. Underbump Sensor | Under Bump Crack | Thermal Cycle | Electrical Test (opens)<br>Acoustic microscopy<br>Optical inspection |
| 5. Interconnect Stitch Chains | BEOL Cracking Sub-interconnect<br>Interconnect Resistance Increase/ Open<br>Interconnect/ Final Via Defects<br>BLM Undercut<br>Chip Corner Crack<br>Marginal interconnect to the substrate | Thermal Cycle<br>HTS | Electrical Test (opens)<br>Acoustic microscopy |
| 6. BEOL Serpentines | Corrosion / Extrusions | THB/HAST<br>HTS | Electrical Test<br>(shorts & opens) |
| 7. BEOL Via Chains | BEOL Crack<br>BEOL Delamination<br>BEOL Chain Short | Thermal Cycle | Electrical Test<br>(opens & shorts)<br>Acoustic microscopy |
| NOTE If it is known that the failure mode of interest does not result from visco-plastic or visco-elastic behavior, then the use of thermal shock instead of thermal cycling, for test time reduction, may be considered. | | | |

### 6.2 Test samples

For these test samples, preconditioning of the component should be performed per JESD22-A113. The reflows should reflect the solder regimen being used in the actual application, as well as the packages with maximum dimensions for that application.

#### 6.2.1 Lot requirements

To assess manufacturing variability and its impact on reliability, the component test samples should be comprised of several wafer, bumping, substrate, and assembly lots to evaluate variability from the component qualification family. Refer to the specific qualification test method, such as JESD47, for the recommended number of lots for that stress test. Other appropriate means may be used with justification.

#### 6.2.2 Test hardware

It is recommended that the test hardware include the recommended structures discussed in Clause 5. If this is not possible, employment of functional components may be acceptable and can provide insight into actual product performance. However, if improperly selected, the functional device parameters could mask test failures by lack of test sensitivity. Thus the use of a test vehicle is the preferred method to detect CPI reliability concerns. In general, the devices used for reliability investigations should be chosen according to the following criteria: 1- relevancy for the intended use, 2- ease of analysis and 3- dominant failure mechanism to be investigated under the planned stress condition.

## 7 Stress test

### 7.1 Procedure

Once the test hardware is assembled and prepared for testing, appropriate test procedures should be followed for the stress test being performed. Test performance can be tracked by both discrete interval measurements or by in-situ continuous monitoring. The measurement regimen should be determined based on product requirements and tester availability. Appropriate tester setups should be followed, with care taken to guarantee that the test interval, tester accuracy and tester setup meet appropriate industry standards. If in-situ continuous monitoring is not used, a test method capable of resolving a low resistance change in each test pattern is necessary, such as the four-point probe methodology. With in-situ interval testing, the resistance change criteria used can be critical in the timely discovery of test fails.

Failure criteria, test regimen and test duration need to be set to the specific failure mode and application requirements. For leakage testing, fail criteria can be leakage current above 1 µA. For resistance testing, failure criteria can be either an absolute value, based on actual product resistance sensitivity, or a representative change in measured electrical resistance representing a test failure in each test pattern, often set at an increase of 20%. In either case, the electrical test should record the value of the resistance shift. If the test method selected is not capable of resolving this level of resistance shift then there is the likelihood that test failures will not be detected in a timely manner, thus affecting any failure models or statistics being formulated. If a bench top discrete measurement technique is used, the test interval readout schedule should be determined based on the failure mechanisms of interest. Readouts can be made more often in the early portion of the reliability test sequence if capturing early test fails or test setup problems is a concern.

## 8 Failure analysis

Failure analysis is used to verify the location and mechanism of the failure. See Annex A for a list of failure mechanisms and contributing factors. The most important aspect of failure analysis is the verification of the failure location. Also it must be determined that it would be the type of failure that is relevant to application conditions and situations. As such it is important to isolate the failure and assure that it is associated with the component and not the test setup, including the tester, cabling or the PWB on which the component of interest may have been assembled. Care must be taken during failure analysis not to disturb the failure. In particular, if the component needs to be removed from a printed wiring board (PWB), extreme care must be taken. Non-destructive failure analysis tools can also be used. They include acoustic microscopy (AM), x-ray, time domain reflectometry (TDR), and side view optical microscopy, infrared (IR) microscopy. Common methods used in destructive failure analysis include, but are not limited to, cross section, dye penetrant, focused ion beam (FIB), scanning electron microscopy (SEM) and energy dispersive x-ray (EDX).

## 9 FEOL Effects

Mechanical stress as a result of packaging and wafer finishing (including thinning) can affect carrier mobility and the functioning of transistors. Those effects can potentially change the functionality of a chip while under load and should be considered in design verification of the product. For planar (i.e., 2D / non-3D) chips, such mechanical stresses are not reported to influence FEOL aging phenomena such as bias temperature instability or hot carrier injection.

Where gettering is insufficient, metal contaminants (particularly Cu) can diffuse through the backside of a chip and affect device characteristics or collect causing leakage paths. The risk is foremost when the wafer or chip is thinned, contaminants exist in the downstream processes, and gettering properties of the backside are not optimized. This risk can be avoided in the presence of adequate barriers to diffusion.

Refer to JEP158 for FEOL effects associated with 3D chip stacking using Through-Silicon Vias (TSVs).

## 10 Documentation

In general, details of the evaluated product, test set-up, and results should be reported. The request for this information should be specified in the applicable procurement documentation. Because the materials and geometries of the device and package can affect the chip to package interaction, Annex B is an example of suggested information that might be provided in a report or available on request.

## Annex A (informative) Examples of failure mechanisms and contributing factors

| FAILURE MECHANISMS | CONTRIBUTING FACTORS |
|---|---|
| Weakening or loss of dielectric film adhesion | Properties of the dielectric passivation film, especially with low-k dielectric film |
| Reduction of dielectric mechanical strength | Properties of the dielectric passivation film, especially with low-k dielectric film |
| Dielectric breakage beneath the interconnection | Especially with solder bump structures, occurring during cycled thermal excursions such as flip chip join or thermal cycle testing |
| Dicing process crack propagation | Seen in the chip edge seal and crack stop area where cracks form and are propagated from the wafer dicing operation |
| High DNP location cracking | Due to thermal stresses, especially at chip corners with large die |
| Stress migration | Residual or environmental stresses cause a diffusion of vacancies within metal structures to a common point, possibly resulting in an electrical open. This may be seen in temperature cycle or HTS. |
| Bump non-wet in flip chip | Oxidation or contamination on the package or solder bump, poor fluxing, substrate warpage, or bump planarity. |
| Metal peel-off in wire bond applications | Wire composition, under-pad wiring density, and hard dielectric thickness can reduce the process window width |
| Wire bond displacement | High DNP thermal stress effect |
| Passivation cracks | Non-uniform cooling, causing CTE strain to be concentrated |

## Annex B (informative) Example of Report Information

**Materials and geometries:**

Device:
Silicon metallization: materials, thickness, and dimensions of all metal layers
Overall device thickness
For each UBM layer: material, thickness, and deposition technique
UBM size
Passivation or repassivation opening size (where UBM contacts silicon metallization)
Passivation/repassivation materials and thickness
Bump composition
Bump deposition method
Bump height, both non-reflowed and after attaching to substrate
Bump pitch
Backside surface finish (mirror, matte, roughness)

Substrate:
For each layer of substrate metallization: material, thickness, and deposition technique
Substrate pre-solder composition, thickness, and deposition method, if applicable
Substrate solder resist opening (if applicable)
Solder mask
Substrate metal pad size
Substrate material
Substrate internal metallization composition
Substrate thickness
Substrate flatness

Package:
Underfill material (if applicable)
Die attach adhesive (if applicable)
Overmold / Glob Top

Lid / Heatsink (if applicable):
Mass/ weight
Material
Size (x, y, z)
Thermal interface material
Attach methodology

**Annex B (informative) Example of Report Information (cont'd)**

**First Level Assembly Processing:**

Fluxes
Solders
Cleaning fluids
Reflow profile for die and BGA attach to substrate
Cure profiles

**Second Level Assembly Details, if applicable**

Profile
Solder
Flux
Cleaning
PWB details, such as, thickness, layers and copper content

**Testing:**

Diagram of how package is daisy chained under test
Method of measuring device / package temperature
Test parameters (current, voltage, limits, etc,)
Test structures under test

**Failure criterion**

**Test chamber / procedure:**

Temperature variation across chamber
Temperature profile
Chamber start up procedure
Initial device resistance at the stress condition (average and spread)
Device current
Chamber temperature / humidity
Chamber loading
Temperature rise of device due to Joule heating
Device temperature
Preconditioning details
Sample size

## Annex C (informative) Differences between JEP156A and its predecessors

This table briefly describes most of the changes made in this publication, JEP156A, compared to its predecessor JEP156 (March 2009).

| Clause | Description of Change |
|---|---|
| 1, 3, 4 | Add reference to JEP158 for TSV-related considerations |
| 4 | Add paragraph on saw dicing and laser grooving risks |
| 5.2.1.1 | Add consideration of dicing channel width at end of clause |
| 5.3.1.3, Table 1 | Add clause on perimeter stitch (within die) |
| 5.3.1.4, Table 1 | Add clause on under bump sensor |
| 5.3.1.6 | Add considerations for serpentine design and testing |
| 7.1 | Introduce a suggested leakage criterion |
| 8 | Recognize IR microscopy and FIB as techniques |
| 9 | Add clause on FEOL considerations |
| various | Editorial grooming |

## Standard Improvement Form

**JEDEC** _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

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