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Procedure for the Evaluation of Low-k/Metal Inter/Intra-Level Dielectric Integrity

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PROCEDURE FOR THE EVALUATION OF LOW-*K*/METAL INTER/INTRA-LEVEL DIELECTRIC INTEGRITY

Contents

Foreword

This document is intended for use in the semiconductor IC manufacturing industry and provides reliability characterization techniques for low-*k* inter/intra level dielectrics (ILD) for the evaluation and control of ILD processes. It describes procedures developed for estimating the general integrity of back-end-of-line (BEOL) ILD. Two basic test procedures are described, the Voltage-Ramp Dielectric Breakdown (VRDB) test, and the Constant Voltage Time-Dependent Dielectric Breakdown stress (CVS). Each test is designed for different reliability and process evaluation purposes. This document also describes robust techniques to detect breakdown and TDDB data analysis.

Introduction

Two test procedures are described within this document: a fast VRDB test, and a constant voltage TDDB test (CVS). Each of these procedures is designed for different evaluation purposes and can be implemented separately or complementally.

The VRDB test starts at zero voltage or V_{use} and ramps linearly until dielectric breakdown occurs and can be conducted at either room temperature or at higher temperatures to accelerate the occurrence of the degradation mechanism to failure. VRDB tests are important to characterize the defects at lower electrics fields and the dielectric breakdown strength of dielectric for a given process. The CVS test starts at a fixed voltage and is kept at this fixed voltage until dielectric breakdown occurs. The test can also be performed at higher temperatures to accelerate failure. TDDB tests are important to characterize the long-term dielectric acceleration parameters and to calculate the ILD based fraction of the failure rate or lifetime of a product.

PROCEDURE FOR THE EVALUATION OF LOW-*K*/METAL INTER/INTRA-LEVEL DIELECTRIC INTEGRITY

(From JEDEC Board Ballot JCB-15-23, formulated under the cognizance of JC-14.2 Subcommittee on Wafer Level Reliability.)

1 Scope

The continued scaling of advanced VLSI circuits, particularly of high performance logic circuits, is driving the need for low-*k* materials and copper metallization in back end of the line (BEOL) interconnect systems to reduce the resistance-capacitance (RC) delay, cross talk noise, and power dissipation. With the wide applications of low-*k* and ultra-low-*k* dielectric materials at the 90nm technology node and beyond, the long-term reliability of such materials is rapidly becoming one of the most critical challenges for technology qualification. Low-*k* time dependent dielectric breakdown (TDDB) is commonly considered as an important reliability issue because low-*k* materials generally have weaker intrinsic breakdown strength than traditional SiO_2 dielectrics. This problem is further exacerbated by the aggressive shrinking of the interconnect pitch size due to continuous technology scaling.

The procedures outlined herein were developed to estimate the electrical breakdown performance of low-*k* ILD and as a tool for driving constant improvement in the low-*k* ILD process. The test procedure described within this document should be used as common methodology for low-*k* ILD process control and improvement and could be used as a guideline to predict the effect of ILD TDDB on product lifetime or failure rate. In actual practice the ILD TDDB reliability of a semiconductor product is a complicated function of the interconnect critical area, power duty cycles, transient voltage variation, and series resistance. These parameters are not considered within this document.

The purpose of this document is to describe test procedures for characterizing the reliability of inter/intra level dielectrics. It does not specify acceptance or rejection criteria for any of the described procedures.

2 Terms and definitions

The following abbreviations and symbols are used in this document. They have been listed alphabetically for the convenience of the reader.

2.1 Abbreviations

BEOL: Back end of line

CVS: Constant voltage stress

DUT: Device under test

ILD: Intralevel and/or interlevel dielectric

MLE: Maximum likelihood estimation

TDDB: Time dependent dielectric breakdown

VRDB: Voltage ramp dielectric breakdown

2.2 Symbols

A_{ILD} (cm^2): Total active area of dielectric.

E_{ILD} (V/cm): The ILD electric field. The general formula for E is:

$$E_{ILD} = V_{ILD} / S_{ILD}, \qquad (1)$$

where V_{ILD} is the ILD voltage and S_{ILD} is the physical ILD spacing between two metal lines. S_{ILD} must be determined by a consistent, documented method. The method of determining S_{ILD} or a reference to the documented standard must be included in the data report.

E_{bd} (V/cm): The estimated ILD electric field just before ILD breakdown.

I_{bd} (A): ILD current measured just before ILD breakdown.

Icomp (A): The maximum current of the voltage forcing equipment. Often the user can specify a compliance limit for a particular test.

I_{init} (A): ILD failure current when V_{use} is applied. This value is determined as a deviation from typical current vs. voltage characteristics measured from good devices. For maximum sensitivity the value should be well above the worst case ILD leakage current of a "good" ILD and at least 10 times greater than the noise floor of the test systems. A recommended value is 50 times the measured value for a good structure. Or a pre-defined absolute leakage level such as 100nA, which could critically affect chip performance and cause chip operation failure, could be used as failure criterion.

I_{meas} (A): The measured ILD current.

2.2 Symbols (cont'd)

I_{use} (A): The typical measured current through the ILD at the normal use voltage.

I_{stress} (A): The ILD current measured during the CVS test.

$I_{previous}$ (A): The previously measured ILD current.

$I_{stress-t0}$ (A): The initial dielectric current measured at V_{stress} during the CVS test.

t_{bd} (s): The recorded time at ILD failure.

t_{int} (s): The time interval to sense ILD current during the CVS test. This value should be <1% of the anticipated t_{bd} and should be decided for each stress condition

t_{meas} (s): The time interval for measuring the stress current (I_{stress}) during the constant voltage test.

t_{record} (s): The time interval for recording current measurements (I_{meas}) during the constant voltage test.

t_{step} (s): The voltage ramp step time is determined from the ramp-rate and V_{step}. The step time should be less than or equal to 100 ms.

S_{ILD} (nm): Physical space of remaining ILD between metal interconnects.

V_{bd63} (V): The scale parameter of the V_{bd} Weibull distribution

V_{post} (V): The voltage measured when I_{init} is forced into an ILD that been detected as broken down but does not exhibit excessive leakage current during the post-VRDB or CVS test. This situation results when the interconnect metal electrode is evaporated off during the high temperature transient during breakdown.

V_{stress} (V): The ILD stress voltage.

V_{use} (V): The test voltage that is applied during pre- and post-test to determine device validity. This voltage is usually the power supply voltage or use voltage of the technology.

3 Test structure overview

Test structures for the VRDB and TDDB are usually the same and can be categorized in two groups: intra-level test structures and inter-level test structures. For intra-level assessment, both trench only structures such as comb-comb or comb-serpentine structures (Figure 1), AND via structures such as intertwined via-chain and via-comb structures (Figure 2) could be used. Comb length less than 100 μm is recommended to minimize voltage drop. Via structures are required to have via counts that are representative of the products. A minimum via count of 0.01% of the actual via count on the largest product die size is recommended for Via structures. In case, a product/die size is unknown, it is recommended to use a reference product die size from a previous process technology. For inter-level assessment, orthogonal comb-comb (serp) to comb-comb (serp) or plate-to-plate structures could be used. Identical structures with at least 12 clone copies per die with a fixed area are strongly recommended for in-die Weibull slope determination and cross-wafer data deconvolution. Identical structures with at least three different areas are strongly recommended for area scaling. A larger area structure (0.1 mm^2 to 1 mm^2) should be used for a reliable estimation of chip defect density of both inter- and intra-level dielectric leakage and shorts.

VRDB test can be used to discern extrinsic defects versus intrinsic breakdowns by fitting the breakdown voltages in a Weibull or a Normal distribution bi-modally or multi-modally. The details of defect density estimate are taught by a method described in JESD35. However, in order to minimize extrinsic defects and determine the intrinsic breakdown behavior, relatively small area test structures are preferred. On the other hand, device lifetime under constant voltage stress is a strong function of device area and small area structures will have a much longer time-to-failure than larger devices under the same stress conditions. To accelerate failure and to decrease testing time higher stress electric fields could be used. However, high stress fields could be a testing problem due to hardware limitation and could also impose modeling uncertainties due to highly accelerated conditions. Therefore, in practical terms, effective structure areas in the range of 0.001mm^2 to 0.1mm^2 are suitable for TDDB testing of ILD. All test structures should be designed so that parasitic series resistance effects are minimized. High series resistance can severely impact the accuracy of both VRDB and TDDB measurements. The structure must maintain a uniform electric field over the whole tested ILD area. Multiple tabs for long serpentine structures and wide metal power feeding buses are strongly recommended to minimize potential parasitic voltage drops, which lead to reduced stress/ramp voltages and currents, longer TDDB lifetime than expected, wider spread in data, and ultimately a falsely projection. A second requirement of the capacitor test structures is that they should have edge seals to prevent potential cracking induced oxygen and moisture ingression, especially for testing ultra low-*k* dielectrics at the package level.

3 Test structure overview (cont'd)

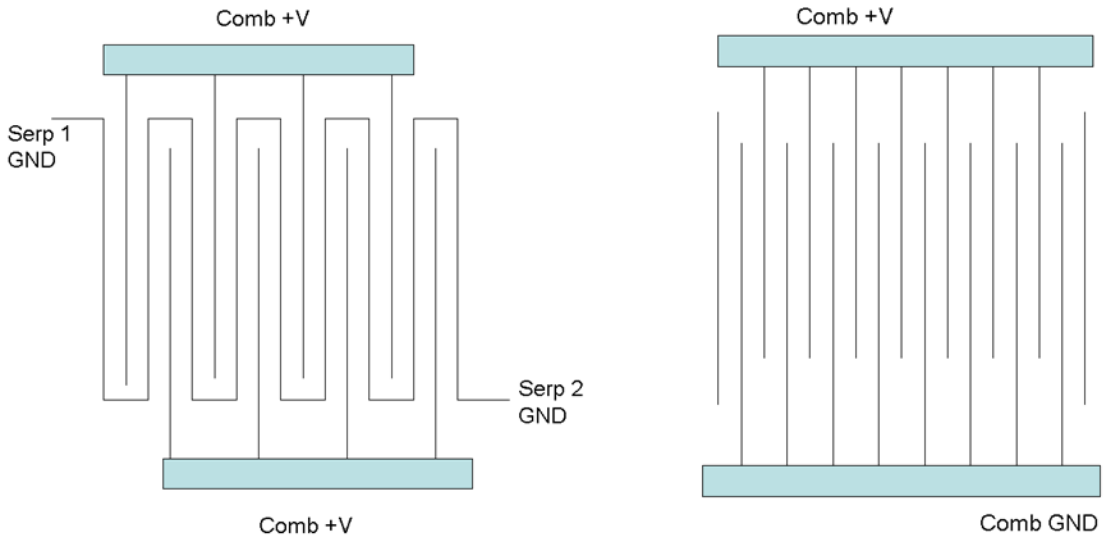

Figure 1 — a) Comb-serpentine test structures, and b) Comb-comb

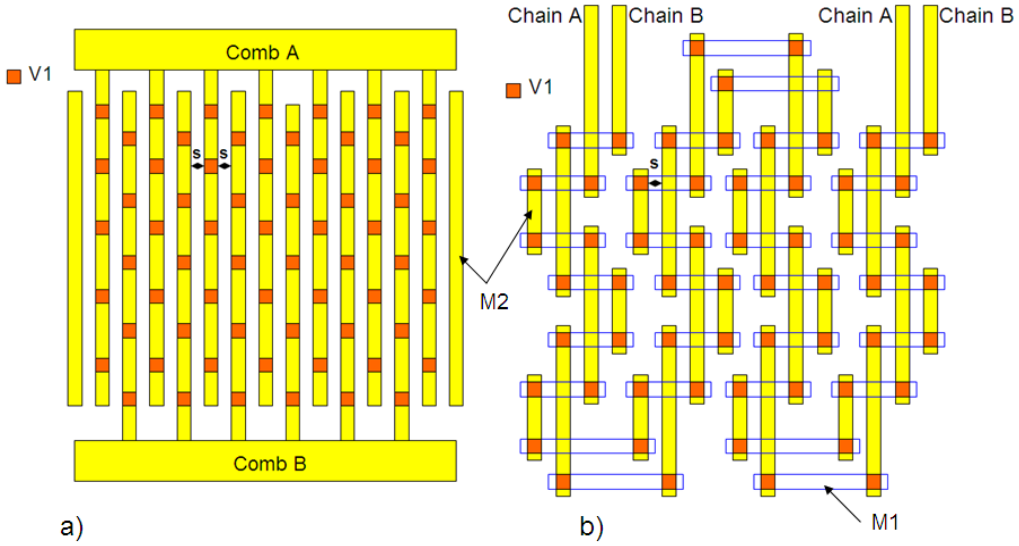

Figure 2 — a) Via-comb and intertwined, b) Via-chain test structures

One recommendation of the capacitor test structures design is to include dummy edge lines to minimize the lithographic variations at the edges of the structures. In order to have sufficient statistics at least 100 or more devices per test are recommended for the VRDB test and the TDDB test.

4 VRDB test overview

The following sections describe the details of the VRDB test. This measurement is performed in three parts. First, a pre-VRDB test is conducted to determine if the test structures are not damaged or initially shorted. Second, a voltage ramp is performed until dielectric breakdown. Third, a post-VRDB test is performed to confirm the final state of the dielectric structure.

4.1 Pre-VRDB test

The purpose of the pre-VRDB screen test is to identify initially failed devices and to estimate the initial short yield of the wafer. The test is performed by applying V_{use} and measuring I_{use}. If I_{use} is greater than I_{init} then the sample will be recorded as an initial failure and not used in subsequent tests. I_{init} is determined as a deviation from typical current vs voltage characteristics measured from good devices. A recommended value is 50 times the anticipated value for a good structure. Or a predefined absolute leakage level such as 100 nA, which could critically affect chip performance and cause chip operation failure, could be used as failure criterion. The test temperature usually is set at the worst case product use temperature (i.e., 125 °C) to avoid using temperature extrapolation due to potential intercorrelation of dielectric breakdown voltage and temperature.

1) Set and record stress temperature
2) Apply V_{use}.
3) Measure I_{meas}
4) If $I_{meas} > I_{init}$, record as initial failure
5) Repeat for all available DUTs on wafer

4.2 VRDB test

A linear or stepped voltage ramp is applied to the dielectric test structure. The voltage starts at zero voltage or the use voltage V_{use}, and ramps at a predefined ramp rate, or is stepped by the voltage, V_{step}, for a duration t_{step}. During the voltage ramp, the current is monitored as least as often as t_{step}. For the stepped voltage ramp, the current measurement should be delayed at each voltage step to allow displacement currents to settle. This indicates that t_{step} must be longer than the instrument's settling time plus the measurement time of the test system.

4.2 VRDB test (cont'd)

Table 1 — Recommended values for the VRDB and CVS tests

Parameter	Units	Comments
K_{slope}		Slope increase factor when comparing subsequent slopes during the VRDB tests. K_{slope} can vary between 3 and 10. See 4.2.1.2
I_{init}	A	ILD breakdown failure current when V_{use} is applied. This value is determined as a deviation from typical current vs. voltage characteristics measured from good devices. For maximum sensitivity the value should be well above the worst case ILD leakage current of a "good" ILD and at least 10 times greater than the noise floor of the test systems. A recommended value is 50 times the anticipated value for a good structure. Or a pre-defined absolute leakage level such as 100 nA, which could critically affect chip performance and cause chip operation failure, could be used as failure criterion.
I_{use}	A	ILD current measured when V_{use} is applied during the pre-ramp test. This current density should be at least 10 times greater than the noise floor of the test system.
Ramp rate	MV/cm·s	The ramp rate is specified at 1 MV/cm·s
t_{int}	s	Interval time to sense ILD current during the CVS test. This value should be <1% of the anticipated t_{bd} and should be decided for each stress condition
t_{step}	s	The voltage ramp step time is determined from the ramp-rate and V_{step}. The step time should be less than or equal to 100 ms.
V_{max}	V	The maximum voltage limit can be determined by the maximum stress electric field of 15 MV/cm. For example, this results in 150 volts for a 100 nm thick dielectric layer.

At each voltage step, the measured dielectric leakage, I_{meas}, should be compared to the dielectric breakdown criterion discussed below in 4.2.1. If dielectric breakdown has been detected, the voltage ramp should be stopped and the final post-ramp leakage test should be carried out.

Other test conditions besides a dielectric breakdown may stop the voltage ramp test. These include reaching the specified maximum test voltage, V_{max} or reaching the specified current compliance of test system.

4.2.1 Dielectric breakdown criteria

Dielectric breakdown criteria can be defined in several ways. Due to the unique nature of ILD Cu/low-k dielectric system, it is essential that the dielectric failure criteria should be carefully specified. Described below are the dielectric failure criteria. Both criteria should be tested during the ramp. Dielectric breakdown is defined when one of the following criterion is met.

4.2.1 Dielectric breakdown criteria (cont'd)

4.2.1.1 Absolute current level

This criteria specifies that breakdown occurs when the magnitude of the dielectric current exceeds ten times I_{use}, ($I_{meas} > 10 \text{ X } I_{use}$). This level must be carefully selected by measuring IV curves from representative samples as huge variations of ILD leakage and breakdown voltage are expected for test structures with different design geometries, at different metal levels, and with different process splits. Therefore, the criteria should be carefully selected to assure a real catastrophic ILD breakdown detection. This method is not suitable for ILD breakdown exhibiting an "open" signature instead of a "short" due to metal damage caused by extremely high transient discharge current during the breakdown event.

4.2.1.2 Slope change of dielectric current versus voltage – An abrupt current increase

This criteria specifies that dielectric breakdown occurs when the logarithmic slope of I_{meas} vs. V_{stress} curve continuously increases by a slope increase factor (K_{slope}) greater than the previously calculated slope with at least four points and three slope comparisons.

The previous logarithmic slope (Slope1) is calculated from

$$Slope1 = \frac{Abs\left(Ln\left(Abs\left(I_{n-1}\right)\right) - Ln\left(Abs\left(I_{n-2}\right)\right)\right)}{V_{n-1} - V_{n-2}}$$

where $I_{n-1,}$ $V_{n-1,}$ $I_{n-2,}$ and V_{n-2} are the measured currents and voltages of the previous two data points, respectively. The new slope (Slope2) is calculated using

$$Slope2 = \frac{Abs\left(Ln\left(Abs\left(I_{n}\right)\right) - Ln\left(Abs\left(I_{n-1}\right)\right)\right)}{V_{n} - V_{n-1}}$$

where $I_{n,}$ $V_{n,}$ $I_{n-1,}$ and V_{n-1} are the measured currents and voltages of the second most recent and previous data points, respectively.

The third slope (Slope3) is further calculated to verify true slope increase

$$Slope3 = \frac{Abs\left(Ln\left(Abs\left(I_{n+1}\right)\right) - Ln\left(Abs\left(I_{n}\right)\right)\right)}{V_{n+1} - V_{n}}$$

where $I_{n,}$ $V_{n,}$ $I_{n-1,}$ and V_{n-1} are the measured currents and voltages of the most recent and previous data points, respectively. If slope3 > K_{slope} X (slope2) > K_{slope} X (slope1) then the test should be terminated and the device is considered to be broken down.

K_{slope} can have a value between 3 and 10 and can be varied for actual hard breakdown events depending on device area, ILD thickness, structure layout, or process. Voltage-to-breakdown, V_{bd} is defined as V_n. This method is suitable for detecting both "short" and "open" breakdowns.

4.3 Post-VRDB dielectric current test

Once the voltage ramp is completed, following the detection of breakdown defined in 4.2.1, a post-ramp current test with V_{use} applied to the metal interconnect is used to determine the final state of the tested device. Hard breakdown is attributed to all the devices with post-VRDB $I_{use\text{-}post} > I_{init}$ and is classified as a valid failure. If $I_{use\text{-}post} < I_{init}$ then force I_{init} and measure V_{post}. If $V_{post} >= .9\ V_{max}$ then the device has broken down, but is open circuited and is classified is a valid failure.

During the breakdown event, extremely high transient currents flow. Such large discharge current comes from the charge stored in the test structure. The greater the local dielectric voltage, the greater the energy released into the breakdown electrodes. Peak discharge currents may occur during the ILD rupture event caused by voltage ramping. This high peak current could destroy metal to form open circuits or burn-out contacts. Therefore, a false "open" event instead of "short" could be detected by the instrument. As those "opens" are indeed induced by first electrical "shorts", and the time interval between "short" and "open" is very short, the voltage at the onset of "open" could be treated as the breakdown voltage.

An invalid breakdown would indicate a potential problem with the test fixture setup or with the instrumentation.

4.4 Data recording

For VRDB test, the following information should be recorded and analyzed,

- V_{bd} – the dielectric voltage to breakdown
- I_{bd} – the dielectric breakdown current
- I_{use} – the measured dielectric leakage at V_{use} prior to the application of the ramp.
- $I_{use\text{-}post}$ – the post breakdown measured dielectric leakage at V_{use}

4.5 VRDB data analysis

The VRDB results can be fitted with a Weibull (the most popular distribution for dielectric breakdown data) or a Normal distribution. The following parameters should be determined:

- V_{bd63} or V_{mean} – the scale parameter of the V_{bd} Weibull distribution or mean voltage of the V_{bd} Normal distribution
- Beta of V_{bd} or sigma of V_{bd} – the shape factor of the V_{bd} Weibull or sigma of the V_{bd} Normal distribution
- Distribution of I_{use} and $I_{use\text{-}post}$

A complete discussion of data analysis including estimating defect density can be found in JEDEC standard JESD35.

4.5 VRDB data analysis (cont'd)

Note that low-*k* dielectric breakdown depends on voltage ramp rate and test structure size. It is not meaningful to compare dielectric breakdown voltage and leakage with different test conditions on different test structures. It has been reported by various research groups that Cu/ILD TDDB failure could be mainly dominated by Cu out-diffusion under high bias and temperature [1-3]. Cu diffusion induced dielectric breakdown is a complicated time-dependent process including ionization, injection, diffusion, neutralization, and Cu particle accumulation processes. Therefore, the fast VRDB test may not be suitable for the characterization of time-dependent dielectric breakdown processes.

At the completion of the VRDB test, failure analysis is recommended to be performed on representative structures. A visual inspection is also recommended to verify that the breakdown locations occurred at random locations over the test structure area (if breakdown spots could be seen by visual inspection under microscopy). The failure location should not show a systematic pattern for intrinsic breakdowns.

5 CVS stress overview

The following sections describe the details of the constant voltage stress (CVS) procedure for characterizing time-dependent dielectric breakdown or "wear-out" of BEOL inter- and intra-level dielectrics. The test is designed to obtain voltage and temperature acceleration parameters required to estimate ILD lifetime at use conditions. Unlike highly accelerated voltage ramp tests that are designed to be extremely fast and performed at the wafer-level, the constant voltage TDDB test could be conducted over long periods of time, and be applied at the wafer-level or at package level.

5.1 TDDB test

A constant voltage is applied to the dielectric test structure at a constant temperature. The complete CVS test procedure includes three tests. First, a pre-CVS screen test is performed to remove initially damaged or shorted devices prior to starting the CVS test. Second, the CVS test is conducted, and finally, a post-CVS test is performed to confirm that a valid dielectric breakdown has occurred during the CVS test.

In order to determine the voltage acceleration parameter γ and the thermal activation energy E_a required to extrapolate product lifetime from accelerated stress conditions, the CVS test is performed for a minimum of three voltages and temperatures. Due to the reported intercorrelation of voltage acceleration parameter γ and the thermal activation energy E_a, the test temperature for the voltage acceleration parameter γ determination should be set at the worse case product use temperature (i.e., 125 °C) to avoid temperature transformation for a direct projection. Weibull statistics are recommended to analyze the failure distribution. Note that the extrapolated product lifetime must also take into consideration the area differences between the test devices and the product. It is recommended that at least three different test structure areas are used in characterizing the area dependence of TDDB. One of the key properties of Weibull statistics is its parallel shift of the distribution with device area (shape factor preservation). It is recommended to use larger area ratio (i.e., 10x) to overcome possible TDDB variations caused by other factors such as spacing and line edge roughness due to BEOL process. The sample size at each stress condition should be carefully chosen to provide acceptable confidence levels. It is recommended to use the overall Maximum likelihood estimation (MLE) of combined accelerated lifetime test data to gain several desirable features such as optimal statistical properties with larger sample size, universal application for any distribution model and acceleration model, and statistical tests of key assumptions by likelihood ratio test. It is recommended to calculate confidence limits for each data set based on MLE method. In order to accurately model intrinsic dielectric wear-out, the extrinsic failures may be censored.

5.2 Test procedure

In order to successfully implement the CVS test, the VRDB test previously described is expected to have been performed first. Based on the VRDB test, the CVS stress voltage values, V_{stress}, are selected to not only provide long enough breakdown times for adequate time resolution (< V_{bd}) but also short enough breakdown times to provide reasonable stress times.

5.2.1 Pre-CVS current screen test

Similar to the pre-VRDB test, the purpose of the pre-CVS current screen test is to identify initially failed device and to estimate the initial short yield of the wafer. The procedure of pre-CVS screen test is:

1) Set and record stress temperature
2) Apply V_{use}.
3) Measure I_{meas}
4) If $I_{meas} > I_{init}$, record as initial failure
5) Repeat for all available DUTs on wafer

5.2.2 Constant voltage stress test

Devices that pass the pre-CVS test are then subjected to the constant voltage test. Set the compliance current in the test equipment 10X higher than I_{stress} to ensure that the compliance will not interfere with the determination of breakdown during CVS. Higher compliance is not recommended as it could potentially cause top passivation damage or edge seal breakage during the catastrophic breakdown, which could impose the risks of oxygen and moisture contaminations for the following tests. The procedure for the CVS test is:

1) Apply a stress voltage (V_{stress}). Assure that there are no voltage overshoots exceeding 1% of V_{stress}. The voltage is held at V_{stress} and the current is monitored at time intervals (t_{int}). The current could be recorded at log time intervals (t_{record}). The record time interval should be less than 1% of the anticipated time-to-fail (t_{bd}).

2) The device is considered to have failed when one of the following breakdown criteria has been detected:

   a) A sudden increase in monitored leakage current, I_{meas}, at V_{stress}.

   b) A sudden increase in leakage current using the criteria as described in 4.2.1 is considered failed. Also note a sudden *decrease* in leakage current at V_{stress} indicates an open circuit failure caused by the breakdown current surge destroying a segment of the interconnect metallization.

   c) If monitored leakage current, I_{meas}, is > I_{init}

5.2.3 Post-CVS dielectric current test

Once the CVS is completed, following the detection of breakdown defined in 4.2.1, a post-CVS current test with V_{use} applied to the gate is used to determine the final state of the tested device. Hard breakdown is attributed to all the devices with post-CVS $I_{use\text{-}post} > I_{init}$ and is classified as a valid failure.
If $I_{use\text{-}post} < I_{init}$ then force I_{init} and measure V_{post}. If $V_{post} \geq 0.9\ V_{max}$ then the device has broken down, but is open circuited and is classified is a valid failure.

5.3 Data recording

For TDDB stress, the following information should be recorded and analyzed,

- t_{bd} – the dielectric time to breakdown
- I_{bd} – the dielectric breakdown current measured at V_{stress}.
- $I_{stress\text{-}t0}$ – the initial (t=0) dielectric leakage measured at V_{stress}

5.4 TDDB data analysis

- t_{bd63} – the scale parameter of the t_{bd} Weibull distribution
- Beta of t_{bd} – the shape factor of t_{bd} Weibull distribution. The preferred way of obtaining the Beta is by analysis of data from varying test structure areas. Refer to 4.1 in JESD92, if Poisson area scaling is proved to be valid by vertical overlapping of data from different areas along Weibull scale based on designed area ratios.
- Distribution of I_{use} and $I_{use\text{-}post}$

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Annex A (informative) Supplemental data analysis

A.1 Determining ILD electric field

An accurate determination of ILD electric field is essential if the underlying physical mechanism for dielectric breakdown is to be understood. The electric field across the capacitor (E) is given by:

$$E = \frac{V_{app} - V_s}{s}$$

where V_{app} is the applied voltage, V_s is the parasitic series resistance induced voltage drop, and s is the line-to-line spacing. The spacing s could be estimated from CV measurements with structures of different areas.

$$C = \frac{kA}{s}$$

where A is the test structure area, k is the dielectric constant. By plotting the capacitance versus A, the extracted slope divided by known dielectric constant could give an average s for the structure. This method is non-destructive so that it could be used for a one-on-one TDDB vs. ILD spacing correlation.

A.2 Extrapolation models

A.2.1 Field extrapolation model

Two field dependent TDDB models are commonly used to analyze low-k TDDB breakdown data. The E model is preferred unless additional data taken as described below demonstrates a square root of E dependence. In this case the square root of E model can be used. The E model is based on a thermo-chemical model. In this model ILD breakdown is due to coupling between applied electric field (E) with the dielectric dipole moments (field enhanced bond breakage) and predicts that the time-to-breakdown (t_{bd}) has an exponential linear dependence on applied electric field

$$tbd = t_0 e^{-\gamma E}$$

where t_0 is a constant and γ is the field acceleration factor [4], which could be temperature dependent.
A new low-*k* TDDB model called square-root of E (sqrt-E) model was proposed by several research groups [5-6]. In this model, low-*k* breakdown is driven by electron fluence and could be accelerated by out-diffusion of Cu. The square root term comes from either Poole-Frenkel conduction mechanism or Schottky emission conduction mechanism. In the sqrt-E model, the t_{bd} has an exponential linear dependence on square-root of applied electric field

$$tbd = t_1 e^{-\alpha\sqrt{E}}$$

where t_1 is a constant. α is the field acceleration factor, which could be temperature dependent.
As both mechanisms fit high field breakdown data equally well but they do differ by orders of magnitude in their lifetime prediction at use bias condition, therefore, a model should be carefully selected to assure an accurate lifetime prediction. In general, both models could coexist and one may be favored over the other depending on the low-*k* material properties and process integration. In order to have an accurate determination of which field acceleration model to be used, three high voltage stress points at wafer level plus one or two low voltage stress points (at least 5 – 10V lower than the lowest wafer level voltage point) at module level are recommended during the technology qualification for TDDB model verification and demonstration. A careful check of VRDB I-V slope change to select appropriate stress fields for all TDDB model verification studies is mandatory. Over-stressing at high fields caused by leakage conduction mechanism change or series resistance induced voltage drop could lead to an optimistic TDDB model other than sqrt-E and E models. E model is more conservative than sqrt-E model.

A.2.2 Thermal acceleration model

The temperature dependence of intrinsic lifetime should be modeled using the usual Arrhenius expression:

time-to-fail $t \propto \exp(Ea/kT)$, or $\frac{t1}{t2} = \exp\left[\frac{Ea}{k}\cdot\left(\frac{1}{T1}-\frac{1}{T2}\right)\right]$

where T = temperature in Kelvin and k = Boltzmann constant = 8.6143E-5 eV/K. A thermal activation energy should be determined by TDDB stresses performed at a minimum of three different temperatures.

NOTE E_a was experimentally found to be dependent on field [5]. A comprehensive study of the field and temperature interrelationship may be needed.

A.2.3 Area scaling model

The failure probability for a Weibull distribution scales with area by Poisson area scaling law:

$Fp = 1 - (1 - Ft)^{(Ap / At)}$

where Fp = Product Fail, Ft = test structure fail, Ap = product critical area, At = test structure critical area.

If Poisson area scaling law can be applied by merging data from different areas to a reference area, Weibull slope can be determined by

$$\beta = \ln(n_A)/\ln(r_t)$$

Where n_A is the area ratio, and r_t is the 63.2% ratio from different areas. If the area scaling does not give expected results, then failure analysis must be performed to verify the fail locations. It should be aware that non-random distributed defects, local line edge roughness variation, and global line spacing variation all could cause Poisson model based low-*k* TDDB area scaling law to be broken as the Poisson model only works for Weibull distribution with one random variable. Experimentally, a non-Poisson area scaling usually has been observed for many low-*k* breakdown cases simply due to their actually compound Weibull distributions induced by severe did-to-die variations. For such cases, a careful data deconvolution procedure is strongly recommended to determine in-die Weibull shape factor and to quantitatively determine die-to-die t63 or V63 variations [7].

A.2.4 Determining failure rate

For a technology qualification, a final product failure rate calculation should include all three necessary transformations mentioned above: field transformation, temperature transformation, and area transformation, and should be based on Weibull statistics.

A.2.5 Sample size

For all structures and for all various configurations of ILD layers, testing of minimum three wafers per lot and total three lots are required. Wafer-to-wafer and lot-to-lot TDDB variations should be monitored and reported. If data are consistent from different wafers and lots, combining data for a final failure rate analysis is recommended. Otherwise, separate failure rates should be reported for different wafers from different lots. The measured devices should be uniformly spaced across the wafer for wafer mapping purposes.

For extrinsic failure assessment it is recommended that a 1 cm^2 area should be tested over several wafer lots.

At the completion of the TDDB test a visual inspection is also recommended to be made to verify that the breakdown locations occurred at random locations over the test structure area (if breakdown spots could be seen by visual inspection under microscopy). The failure location should not show a systematic pattern.

A.2.6 TDDB distribution

Weibull statistics should be used to model TDDB distribution, especially when Poisson area scaling is needed for lifetime projection. The failure probability for a Weibull distribution is

$$F(t)= 1-\exp[-(t/\eta)^{\beta}]$$

Where η is scale parameter, and β is shape parameter or slope.

A.2.7 In-die Weibull slope determination and data deconvolution

Generally, BEOL low-*k* dielectric breakdown data are commonly convoluted with multiple variables originating from multiple process steps. Such variations could be significant from die to die, and even within dies. The actual die-to-die variation could be composed of several subpopulations with distinct parameters that cannot be described by a single Poisson distribution. This could be why non-Poisson area scaling is often observed from BEOL low-*k* dielectric breakdown data. During technology qualification, this problem can challenge process and reliability engineers to determine the true intrinsic breakdown behavior while correctly diagnosing process variations. This is important because process issues can appear to degrade measured intrinsic behavior. The traditional method of stressing one DUT per die or multiple DUTs per die, without careful data deconvolution, is incapable of addressing current complex BEOL low-*k* dielectric breakdown challenges. In order to establish a true in-die Weibull slope and quantitatively determine a die-to-die variation, an end-to-end big data generation method is proposed, together with a deconvolution procedure, to soundly evaluate convoluted BEOL dielectric time-dependent-dielectric breakdown (TDDB) data [7].

One straightforward method to investigate the local within die variation is do design a special set of structures with 10-100 clone copies per die. Traditional constant voltage TDDB stress can be conducted on 10-100 clone structures per die, and repeat each stress for all dies or selected dies on the entire wafer. In Figure 3, the 70-90 individual black distributions are the actual local distributions from each die, each data point representing the breakdown value of one of the test structure clones. Therefore, each one of these local distributions captures the within-die variation of the breakdown. Generally, such massive parallel stressing data generation can easily collect a total of about 500-5000 data points per wafer.

A.2.7 In-die Weibull slope determination and data deconvolution (cont'd)

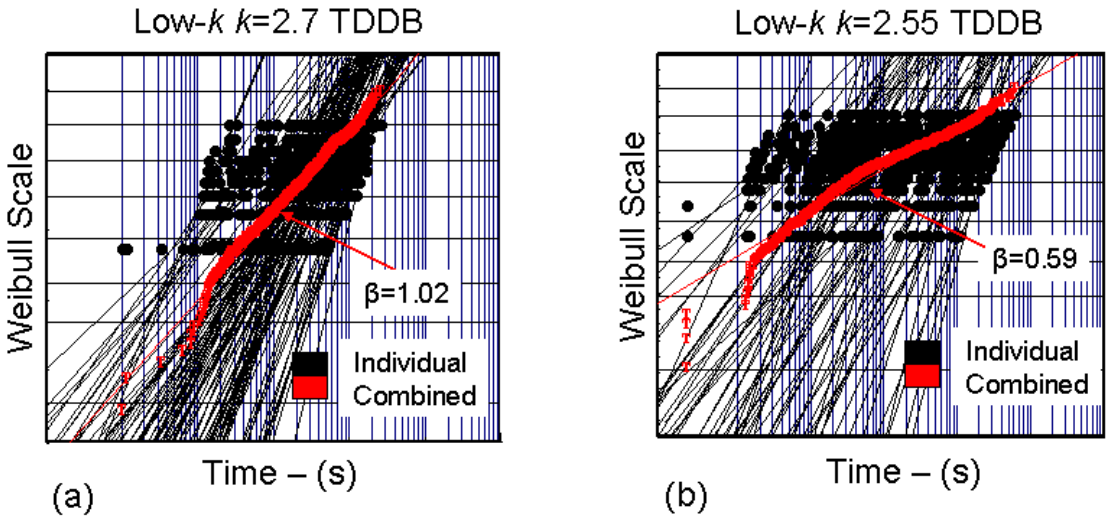

Figure 3 — Experimental proof of various compound Weibull distributions for BEOL low-*k* TDDB with a) *k*=2.7, b) *k*=2.55.

By analyzing all the individual distributions separately, a critical die-to-die variation index chart can be quickly constructed. All t63 or V63 data points from the population (e.g. one wafer or multiple wafers together) can be plotted. Figure 4 shows such data, corresponding to the data shown in Figure 3. Since for a Weibull distribution, the characteristic scale parameter at 63.2% always has the highest confidence bounds, such cross-wafer(s) t63 distributions represent the real die-to-die variation much better than the single DUT from one die approach does. In other words, the distributions of Figure 4 are much more accurate than the red lines on Figure 3. In order to establish a quantitative assessment of any process induced die-to-die variation, this t63 across-wafer distribution is now the new standard for further process diagnostics and reliability evaluation. It should also be noted that electrically measured t63 values obtained by this method capture all relevant breakdown parameters, not just spacing. Therefore, such die-to-die t63 distributions provide more comprehensive information about die-to-die variation than does a spacing distribution alone. This t63 across-wafer(s) distribution can take various shapes as shown in Figure 4. From a reliability modeling perspective, those t63 data points only represent the rate occurrence of each die, not the failure rate of each die. They can be formed in different statistical distributions (Weibull, Lognormal, Normal, etc.). Those t63 data together with within-chip local Weibull slopes ultimately determine the true product chip level failure rate and are less conservative.

A.2.7 In-die Weibull slope determination and data deconvolution (cont'd)

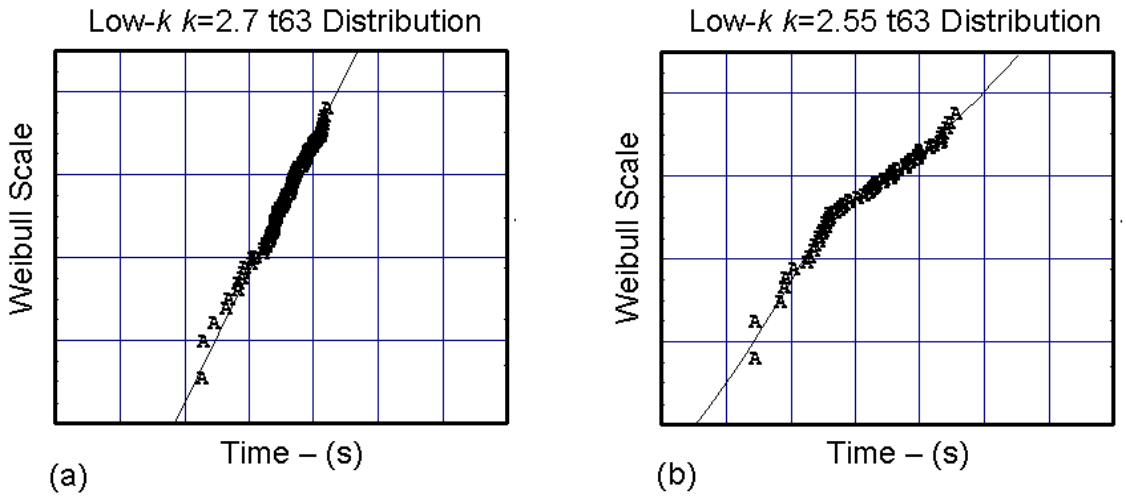

Figure 4 — t63 die-to-die distributions for low-*k* TDDB in Figures 1a and 1b.

Next step is to determine in-die Weibull slope. First, there is always a wide experimentally determined in-die Weibull slope variation (i.e., 3-5X delta) across the wafer if in-die sample size is limited (less than 20). It seems unlikely that such a large spread on the same wafer would be caused solely by an intrinsic nature. Extensive Monte Carlo (MC) simulations confirm that the observed Weibull slope variation could be simply due to the statistical variation of our relatively small sample size per die (i.e., 10-20 points). Therefore, in order to eliminate the substantial cross-wafer die-to-die variation but still utilize the in-die data collected, it is proposed to normalize all data points with a fixed t63 point. By considering the fact of potential Weibull slope dependence on, it is recommended to use the median t63 as the normalization point. Even a minor Weibull slope deviation existed for extremely low and high t63 data points from a wafer, such deviation effect could be cancelled out at median t63. By linking the Weibull slope obtained from normalization to the corresponding median t63, the established Weibull slope should have a better physical meaning. Figure 5 illustrates this analytics procedure in detail. After such normalization, clean mono-modal distributions with substantially improved Weibull slopes were usually observed (Figure 6). As compared to the compound distributions shown in Figure 3, the Weibull slopes in Figure 6 are substantially improved (2-4X). Alternatively, simply taking the median value of all obtained local Weibull slopes could also be used. Such median Weibull slope should be consistent with the Weibull slope obtained by normalization method shown in Figure 5. The third method is to do a forced common Weibull slope fitting with MLE algorithm for all individual in-die distributions. It was found that all those three methods generated a very similar overall in-die Weibull slope. An example of comparisons of all three methods is shown in Figure 7.

A.2.7 In-die Weibull slope determination and data deconvolution (cont'd)

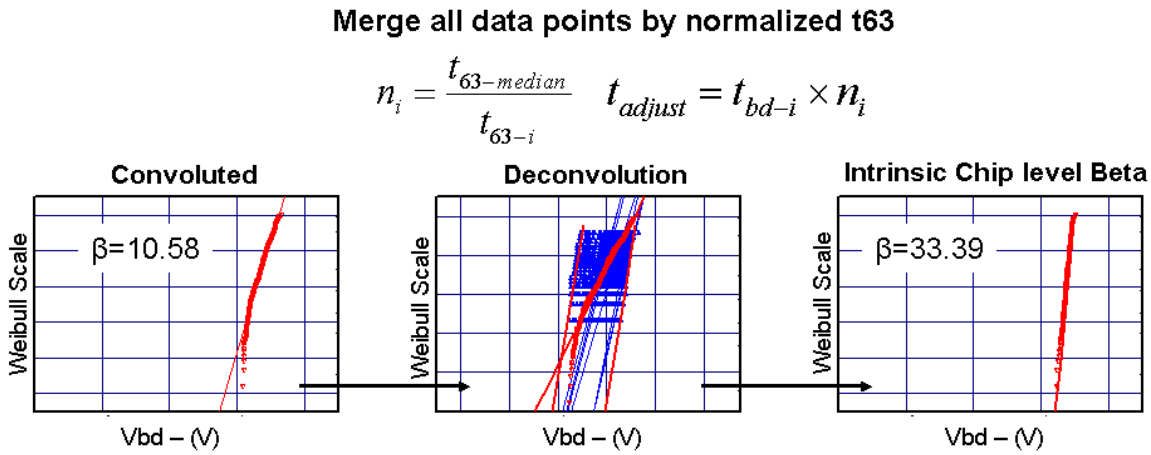

Figure 5 — Data deconvolution procedure details and its outcome of local intrinsic Weibull slope determined from large sample size data.

If a strong wafer regional pattern is found for t63 or V63 distribution, separated evaluation of different groups of dies from different wafer regions based on proposed in-die Weibull slope determination method could be used. As an example, it is recommended to group dies at wafer edge with similar t63 or V63 values only to determine their own common in-die Weibull slope, and to group dies at wafer center only with similar t63 or V63 values to determine their own common in-die Weibull slope, and to group the rest dies at wafer donut region with similar t63 or V63 values to determine their own common in-die Weibull slope. Similar concept can be applied to the samples showing a strong t63 or V63 dependent Weibull slope relation as described in reference [7].

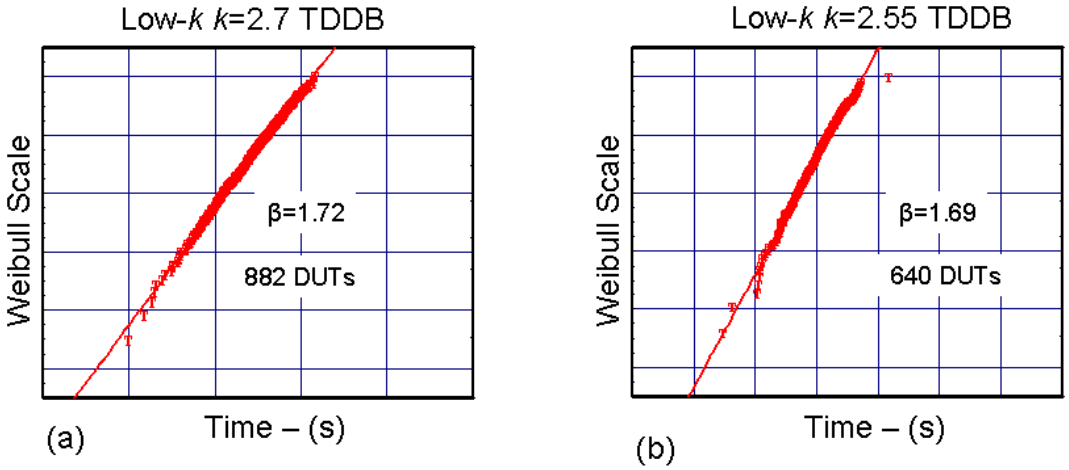

Figure 6 — Local intrinsic TDDB distributions with improved in-die Weibull slopes after deconvolution for BEOL low-*k* TDDB data in Figure 3.

A.2.7 In-die Weibull slope determination and data deconvolution (cont'd)

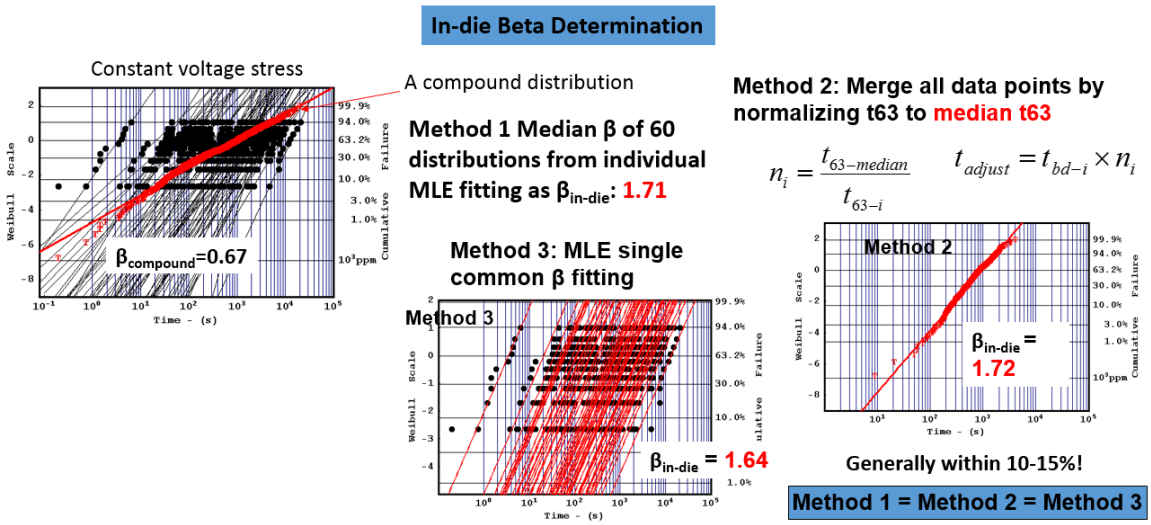

Figure 7 — An example of showing how to determine in-die Weibull slope from three different methods.

The traditional Poisson distribution is not always adequate to predict TDDB area scaling in IC. As shown in Figure 8, based on traditional one DUT per die TDDB stress method, compound Weibull distributions usually exhibit non-Poisson vertical area scaling. In-die TDDB data generation and deconvolution method offers a powerful way to further study low-*k* TDDB area scaling. As shown in Figure 9, Poisson area scaling could be still preserved for local, within-die area scaling as experimentally demonstrated. Therefore, it is assumed that there is no fundamental area scaling physics change for all BEOL low-*k* TDDB, and single Poisson area scaling physics could still works nicely at local per-die level. It is recommended to perform local area scaling and do comparison to in-die Weibull slope determined by data merging method described in Figure 5.

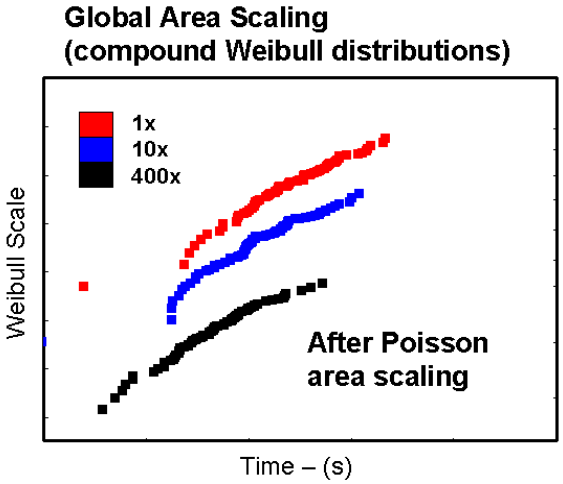

Figure 8 — Compound TDDB Weibull data transformed by Poisson area scaling. The Weibull slope by flat fitting of all three transformed distributions is 0.51.

A.2.7 In-die Weibull slope determination and data deconvolution (cont'd)

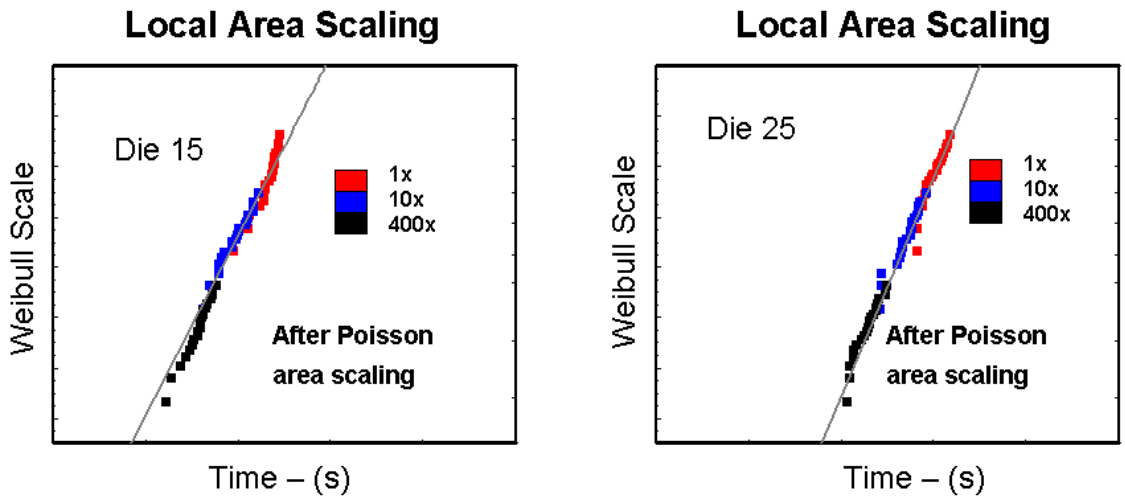

Figure 9 — Local area scaling by single Poisson area scaling. The Weibull slope for die 15 is 1.55 and for die 25 is 1.91.

In-die TDDB data generation and analytics method has a profound impact on reliability failure rate determination. Generally, the traditional "one DUT per die" stress method is only valid if all dies on the wafer are exactly identical. Otherwise, the failure rate calculated from the traditional method is just a wafer-based failure rate, and has nothing to do with the required die-level failure rate. Furthermore, using a convoluted distribution at test structure level to predict a convoluted distribution at die level but without knowing the convolution details at both levels will most likely cause an erroneous projection. Based on the experimentally deconvoluted data, a probability associated TDDB concept as shown in Equation 1 should be considered.

A.2.7 In-die Weibull slope determination and data deconvolution (cont'd)

The total failure probability of chips with different distribution parameters should be a sum of individual chip failure probabilities of all the chips and the correspondingly different probabilities over the probability density function (individual failure rate weighted with its occurrence) as the following:

$$CDF(chip) = \sum_{i=1}^{m} cdf(x_i)/m = \int_{x_{\min}}^{x_{\max}} cdf(x) \times P(x) dx \quad (1)$$

$$cdf(x) = 1 - \left(Exp\left[-\left(\frac{x_{target}}{x} \right)^{\beta(x)} \right] \right)^{n} \quad (2)$$

$$P(x) = \frac{1}{\sqrt{2\pi\sigma^2}} Exp\left[\frac{-(x - x_{mean})^2}{2\sigma^2} \right] or$$

$$P(x) = \left(\frac{k}{\lambda} \right) \left(\frac{x}{\lambda} \right)^{k-1} Exp\left[-\left(\frac{x}{\lambda} \right)^{k} \right] \quad (3)$$

where n is the area scaling ratio, x could be time scale parameter t63, voltage scale parameter t63, or space scale parameter. P(x) is a specific probability density function of parameter x. P(x) could be in Weibull or Normal format as shown in Equation 3. In order to make sure that P(x) obtained from the testing structure can be applied to real product, using three testing structure sizes to check the consistency of P(x) at different sizes is recommended. Equation 1 calculates the overall chip level failure probability weighted with different occurrences of different chips if a strong chip-to-chip variation presents in the product. It is recommended to calculate failure probability by integrating Equation 1 from minimum x to maximum x. The total chip failure probability calculated by Equation 1 usually is smaller than the number calculated by traditional method. Alternatively, based on Equation 3, if a worst case rate of x (i.e., 1000 ppm) based on Equation 3 is selected and if it is further assumed that the entire chip level population consists of such worst case x, a simple but more pessimistic failure probability can also be calculated by Equation 2.

Other deconvolution methods may also be considered as far as they can provide a correct in-die Weibull slope and quantitative die-to-die variation information. An alternate approach to de-convolute intrinsic reliability from sources of variation is to generate a TDDB model that is normalized by E-field based on the space of the test structures. The 'shorting space' information can be extracted either through electrical measurements or optical metrology. The final product fail rate can be estimated by integrating the failure rate over the actual product shorting space distribution.

Disclaimer: If traditional method can pass TDDB qualification, new deconvolution method is not necessary required as traditional method should be more conservative. If in-die sample size is small (i.e., less than 10), a careful validation of in-die Weibull slope with a good mono-modal distribution after data normalization and grouping MLE fitting with a single common Weibull slope are strongly recommended. Possible overestimation and underestimation of Weibull slope by merged local distributions could occur if in-die sample size is small.

Annex B (informative) Differences between JEP159A and JEP159

This annex briefly describes most of the changes made to entries that appear in this publication, JEP159A, compared to its predecessor, JEP159 (August 2010). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of change
Intro	revise entire "introduction" section to take out test structure contents for a new section 3.
1	add "the effect of ILD TDDB" before "on product lifetime or failure rate".
3	add a new independent section 3 of "Test Structure Overview".
4.1	add "The test temperature usually is set at the worst case product use temperature (i.e., 125 °C) to avoid using temperature extrapolation due to potential intercorrelation of dielectric breakdown voltage and temperature".
4.5	modify VRDB data analysis section to add Normal distribution as another option for V_{bd} data analysis.
5.1	add "Due to the reported intercorrelation of voltage acceleration parameter γ and the thermal activation energy E_a, the test temperature for the voltage acceleration parameter γ determination should be set at the worse-case product use temperature (i.e., 125 °C) to avoid temperature transformation for a direct projection".
5.2.2	add "If monitored leakage current, I_{meas}, is > I_{init}" as a third failure criterion for constant voltage stress test.
6	add Reference 7 on page 12
A.2.1	add "A careful check of VRDB I-V slope change to select appropriate stress fields for all TDDB model verification studies is mandatory. Over-stressing at high fields caused by leakage conduction mechanism change or series resistance induced voltage drop could lead to an optimistic TDDB model other than sqrt-E and E models".
A.2.3	add "Experimentally, a non-Poisson area scaling usually has been observed for many low-*k* breakdown cases simply due to their actually compound Weibull distributions induced by severe did-to-die variations. For such cases, a careful data deconvolution procedure is strongly recommended to determine in-die Weibull shape factor and to quantitatively determine die-to-die t63 or V63 variations [7]".
2.7	add an entire new Annex 2.7 to describe a procedure of how to do in-die Weibull slope determination and data deconvolution.

Standard Improvement Form JEDEC JEP159A

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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