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Discontinuing Use of the Machine Model for Device ESD Qualification

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DISCONTINUING USE OF THE MACHINE MODEL FOR DEVICE ESD QUALIFICATION

Contents

Foreword

The machine model test, as a requirement for component ESD qualification, is being rapidly discontinued across the industry. This publication is intended to document why MM evaluation is not necessary for qualification. The following major conclusions can be made about MM in general:

- MM is redundant to HBM at the device level since it produces the same failure mechanisms, and the two models generally track each other in robustness and in failure modes produced.

- The MM test has more variability and, consequently, less repeatability than HBM due to the MM's greater sensitivity to parasitic effects in the tester circuitry.

- There are no significant engineering studies (with verified data) which could be used to establish a required passing level for MM.

- The test method was incorrectly given the name "machine model", though no firm, unique connection between the model and actual machine-induced device failures was ever established. In fact the model was developed as a "low-voltage HBM".

- CDM does a better job of screening for fast metal-to-metal contact events than MM.

- The vast majority (> 99%) of electrical failures in manufacturing correlate to CDM or to EOS and not to MM.

- MM testing has not shown any additional failures not explained by CDM, HBM or EOS.

- MM testing consumes resources and creates time-to-market delays while providing no additional failure modes or protection strategies which have not been covered by HBM and CDM.

- *It is important to understand the scope of this memorandum*. It summarizes what has been learned about the test method *only*. The information summarized here in no way diminishes the importance of proper grounding of any metal which may come in contact with ESD-sensitive devices or the importance of avoiding hard metal-to-metal discharges.

DISCONTINUING USE OF THE MACHINE MODEL FOR DEVICE ESD QUALIFICATION

(From Board Ballot JCB-15-26, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices Reliability Qualifications and Monitoring.)

1 Scope

Over the last several decades the so called "machine model" (aka MM) and its application to the required ESD component qualification has been grossly misunderstood. The scope of this JEDEC document is to present evidence to discontinue use of this particular model stress test without incurring any reduction in the IC component's ESD reliability for manufacturing. In this regard, the document's purpose is to provide the necessary technical arguments for strongly recommending no further use of this model for IC qualification. The published document should be used as a reference to propagate this message throughout the industry.

2 References

[1] JEDEC JESD47 “Stress-Test-Driven Qualification of Integrated Circuits”, www.jedec.org

[2] JEDEC JESD22-A115 “Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)”, www.jedec.org

[3] ANSI/ESD STM5.2-2012 “Machine Model (MM) – Component Level “ www.esda.org

[4] M. Tanaka, JEITA/JEDEC Meetings, Tokyo, September 2011.

[5] M. Tanaka, K. Okada, and M. Sakimoto, “Clarification of Ultra-high-speed Electrostatic Discharge and Unification of Discharge Model,” EOS/ESD Symposium, pp, 170-181, 1994.

[6] Industry Council on ESD Target Levels, “White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements,” August 2007, at www.esda.org or JEDEC publication JEP155, “Recommended ESD Target Levels for HBM/MM Qualification”, www.jedec.org

[7] ANSI/ESD S20.20 - For the Development of an Electrostatic Discharge Control Program

[8] ESDA standards document definitions and hierarchy are summarized at www.esda.org/Documents.html

3 Terms, Definitions, and Letter Symbols

AEC	Automotive Electronics Council
ANSI	American National Standards Institute
CDM	charged-device model
EOS	electrical overstress
EPA	ESD protected area
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association
FAR	failure analysis report
HBM	human body model
IC	integrated circuit
JEDEC	JEDEC Solid State Technology Association
JEITA	Japan Electronics and Information Technology Industries Association
MM	machine model
OEM	original equipment manufacturer
STM	standard test method

4 Background

As will be explained below, the machine model (MM) is a widely misunderstood component ESD qualification test method. It continues to generate confusion for both OEM customers and their IC suppliers during ESD qualification. Many companies and design organizations continue to use MM, mostly as a legacy "required" practice, despite the fact that it has been downgraded by three standards bodies and is no longer recommended for qualification testing in accordance with JEDEC JESD47 [1]. The automotive industry, a longtime user of this method, no longer requires it in their AEC-Q100 list of qualification tests. The scopes of the JEDEC (JESD22-A115) [2] and ESDA (ANSI/ESD STM5.2) [3] test method documents have also been changed to reflect this status. There are a number of reasons for these changes, as will be outlined below. The continued use of MM for qualification based solely on legacy requirements has no technical merit given the information that has been gathered over the last few years. Those companies who continue to use MM will take on an unnecessary and burdensome business approach without any technical benefit. The reasons against use of the MM are as follows:

1) Historically speaking, the 200 pF, "0 ohm" model, which later became known as the machine model, originated from several Japanese semiconductor corporations as a worst-case representation of the Human Body Model (HBM). The model was later presumed by some, because of the lower discharge impedance, to simulate abrupt discharge events caused by contact with equipment and empty sockets (functional test, burn-in, reliability testing, pick and place operations, etc). This happened at a time when the very fast rise time of metal-metal discharges was not well-understood. Since that time, the Charged Device Model (CDM) has been proven to quite adequately cover these events.

2) Recently, M. Tanaka-san (Renesas Electronics) at the September 2011 JEITA meetings [4] presented rationale and data supporting the elimination of the MM test. According to his historical account, the so-called Machine Model originated at Hitachi (now Renesas Electronics) about 45 years ago and was introduced to Japanese semiconductor customers as a test case to represent the HBM test in their IC product test report. This test method spread widely to the Japanese customer base and was later established as an ESD test standard by the EIAJ in 1981. Around 1985 and onwards, some began to mistakenly refer to the test as the Machine Model. Then, starting in 1991, ESDA, JEDEC and IEC adopted the model and its name as a new test standard. As use of the model increased, it was realized that the Machine Model name caused a lot of misunderstanding that needed to be clarified.

3) In the early days of ESD device testing there was also a desire to avoid the high pre-charging voltages of the HBM test (2 kV and higher), and the 200 pF and low impedance of the "MM" was thought to be an equivalent but safe lower voltage test to address the same failure mechanisms as HBM. However, establishment of a single translation from MM voltage to HBM voltage has been difficult to achieve. Protection design has traditionally been focused on meeting the HBM requirement, but MM testers are susceptible to parasitic circuit elements, with these parasitics from relay switching networks in the simulators causing more variation in the MM waveform than waveforms from HBM testers. In spite of this and without any supporting data, 200 V MM became established as a *de facto* requirement. It was thought to be the safe level for handling and that this level had to be simultaneously met along with the *de facto* 2 kV HBM standard. In reality a device with a 2 kV HBM withstand voltage might have an MM withstand voltage anywhere from 100 to 300 V, depending on the device characteristics and the MM tester parasitics. This led to much of the confusion associated with specifying both HBM and MM levels.

4 Background (cont'd)

The next important reason for discontinuing MM is that fast discharges to or from a metal surface are not correctly represented by the MM. The characteristics of the MM rising pulse were not established based on comparison of measurements on machine pulses, but rather were determined by characteristics of the already developed HBM simulators. The fast rising leading edge of metal-to-metal discharges are actually more effectively simulated using the current standard CDM test methods. This is known today because of the development of high speed oscilloscopes. However, during the 1980s, there was a misunderstanding that MM was a good representation for CDM. This misunderstanding actually delayed the eventual development and acceptance of the CDM standards used today. Later in the 1990s, with the much improved and accurate test for CDM and with the wider recognition that the fast discharges are covered by CDM alone, the test for MM became more frequently replaced by CDM.

5 MM vs. HBM and CDM

The waveforms for HBM, MM and CDM are compared in Figure 1. The HBM and MM have similar ranges of rise time (2-10 ns). Therefore, any thermal heating in silicon taking place in this time period leads to the same failure mechanisms for both models. This holds true for all technologies, including advanced technology nodes. This early part of the waveform determines where and how protection circuits must be deployed in design. With similar rise time characteristics, HBM and MM encourage the same protection designs. For CDM, on the other hand, the rise time is much faster (0.1 – 0.5 ns) and often leads to a unique failure mechanism, like oxide breakdown. Even more important, the observed ESD field failures are dominated by oxide breakdown when the CDM level is not adequate. Thus, a different set of protection strategies are generally needed for CDM. This makes it even more critical to focus on CDM qualification, instead of duplicating the HBM test information by using the MM. In Figure 1, we also show the observed failure modes for the same I/O pin after stressing with HBM, MM and CDM. It is clear that, with HBM and MM, the damage sites were the same, occurring in the protection diode. However, with CDM stress, the damage site corresponds to oxide breakdown in the output transistor. This also illustrates the fact that meeting high levels of MM does not improve the CDM performance until the right effective design techniques are employed.

5 MM vs. HBM and CDM (cont'd)

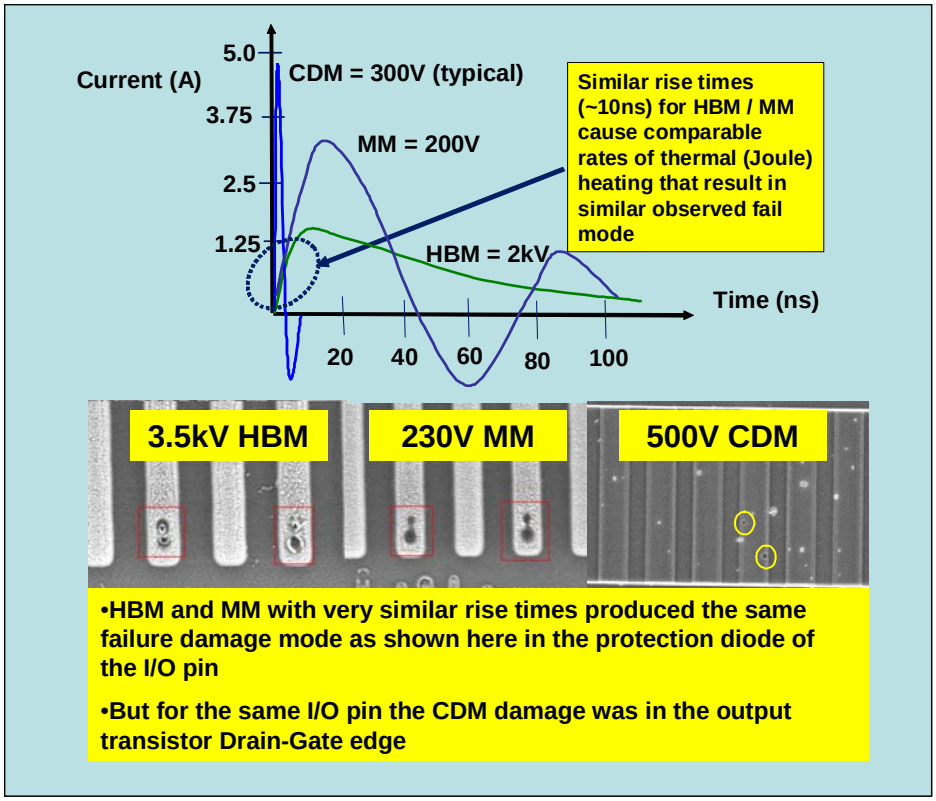


Figure 1 — Comparison of HBM, MM and CDM Waveforms

Commercial MM testers have inductors built into the MM stimulus circuit. These inductors must be present to produce the oscillatory waveform required in the MM test method. The inductors, however, actually slow down the MM waveform (Figure 1), and, therefore, MM cannot represent very fast metal-to-metal contact discharge as CDM does. On the other hand, the CDM test is directly represented by elevating the package potential and directly grounding the pin to produce the fast discharge. MM cannot be relied on to accurately model fast metal-to-metal contact discharges, which are known to occur in the field.

6 Metal Discharge versus CDM Discharge

The analysis of M. Tanaka [5] is shown here to demonstrate that a metal discharge from a small metallic object to a device is similar to the commonly used CDM test. Tanaka considers small objects because large machines (typically >10 pF) are almost always grounded for reasons beyond ESD, and thus pose little practical threat for these events. On the other hand, tools and small machines are difficult to ground and may lead to charging effects where the capacitance of the metal object is related to surface area and distance. These values can range from < 1 pF to nearly 10 pF. For example, this could be as much as 1 pF for a small metal object of 10 cm^2 at a distance of 0.5 cm. Both the small metal discharge and the CDM discharge can be represented by the same set of equations for I(t), and thus both can be expected to generate the same discharge event if the values of the parameters are similar. Figure 2 illustrates the case for a small object of 10 pF for both metal discharge and CDM discharge.

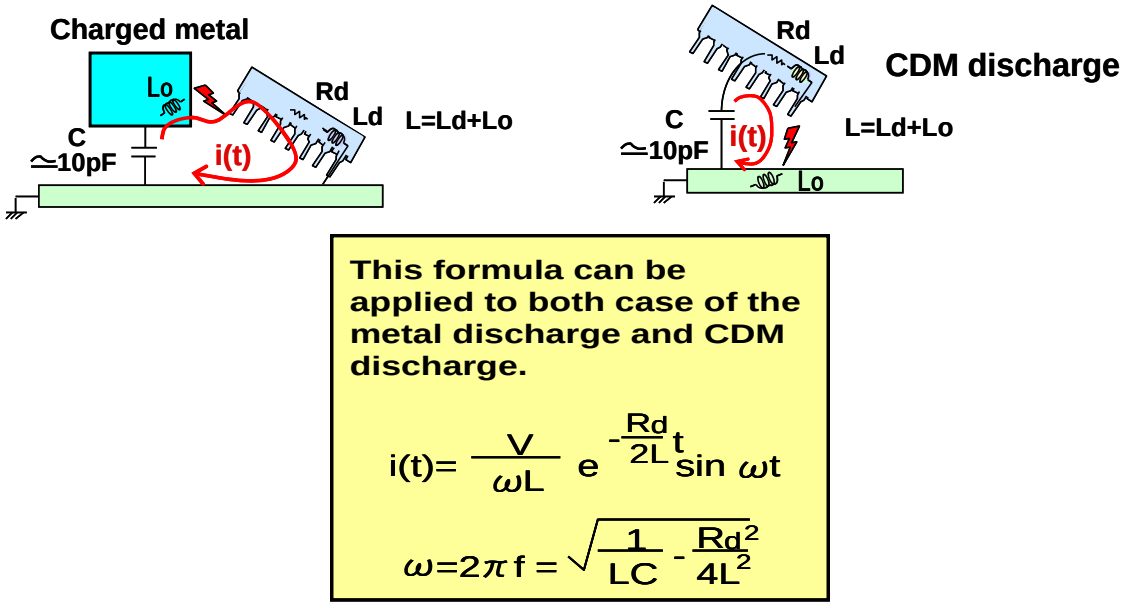
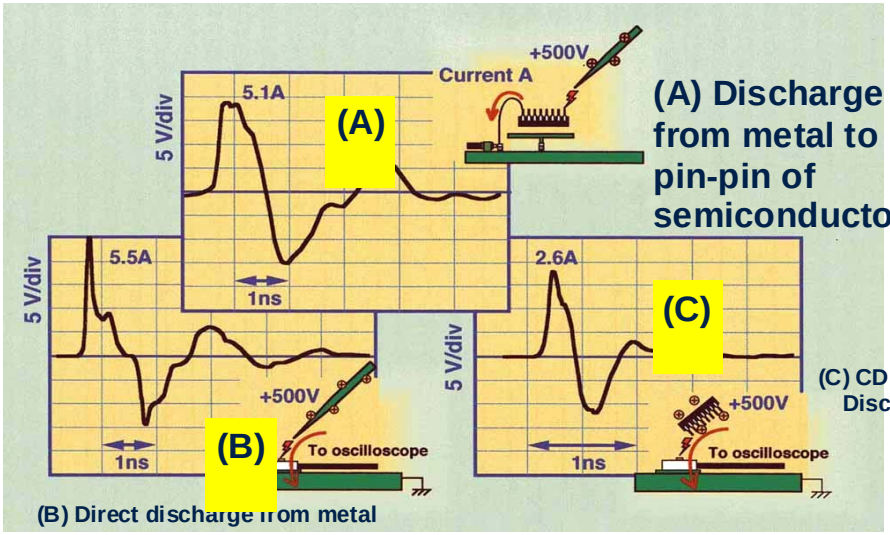


Figure 2 — Discharge current equation for metal discharge or CDM discharge [4]

The above analysis is confirmed by measurements [5] as shown in Figure 3, where the discharge in (A) from charged tweezers to an IC pin is the same as direct discharge from metal as shown in (B), and both are similar to the generated CDM discharge in (C). The time scale for both metal discharge and CDM discharge is indeed the same, clearly indicating that CDM is a good representation of the metal discharge in the EPA.

6 Metal Discharge versus CDM Discharge (cont'd)



(A) discharge from a charged tweezer on pin, (B) direct discharge from metal and (C) CDM test discharge

Figure 3 — Comparison of measured waveforms for metal discharge and CDM discharge events [5]

In summary:

- Metal discharge events are well represented by the CDM test.

- Upon analysis of the ESD field returns, in a vast majority of the cases, the damage mechanism can be replicated with either HBM or CDM test but cannot be replicated with the MM test. Hence, the MM test, even though it may generate some rare unique design failure modes, does not represent field failure reliability.

The Industry Council on ESD Target Levels has studied the HBM and MM results on a wide variety of designs in many technologies and has concluded that MM is intrinsically related to HBM, with a correlation factor "range" that is dependent on the HBM design level [6]. This data is represented in Figure 4. In some rare cases, due to a design issue, the relative HBM:MM ratio could rise above this range. However, the most important conclusion of the study was that MM is a redundant test and that a sufficient level of MM field robustness is automatically included in an adequate HBM design. This also includes the bipolar nature of the MM stress. Any oscillatory waveform which might be measured during discharges in the field is sufficiently covered if the part is proven to have an adequate HBM design.

This minimum design value, as measured by a MM tester, is well above any voltage remaining on all properly grounded machines in an ESD protected manufacturing environment. In essence, meeting a safe value for HBM (and CDM) is sufficient for production of ICs, without needing to evaluate MM as an additional qualification. Therefore:

- **The machine model test method specification to qualify ICs does not model or advance the real-world ESD protection of IC products.**

- **IC evaluation with MM does not give any additional information as to how to address machine ESD control.**

6 Metal Discharge versus CDM Discharge (cont'd)

- **While MM is an unnecessary qualification test, it is important to emphasize that control of voltage on machine parts that might contact device pins in accordance with an ESD control program, such as ANSI/ESD S20.20 [7], is still important.**

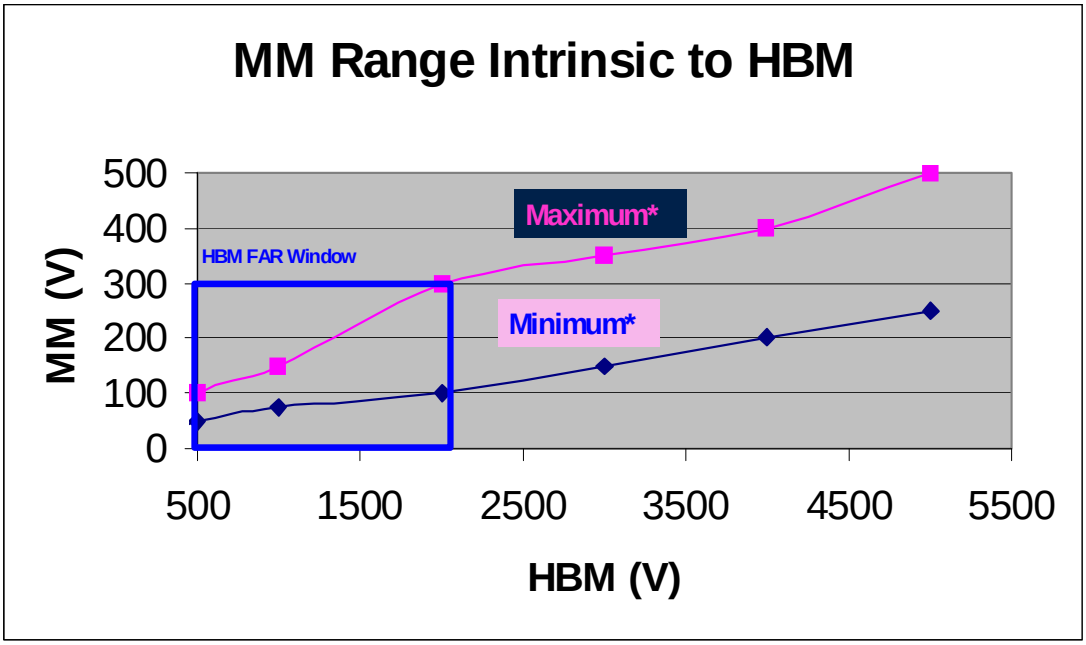


Figure 4 — Correlation between HBM and MM measured on the same devices, representing more than 95% of the cases

7 Field Data Analysis

The work from the Industry Council [6] has shown that most of the overstress field returns exhibit failure signatures of a higher energy EOS event, and that the level of HBM ESD from 500 V to 2000 V (shown as the HBM failure analysis return (FAR) window in Figure 4) for 21 billion shipped units did not show a correlation to the customer field return rates. Similarly, these very same shipped units (500 V to 2 kV HBM) also had MM levels in a range between 50-300 V, as also shown in Figure 4. Therefore it can be concluded that the EOS field returns are indeed not related to this range of intrinsic MM levels. That is, it does not matter if a shipped device has a measured MM value of 50 V or 300 V.

Devices with various measured MM levels have shown no correlation to real world EOS failure returns.

8 Standards Bodies and Positions on MM

During the last two decades, the electronic industry's standards bodies have changed their viewpoint with regard to MM and its requirement for IC qualification. At present, JEITA in Japan does not recommend MM. The Automotive Electronics Council's AEC Q100 standard gives a choice between HBM and MM, but does require CDM. In recent years, JEDEC has strongly recommended discontinuing use of MM for ESD qualification because of its test variability and non-correlation to real-world failure modes. In general, standards bodies have come to recognize that:

- IC Qualification to HBM and CDM provides all the necessary ESD test requirements.
- MM testing of ICs is redundant to HBM and does not reflect unique real-world component ESD failure modes.
- Billions of IC components have been shipped worldwide and qualified using HBM and CDM testing only. No field failures have been found that would have been prevented by additional MM qualification.

The following statements are from the JEDEC web site:

- "JESD22-A115 [2] is a reference document; it is not a requirement per JESD47 [1] (Stress-Test-Driven Qualification of Integrated Circuits)."
- "Machine model as described in JESD22-A115 [2] should not be used as a requirement for integrated circuit ESD qualification."
- "Only human body model (HBM) and charged-device model (CDM) are the necessary ESD Qualification test methods as specified in JESD47 [1]."

The ESD Association has downgraded the MM document from a Standard (S5.2) to a Standard Test Method (STM5.2) [8], and has adopted the following position:

The ESD Association does not recommend using MM ESD as described in STM5.2 for IC qualification. IC Qualification should be done using the current standard HBM and CDM methods.

9 Conclusions

The information in this document supports discontinuing MM as part of IC qualification. The most important point to note is that a wide range of products, having only HBM and CDM testing performed, are being shipped today at volume levels in the billions, with no field returns that could be prevented by MM qualification. These products, passing at or above the recommended minimum HBM and CDM levels, are being routinely shipped by major suppliers and are accepted by major OEMs. No increase in field return rates has been observed with MM removed from qualification for these products.

The confusion generated by MM has persisted in the industry for over two decades. The presumed need for this test is causing additional qualification and time-to-market delays due to an extraordinary consumption of design / test resources and, in some cases, is also having an impact on IC speed and performance. Maintaining safe HBM and CDM levels is sufficient to meet all IC manufacturing, handling and assembly needs.

10 Epilogue

Different customer sectors may feel that they need enhanced ESD requirements for specific reasons. For example, some automotive customers have more consistently required MM model testing, the assumption being that an independent and redundant test provides enhanced safety, improved quality or reduced defectivity. However, industry experience has shown that passing a redundant (to HBM) MM qualification test does not help automotive manufacturers achieve these goals. Meeting current industry standard HBM / CDM will insure that a product can be safely handled with sufficient margin to prevent ESD damage and maintain the quality/reliability of the product as shipped from the component manufacturer. Since many suspected ESD failures turn out to be higher energy EOS in nature, methods to prevent electrical overstress during manufacturing will also help maintain product reliability.

11 Common Goals

We have presented evidence and arguments that the MM test of ICs is redundant and there is no proof that devices have failed in the field because MM evaluation was not done. We strongly recommend that this test be discontinued for ESD qualification. This will save the semiconductor industry a tremendous and an unnecessary burden by greatly reducing the routine characterization that is done to support the qualification process. The ESD robustness designed into integrated circuits to survive HBM and CDM testing will provide protection against any MM-like stress. Eliminating MM testing of ICs has no deleterious effects and will free up resources for more important engineering challenges.

Annex A (informative) Differences between JEP172A and JEP172

This annex briefly describes most of the changes made to entries that appear in this publication, JEP172A, compared to its predecessor, JEP172 (July 2014). Some punctuation changes are not included.

Clause	Description of change
Cover pages	Add ESDA Logo
2	Modified reference 7, S20.20
3	Updated term JEDEC, from JEDEC Joint Electronic Devices Engineering Council to JEDEC Solid State Technology Association

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