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Constant-Temperature Aging Method to Characterize Copper Interconnect Metallization for Stress-Induced Voiding

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CONSTANT-TEMPERATURE AGING METHOD TO CHARACTERIZE COPPER INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING

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CONSTANT-TEMPERATURE AGING METHOD TO CHARACTERIZE COPPER INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING

(From JEDEC Board Ballot JCB-15-06, formulated under the cognizance of the JC-14.2 Committee on Wafer-Level Reliability.)

1 Scope

This document describes a constant temperature (isothermal) aging method for testing copper (Cu) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding (SIV). This method is to be conducted primarily at the wafer level of production during technology development, and the results are to be used for lifetime prediction and failure analysis. Under some conditions, the method may be applied to package-level testing. This method is not intended to check production lots for shipment, because of the long test time.

Dual damascene Cu metallization systems usually have liners, such as tantalum (Ta) or tantalum nitride (TaN) on the bottom and sides of trenches etched into dielectric layers. Hence, for structures in which a single via contacts a wide line below it, a void under the via can cause an open circuit at almost the same time as any percentage resistance shift that would satisfy a failure criterion.

The method assumes that void growth (and therefore resistance changes) can be modeled as described by Ogawa, et al.[1], Yao, et all [2, 3] Fischer et al. [5,6], to obtain a median lifetime, an effective activation energy, and an acceleration factor for lifetime.

2 Stress induced voiding in copper

2.1 Stress-induced voids

Stress migration (SM) or stress-induced-voiding (SIV) is one of the key aspects of Cu interconnect technology reliability qualification. The SIV damages are caused by the stress gradient as driving force through the means of diffusion. For Cu interconnects, it is known qualitatively that the intrinsic SIV risk is higher for a wide line relatively to a narrow line structure with a fixed single via size [1-4, 7-11]. As industrial standards, SM reliability data have been treated qualitatively to define pass or fail criteria. The agreed guard-band of “zero fails during a fixed time period” as SM qualification passing criteria has been generally accepted by the industry [8]. This approach was inherited from Al SIV testing method for Cu SIV guard-band but with certain degrees of uncertainty. With the further technology scaling, the Cu SIV reliability margin becomes narrower. Therefore, the old traditional standard could lead to even larger error bars for reliability projections. In order to overcome this known trend of increasing SIV risk, a quantitative SIV lifetime estimation method is needed.

2.1 Stress-induced voids (cont'd)

In recent years, the SIV mechanism has been investigated to reduce SIV risk and established SM qualification methodology [1-4, 7]. Due to the improvement of integration process, progress has been made in SM reliability performance in meeting the design lifetime goals. In general, observation of SM fails is not expected for design rule compliant (DRC) linewidth structures even at the worst temperatures during SM reliability testing period (i.e., 500 h to 1000 h). It is possible to measure SM fails from reasonable wide linewidth test structures within reasonable testing period of time. In [2,3], a geometry linewidth dependent factor was introduced to support an SM model for lifetime extrapolation. The quantified linewidth dependent SM data from 45 nm, 32 nm, and 28 nm show a common power-law factor M. This further supports the SM model with a geometry linewidth factor for acceleration [2,3]. In this spec, in addition to the traditional method, we will apply the SM lifetime model and the equation to develop an SM reliability qualification methodology for meeting the product design lifetime.

2.2 Stress temperature

Cu SM data show a strong temperature dependence of SM lifetime. Based on the Creep voiding rate model by McPherson & Dunn [1, 2, 3, 16,17], we have the median time-to-fail (MTF) relationship:

$$MTF = A(T_0 - T)^{-N} \exp(E_A / k_B T) \qquad (1)$$

where T_0 is the stress-free temperature at which the thermomechanical stress transits from tensile to compressive, N is the thermal stress component, E_A is the diffusion activation energy, k_B is the Boltzmann constant and A is normalization constant.

As an example, Figure 1 shows the MTF distribution of the 5 μm linewidth via chains from 32 nm wafers as a function of temperature in the range of 125 ºC to 275 ºC. No SM fails were measured from the 325 ºC test.

Equation (1) was used to fit the five-temperature failure distributions from the PL-SM data of the 5 μm via chains as shown in [2,3]. During the fitting process, parameters of T_0 , N and E_A are allowed to vary to minimize the standard fitting error function. As results, the T_0 value is 277 ºC, N is 1.25, and E_A is 0.72 eV in this case. The results of fitting parameters were applied to (1) and the calculated MTF values are shown as model fit in Figure 3. The model fit calculations and the MTF SM data distributions are consistent with each other. It is necessary to point out that the E_A value can vary depending on the quality of Cu/cap interface and Cu grain boundary diffusion. A relative weak Cu/cap interface assisted by gain boundary diffusion will lower the E_A. The E_A values can be in the range of ~1.0 eV to 0.5 eV.

2.2 Stress temperature (cont'd)

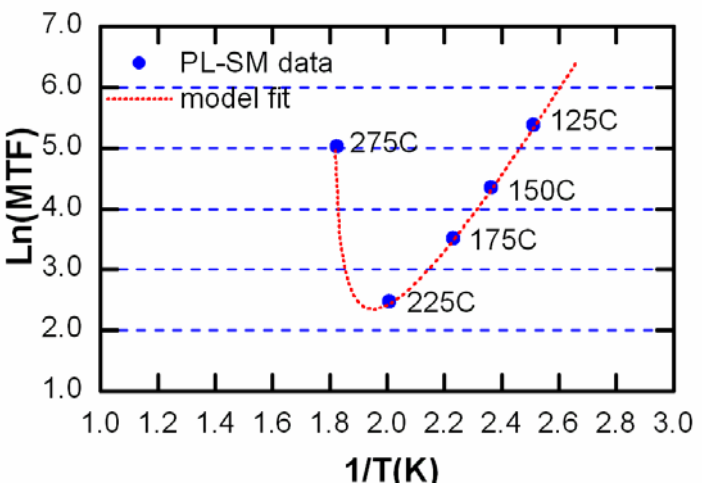


Figure 1 — Temperature dependent behavior of SM MTF values of 5 μm via chains in the range of 125 ºC - 275 ºC

The results shown in Figure 1 demonstrate the following important SM behavior: 1) above T_0, no SM fails will occur due to the compressive thermo-mechanical stress. The fact we have measured no SM fails from the 325 ºC tests confirms this; 2) MTF increases as temperature decreases below T_0. MTF reaches its minimum at a "sweet spot" near 200 ºC to 225 ºC. The location of the "sweet spot" may vary depending on wafer process details; 3) below T_0 but above the "sweet spot", the MTF distribution reverses its direction; 4) Close to the operating temperature range, i.e., ~125 ºC to 100 ºC, the SM data are mostly Arrhenius-like and dominated by the diffusion term. The temperature dependence below the "sweet spot" (i.e., ~175 ºC to 100 ºC) can be approximately treated by Arrhenius model.

2.3 Geometry linewidth dependence of SIV risk

The linewidth dependence of SIV risk is an important feature for setting design rules and reliability qualification tests. As we have shown in section A that SM MTF values are linewidth dependent. In general, the SIV risk increases as linewidth increases for a single via. The MTF values follow a power-law as a function of linewidth as shown in Figure 2. The MTF power-law relation can be expressed as:

$$MTF=CW^{-2.94} \quad (2)$$

where W is the linewidth or plate size and C is a normalization constant. 2.94 is the power-law component value from the fit.

2.3 Geometry linewidth dependence of SIV risk (cont'd

Figure 2 shows the MTF power-law relation of linewidth measured from wafers of technologies of 45 nm, 32 nm, and 28 nm. It is noticeable that SM data from all three technologies follow the power-law by linewidth and the power components of the three set of data are nearly the same, ~2.94. The power component value of ~3 indicates the possible relation to a particular voiding nucleation mechanism [14,15]. We believe that the MTF power-law relation of linewidth reflects the intrinsic nature of SM linewidth scaling. It can be expressed in general terms as:

$$MTF=CW^{-M} \tag{3}$$

where M is the geometry stress component. The M values can be fitted and checked from SM testing results. Its value may be altered in accordance to the wafer process and presence of intrinsic failures. For this illustration, the M values extracted from three technologies are consistently close to 3. It is recommended that characterization is performed to understand the intrinsic SM property and establish validity and correlation to this prescribe model in order to determine applicability, especially in the smaller regions adjacent or outside line width of figure 2.

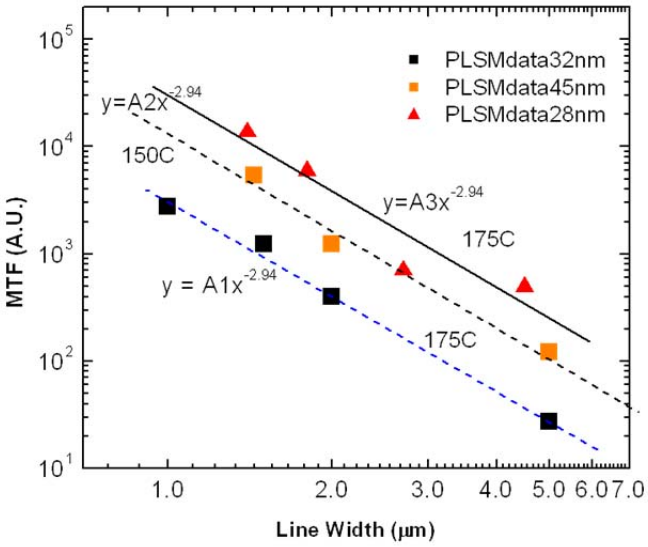


Figure 2 — Power-law relation of MTF vs linewidth

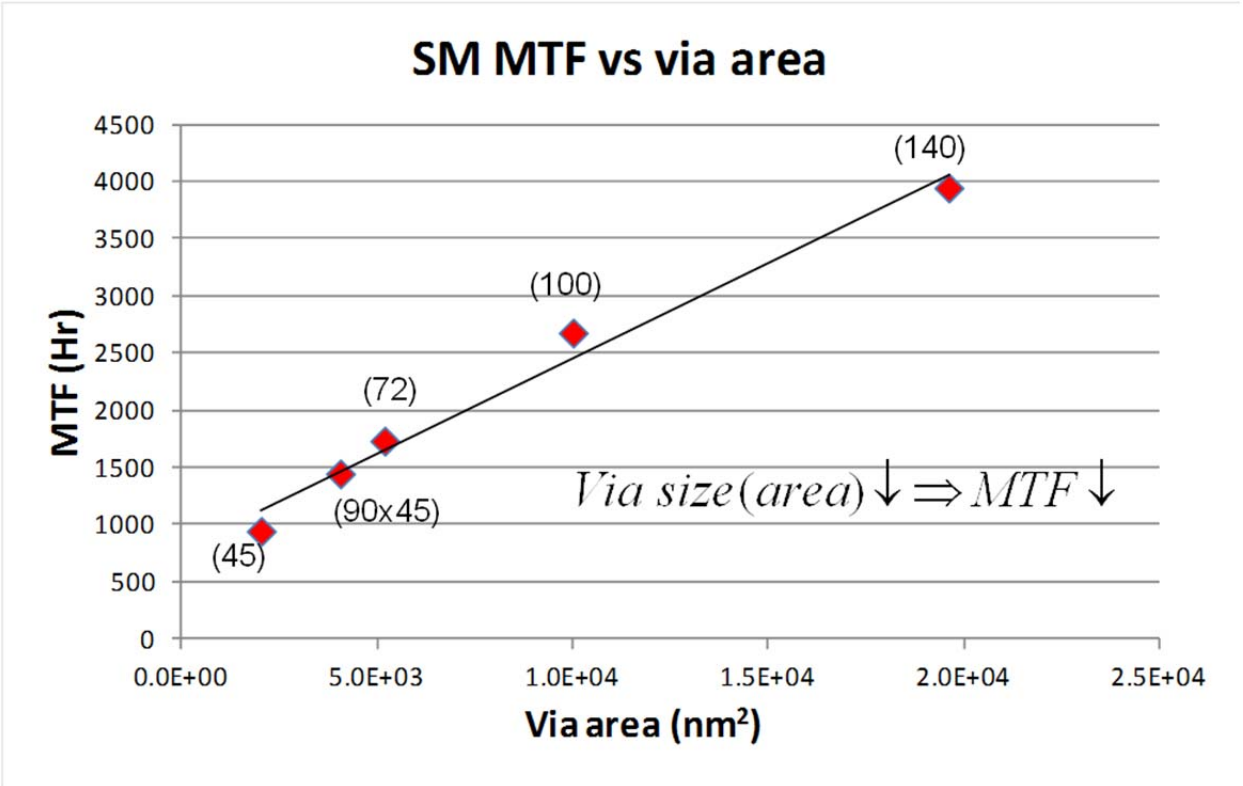
From Figure 2, it is noticeable since the DRC linewidth is << 1 μm, the MTF values of DRC via chains are in years and are unmeasurable during realistic testing timeframe. On the other hand, the MTF values of wide line via chains, e.g., 5 μm via chains, are in the order of 100 h. The new linewidth dependent relation (3) provides the possibility to accelerate the SM tests by using the wide line or wide plate test structures and estimate the DRC SM lifetime quantitatively for the reliability evaluations.

2.3 Geometry linewidth dependence of SIV risk (cont'd)

It has been reported that some of the nose via cases, in which a nose via connected to a wide plate through a minimum width narrow line in highly scaled technology, showed voiding in trenches, vias as well as under the nose vias [12,13]. In those cases, the linewidth dependence of SIV and traditional SM multiple via rules were not effective to protect the circuits from SIV damages. However, the voiding mode can be controlled by optimizing the integration process, e.g., trench barriers, etc. We believe those voiding modes were caused by the extrinsic defects related with non-optimized process especially during the early stage of a highly scaled new technology.

2.4 Via size dependence of SIV risk

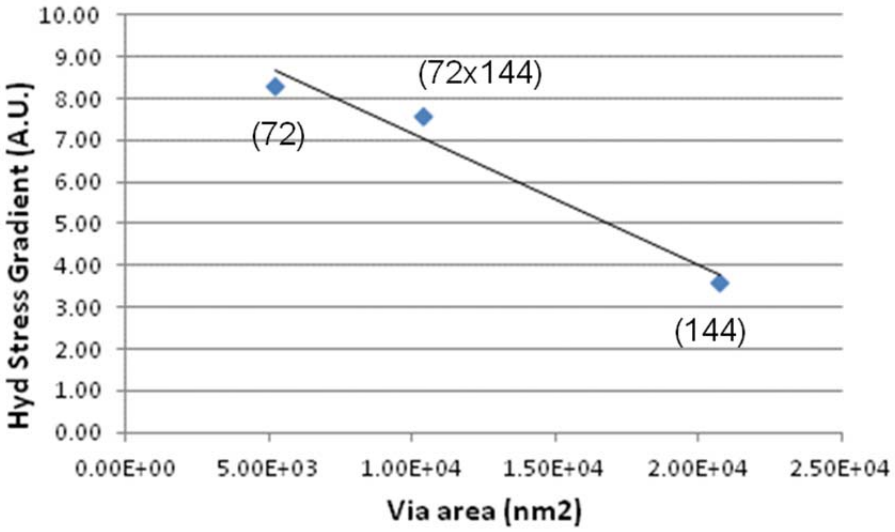
Figure 3 shows the SM MTF values from a group of 100 via chains with different via sizes ranging from 45 nm to 140 nm, including a via bar, measured by PL-SM at 175 ºC, respectively. The SM data show that the MTF values are a linear function of via cross section area. As the via size decreases, the MTF decreases, i.e., the SIV risk increases. This is consistent with the calculation of maximum stress gradient vs via cross session area under a 3D linear elastic model assumption as shown in Figure 4. As Figure 4 shows that a smaller via is related with higher stress gradient and thus resulting in higher SIV risk.



NOTE The via diameters are labeled in brackets in the units of nanometers.

Figure 3 — Median time-to-fail SM data as a function of via sizes

2.4 Via size dependence of SIV risk (cont'd)



NOTE The via diameters are labeled in brackets in the units of nanometers.

Figure 4 — Hydrostatic stress gradient at near room temperatures vs via size (area)

2.5 SIV under multiple vias

The cause of SIV damages can be avoided by using multiple via configurations, in which the additional vias are sacrificed, reducing the stress gradient by non-fatal voiding. The electrical connectivity is maintained by keeping at least one via being undamaged in multiple via configuration.

Figure 5 shows an example of a two-via case (a). The FA images of unstressed vias are shown in (b) and SM stressed vias in (c). We can see the structure is still electrically functioning after the SIV damage of one via occurred. The MTF value can be greatly increased under multiple via configurations. As shown in Figure 8 (d), MTF values from a 5.0 μm via chain were measured under 1- 4 via configurations, respectively. It is shown that the ~10x MTF value increase was observed from 1 via to 4 via cases. The SM multiple via rule method is commonly used today in integrated circuits (ICs) designs to prevent or reduce the SIV risk to the product.

2.5 SIV under multiple vias (cont'd)

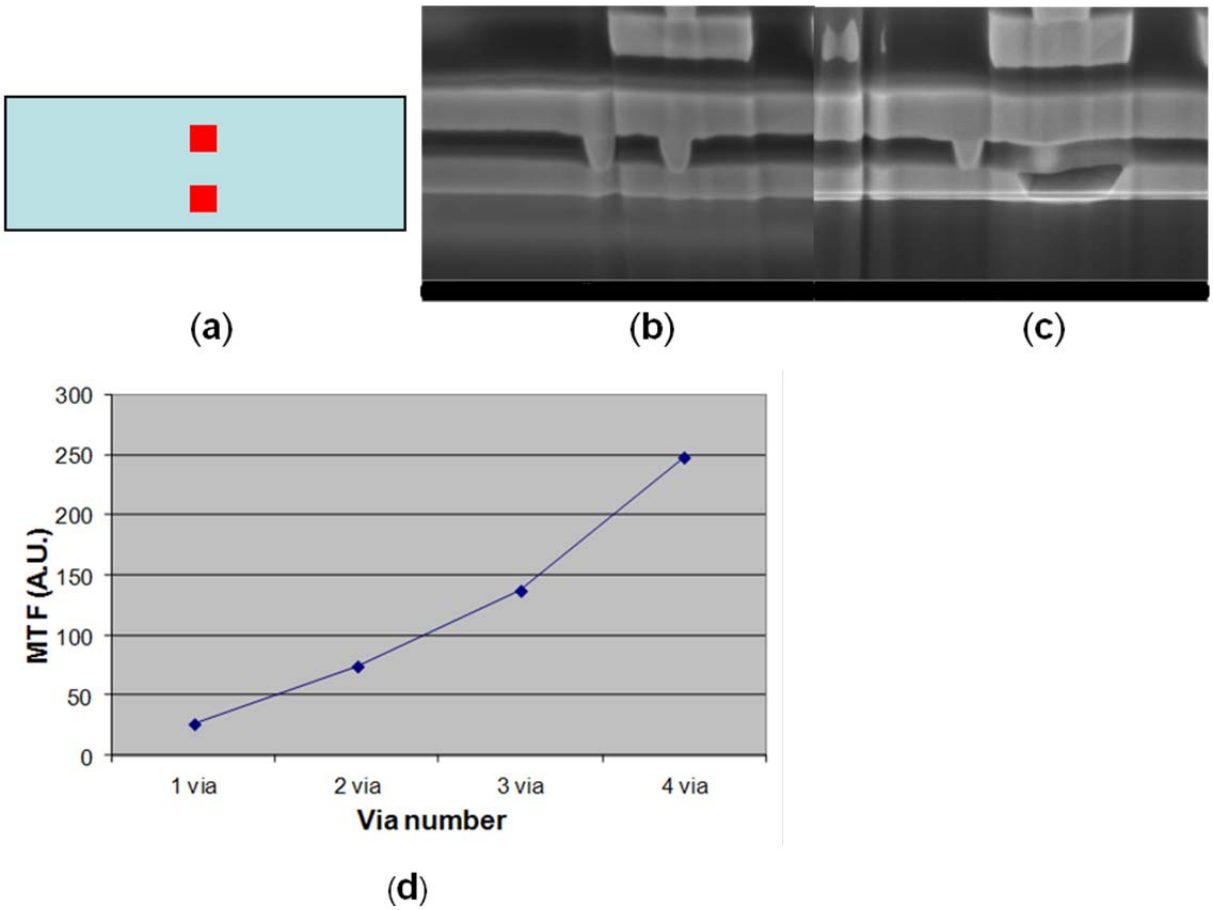
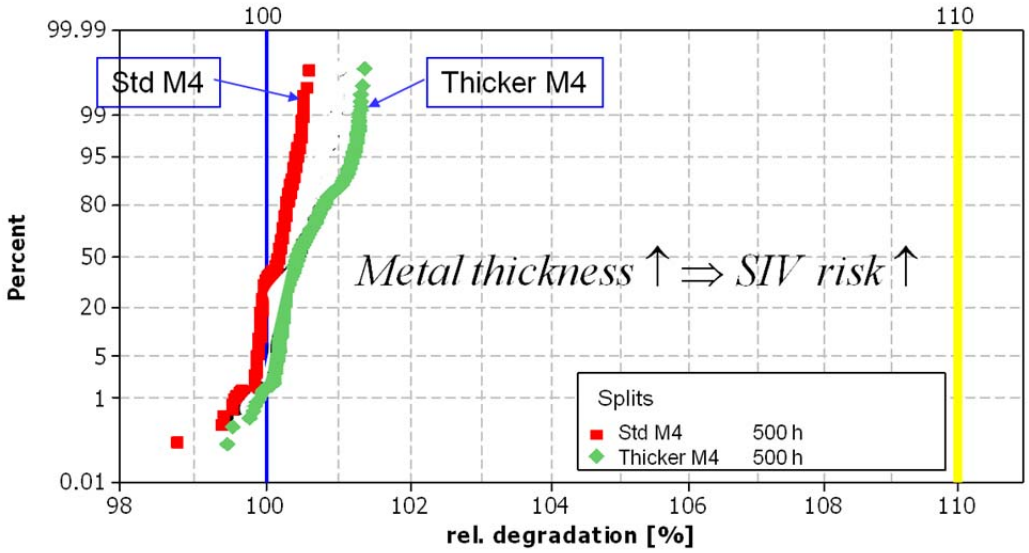


Figure 5 — FA images of two via case and MTF vs multiple via of SM

2.6 Metal thickness dependence of SIV risk

Figure 6 shows the resistance changes vs via chains with different metal thicknesses under SM testing at 175 ºC. The SM data show the thicker the metal the larger the resistance changes. This means that an increase in metal thickness will lead to SIV risk increase.



NOTE "Std M4" (in red) and "thicker M4" (in green) were measured after 500 h testing at 175 ºC.

Figure 6 — Metal thickness vs resistance increase under SM tests

2.7 SM lifetime model

Based on the studies of SIV dependence on both temperature and linewidth, we can combine (1) and (3) into (4) as a SM lifetime model:

$$MTF = A W^{-M} (T_0 - T)^{-N} \exp(E_A / k_B T) \quad (4)$$

where W is the linewidth or plate size, M is the geometry stress component, T_0 is the stress-free temperature, N is the thermal stress component, E_A is the diffusion activation energy, k_B is the Boltzmann constant and A is normalization constant.

Equation (4) is in essence an empirical equation based on SM experimental data and the Creep model assumptions. The SIV driving forces are 1) stress temperature T, and 2) linewidth W. The diffusion term serves as a path for SIV. The establishment of (4) provides us opportunities of making quantitative SIV risk analysis and SM lifetime estimation. Figure 1 shows the ratio of temperature dependent MTF values from 125 ºC to 225 ºC is ~18x for the 5 µm VIM via chains. Figure 2 shows the linewidth dependent MTF ratio from DRC (i.e., 0.18 µm) to 5 µm is ~16400x. It is clear that the linewidth geometry provides much better acceleration for SM testing. We now can apply this equation to design SM reliability qualification methodology to quantitatively meet the design lifetime goals. We can perform the SM tests on DRC and selected wide line test structures and estimate the lifetime of unmeasurable DRC test structures in an accelerated manner.

It should be pointed out that the essence of SIV driving force is the stress gradient. The stress gradient can be generated by absolute stress under stress temperature and geometric configuration including linewidths as shown in (4). In addition, SIV mechanism is also critically related with diffusion mechanism and nucleation site density including T0 defects. Those factors are closely related with Cu interconnect process and are not expressed by separate terms in (4) but their influences are included in components N, M, E_A and A.

The extrinsic defects induced SIV described in 2.3 is not covered by this model and (4). Addressing extrinsic related SIV issues should be explored and appropriately mitigated during process development and accounted for during qualification periods to understand their overall impact

3 Constant temperature aging test method

3.1 Test structures

To test the susceptibility to stress voiding of the technology under evaluation, structures that emphasize each extreme risk of the technology should be designed, evaluated, and used in the test procedure.

Typical SM test structures are in the formats of via chains and single vias. Special considerations have to be carried out to assure that the appropriate test structures are used. The following are the structures that must be used in the evaluation of stress migration reliability:

1. Design rule compliant (DRC) linewidth test structures:

    a. ~100-via chains, both conventional (via-at-end) and the via-in-the-middle (VIM) via chains. Bi-polar or plate-above via and plate-below via types. Modest via numbers of ~100 to a few hundred are recommend to ensure resistance sensitivity for SIV risk detections.

    b. Via chains with larger via numbers such as ~1000 to around 1E5, are used at the individual company's discretion in case of needs for via scaling.

    c. Single Kelvin via structures, VIM type.

2. For test structures, specific dimensions (nose length/width) will correspond to each user's processes and designs. Potential options may range from 10x min to 100x min width or its equivalence (e.g., slotted plates) VIM via chains, for measuring SM margin and estimated SM lifetime within limited testing time.

3.1 Test structures (cont'd)

Figure 7 shows the sketches of test structure formats of (a) conventional via chains (~10 µm interconnect length), (b) via-in-the-middle (VIM) via chains (~10 µm interconnect length), (c) Single Kelvin via (L-shaped), and (d) SM nose via chain structure of plate-below and plate – above via chains. The plate widths of via chains, single Kelvin via and SM nose via chains can be DRC and wide plate widths.

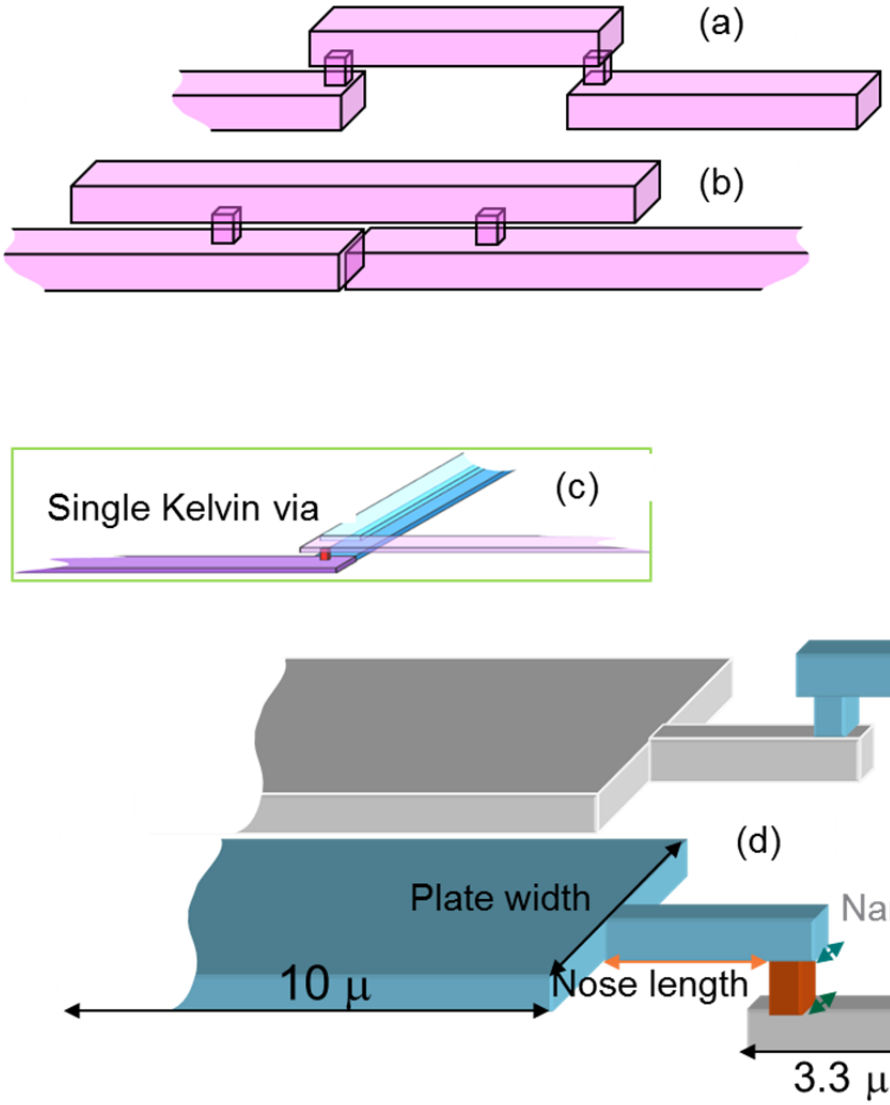


Figure 7 — SM test structure sketches: (a) conventional via chain; (b) via-in-the-middle (VIM) via chain; (c) Single Kelvin via (L-shaped); (d) SM nose via chains.

3.1 Test structures (cont'd)

Due to the nature of stress gradient distribution in via/Cu line configurations [1,4], the sensitivity of exploring the SIV risk can be different for SM test structures with different designs. Figure 8 shows two types of via chains for SM testing in (a) and (b). In (a), a conventional via chain is designed with the vias located near the end of the metal lines. In (b), a via-in-the-middle (VIM) via chain is designed with the vias located in the middle of the metal lines. Due to the via location difference, the stress gradient distributions are quite different, i.e., single side towards the middle of line for (a) and both sides towards both ends of line for (b). The double side stress gradient distributions for VIM via chains in (b) determines that the sensitivity of SIV risk is higher for VIM than conventional via chains.

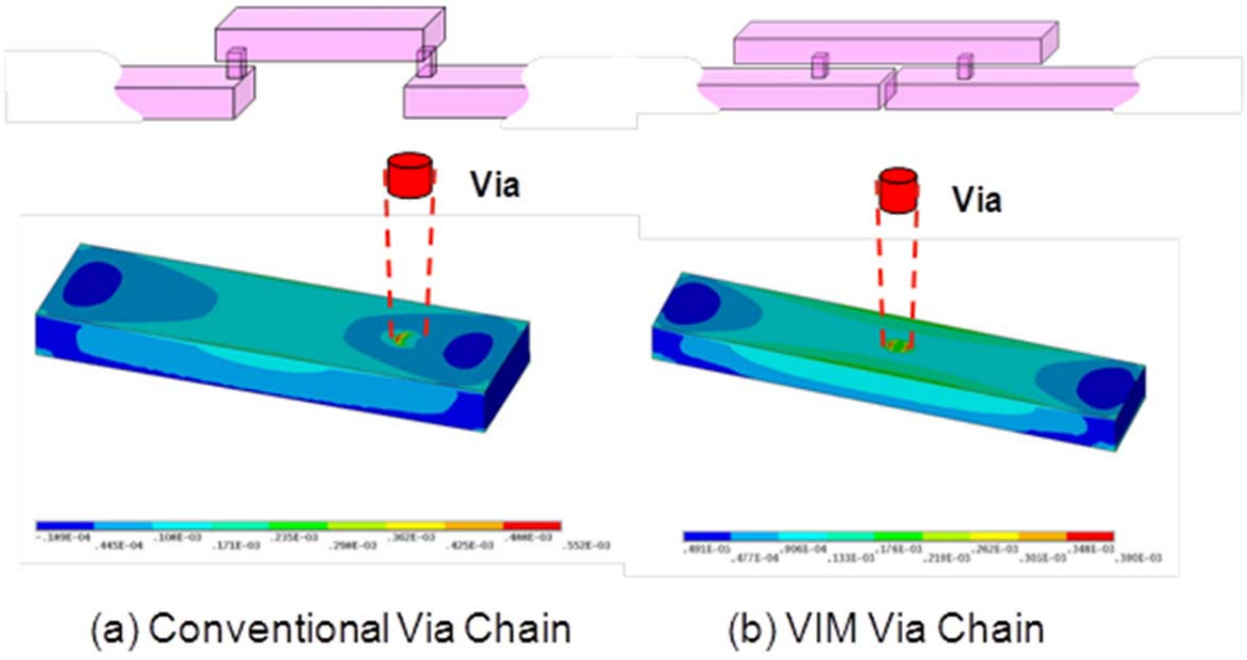


Figure 8 — Stress profile of conventional and VIM via chains

Figure 9 shows the comparison of results between conventional and VIM via chains from both PL-SM and wafer-level (WL) SM tests. PL-SM results show higher time-to-fail (TTF) values for conventional via chains in (a) while WL-SM results in (b) show higher failure percentage for VIM via chains at each readout of 250 h, 500 h, and 750 h, respectively. Both tests were performed at 175 ºC on 5.0 µm width via chains from 28 nm wafers. Both results indicate that the VIM via chains are more sensitive to SIV risk under the same linewidth and testing temperature. This is consistent with the stress gradient distribution shown in Figure 8 and stress analysis studies in [1,4]. It is necessary to point out that in general, most of the via/metal line configurations in ICs products are VIM cases. Therefore, the types of VIM via chains or single via structures are recommended for SM qualification tests.

3.1 Test structures (cont'd)

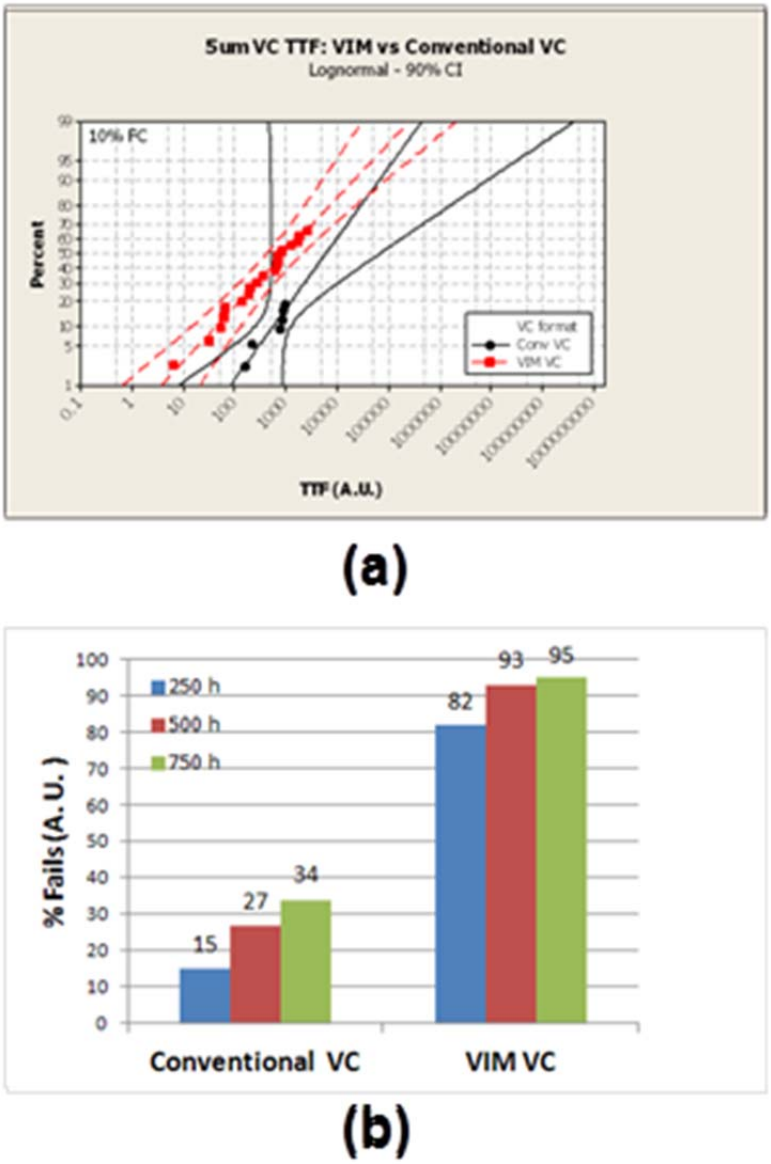


Figure 9 — SM data of conventional and VIM via chains

For SM nose via cases where a narrow extension connecting to a via is attached to a wider plate, the SIV risk of this via is determined by the width of the plate and the distance of the via away from the plate [3]. The application of nose via structures for SIV reliability assessment should correspond to their allowable design rules and technologies. If nose via designs are permissible, then nose via test structures are part of the product-level SIV evaluation for SM quantification. Technologies that do not allow nose via designs would naturally conduct SIV evaluations without nose via test structures. SM in nose via cases are product specifics and it is each individual company's discretion to handle the specifics based on the principle of SM mechanism introduced in this standards.

3.1 Test structures (cont'd)

Additional optional SM test structures for the qualification include (1) stacked co-axial via chains; (2) off-center stacked via chains; (3) mesh type via chains (minimum line widths) with mesh-above and mesh-below the via. The illustrative sketches of those structures are shown in Figure10. Those SM test structures are designed to explore the SIV risk under certain extreme and specific product geometry cases and they are optional choices of each individual company for its SM qualification tests.

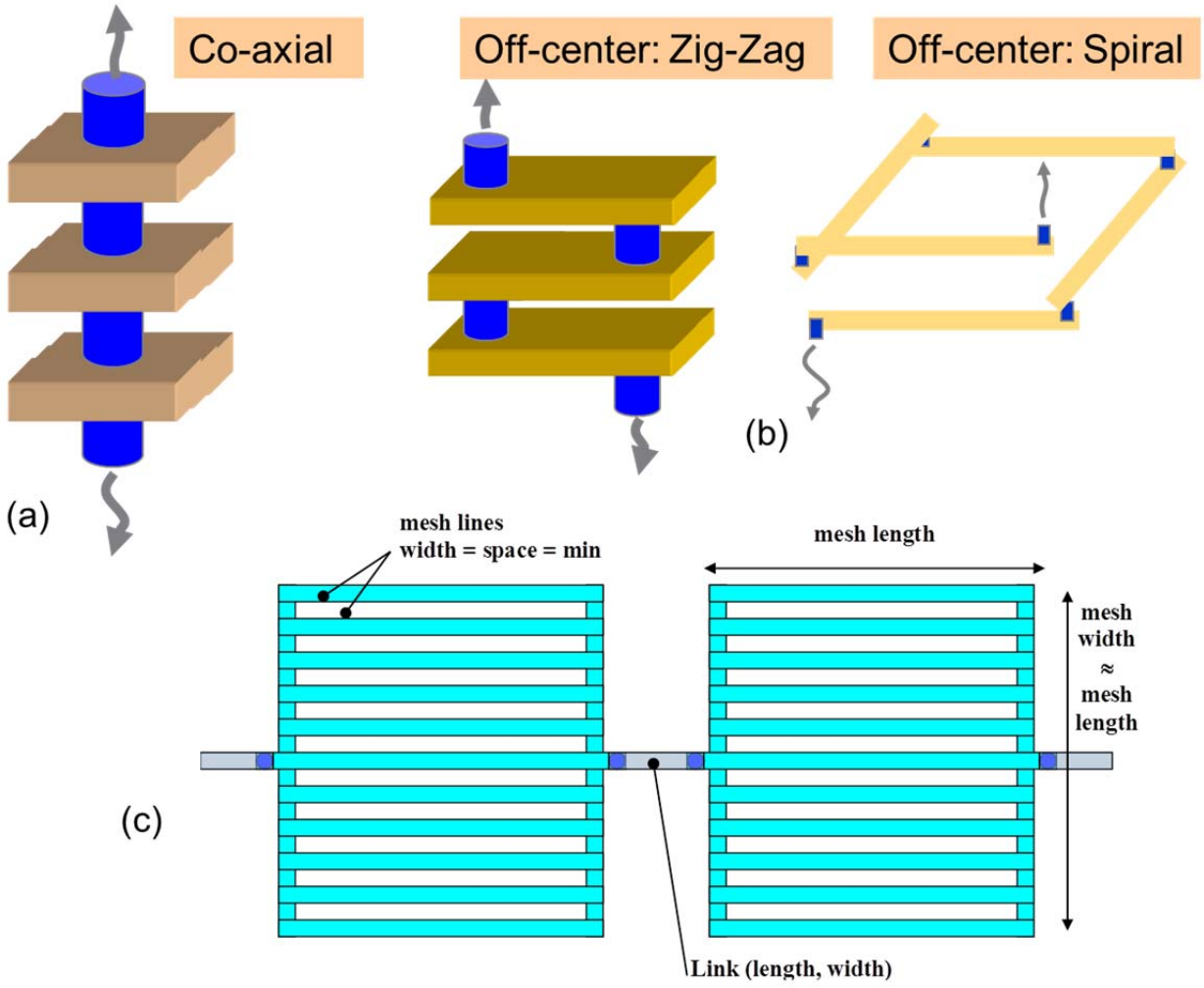


Figure 10 — Illustrative sketches of proposed optional SM test structures: (a) co-axial stacked via chain; (b) two formats of off-center stacked via chain; (c) mesh type via chains (minimum line widths).

3.2 Test temperatures

Based on the temperature dependence described in 2.2, wafer level SM stress temperatures are the following:

1) Selected constant temperatures between 150 ºC to 275 ºC.
2) For each SM tests, minimum three temperatures are required, covering temperature range from low to high, e.g., 150 ºC, 175 ºC, and 225 ºC.

3.3 Test conditions, sample size and measurements

Wafer level tests are recommended for constant Cu stress migration reliability tests due to the following advantages: 1) capable of testing chips throughout the wafer without possible influence introduced by packaging tests, and 2) capable of testing large number of SM test structures from the same wafer which is not possible for packaging tests.

Sample size of the wafer level SM tests:

1) Minimum 3 wafers (i.e., 1 wafer/lot from 3 lots) for each stress temperature, e.g., 150 ºC, 175 ºC, and 225 ºC.
2) Minimum 30-40 die per wafer, per metal level, to be tested.

Additional test temperatures (at least four temperatures is recommended) and wafers may be added for quantitative SM modeling verification and lifetime extrapolations if desired by each individual company.

Test measurement readout:

Resistance value changes of each test structures are monitored on a required schedule. The minimum is readout at 0 h and 1000 h. It is optional to perform additional readout within the 1000 h for better tracking the SM behavior. For example, 0 h, 250 h, 500 h, 750 h, 1000 h.

3.4 Failure criteria

1) Resistance increase (ΔR) for via chains > 10%;
2) Resistance increase (ΔR) for single via > 100%

These are failure criteria for general practice in SM reliability evaluations. Individual company can revise the resistance increase numbers in their special cases if needed.

3.5 Passing criteria

a) Zero DRC test structure fails for all testing temperatures within **1000 h.**

The a) criteria is the traditional method of "zero fails during a fixed time period", which will explore the SIV risk of DRC test structures as well as extrinsic defects during the 1000 h tests. This is a **must-have** passing criterion.

For the purpose of estimating the SM margin and the extrapolation of product SM lifetime, we introduce the 2nd criterion for company to follow. The details of the execution of this b) criterion are based on company's choice on an accelerated method of SM lifetime model (see 2.7).

b) Zero SM fails for selected wide line via chains within a fixed period, e.g., 250 h, 500 h, or shorter, depending on the choices of wide line widths of the test structures. For example, if there is zero 2 μm via chain fail within 500 h at 175 ºC for 32 nm and 28 nm, the product SM lifetime will reach the 10 year goal. The detailed choices of selected line width value and no fail hour period can be determined by each company, based on the SM model described in 2.7.

4 Data to be reported

After completion of the test, the information listed in the following paragraphs should be reported.

4.1 Bake Temperatures

(see 3.2)

4.2 Measurement Intervals

List the cumulative time between the beginning of the test and each resistance readout (see 3.3).

4.3 Failure Criterion

List the criteria used to define failure (e.g., percentage resistance shift, open circuit, etc.) (see 3.4).

4.4 Sample Tested

Describe the sample tested, including the number of wafers, the number of chips per wafer, the macro names and number of structures on each chip (see 3.3 and 3.1).

4.5 Stress Structure

Describe the features of each test structure used, and illustrate with drawings if practical (refer to 3.1).

4.6 Initial Resistance

Plot distribution plots of initial resistance of each test structure (see 3.3).

4.7 Stress Data

Plot the distributions of fractional resistance change versus stress time for each structure and indicate the failure criteria on the plot (see 3.3 and 3.4).

4.8 SM Reliability lifetime

Estimated SM margin and lifetime at use conditions: based on the failure conditions of wide line SM test structures, which are non-DRC. We can estimate the SM reliability lifetime by applying the SM lifetime model in 2.7. As an example, if there are no fails from 2 μm width via chains within 500 h at 175 ºC for 32 nm and 28 nm technology wafers, the SM lifetime will reach 10 year lifetime goal.

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Annex A (informative) Differences between JESD214.01 and JESD214

This annex briefly describes most of the changes made to entries that appear in this standard, JESD214.01, compared to its predecessor, JESD214 (February 2015). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of change
2.4	1st paragraph, 3rd sentence: Changed “decreases” to “increases”. (JC-14.2-17-359)

Standard Improvement Form JEDEC _____

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1. I recommend changes to the following:

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