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RF BIASED LIFE (RFBL) TEST METHOD

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Foreword

A unique application of semiconductor integrated circuits is within a module. Modules are sometimes referred to as a system-in-package (SIP) or hybrid. For the purpose of this document, we define a *module* as an assembly that integrates multiple semiconductor die within one package. Such a module is not restricted to semiconductors – it can also contain passive devices that include components such as resistors, capacitors, inductors, filters, and couplers that are either built-in to the substrate or added as Surface Mount Devices. Another unique aspect of Laminate-based Power Amplifier Module (PAM) is the application of Compound Semiconductors. To further refine the classification of modules, we have specifically selected amplification to be the core function. But amplification is not necessarily the only function. Switching, power control, power detection, signal reception, filtering, and ESD suppression may be other functions performed within a module. Additionally, many of the functions may be employed over various frequencies and at various output power levels – such that these functions are arranged in a parallel fashion within the module. A typical module application is a Power Amplifier Module (PAM) used at or near the "front-end" of a cellular phone or mobile device. PAMs are an enabling component of cell phones that transmit signals with high efficiency, linearity, and reliability in a manner that is yet unmatched by monolithic devices. A typical PAM consists of a substrate, which may be a leadframe material, but is more commonly a ceramic or laminate multi-layer base. Upon the base, the aforementioned die and components are mounted, and all components are encapsulated, using packaging materials, such as an epoxy, most commonly formed by a transfer mold process. Hermetic versions of PAMs utilize ceramic substrates and lids or caps that seal the various components within. Even though similar types of modules have been utilized for semiconductors in the past, the use of Compound Semiconductors, with a laminate substrate, for relatively high power dissipation wireless application at radio frequencies (RF) is seemingly unique.

Introduction

This standard is intended to address one of the unique operational regimes of a PAM: RF bias. DC bias and RF bias are different in many respects. One reference provided evidence that the thermal impact of RF Vs. DC was clearly evident. Specific comparisons between DC bias and RF bias are summarized by the following publication:

[1] Y. Qu, P. Scott, L. Marchut, & M. Ferrara, "An Overview of Reliability Testing Challenges in Integrated Power Amplifier Modules for Wireless Applications," pp 95-109, 2005 ROCS Workshop, Palm Springs, CA., October 30, 2005.

But temperature is not the only consequence of applying RF biasing to an amplifier. The peak voltages and currents are likely to have particular accelerating effects that are different than constant DC bias. Many Power Amplifier Modules (PAMs) employ circuitry for different bands and for different power levels – just how each circuit should be exercised in an RF biased lifetest will be described here.

RF BIASED LIFE (RFBL) TEST METHOD

(From JEDEC BoD Ballot JCB-12-53, formulated under the cognizance of the JC-14.7 Subcommittee on Gallium Arsenide Reliability and Quality Standards, through a JC-14.7 Task Group on a Power Amplifier Module Standard)

1 Scope

This stress method is used to determine the effects of RF bias conditions and temperature on Power Amplifier Modules (PAMs) over time. These conditions are intended to simulate the devices' operating condition in an accelerated way, and they are expected to be applied primarily for device qualification and reliability monitoring.

This method does not attempt to address stressing that would be used to determine acceleration factors for RF driven wear-out. Another form of high temperature bias life using a short duration, popularly known as burn-in, may be used to screen for infant mortality related failures. The applicability and detailed application of burn-in is also outside the scope of this document.

There is a lot of operational space between applying a sine wave on one input and operating a device "*like it runs in a phone*." This method is intended to refine and focus the myriad of biasing options down to a standard that can be applied industry-wide so that users of PAMs can gain confidence that devices successfully completing this test method will exhibit adequate reliability for the anticipated use conditions.

The tests described in this method are capable of stimulating and precipitating anomalous semiconductor device and packaging failures. The objective is to bring out anomalies in an accelerated manner compared to use conditions. Failure Rate projections usually require larger sample sizes than are called out in qualification testing. For guidance on assessing thermal acceleration factors refer to JEP118, Guidelines for GaAs MMIC and FET Life Testing. For guidance on projecting failure rates refer to JESD85, Methods for Calculating Failure Rates in Units of FITs. This method is not aimed at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments, nor does it address 2nd level reliability considerations, which are addressed in JEP150.

The purpose of this test is for use to determine the effects of nominal DC and RF bias conditions and high temperature on Power Amplifier Modules (PAMs) over time. It simulates the devices' operating condition in an accelerated way, and is primarily intended for device qualification testing and reliability monitoring which stresses all of the modules' thermal and electrical failure mechanisms anticipated in typical use.

RF Biased Life (RFBL) is intended to supersede High Temperature Operating Life by providing a superset of aging conditions. RFBL and HTOL are considered exclusive methods in the life test regime. For example, if RFBL is performed, then no other product HTOL will be required. If we define traditional HTOL as a DC test and RFBL as the RF counterpart, then it really becomes a choice for which test best represents field stresses. For some parts with simple architectures, DC stress may adequately represent field conditions. In other cases, RF power may be necessary to truly exercise the product.

2 Applicable documents

Stress-Test Driven Qualification of Power Amplifier Modules (in draft form), Alternate to JESD47

JEP153, *Characterization and Monitoring of Thermal Stress Test Oven Temperatures*

3 Apparatus

The performance of this test requires equipment that is capable of providing the particular thermal and electrical stress conditions to which the test samples will be subjected.

3.1 Circuitry

The circuitry through which the samples will be biased must be designed with several considerations:

3.1.1 Device schematic

The biasing and operating schemes must consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

3.1.2 Power Compliance Limits

As much as possible, the bias circuitry should be designed to limit power dissipation such that, if a sample failure occurs, excessive power will not be applied to other samples in the stress population.

3.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under stress, (e.g., improper or non-uniform heat dissipation).

3.3 Power supplies and signal sources

Instruments (such as DVMs, oscilloscopes, etc.) used to set up and monitor power supplies and signal sources shall be calibrated and have good long-term stability.

3.4 Environmental chamber

The environmental chamber shall be capable of maintaining the specified temperature within a tolerance of ± 5 °C throughout the chamber while parts are loaded and unpowered. Airflow within the chamber or active thermal control on a part-by-part basis shall be uniform enough to ensure that part-to-part thermal variation shall be less than ± 5 °C. Part-to-part uniformity shall be waived if individual sample temperatures are measured, monitored and recorded throughout the aging. JEP153, *Characterization and Monitoring of Thermal Stress Test Oven Temperatures* is recommended to baseline larger chambers.

4 Terms and Definitions

4.1 Maximum operating voltage

The maximum sustained supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

4.2 Absolute maximum rated voltage

The maximum instantaneous voltage that may be applied to a device, beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

4.3 Absolute maximum rated hot spot temperature

The maximum hot spot temperature of a module, beyond which damage (latent or otherwise) may occur, is frequently specified by device manufacturers for a specific device and/or technology. The hot spot refers to the hottest element within any component or die within the module. The hot spot is typically a transistor junction, channel, or power dissipating element.

NOTE Manufacturers may also specify maximum case temperatures for specific packages if the hot spot to case differential is known.

4.4 Absolute maximum rated RF input power

The maximum applied RF signal to the module input, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

5 Procedure

The sample devices shall be subjected to the specified or selected stress conditions for the time and temperature required. It is desirable to perform RF stressing on the entire module. However, if the fully assembled module cannot be stressed, then RF lifetesting of the individual subcomponents can be considered. If subcomponents are RF stressed, then measures must be taken to ensure the subassemblies represent the finished product as closely as possible. For example, the same thermal resistance, same junction temperature, and other similar conditions must be applied.

5.1 Stress duration

The bias life duration is intended to meet or exceed an equivalent field lifetime under use conditions. The duration is established based on the acceleration of the stress (see each specific failure mechanism - JEP122 for example). The stress duration is determined by the specified qualification requirements (example, JESD 47) or the applicable procurement document. Interim measurements may be performed as necessary per restrictions in clause 7.

5.1 Stress duration (cont'd)

Without specific guidelines for a product, family, or technology expectation, the minimum duration would be 500 hours, and the default duration would be 1,000 hours. The combination of stress conditions and duration should be chosen so that the RFBL test represents an accelerated version of the expected product lifetime.

For example if the expected product lifetime is 5 years then the stress conditions should be chosen so that the minimum duration is determined by the following equation:

$$\text{Test Duration (hours)} = \frac{\text{(5 years) x (365.25 days/year) x (24 hours/day) = 43,830 hours}}{\text{AF}}$$

Here the Acceleration Factor (AF) is the acceleration factor as discussed in 5.2.

5.2 Acceleration factor

Many of the parameters used for biasing the device during the RFBL test can be used to stress the device beyond its normal use condition and contribute to the acceleration factor of the test. Common parameters used for PA modules include ambient temperature, current, voltage and duty cycle. These factors should be chosen to be small enough to avoid device wear out during the duration of the test or inducing failure modes or mechanisms not expected during normal device operation. Each of these factors is discussed in more detail in the sections which follow.

In this case the acceleration factor (AF) is given as:

$$AF = \left(\frac{I_{Stress}}{I_{Use}} \right)^{N} \times \exp\left(\frac{E_a}{k} \right) \times \left(\frac{1}{T_{Use}} - \frac{1}{T_{Stress}} \right) \frac{DutyCycle_{Stress}}{DutyCycle_{Use}}$$

N is the Black's Law factor for current acceleration, typically between 1 and 3. T is the junction temperature in Kelvin with contributions due both to ambient temperature and dissipated power. k is Boltzmann's constant. E_a is the activation energy for extrinsic or random failures. If the activation energy is not known a nominal value of 0.7 eV is suggested for easy comparison purposes with other results. The applied voltage is not included in the equation above, both voltage and current contribute to the junction temperature by increasing the dissipated power.

Other acceleration models may be used if they are shown to accurately represent the technology used and expected application conditions for the product under test.

5.3 Stress conditions

The stress condition shall be applied continuously (except during interim measurement periods). The time spent elevating the chamber to accelerated conditions, reducing chamber conditions to room ambient, and conducting the interim measurements shall not be considered a portion of the total specified test duration.

5.3.1 Ambient temperature

Unless otherwise specified, the ambient temperature and bias for high temperature stress shall be adjusted to result in a minimum hot spot temperature of the devices under stress high enough so that the accelerating condition requirement in section 5.2 is met but below any temperature where a failure mechanism not expected during normal use conditions becomes activated. One particular concern for overmolded modules is the glass transition temperature of the mold compound.

As a minimum requirement, chamber temperature must be set and recorded during stressing. If set or measured, package temperature, die temperature, and/or hotspot temperatures are beneficial and should be recorded for each sample or location. Estimates of the relationships of hot spot temperatures to any other empirical temperatures should be recorded and included as part of the degradation analysis.

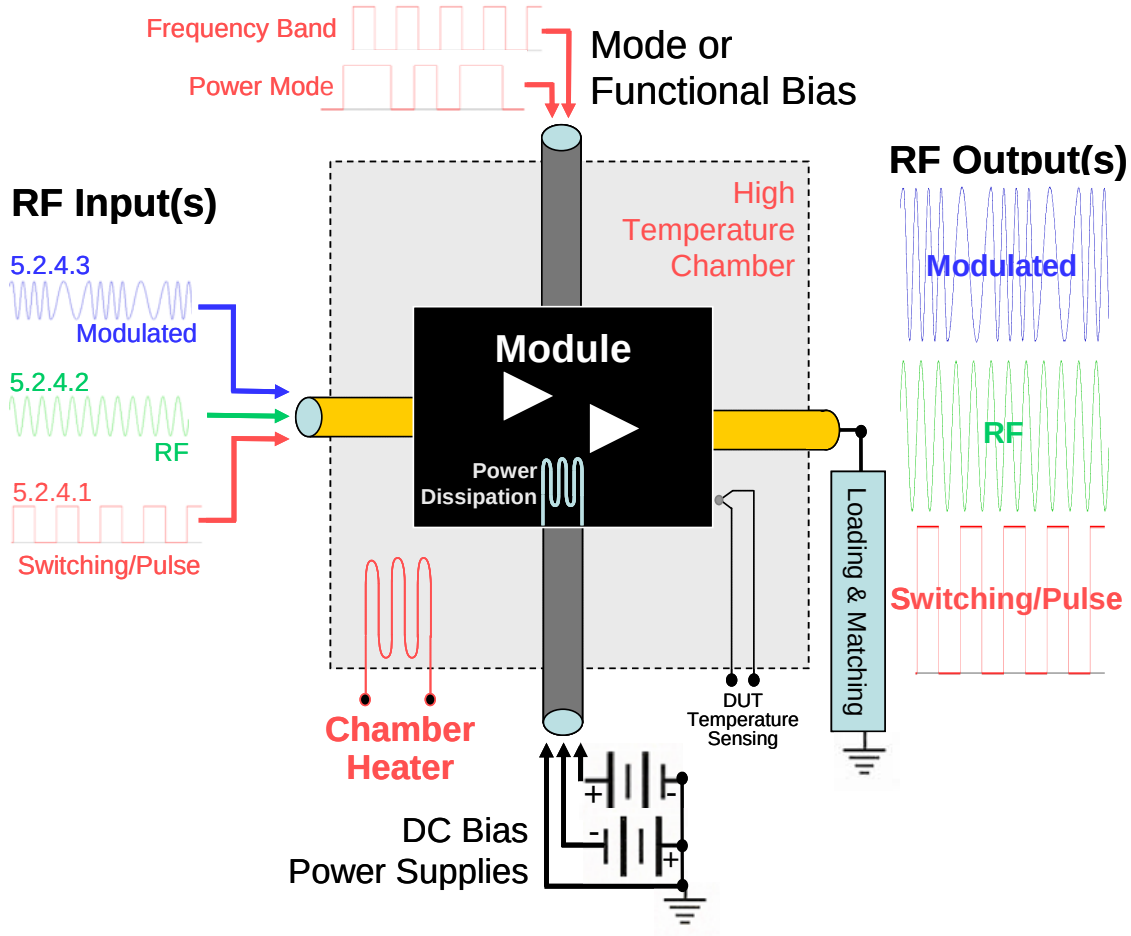

Figure 1 — Bias and Stress Considerations for RFBL

5.3 Stress conditions (cont'd)

5.3.2 Operating DC voltage

Unless otherwise specified, the operating voltage should be the maximum operating voltage specified for the device unless the conditions of 5.3.1 cannot be met. A higher voltage is permitted in order to obtain lifetime acceleration from voltage as well as temperature; this voltage must not exceed the absolute maximum rated voltage for the device, including guard-banding, and must be agreed upon by the device manufacturer.

5.3.3 Mode bias or functional dynamic bias

Unless otherwise specified, the Module is expected to exercise all of the operational modes anticipated in normal use. For example, all bands and all power levels should be cycled during the life test using dynamic or pulsed signals on the Module. Periodicity of the mode switching should approach the dynamics of operational expectations, if possible. If all of the operational modes cannot be induced and stimulated, then preference to the highest stress mode should be selected. Highest stress is to be determined by using the following priorities:

1) highest power dissipation, then
2) the highest voltage, then
3) the maximum number of internal nodes available to RF stimulus (see 5.3.4).

Care must be taken not to exceed maximum voltage fields, current densities, power dissipation, or induce prohibited truth table logic conditions.

Testing all non-amplified RF pathways is desirable but not always possible. Stressing all switch legs may not be realistic, so representative pathways may have to be selected. An assumption is that stress will be maintained for 1,000 hour duration, so any switching of circuitry will result in less overall stress time for each section that is sharing signals.

5.3.4 RF biasing configurations

Biasing configurations involving the signal path through the PAM may be: 1) switching stress (dynamic or pulsed), 2) operating stress (Radio Frequency), or 3) modulated stress (RF and duty cycle combination). Rated Duty Cycle should be demonstrated if possible. Modulation scheme should also be considered. It may not be possible to reproduce exact duty cycle/ modulation schemes in RFBL – if not, then appropriate measures should be taken to ensure maximum junction/channel temperature is reproduced. Depending upon the biasing configuration, supply and mode bias input voltages may be grounded or raised to a maximum potential chosen to ensure a stressing temperature not higher than the maximum-rated junction temperature. Device outputs may be unloaded or loaded, to achieve the specified output power level. If a device has a thermal shutdown feature it shall not be biased in a manner that could cause the device to go into thermal shutdown. If dynamic bias is not applied to the signal path, then HTOL should be used instead of RFBL.

5.3 Stress conditions (cont'd)

5.3.4 RF biasing configurations (cont'd)

The goal for RF bias is use the maximum possible level expected for sustained operation. Care is necessary in applying an RF bias level when the ambient temperature is raised above datasheet conditions (e.g., 125 ºC). If the RF drive level is set prior to raising the ambient temperature, then the RF drive may impact the circuit differently at the high temperature of the life test. Therefore, the RF level should be set according to best known practices for the highest stress conditions and then carefully monitored as the temperature is elevated up to levels when oven stabilization is achieved during RFBL. With the primary goal to duplicate die temperature at worst case datasheet conditions, the shifting of RF power levels away (lower) from their maximum settings may be necessary to elevate the oven temperature to the maximum for the duration of the RFBL stress.

5.3.4.1 Switching stress bias

The Switching stress bias is defined as a pseudo RF condition. If actual RF signals cannot be applied, then low frequency or "digital" signals or pulsed signals may be substituted which exercise the signal path. The intent is to exercise the major power handling junctions of the device samples. The devices may be operated in either an alternating or a pulsed forward bias mode. Switched operation is used to stress the devices at, or near, maximum-rated current levels. The particular bias conditions should be determined to bias the maximum number of the solid state junctions in the device. Typically, several input parameters may be adjusted to control internal power dissipation. These include: supply voltages, mode biasing frequencies and signals, etc that may be operated even outside their specified values, but resulting in predictable and nondestructive behavior of the devices under stress. The particular bias conditions should be determined to bias the maximum number of potential operating nodes in the device. The switched stress test is typically applied on power amplifiers that are unstable or have other difficulties in meeting any maximum rated conditions at high temperature.

5.3.4.2 RF stress bias

The RF stress is configured to bias the operating nodes of the device samples at typically expected RF frequencies and power levels. The devices are operated in a dynamic operating mode using a Continuous Wave RF bias applied to the signal path. Typically, all other device input parameters may be adjusted to control internal power dissipation. These include: supply voltages, mode biasing frequencies, and all other control pins, that may be operated even outside their specified values, but resulting in predictable and nondestructive behavior of the devices under stress. The particular bias conditions should be determined to bias the maximum number of potential operating nodes in the device. The RF bias is applied on at least one signal path through the PAM. Preferably, all signal paths are subjected to the RF input and the mode bias will alternate each of the active paths through normal operation. The RF stress bias test is intended to exercise the PAM in a manner that is representative of the cyclical signal anticipated in normal operation.

Actual RF biasing will best be determined on a case by case basis. It is possible that all of the operational permutations may not be evoked, but the conditions covering highest risks are to be applied. The choice of conditions must be logical and accepted by supplier and customer alike. Exercising as many different frequency bands of operation as possible is recommended since these bands will exclusively stress different circuits and in some cases entirely different die, as the different bands may occupy entirely different swaths of circuitry. Testing all switch legs may not be realistic, so representative pathways may need to be selected.

5.3 Stress conditions (cont'd)

5.3.4 RF biasing configurations (cont'd)

5.3.4.3 Modulated stress bias

The Modulated stress bias is intended to operate the PAM in the most complex manner that emulates actual operation. The RF modulation scheme is an important consideration to obtain the truest form of emulation. It may not be possible to reproduce exact duty modulation schemes in RFBL. If not, then simple RF bias (5.3.4.2) or switching stress bias (5.3.4.1) should be considered. The modulated bias should not only duplicate the radio frequency aspects through the signal path, but also the expected mode biasing dynamics that will exercise all frequency paths and power levels. The inputs include supply voltages, mode biasing frequencies, and all other control pins, that may be operated even outside their specified values, but resulting in predictable and nondestructive behavior of the devices under stress. The particular bias conditions should be determined to bias the maximum number of potential operating nodes in the device. The modulated RF bias is applied on at least one signal path through the PAM. Preferably, all signal paths are subjected to the RF input and the mode bias will alternate each of the active paths through normal operation. The RF stress bias test is intended to exercise the PAM in a manner that is closest to duplicating the cyclical signal anticipated in normal operation. Care should be used to minimize the external radiated output of the modulated RF signals so that RF interference is contained within the stress apparatus.

5.3.5 Loading and matching

Loading and mismatching of RF outputs can have a profound effect on power dissipation and electrical signal levels resulting within the module. The thermal impacts of loading should be evaluated during characterization and this will need to be part of the margin required for each part. Mis-matched output conditions are an important consideration, but the load stress is a lower priority behind applied RF power application levels and thermal acceleration. It is recommended that samples should be isolated so that RF changes in one sample do not affect the RF inputs to other adjacent samples.

As outlined in 5.3.4, the goal for RF bias is use the maximum possible level expected for sustained operation. However, just as much care is necessary in selecting the appropriate loading as in applying an RF bias input level. When the ambient temperature and RF input levels are expected to be raised above datasheet conditions, then the worst case loading may not be possible to attain. Therefore, the loading may need to be set at nominal levels (approximately 1:1) to ensure that maximum temperatures and maximum RF drive levels can be applied for the duration of the life test. In order to achieve any additional stress at particular mismatch loading conditions, then the ramp of thermal stress should be carefully monitored as the temperature is elevated up to levels when oven stabilization is reached, including steady application of all of the appropriate thermal and RF drive maximums under a mismatched load.

Regardless of the loading, the operational conditions of the biasing and thermal stresses need to be identified.

5.3 Stress conditions (cont'd)

5.3.6 Combined Stresses

Ideally the RF-HTOL test would be run at a worst case combination of operating voltage, output power and duty cycle at an ambient temperature of 125 °C. However the combination of stresses may not represent a real world operating condition of the device. For example for higher duty cycles the PA is often run at a lower output power. The combination of stresses plus elevated temperature may also introduce failure modes not expected during normal device operation. To avoid this it may be necessary to reduce one or more of the stresses. The acceleration factor for the RF-HTOL test can be estimated as described in 5.2 to evaluate the effectiveness of the combined stresses used.

6 Cool-down

Devices on high temperature stress shall be cooled to 55 °C or lower before removing the bias. Cooling under bias is not required for a PAM that utilizes technologies that are immune to thermally induced bias effects. If biased cool-down is required, all specified electrical measurements shall be completed prior to any reheating of the devices, except for interim measurements subject to restrictions of clause 7.

Caution: As alluded to in 5.3.4, RF bias will behave differently at high temperature than at low temperature. If full RF bias is left intact during cool down, current and temperature may elevate substantially – possibly to levels which are unrealistic. Care should be taken to prevent overstress of any condition if a biased cool-down is utilized.

NOTE Bias refers to application of voltage to power pins.

7 Samples

Devices for evaluation are expected to represent standard production material in every way possible. Generally, no preconditioning or burn-in shall be applied to samples unless it is part of a normal production flow that is applied to all populations for the expected product lifetime. RFBL is expected to be among the longest duration stresses of a qualification test suite. Completing preconditioning would further extend the duration and unduly delay qualification testing.

If package-related degradation is anticipated, the package integrity should be investigated by other tests which have stress intended for package-related mechanisms.

Samples for RFBL should be picked in the same way samples for customers are picked. Ideally these should be random samples straight out of the production process as they would be shipped to the customer.

8 Measurements

The measurements specified in the applicable life test specification shall be made initially, at the end of each interim period, and at the conclusion of the life test. Interim, monitoring, and final measurements may include data taken during high temperature stress aging. However, measurements at elevated temperatures shall only be performed after completion of specified room (and lower) temperature test measurements.

8.1 Stress pauses

After interim measurement pauses, bias shall be applied to the parts before heat is applied to the chamber, or within ten minutes of loading the final parts into a hot chamber. At each interval, electrical testing shall be completed as soon as possible and no longer than 96 hours after removal of bias from devices. If the availability of test equipment or other factors make meeting this requirement difficult, bias must be maintained on the devices either by extending the RF Bias Life Stress or keeping the devices under bias at room temperature until this 96 hour window can be met. If the devices have been removed from bias and the 96 hour window is exceeded, the stress must be resumed for the duration specified in Table 1 prior to completion of the measurements. After an interim measurement, the stress shall be continued from the point of interruption. This and the high temperature testing restrictions of this clause need not be met if verification data for a given technology is provided.

Table 1 — Additional Stress Requirements for parts not tested within 96 hours

Hours by which 96 hour window has been exceeded	> 0 but ≤ 168	> 168 but ≤ 336	> 336 but ≤ 504	Other
Additional stress hours required prior to performing electrical test	24	48	72	24 hours for each 168 hours (week) by which the 96 hour window has been exceeded

9 Failure criteria

A device is most clearly defined as a failure if it does not meet the requirements of the applicable procurement document (the module specification). If possible, parametric changes in device performance should be utilized to assess module degradation and determine fallout. In order to assess individual sample parametric degradation, samples shall be measured on a part-by-part basis. Typically, changes exceeding 1 dB and/or 10% can be considered to be significant.

10 Summary

The following items shall be specified in the applicable life test specification:

a) Special preconditioning, when applicable.

b) Stress temperature (chamber ambient, case temperature, hot spot temperature – whichever is most directly monitored)

c) Stress duration in hours.

d) Stress mounting, if special instructions are needed.

e) Stress condition and stress circuit schematic.

f) Sample size and acceptance number.

g) Time to complete endpoint measurements, if other than specified in clause 8.

h) Operating modes of DC bias, mode bias, RF bias, and loading.

i) Interim read points, if required.

j) Maximum hot spot temperature (measured, modeled, or otherwise estimated) during stress.

k) Verification data if cool-down under bias is not performed.

l) Failure criteria definition if any criterion is used besides the module data sheet.

Standard Improvement Form JEDEC JESD226

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1. I recommend changes to the following:

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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