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Reliability Qualification of Power Amplifier Modules

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RELIABILITY QUALIFICATION OF POWER AMPLIFIER MODULES

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Foreword

A unique application of semiconductor integrated circuits is within a module. Modules are sometimes referred to as a system-in-package (SIP) or hybrid. For the purpose of this document, we define a *module* as an assembly that integrates multiple semiconductor die within one package. Such a module is not restricted to semiconductors – it can also contain passive devices that include components such as resistors, capacitors, inductors, filters, and couplers that are either built-in to the substrate or added as Surface Mount Devices. Another unique aspect of a Laminate-based Power Amplifier Module (PAM) is the application of Compound Semiconductors. To further refine the classification of modules, we have specifically selected amplification to be the core function. But amplification is not necessarily the only function. Switching, power control, power detection, signal reception, filtering, and ESD suppression may be other functions performed within a module. Additionally, many of the functions may be employed over various frequencies and at various output power levels – such that these functions are arranged in a parallel fashion within the module. A typical module application is a Power Amplifier Module (PAM) used at or near the "front-end" of a cellular phone or mobile device. PAMs are an enabling component of cell phones that transmit signals with high efficiency, linearity, and reliability in a manner that is yet unmatched by monolithic devices. A typical PAM consists of a substrate, which may be a leadframe material, but is more commonly a ceramic or laminate multi-layer base. Upon the base, the aforementioned die and components are mounted, and all components are encapsulated, using packaging materials, such as an epoxy, most commonly formed by a transfer mold process. Hermetic versions of PAMs utilize ceramic substrates and lids or caps that seal the various components within. Even though similar types of modules have been utilized for semiconductors in the past, the use of Compound Semiconductors, with a laminate substrate, for relatively high power dissipation wireless application at radio frequencies (RF) is seemingly unique.

Introduction

This standard is intended to identify a core set of qualification tests that apply specifically for Power Amplifier Modules and their primary application in mobile devices such as cellular phones.

There is a substantial amount of confusion and inefficiency in module reliability testing that is driven by:

a) frequent attempts to apply silicon standards to compound semiconductor modules, and

b) lack of ability to steer customers away from the silicon oriented standards that have dominated the industry for years.

This standard is intended to describe specific stresses and failure mechanisms that are specific to compound semiconductors and power amplifier modules. It is intended to establish more meaningful and efficient qualification testing.

RELIABILITY QUALIFICATION OF POWER AMPLIFIER MODULES

(From JEDEC Board Ballot JCB-14-09, formulated under the cognizance of the JC-14.7 Task Group on a Power Amplifier Module Standard)

1 Scope

This standard describes a baseline set of acceptance tests for use in qualifying power amplifier modules as an individual new product, a product family, or as products in a process which is being changed. These tests are capable of stimulating and precipitating semiconductor device, internal component, laminate, and packaging failures. The objective is to precipitate failures in an accelerated manner compared to use conditions. Failure rate projections usually require larger sample sizes than are called out in qualification testing and durations or stresses which would exacerbate normal wearout. For guidance on projecting failure rates, refer to JESD85 *Methods for Calculating Failure Rates in Units of FITs*. This qualification standard is not aimed at extreme use conditions such as military applications, automotive under-the-hood applications, or uncontrolled avionics environments, nor does it address 2nd level reliability considerations, which are addressed in JEP150.

This set of tests should not be used indiscriminately. Each qualification project should be examined for:

a) Any potential new and unique failure mechanisms.

b) Any situations where these tests/conditions may induce invalid or overstress failures.

If it is known or suspected that failures either are due to new mechanisms or are uniquely induced by the severity of the test conditions, then the application of the test condition as stated is not recommended. Alternatively, new mechanisms or uniquely problematic stress levels should be addressed by building an understanding of the mechanism and its behavior with respect to accelerated stress conditions (Ref. JESD91 *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms.*)

Another alternative qualification method is described in JESD94 *Application Specific Qualification using Knowledge Based Test Methodology*. This technique involves establishing the (worst case) use conditions and tailoring the stress methods, stress levels, and durations to match the use conditions.

Since the assembly is considered an integral part of the power amplifier module, this standard includes the applicable package-related stresses. However, if special consideration of assembly-level effects is necessary, then guidance from JEP150, Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components, is recommended.

2 Reference documents

J-STD-020, Joint IPC/JEDEC Standard, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices.*

JP-001, *Foundry Process Qualification Guidelines* (Wafer Fabrication Manufacturing Sites).

JESD22 Series, *Reliability Test Methods for Packaged Devices*

JESD46, *Guidelines for User Notification of Product/process Changes by Semiconductor Suppliers*.

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*.

JESD69, *Information Requirements for the Qualification of Silicon Devices*.

JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components*.

JESD78, *IC Latch-Up Test*.

JESD85, *Methods for Calculating Failure Rates in Units of FITs.*

JESD86, *Electrical Parameters Assessment*.

JESD94, *Application Specific Qualification using Knowledge Based Test Methodology*.

JESD91, *Methods for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JEP122, *Failure Mechanisms and Models for Semiconductor Devices*.

JEP150, *Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components*.

JESD226, RFBL – Test Method for RF Biased Lifetesting

3 General requirements

3.1 Objective

The objective of this procedure is to ensure that the power amplifier module to be qualified meets a generally accepted set of stress test driven qualification requirements. Qualification is aimed at components used in commercial or industrial operating environments.

3.2 Qualification family

While this specification may be used to qualify an individual component, it is designed to also qualify a family of similar components utilizing the same fabrication process, design rules, and similar circuits. The family qualification may also be applied to a package family where the construction is the same and only the size and number of leads differs. Interactive effects of the semiconductor and package shall be considered in applying family designations.

3.3 Lot requirements

Test samples shall comprise representative samples from the qualification family. Manufacturing variability and its impact on reliability shall be assessed. Where applicable, the test samples will be composed of approximately equal numbers from at least three (3) nonconsecutive lots. Other appropriate means may be used to evaluate manufacturing variability. Sample size and pass/fail requirements are listed in Table 1 and Table 2. Table A and Table B give guidance on translating pass/fail requirements to larger sample sizes.

3.3 Lot requirements (cont'd)

ELFR requirements shall be assessed at a 60% confidence level as shown in Table B. If a single unique and expensive component is to be qualified, a reduced sample size qualification may be performed using 1/3 the sample size listed in the qualification tables.

3.4 Production requirements

All test samples shall be fabricated and assembled in the same production site and with the same production process for which the device and qualification family will be manufactured in production. Samples need to be processed through the full production process including subcomponent testing, probe, handling, test, and any production screening operations.

3.5 Reusability of test samples

Devices that have been used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used in destructive qualification tests may not be used in subsequent qualification stresses except for engineering analysis. Non-destructive qualification tests are: Early Life Failure Rate, Electrical Parameters Assessment, External Visual, and Physical Dimensions.

3.6 Definition of electrical test failure after stressing

Post-stress electrical failures are defined as those devices not meeting the individual device specification or other criteria specific to the environmental stress. If the cause of failure is due to causes unrelated to the test conditions, the failure shall be discounted with a detailed explanation. All samples must be accounted for.

3.7 Required stress tests for qualification

Table 1 and Table 2 list the qualification requirements for new products. Power supply voltage for biased reliability stresses should be at maximum voltage as defined in the device datasheet as the maximum specified power supply operating voltage, usually the maximum power supply voltage is 5% to 10% higher than the nominal voltage. Some tests such as HTOL may allow for higher voltages to gain additional acceleration of stress time. JEP122 can provide guidance for accelerating common failure mechanisms. Table 2 lists the required stresses for a qualification family or category of change. Interactive effects from the unchanged aspects of both the semiconductors and packaging must be assessed.

3.8 Pass/Fail criteria

Passing all appropriate qualification tests specified in Table 1 and Table 2, either by performing the test, showing equivalent data with a larger sample size, or demonstrating acceptable generic data (using an equivalent total percent defective at a 90% confidence limit for the total required lot and sample size), qualifies the device per this document. Generic data and larger sample sizes may be employed based upon a Chi Squared distribution using a total percent defective at a 90% confidence limit for the total required lot and sample size. Statistical definitions are defined in MIL-PRF 38535. (see www.dscc.dla.mil/Programs/MilSpec/).

The minimum number of samples for a given defect level can be approximated by the formula:

$$N >= 0.5\,[X^2\,(2C+2,\,0.1)]\,[1/LTPD - 0.5] + C$$

where C = accept #,
N = Minimum Sample Size,
X^2 = the Chi Squared distribution value for a 90% CL, and
LTPD = the desired 90% confidence defect level.

JESD47, Table A is based upon this formula.

3.8 Pass/Fail criteria (cont'd)

Table A — Sample Sizes for LTPD at 90% Confidence

Acceptance Number C	LTPD = Lot Tolerance Percent Defective								
	20	**10**	**7**	**5**	**3**	**2**	**1**	**0.5**	**0.1**
0	11	22	32	45	76	114	230	461	2303
1	18	38	55	77	129	194	389	778	3891
2	25	53	76	106	177	266	532	1065	5223
3	32	67	96	134	223	334	668	1337	6881
4	38	80	115	160	267	400	800	1599	7994

EXAMPLE: Using generic data for HTOL with a requirement of 0 rejects from 230 samples. If 700 samples of generic data are available, the maximum number of failures that will meet the qualification test requirement is 3 failures from the LTPD=1 column.

4 Qualification and requalification

4.1 Qualification of a new device

New or redesigned products (die revisions) manufactured in a currently qualified qualification family may be qualified using one (1) wafer/assembly lot. Electrical parameter assessment is one of the most important tests to run.

4.2 Requalification of a changed device

Requalification of a device will be required when the supplier makes a change to the product and/or process that could potentially impact the form, fit, function, quality and/or reliability of the device. The guidelines for requalification tests required are listed in Table 3.

4.2.1 Process change notification

Supplier will meet the requirements of JESD46 "Guidelines for User Notification of Product/Process Changes by Semiconductor Suppliers" for product/process notification changes.

4.2.2 Changes requiring requalification

All product/process changes should be evaluated against the guidelines listed in Table 3.

4.2.3 Criteria for passing requalification

Table 3 lists qualification plan guidelines for performing the appropriate Table 1-2 stresses. Failed devices should be analyzed for root cause and correction; only a representative sample needs to be analyzed. Acceptable resolution of root cause and successful demonstration of corrective and preventive actions will constitute successful requalification of the device(s) affected by the change. The part and/or the qualification family can be qualified as long as containment of the problem is demonstrated until corrective and preventive actions are in place.

5 Qualification tests

5.1 General tests

Test details are given in Table 1 and Table 2. Not all tests apply to all devices. Table 1 tests generally apply to design and fabrication process changes. Table 2 tests are for laminate based modules. Table B lists the pass/fail requirements for common infant mortality levels. Table 3 gives guidance as to which tests are required for a given process change. Some of the data required may be substituted by generic process or package data.

5.2 Wearout reliability tests

Qualification testing is intended to demonstrate reliability performance for a range of expected application conditions free of wearout. Qualification testing is not intended to measure the onset of wearout, nor the acceleration factors applicable to wearout failure mechanisms. However, technology or family testing for the failure mechanisms listed below must be available upon request for each wafer fabrication technology, family, or material relevant to the appropriate wearout failure mechanisms to be validated by the suite of stresses used to validate adequate reliability during qualification. JP001 lists recommended requirements for Fabrication Process Qualification. JEP122 explains how to project wearout lifetime for these failure mechanisms. The following mechanisms need to be considered, but there may be other mechanisms to consider based upon technology details.

- HBT Beta or Base Current Degradation; such as a recombination defect reaction.
- Electromigration; EM.
- Metal interdiffusion; such as sinking gates or ohmic contact degradation.
- Time-Dependent Dielectric Breakdown; TDDB or dielectric integrity tests such as charge to breakdown.

5.3 Device qualification requirements

Table 1 — Device Qualification Requirements

Type	Stress	Ref.	Abbv.	Conditions	Requirements	
					# lots/SS per lot	Duration/Accept
Life Test	Preferred: RF Biased Life Test Alternates: HTOL, HTSL, ELFR,	JESD226	RFBL	Tj≥125ºC Tj<Tg (NOTE 1)	3 lots / 76 units (NOTE 2)	1000 hrs / 0 fail
Device specific	Latch-up	JESD78	LU	Ta = 25ºC	6 units	0 fail
Device specific	Electrical Paramerter Assessment	JESD86	ED	Datasheet	3 lots / 10 units (NOTE 2)	Characterization
ESD	Human Body Model	JESD22-A114	ESD-HBM	Ta = 25 °C	3 units	Classification
	Charged Device Model	JESD22-C101	ESD-CDM	Ta = 25 °C	3 units	Classification

NOTE 1 Tj < Tg may be restrictive for green mold compounds. The HTOL test should not generate any failure mechanisms not observed or expected in operation at use conditions. This should be verified if the Tg of the mold compound is exceeded.

NOTE 2 Multiple lot requirement is for wafer, Fab, or semiconductor –type lots.

NOTE 3 Number of lots and sample size is recommended. Alternate sizes will be enumerated and described in the report/result document.

5.3 Device qualification requirements (cont'd)

5.3.1 Life testing

Overall module reliability is determined by testing samples for their expected lifetimes without experiencing degradation. Stress and bias conditions that approximate normal application conditions are preferred; however some type of acceleration is needed to make the life test duration practical for a qualification. Only one lifetest methodology should be selected from the four types as follows:

a) **RFBL** (RF Biased Lifetest) - The duration listed here is generally acceptable to qualify for the given application level for handheld mobile devices. The application of all dynamic stress conditions, including RF is preferred and described per JESD226.

b) **HTOL** (High Temperature Operating Lifetest)- The duration listed here is generally acceptable to qualify for the given Application Level. However, it does not necessarily imply the demonstration of the lifetime requirement for a particular use condition. It depends on failure mechanisms and application environments. For example, with apparent activation energy of 0.7eV, 125 °C stress temperature and 55 °C use temperature, the acceleration factor (Arrhenius equation) is 78.6. This means 1000h stress duration is equivalent to 9 years of use. This might be shorter than the application requirement. In order to assure adequate lifetime requirement, it would be necessary to include Wafer Level Reliability Test information. Wafer Level Reliability can provide information about long term or intrinsic reliability of specific wearout mechanisms, the onset to failure time and design rule limits (e.g., maximum current density). For many failure mechanisms, such as dielectric breakdown, elevated voltage will provide additional acceleration and can be used to increase effective device hours or achieve an equivalent life point with a shorter stress duration. Refer to JEP122 for voltage acceleration models.

c) **HTSL** (High Temperature Storage Lifetest) – High temperature storage may be accelerated by utilizing a higher temperature than biased lifetesting; however care must be taken that new failure mechanisms are not introduced such as mold compound melting at thermal stress exceeding the packaging material's glass transition temperature. Alternatively, this test may be performed at the wafer level if packaged device reliability has been addressed with generic data. This test is basically used to determine if the effects of diffusion, oxidation, intermetallic growth, and chemical degradation of packaging components will affect product life.

d) **ELFR** (Early Life Failure Rate) - Several methods can be used to calculate the Early Life Failure Rate (ref. JESD74). The objective of ELFR is to measure the failure rate in the first several months or year of operation. Knowledge of the life distribution is generally required to accurately predict ELFR. Equivalently, JESD47, Table B can be used to determine sample sizes to satisfy a particular FPM (cumulative failures per million) target. Voltage and temperature acceleration may be used to further accelerate effective unit hours, however the early life rates are normally highest in the first few hours, so for very low rates large sample sizes are required. ELFR testing does not empirically establish the onset of wearout degradation, so the wearout data defined in 5.2 is critical if ELFR is selected instead of the other life test methods described above.

5.3 Device qualification requirements (cont'd)

5.3.1 Life testing (cont'd)

Table B — Minimum sample size to demonstrate various ELFR targets in FPM (Failures Per Million) at 60% Confidence Level

Number of Observe Failures	Minimum Sample Size at 60% Confidence							
	5000 FPM	4000 FPM	2000 FPM	1000 FPM	500 FPM	250 FPM	100 FPM	10 FPM
0	183	229	458	916	1,833	3,665	9,163	91,630
1	404	505	1,011	2,022	4,405	8,089	20,223	202,230
2	621	778	1,553	3,105	6,211	12,422	31,054	310,540
3	835	1004	2,088	4,175	8,351	16,701	41,753	417,530

5.3.2 Device specific tests

a) **LU** (Latch-Up) – Verify Vcc overvoltage and I/O trigger current resistance to latch-up. Latch-up tests must be performed on the specific device (component) to be qualified for all PAMs incorporating CMOS, BiCMOS, and Bipolar silicon semiconductor technology. Passing or failing this test qualifies or disqualifies only the device under qualification and not the associated qualification family. Latch-up testing can be performed on the individual silicon component and/or on the entire module per JESD78.

b) **ED** - Electrical Parameters Assessment. This study is to be performed on key device parameters, it is not aimed at all datasheet parameters. The supplier shall be capable of demonstrating, over the application temperature range, that the part is capable of meeting parametric limits in the individual device specification or data sheet. JESD86 provides guidelines for this series of evaluations.

c) **ESD-HBM** Classification of Human body Model ESD resistance

d) **SD-CDM** Classification of Charge Device model ESD resistance.

5.4 Module qualification test requirements

Table 2 identifies stress/aging requirements for laminate based modules.

Table 2 — Module Qualification Requirements

Type	Stress	Ref.	Abbv.	Conditions	Requirements	
					# lots SS per lot (NOTE 1)	Duration/ Accept
Reflow Fitness	MSL Preconditioning (Must be performed prior to: humidity and thermal excursion tests)	JESD22 -A113	PC	Per appropriate MSL level per J-STD-020	3 lots / 152 units 456 total	3 reflow / 0 fail
Humidity (Pick One)[a] Use samples from PC[b]	Temperature Humidity Bias (standard 85/85)	JESD22 -A101	THB	85 °C, 85 % RH, max voltage, min power	3 Lots / 76 units	1000 hrs / 0 fail
	Temperature Humidity Bias (Highly Accelerated Temperature and Humidity Stress)	JESD22 -A110	HAST	130 °C / 110 °C, 85 % RH, max voltage, min power	3 Lots / 76 units	Equivalent to 1000 hrs THB / 0 fail
	Unbiased Temperature/Humidity (Unbiased HAST)	JESD22 -A118	UHAST	130 °C / 85% RH 110 °C / 85% RH	3 Lots / 76 units	96 hrs / 0 fail 264 hrs / 0 fail
	Unbiased Temperature/Humidity (Autoclave)	JESD22-C101	AC	121 °C / 100% RH	3 Lots / 76 units	96 hrs / 0 fail
Thermal Excursion (Pick One)[c] Use samples from PC[b]	Temperature Cycling	JESD22 -A104	TC	*G:* -40 °C to +125 °C	3 Lots / 76 units	1000 cycles
				Any other condition		Equivalent to condition G 1000 cycles
	Thermal Shock	JESD22 -A106	TS	Any TC condition	3 Lots / 76 units	Equivalent to TC condition G 1000 cycles
	Solder Reflow (in addition to preconditioning)	JESD22-A113	SR	Standard 260ºC profile	3 Lots / 76 units	Equivalent to TC condition G 1000 cycles
Mechanical Strength (Pick one if internal cavities are used)	Mechanical Shock	JESD22-B104 M2002	MS	Y1 plane only, 5 pulses, 0.5 ms duration, 1500 g peak acceleration	3 lots / 39 units	Accept on 0
	Board Level Drop Test	JESD22-B111	BLDT	Drop height Drops to failure	15 units	Accept on 0 component failures
	Vibration Variable Frequency	JESD22-B103 M2007	VVF	20 Hz to 2 kHz (log variation) in > 4 minutes, 4X in each orientation, 50g peak acceleration	Sequence from MS	Accept on 0
	Board Level Cyclic Bend Test Method for Reliability Characterization of Components for Handheld Electronic Products	JESD22-B113	BLCBT	Characterization	36 units	Cycles to failure

5.4 Module qualification test requirements (cont'd)

Table 2 — Module Qualification Requirements (cont'd)

Type	Stress	Ref.	Abbv.	Conditions	Requirements	
					# lots SS per lot (NOTE 1)	Duration/ Accept
Assembly (if not verified during production)	Solderability	M2003 JESD22-B102	SD	Characterization	3 lots / 22 leads	0 Fail
	Wire Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (NOTE 2)
	Wire Bond Shear	JESD22 -B116	BS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (NOTE 2)
	Solderball Shear	JESD22-B117	SBS	Characterization	30 balls / 5 units	

NOTE 1 Multiple lot requirements are for module, package or assembly-type lots. Number of lots & sample size is recommended. Alternate sizes will be enumerated and described in the report/result document.

NOTE 2 $Ppk = \frac{\bar{x} - LSL}{3\sigma} - \frac{USL - \bar{x}}{3\sigma} \geq 1.66$ Process capability data may be substituted for Ppk with data on more than 30 lots with the requirement that $Cpk \geq 1.33$.

[a] Either THB, HAST, UHAST, or AC may be chosen. The applicability of unbiased testing (UHAST and AC) must be justified. HAST default duration may begin at 96 hours or 264 hours and subsequently justified for other conditions and durations by experimental results.

[b] Preconditioning to JESD22A113 is recommended, specifically for wirebonded products qualified to Pb-free reflow profiles. Moisture soak as part of the preconditioning must match the moisture sensitivity level of the package.

[c] It is recommended that the Temperature Cycling condition is chosen by the following criteria:

- The condition chosen must encompass the range that device will be subjected to in its routine field operating life.
- Annex A explains the failure mechanisms and models used for the choice of temperature cycling conditions.
- Any Temperature Cycling condition specified in JESD22-A104 may be used following the methodology in Annex A.

5.4 Module qualification test requirements (cont'd)

5.4.1 Module Test Descriptions

A) **Reflow Fitness.** PC (Pre-Conditioning) ensures that a device will be able to withstand multiple assembly solder reflow cycles, and to simulate the stress from Printed Circuit Board assembly that a device in a field operation would receive as part of the normal production build. Pre-Conditioning is an applicable precursor stress for both humidity and thermal excursion testing.

B) **Humidity** is intended to accelerate the three basic corrosion models: Galvanic, Electrochemical and direct Chemical. It will also accelerate ion migration. Applied bias in THB and HAST is intended to ensure electrochemical degradation, but if the bias produces any power dissipation then the thermal gradients inside the package will affect the moisture penetration and reduce the effective moisture levels inside the package.

- **THB** (Temperature, Humidity, Bias) is the standard baseline humidity testing. At 85 °C and 85% RH, THB does not include pressurization beyond atmospheric pressure, nor does THB produce condensed moisture. THB is the least accelerated humidity test option, so the durations of THB are similar to lifetesting. THB must be performed at minimum power dissipation.
- **HAST** (Highly Accelerated Stress Test) is a biased test used to accelerate the THB test using temperature and 85% RH pressurized moisture. HAST must be run at minimum power dissipation. The temperature can be adjusted to achieve the desired thermal acceleration. HAST is usually run at either 110 °C or 130 °C.
- **UHAST** (Unbiased HAST) is the preferred technique to test for Galvanic and direct Chemical corrosion since it does not condense moisture (<100% RH) and power dissipation is not a confounding factor since UHAST is unbiased. However, UHAST is still a pressurized humidity test at 85% RH. At the 130 °C condition, the UHAST is at a higher pressure than autoclave.
- **AC** (Autoclave) is the highest humidity test method. At 100% RH and 121 °C, the applied moisture is saturated steam that can introduce condensation and pressure on the DUT surface. The extreme induced humidity is highly accelerated beyond normal package field life stresses so autoclave can induce mechanisms that are not representative of those expected in normal use. Since autoclave is not biased, it cannot evoke electrochemical mechanisms. Autoclave does not require any biasing fixtures so it is easy to apply and short in duration.

C) **Thermal Excursion** testing will accelerate damage caused by thermal-mechanical stress as a result of thermal mismatch and differences in the thermal coefficient of expansion for each of the various materials utilized within a module.

- **TC** (Temperature Cycling) Acceleration factors are established between each of the various cycling conditions. The magnitude of the excursion is what accelerates the mechanisms.
- **TS** (Thermal Shock) Some of the thermal-mechanical mechanisms can be accelerated by the rate of thermal change, making TS an accelerated version of TC for those mechanisms. Another advantage of TS is that liquid emersion is faster than air in transferring sample temperatures. So the reduced transition times can make TS a faster test than TC.
- **SR** (Solder Reflow). The solder reflow temperature is likely to be the highest temperature that modules will experience in normal applications. Since some assemblies will experience several reflows while the system is assembled, the reflow lifetime is an important aspect of thermal excursion testing.

5.4 Module qualification test requirements (cont'd)

5.4.1 Module Test Descriptions (cont'd)

D) **Mechanical Strength** testing is particularly important for components with cavities that are used within a module, but are not required for fully encapsulated products. For example, filters and couplers may have cavities. The mechanical strength tests can be verified by normal characterizations or demonstrated by methods shown in this group.

- **MS** (Mechanical Shock)
- **VVF** (Vibration Variable Frequency).
- **BLDT** (Board Level Drop Test)
- **BLCBT** (Board Level Cyclic Bend Test)

E) **Assembly.** Many assembly properties, such as die attach coverage, wire bond adhesion, and flip chip bump adhesion are monitored and controlled as part of the assembly process. Control, set-up, and/or SPC data is produced as evidence of process capability. Additionally, characterization, designed experiments, and verification data can be produced as described in the following battery of tests. The testing is particularly important for components with cavities that are used within a module. For example, filters and couplers may have cavities. Otherwise, many assembly properties, such as die attach strength, wire bond adhesion, and flip chip bump adhesion are monitored and controlled as part of the assembly process (see assembly tests). The mechanical strength tests can be verified by normal characterizations or demonstrated by methods shown in this group.

- **SD** (Solderability) ensures that the device leads are capable of being wetted by the board attachment solder.
- **BPS** (Bond Pull Strength) ensures that wire bond exhibits the desired tensile strength.
- **BS** (Bond Shear) ensures that the wire ball bond exhibits the desired shear strength.
- **SBS** (Solder Ball Shear) ensures that the BGA balls have the desired shear strength attachment to the package.

5.5 Reporting of Results

Results of qualification testing performed in accordance to this standard should be reported in an overall summary or "package" as described in JESD69.

6 Explanatory comments regarding process/product changes

Classification of various changes is shown in JESD46. As an example, some common changes are listed here and the appropriate generic qualification testing is identified in Table 3.

6.1 Example changes requiring re-qualification

The following are examples of changes require re-qualification:

Active Circuit Element: New type of circuit element or modification of transistors beyond original qualification or spec limits.

Major Circuit Elements: Addition of a major new circuit block to an existing circuit such as adding a Digital Signal Processor or embedded memory block to an existing product.

Wafer Diameter Change

Metallization: New Materials or a significant change in composition

Change In Minimum Feature Size: A reduction of greater than 20% shall be considered a new process.

Wafer Fab Process: Utilizing different process techniques at critical points (excluding wafer transport equipment)

Diffusion/Dopant/Epitaxy: New material or technique

Transistor contact material: Composition, design rules, process

Lithography: Change in wavelength, method (air / immersion / ebeam), or etch technique

Wafer Frontside Metallization: Composition, design rules, process and/or technique

Interconnect or Wafer Via: Composition, design rules, process and/or technique

Passivation Overcoat: Either glass or organic material composition, design rules, process and/or technique

Dielectric Materials: Composition, design rules, process and/or technique

Wafer Backside Operation: Metal composition, design rules, process and/or technique

New Wafer Manufacturing Line: Not already qualified for the fabrication process

Assembly Process: Utilizing different process techniques at critical points

Die Coating: Material, process, and/or technique

Lead Frame: Base material, finish, and critical dimensions

Bond Wire: Material, diameter

Bonding: Process and/or technique

Die Preparation: Separation and clean methods

Die Attach: Material, process, and/or technique

Encapsulation: Material, composition, process and/or technique

Hermetic Package: Material, composition, seal material, process and/or technique

Wafer Bumping Material: process, or technique (including flip chip assembly process)

Package Dimension Change: Larger package body size or reduction in lead or solder ball pitch.

Die Thickness

New device or component location or combination on the laminate

6.2 Changes that may not require re-qualification

The following describes changes that may not require re-qualification:

- Assembly location already qualified for that package.
- The movement of product manufacturing (wafer fab or assembly) from one location to another where the new location is already qualified for the same process and techniques requires only completion of manufacturability tests at the new location.
- The addition of previously qualified equipment requires completion of process capability study only, to assure that the added equipment delivers an adequate process distribution.
- A change to a test program or test equipment requires proof of continued conformance to product specification only.
- Any change in a process, product or material parameter that does not exceed the current specified production process range is not a major change.
- Minor changes to device logic operation may only require functional verification.
- Smaller package or die where the product family has already been qualified.

6.3 Multiple family qualifications

When the specific product attribute to be qualified will affect more than one wafer fab or assembly family, the qualification test vehicles should be:

1) One lot of a single device type from each of the three (3) products that are projected to be most sensitive to the changed attribute, or
2) Three lots total from the most sensitive families if only one or two exist.

The recommended process for qualifying changes across many process and product families is as follows:

1) Identify all products affected by the proposed changes.
2) Identify the critical structures and interfaces potentially affected by the proposed change.
3) Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Note that steps 1 to 3 are equivalent to the creation of an FMEA.
4) Define the product groupings or families based upon similar characteristics as they relate to the structures and device sensitivities to be evaluated, and provide technical justification for these groupings.
5) Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products that will address each of the potential failure mechanisms and associated failure modes.
6) Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process steps.

6.4 Guidelines for stress tests for typical process changes

Table 3 lists the recommended (R) qualification tests for each type of change in the process, package, or device design, and additional tests that should be considered (C) based upon technology considerations.

Table 3 — Guidelines for major process change selection of tests

Process Attribute	RFBL HTOL HTSL ELFR	LU	ED	ESD	PC	THB HAST UHAST AC	TC TS SR	MS BLDT VVF BLCBT	SD BPS BS SBS	Wearout	Other
Active Circuit Element	CR			R		C				R	
Major Circuit Change	R	C	C	C		C					
5% to 20% Die Shrink	R	R	R	R		R	C			R	
Lithography	C		R							C	
Doping/Epitaxy	C	C		C						R	
Metallization	R					R	R			R	
Transistor Contact	R		C			R	R			R	
Dielectric	R					R	C			R	
Passivation	C					R	C				
Interconnect Via	C				C	C	R			R	
Substrate Via	C				C		C			R	
Wafer Diameter	R			C		C	R			R	
Fab Site	R					C	R				
New Package to qualified product	C			C	R	R	R	R	R		
Leadframe plating					C	R	C	R	C		
Leadframe material					C	R	C	C	C		
Package Dimensions					C	R	C	C	C		
Wire Bonding					C	C	R	C	C		
Die Location in module					C		R				
Die Attach					C	C	R	C	C		
Molding Compound	C				C	C	R	C	C		
Laminate Material					R	C	R		R		
Laminate Plating					C	C		R	R		
Molding Process					C	C	R	C	C		
Assembly Site					R	C	R		R		
Screening (Burn-in)	C										
Flip Chip Attach					R	C	R	C	C		
Bump Materials					R	C	R	C	C		
Bump Processing					R	C	R				
Wafer bump under metal					R	C	C	C	C		
Bump Site					R	C		C	C		
Flip Chip Underfill					R	C	R	C	C		
Die Thickness	C				C		R	C	C		

Annex A (informative) Module temperature cycling description

Solder joint Reliability is generally the limiting factor for component life in a system subjected to temperature cycling. Solder joint life is well modeled by a Coffin-Manson relation of ΔT_n where n=2. Other failure mechanisms as reported in JEP122 have larger acceleration factors so this becomes a worst case condition. The temperature cycling requirements have been normalized to the historical requirement of 500 cycles of Condition C using the n=2 factor. As a sanity check the typical use conditions for a number of common applications have been compared to these qualification conditions. As can been seen in Table C the qualification requirements exceed the use conditions by a wide margin.

Table C – Comparisons of temperature cycling conditions for example applications

Use Condition	Use Condition Requirement	Equivalent Condition B -55 °C to +125 °C 700 cycles	Equivalent Condition G -40 °C to +125 °C 850 cycles	Equivalent Condition J 0 °C to +100 °C 2300 cycles
Desktop 5 yr Life	ΔT 40 °C 2000 cy	14,175 cy (12,475 cy)* (11,057 cy)**	14,463 cy (12,761 cy)* (11,332 cy)**	14,375 cy (12,675 cy)* (11,250 cy)**
Mobile 4 yr Life	ΔT 15 °C 1500 cy	100,800 cy	102,850 cy	102,221 cy
Server 11 yr Life	ΔT 40 °C 44 cy	14,175 cy	14,463 cy	14,375 cy
Telecom (uncontrolled) / Avionics Controlled 15 yr Life	ΔT 25 °C 5500 cy	36,288 cy	37,026 cy	36,800 cy
Telecom (controlled) 15 yr Life	ΔT 6 °C 5500 cy	630,000 cy	642,812 cy	638,889 cy
Networking 10 year Life	ΔT 30 °C 3000 cy	25,200 cy	25,712 cy	25,557 cy

*JESD94, Table 1, Consider desktop with add'l ΔT 8 °C for 31,025 cycles and ΔT 20 °C for 1828 cycles

** Consider Desktop with additional ΔT 10 °C for 50,000 cycles

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