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THERMAL TEST CHIP GUIDELINE (WIRE BOND AND FLIP CHIP)

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THERMAL TEST CHIP GUIDELINE (WIRE BOND AND FLIP CHIP)

Contents

Introduction

Thermal Test Chips have three primary purposes in the area of semiconductor device packaging:

1) To provide a well-defined structure for the generation of heat flux with built-in temperature sensor(s) that can be used to compare the thermal performance of semiconductor packages,

2) To use the well-defined structure in a specific package for validating or calibrating thermal model simulations, and

3) To provide a vehicle for thermal investigation of power topology mapping, power transient response, and complex packaging assemblies that would be difficult to accomplish using an application semiconductor device.

THERMAL TEST CHIP GUIDELINE (WIRE BOND AND FLIP CHIP)

(From JEDEC Board Ballot JCB-19-11, formulated under the cognizance of the JC-15 Committee on Thermal Characterization Techniques for Semiconductor Packages.)

1 Scope

The purpose of this document is to provide a design guideline for thermal test chips used for integrated circuit (IC) and transistor package thermal characterization and investigations. The intent of this guideline is to minimize the differences in data gathered due to nonstandard test chips and to provide a well-defined reference for thermal investigations.

The thermal test chips described in this document will apply to single and multiple chip devices. These are designed using standard semiconductor wafer fabrication processes and can be used with a wide variety of industry standard packages. These test chips can operate in a static mode in which constant power is continuously supplied to the device while monitoring the temperature through the measurement of a Temperature Sensitive Parameter (TSP). They can also operate in a transient mode in which the power supply and the TSP are monitored as a function of time (t). This guideline covers test chips meant to be both wire bonded or flip chip bumped to the package external contacts.

1.1 Rationale

The thermal resistance for a specific device varies with many factors. The chip size, location and size of the power dissipation element(s), and location of the temperature sensor(s) will directly affect the thermal test results. It is essential to standardize thermal test chip design guideline in order to provide meaningful measurement results. This allows semiconductor suppliers to compare different packages over a wide variety of conditions, such as power levels and air flows. It will also help the users to estimate their active device junction temperature under actual operating conditions by allowing them to extrapolate the results of a defined standard condition.

2 References

This document contains the guideline for thermal test chip design as a subset of JEDEC methodology for component package thermal measurement. The associated details of test method, environment and test board are given in JEDEC documents [1] - [4]. It is also recommended to read the SEMI test standards ([5] - [9]) and the related documents [10] - [12].

[1] JESD 51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)

[2] JESD 51-1, Integrated Circuit Thermal Measurement Method - Electrical Test Method (Refer to Annex A for a list of terminology and symbols applicable to this document).

[3] JESD 51-2, Integrated Circuit Thermal Test Method, Environmental Conditions - Natural Convection

[4] JESD 51-12, Guidelines for Reporting and Using Electronic Package Thermal Information

[5] JC-15- Low Thermal 95-63, Conductivity Test Board for Leaded Surface Mount Packages.

[6] SEMI Test Method #G43-87, Test Method, Junction-To-Case Thermal Resistance Measurements of Molded Plastic Packages.

[7] SEMI Test Method #G38-87, Still and Forced Air-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages.

[8] SEMI Test Method #G42-88, Specification, Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages.

[9] SEMI Test Method #G30-88, Junction-to-Case Thermal Resistance Measurements of Ceramic Packages.

[10] SEMI Test Method #G32-86, SEMI Guideline for Unencapsulated Thermal Test Chip.

[11] EIA JEDEC EB-20, Accepted Practices for Making Microelectronics Device Thermal Characteristics Test.

[12] Mil Std 883C Method 1012.1, Thermal Characteristics of Microelectronics Devices.

[13] NIST Special Publication 400-86, Semiconductor Measurement Technology: Thermal Resistance Measurements.

3 Test Chip Design

The thermal test chip should be designed to provide uniform or non-heating across the chip surface, and chip temperature sensing. The general design and construction of the thermal test chip includes these basic features: heating source, temperature sensor, and mounting approach. The components of a test chip are discussed as follows.

3.1 Heating Source

Resistor elements or transistors should be used as heating sources. The heating power (P_H) is calculated as follows:

$$P_H = V_H \text{ X } I_H \quad (1)$$

Where: V_H = voltage across the heating source (V)
I_H = current for the heating source (A)

When resistor heating is utilized, the resistance temperature dependence has to be considered in order to set the power supply. If the heater resistance is implemented in a semiconductor structure, the resistance will vary significantly with temperature (typically ≥3% over a 100 ºC range), thus requiring at each measurement point adjustment of either V_H or I_H and monitoring the other because they are dependent on each other. However, if the heater resistance is implemented with a deposited metal film of certain materials, the resistance temperature variation is small enough (typically ≤1% over a 100 ºC range) that the power dissipation only has to be set once for all the measurement points. If the heating resistor is implemented with metal films of materials with high resistance temperature variation, then the heating power supply will have to be adjusted during the measurement to maintain a constant power or the power will have to be measured at the time value of interest. The resistance value should be chosen to limit the current for maximum power dissipation consistent with the current handling capability of the on-chip metal traces and to minimize the Joule heating in those traces. The exact value of Unit Cell resistor(s) is determined by the chip design, fabrication technology, and the selection of resistor material.

When a transistor is used, both V_H and I_H can be adjusted separately. Therefore, the heater power dissipation is easy to control but at the expense of more complex power dissipation control circuitry. For this reason, a transistor is preferred in certain transient applications and when extremely tight control of power levels (typically ≤0.5%) is required. However, due to the way transistors are designed, it is difficult to obtain uniform power distribution with a large transistor. Hence, for a large single unit test chip, the resistor option is preferred.

3.2 Temperature Sensor

The temperature sensing element(s) should function at the operating temperature range of the device. The most commonly used Temperature Sensitive Parameter (TSP) is the voltage drop across a forward biased PN diode. This diode is specifically designed into the thermal test chip. It exhibits a linear forward voltage characteristic with temperature when a fixed measurement current (I_M) is forced through the diode. The temperature rise of most diodes is approximately 0.5 °C for 1 millivolt drop in forward voltage, that is -0.5 °C/mV. This parameter is called the K-Factor. It is process-dependent and must be determined by measuring the voltage of the diode at various temperatures. A typical diode characteristic curve is shown in figure 1. The chip temperature change can be obtained from the voltage drop with respect to a reference (usually zero power) state [2].

Another type of temperature sensor is a Resistance Temperature Detector (RTD), which is a single, specially designed metal trace. The advantage of resistance type sensors is that they are more linear than diodes over a much wider temperature range. For a proper local measurement, the RTD may be built as a small spiral or zig-zag patch in the locations on the chip where temperature measurements are to be made. A 4-wire (Kelvin) type electrical connection must be used with RTD sensors.

The temperature sensor should be as small as possible relative to the heating elements so as to provide a defined temperature spatial point with minimum temperature variation across the sensor. Further, the temperature sensor should be in close proximity to the heating elements so as to minimize the temperature drop between the heat source(s) and the temperature sensor. In two dimensional structures, the temperature sensor should be as closely adjacent as possible to the heat source(s). If implemented in three dimensional structures, the temperature sensor should be under the heat sources. In the latter case, with the heater over the sensor, care must be taken that the lower level temperature structure does not cause non-uniform heating in the upper level heater structure.

The temperature sensor should have an easily measureable parameter that is reliably and repeatably proportional to temperature. In the case of either a diode or RTD sensor, usual practice is to force a constant current (i.e., Measurement Current [I_M]) into the sensor and measure the voltage (i.e., Measurement Voltage [V_M]) across the sensor. Typical values for the diode sensor are 1mA and ≈0.7 V at 22 ºC; corresponding typical values for the RTD sensor are 10 mA and ≈0.5 V (for a 50 Ω sensor) or 1mA and ≈0.4 V (for a 400 Ω sensor). For either sensor type, the power dissipation in the sensor should be as small as possible, typically less than 1% of the applied heating source power, so to not cause significant self-heating and resultant perturbation of the temperature measurement and applied heating power.

3.3 Mounting Approach

The interconnection between the test chip and the package external contacts is determined by the package in which the test chip is mounted.

3.3.1 Wire Bond Approach

When the test chip is attached to the package on the back side (i.e., the side away from the chip circuitry – a process called Die Attachment) first, then electrical contact to chip is usually made by bonding wires between the chip wire bond pads to specific wire landings in the package. The bonding pads are obtained through the standard wafer fabrication process. This process results in electrical connection to the chip through the package's external leads or contacts.

3.3.2 Flip Chip Approach

When the test chip has solder bumps applied to its electrical connection pads and then attached to the package by reflowing the solder bumps on to metal contact pads on the package, the process is called Flip Chip Attachment. This process results in electrical connection to the chip through the package's external ball, pin or land contacts.

3.4 Physical Layout

The basic chip unit containing the heating source(s) and temperature sensor(s), commonly referred to as a Unit Cell, can be utilized as a single Unit Cell chip or arrayed to form larger multiple Unit Cell chip. The single Unit Cell chip with a single heat source will generate heat uniformly; multiple heat sources within the Unit Cell provide the capability for non-uniform heating. The Unit Cell array option gives the flexibility to generate heat uniformly if the basic units (i.e., Unit Cells) are electrically interconnected and powered by a single heating power supply, or non-uniformly if the units are connected, either singularly or in groups, and powered by multiple power supplies.

For wire bond packaging applications, interconnection between the Unit Cells can be achieved by wire bonding or by adding metal traces during the test chip fabrication process. The former is usually not practical if the array size is large or if the wire bond pad diameter and/or pitch are small. If metal traces are added between Unit Cells during the fabrication process, care must be taken to ensure an adequate coverage of oxide in the scribe line to avoid shorting the interconnection traces to the substrate and that the interconnection traces are large enough to handle the current required for powering the Unit Cells. Care must be taken when sawing metal-trace-interconnect wafers because –

a) The sawing operation may smear the cut metal trace over the edge of the chip which could potentially short the trace to the chip substrate and cause the chip to fail, and
b) Sawing through the metal trace may require slower sawing speeds and saw blade replacement more often.

3.4 Physical Layout (cont'd)

For flip chip packaging applications the Unit Cells are isolated from each other. Any required interconnect between the cells can be implemented in the package substrate or in the printed circuit board upon which the package is mounted.

Example physical and electrical layouts for single and multiple unit chips are shown in figures 2 and 3, respectively. Recommendations for chip size, heating source area coverage, and temperature sensor placement are given in the following sections.

3.4.1 Chip Dimensions

Both test chip X-Y size and thickness (Z) affect the measurement data. Square and rectangular chips can be obtained using either single or multiple Unit Cell array configurations configuration.

3.4.1.1 Area Dimensions

It is not usually economically feasible to have the test chip exactly match an application chip in both X and Y dimensions. For this reason, it is recommended that a package be characterized for a range of different area thermal test chip sizes. When the resulting characterization data is plotted against chip area, taking into account square and rectangular configurations, an accurate approximation of thermal performance for a specific application chip size is possible.

When a thermal test chip is used to simulate a specific application chip in a specific package, usual practice is that the test chip size should approximate the application chip X-Y size to within ±10%.

3.4.1.2 Thickness Dimension

When performing the package thermal characterization discussed in 3.4.1.1, the test chip thickness should be the same for each different test chip area. If the package is to handle a range of chip thicknesses, the package characterization should be repeated for a range of thicknesses and areas.

When a thermal test chip is used to simulate a specific application chip in a specific package, usual practice is that the test chip thickness should approximate the application chip thickness to within ±10%.

3.4.2 Heating Source Area Coverage

The thermal test chip heating source area should be as large as possible, consistent with commercial semiconductor fabrication and packaging capabilities. The area available for heating source and temperature sensor(s) is limited by the contact pad size, normal spacing requirements between integrated components, and the "keep out" zone around the perimeter of the Unit Cell. Given these constraints, there is a point in Unit Cell size below which heating source area, as a percentage of cell area diminishes significantly.

3.4.2.1 Unit Cell Size ≥2.5 mm square

The outline of the heating source in Unit Cell greater than 2.5 mm square should cover at least 85% of the chip area inside the electrical pads. If a Unit Cell array chip is utilized, each individual unit should meet this area coverage requirement. The heating elements shall be designed to dissipate power at the proper levels and provide uniform heat dissipation per unit area. Sufficient heater electrical contact pads shall be provided to handle anticipated current levels.

3.4.2.2 Unit Cell Size <2.5 mm square

The outline of the heating source in Unit Cell less than 2.5 mm square should cover at least 60% of the chip area inside the electrical contact pads. If a Unit Cell array chip is utilized, each individual unit should meet this area coverage requirement. The heating elements shall be designed to dissipate power at the proper levels and provide uniform heat dissipation per unit area. Sufficient heater electrical contact pads shall be provided to handle anticipated current levels.

3.4.2.3 Array Heating Area Coverage

The Unit Cell area coverage stated above does not apply to arrays of cells. The saw lanes that separate the Unit Cells typically do not have any active heating elements. Thus, it is important to consider the potential heating non-uniformity effects due to the chip's inner saw lanes.

In general, use of a larger Unit Cell size is preferred over the smaller Unit Cell because of the greater heat source coverage. For example, a 2x2 array of 1mm square Unit Cells will have less heat source coverage than a single 2.5mm square Unit Cell. Similarly, a 10x10 array of 1mm square Unit Cells will have considerably less coverage than a 4x4 array of 2.5mm square Unit Cells due to both the heat source coverage of the individual cells and the difference in saw lane total area.

3.4.3 Temperature Sensor Placement

The temperature sensors should be optimally placed to accurately measure the maximum chip temperature. When uniform heating is applied, the maximum chip temperature is normally at the center of the chip active surface. Therefore, in the case of single Unit Cell chip, one temperature sensor must be located at the center of the chip surface. Additional sensors may be placed in a corner and in the middle of an edge for other purposes. When a Unit Cell array chip is utilized, one temperature sensor should be placed at each unit center. It is also recommended, if possible for given Unit Cell size, that a temperature sensor be placed in a cell corner to provide a centrally located sensor if an even array of Unit Cells is used. Similarly, a center edge sensor, if possible for given Unit Cell size, will be helpful for an odd array of Unit Cells. When possible, each temperature sensor should be connected to four pads for the forcing and sensing circuit measurement technique.

NOTE The maximum chip temperature may not be the center of the Unit Cell chip or Unit Cell array chip is the chip is subjected to heat generation by adjacent chips in a multichip package. Therefore, having access to additional temperature sensors may provide access to higher temperature-reading sensitivity.

3.4.4 Electrical Connection Considerations

Electrical connection to the elements of the chip, in either single Unit Cell or arrayed Unit Cells configuration, is made by either wire bonding between the chip and the package (see **3.3.1**) or by a solder reflow process that connects solder bumps on the chip (see **3.3.2**). In either case, the use of Kelvin connections (see **Annex A**) increase the measurement accuracy.

3.4.4.1 Wire Bond Chips

The recommended bonding pad sizes shall be no smaller than 100 μm (4 mils). The wiring for the temperature sensor and heaters shall not be connected to common bonding pads. In the case of arrayed Unit Cells without metal interconnect traces between cells, wire bonding to the outer cells is possible; however, bonding to the inner cells becomes increasingly more difficult as the array of cells increases in size. For this reason, inter-cell wire bonding is not commonly done and use of fabricated inter-connected Unit Cell arrays is required.

The wire size and material used in the bonding process should be consistent with the heating elements current requirements and approximate the wire normally used in connecting the application chip in the packaging assembly process.

3.4.4.2 Flip Chips

The major considerations in the solder bumps on the chip are the diameter and height of the bumps and the bump material. The bump attributes and process should be consistent with the heating elements current requirements. These bump attributes should be reported with the thermal data.

3.5 Surface Properties

The top surface passivation and bottom surface finish and metallization should approximate those present in package assembly process. These surfaces should have a level of adhesion between the chip and adjoining materials similar to that of the application chip. Failure to do so could result in different levels of delamination at the die interfaces, potentially leading to significantly different thermal performance for test and application chips.

4 Application Considerations

4.1 Redistribution Layer

When using thermal test chips to simulate application Wire Bond chips or Flip Chips, the bond pad or bump pitch and location are not likely to match that of the application chip. This may cause difficulty in package assembly, especially in the case of Flip Chips. The common solution to this problem is to apply a Redistribution Layer (RDL) to the connection side of the thermal test chip. The RDL consists of one or more metal layers sandwiched between insulating layers that route the electrical connections on the thermal test chip to different contact locations that match the package assembly requirements. Figure 5 shows how an RDL can be added to a thermal test chip to provide both center and peripheral wire bond pads to facilitate use of single chip in different packages.

4.2 Power Mapping

Actual application chips rarely have uniform heating across the chip. Using a TTC to simulate a specific non-uniform heating topology, referred as a Power Mapping, requires the use of a TTC with isolated cells. Figure 6 shows examples of Power Maps for both size Unit Cells in different array configurations. The red dots in each example represent the diode temperature sensor placement. Thermal measurement data for non-uniform power heating conditions must show a similar map.

5 Data Presentation

The test data presentation should include both thermal parameter data and test conditions. The required data are listed in Table 1.

Table 1 — Thermal measurement test conditions and data parameter summary

Measurement Area	Condition Parameter(s)	Data Parameter(s)
Electrical	Refer to appropriate document	Refer to appropriate document
Environmental	Refer to appropriate document	Refer to appropriate document
Component Mounting	Refer to appropriate document	Refer to appropriate document
Device Construction	Chip name & number Type of Chip (wire bond or flip chip) Chip material Chip size Chip thickness Temperature Sensor type Heating element type Power dissipation maximum	K Factor (ref. [2] sec. 3.3)
For Single Cell Chip	Base Unit Cell size Temperature sensor location(s)	
For Multiple Cell Chip	Base Unit Cell size Array configuration Power Map Temperature Sensor location(s)	
For Wire Bond Chip	Backside surface finish Backside surface coating Wire Bond diagram	
For Flip Chip	Bump height & diameter Bump material Backside surface finish Backside surface coating Connection diagram	

5 Date Presentation (cont'd)

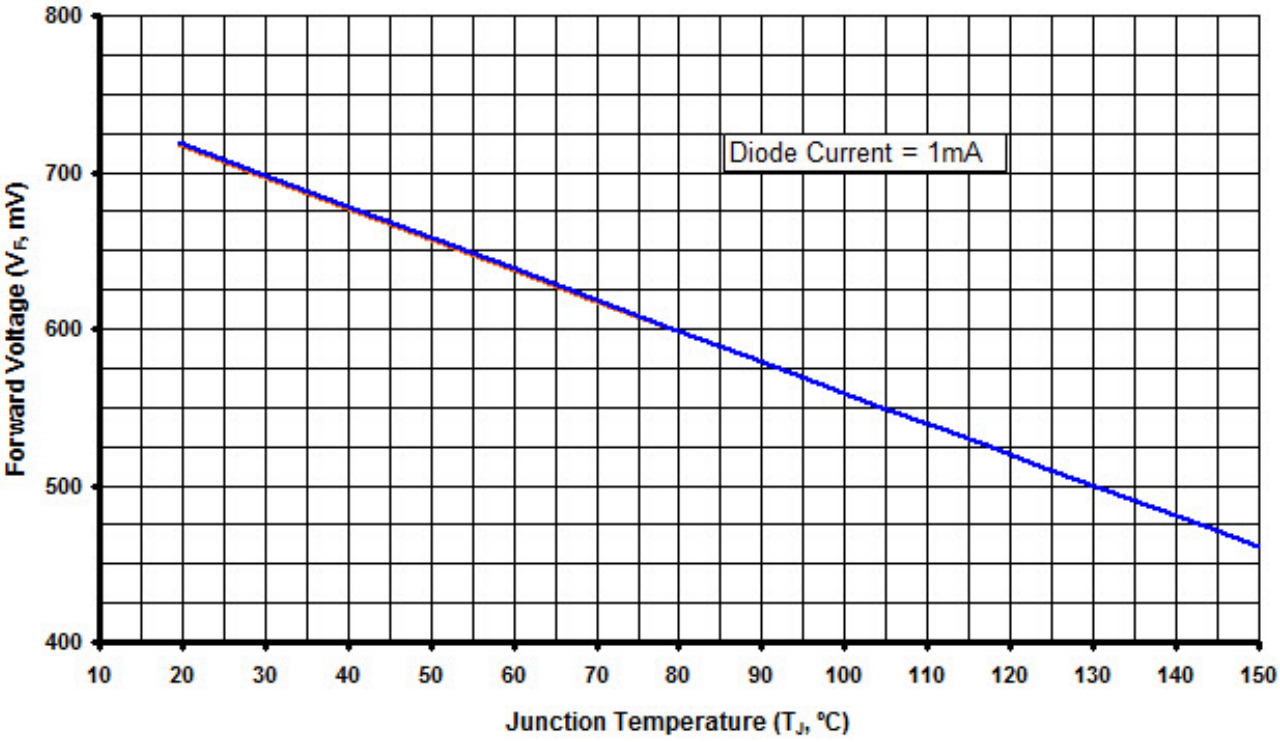
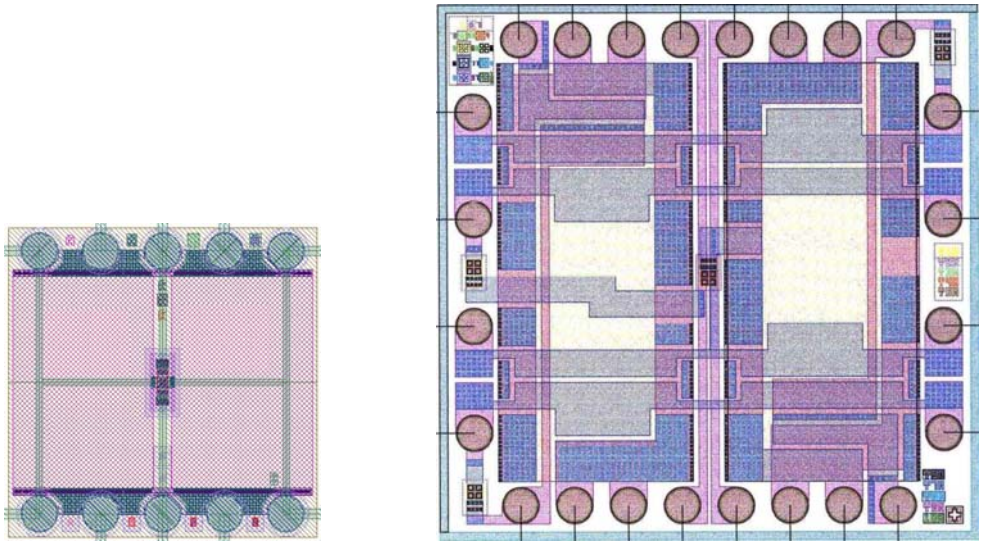


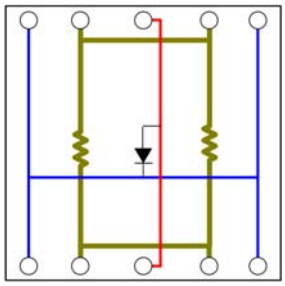
Figure 1 — Typical temperature sensing diode calibration curve



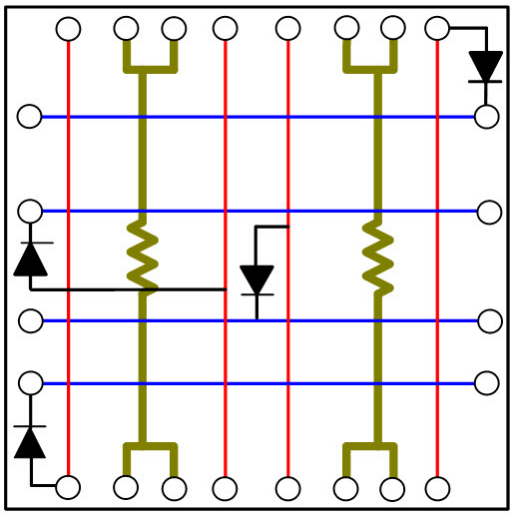
1 mm X 1 mm Unit Cell 2.54 mm X 2.54 mm Unit Cell

Figure 2A — Examples of Unit Cell Physical Layout

5 Date Presentation (cont'd)

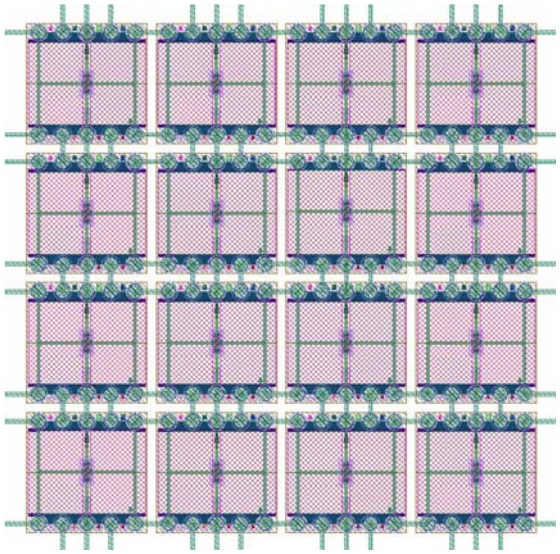


1 mm X 1 mm Unit Cell

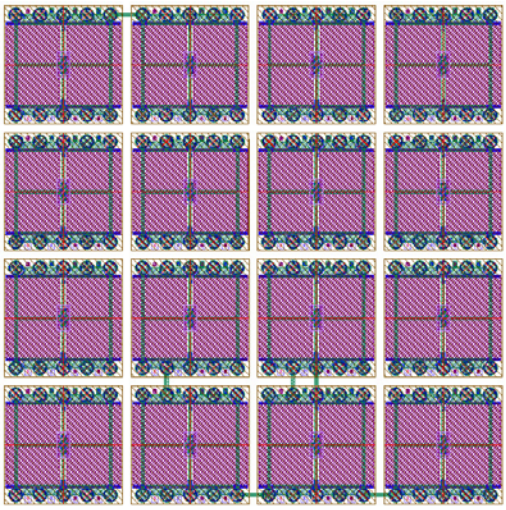


2.54 mm X 2.54 mm Unit Cell

Figure 2B — Examples of Unit Cell Electrical Layout



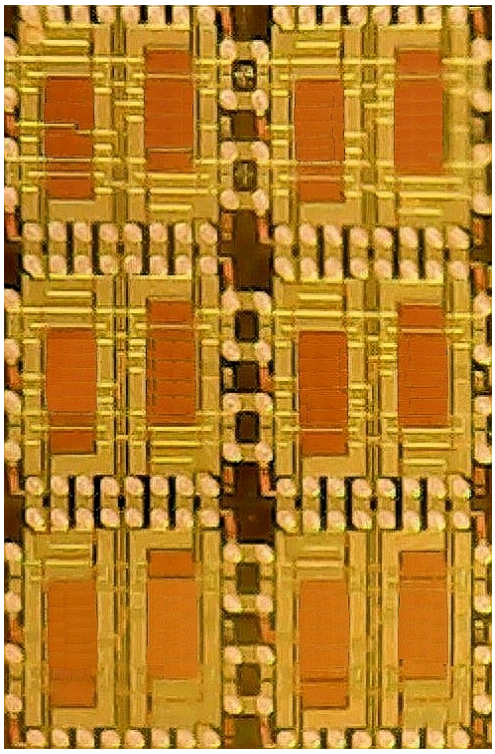
Wire Bond Version
(Connected Cells)



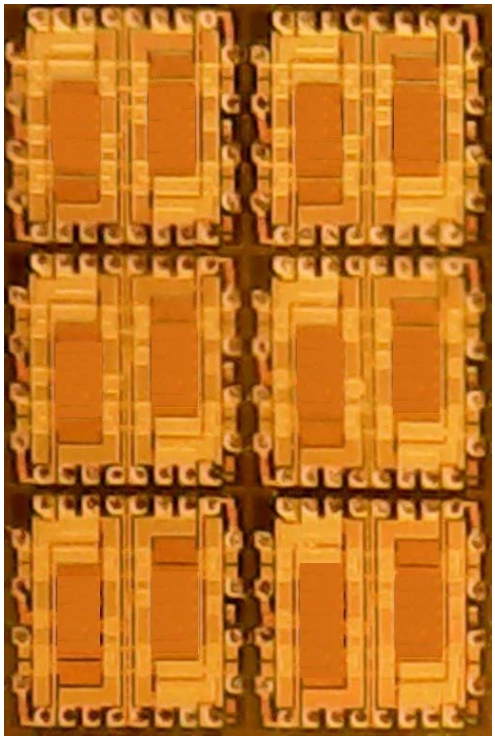
Flip Chip Version
(Isolated Cells)

Figure 3A — Examples of 1 mm X 1 mm Unit Cell 4X4 array chips

5 Date Presentation (cont'd)



Wire Bond Version
(Connected Cells)



Flip Chip Version
(Isolated Cells)

Figure 3B — Examples of 2.54 mm X 2.54 mm Unit Cell 2X3 array chips

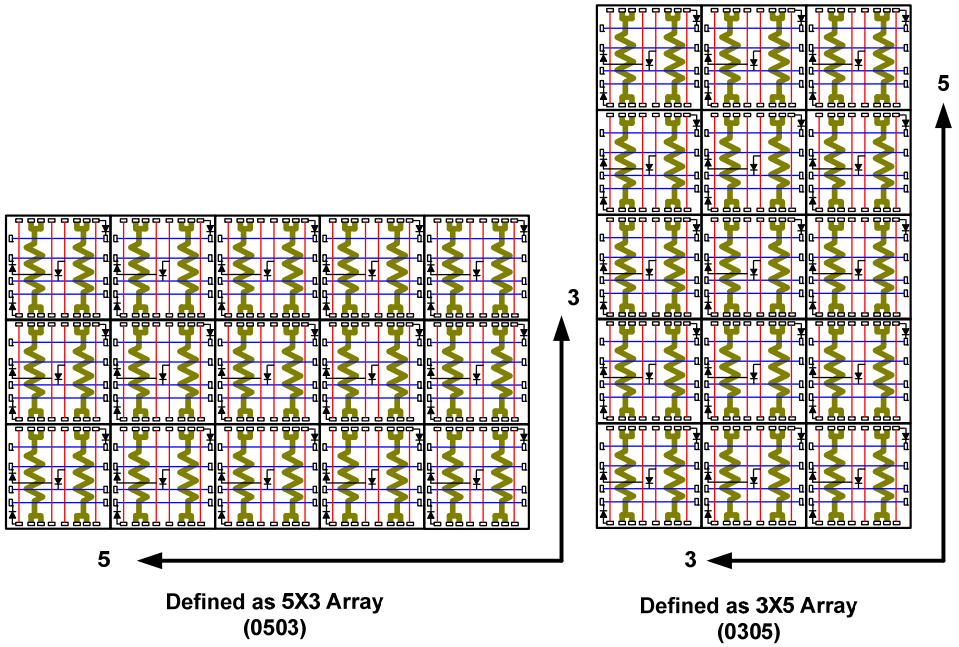


Figure 4 — Array Configuration Nomenclature
(Shown for 2.54 mm square Unit Cell but also applies for 1 mm square Unit Cell)

5 Date Presentation (cont'd)

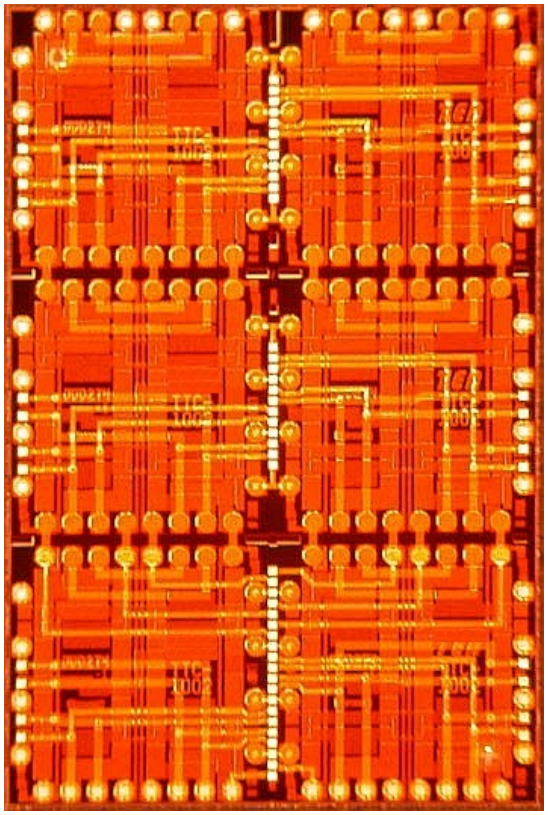


Figure 5 — Example of RDL applied to 2.54 mm X 2.54 mm Unit Cell 2X3 array chip

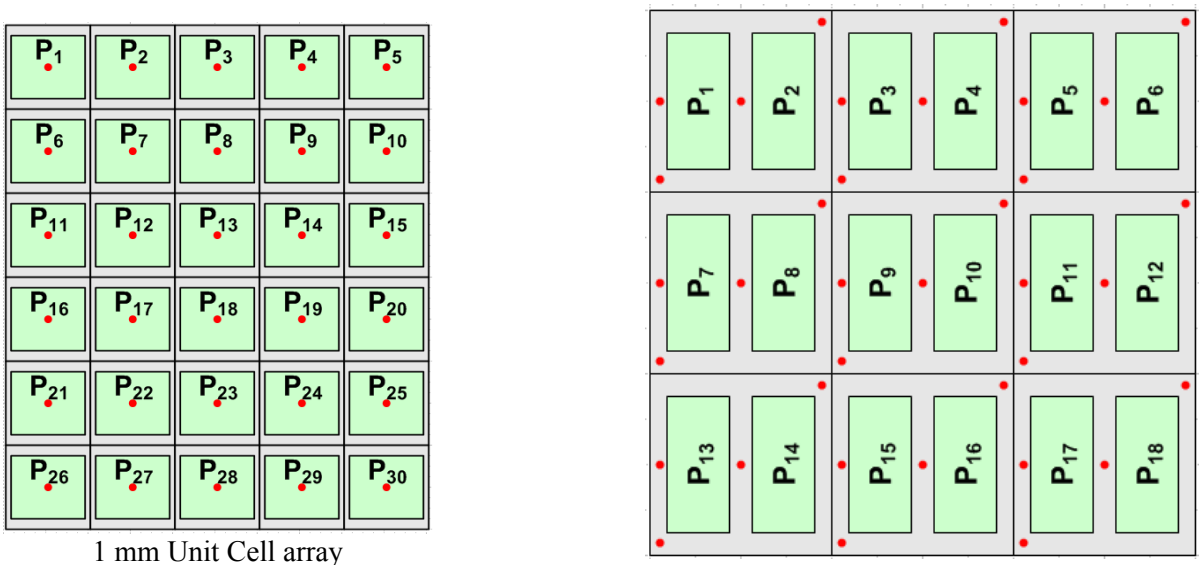


Figure 6 — Examples of Power Maps for array chips

Annex A 4-wire Kelvin Connections

When to use 4-wire Kelvin Connections for voltage measurement is determined by the measurement circuit and the level of current involved in producing the voltage to be measured.

In the case of Heater Voltage measurement for Thermal Test Chips, the connection circuit is -

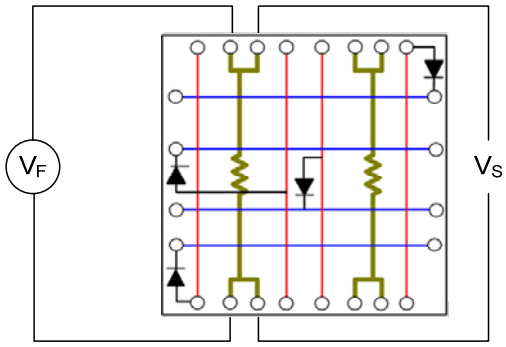


Figure A1a
Simplified Heater Connection Circuit

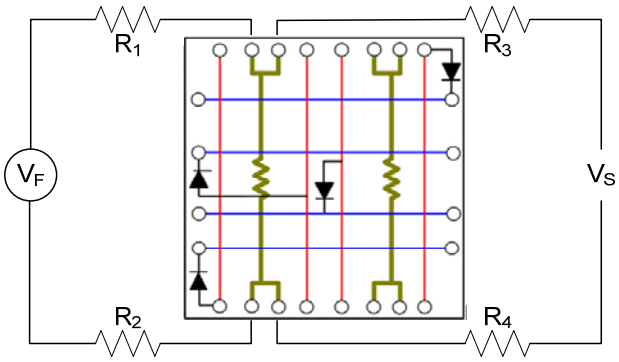


Figure A1b
Detailed Heater Connection Circuit

The simplified circuit of Figure A1a makes use of the dual connection pad at each end of the Heater Resistor – the larger Unit Cell is pictured but the connection circuit is equally applicable to the smaller Unit Cell (see Figures 2A and 2B). In this diagram, the power supply Voltage Force (V_F) is connected to a single pad at each end of the resistor. The voltage sense (V_S) measurement is made by connecting to the other set of resistor pads. When V_F is set to some voltage, V_S will read some lesser voltage, the difference in voltages being proportional to the amount of current drawn from the power supply. The explanation for this difference is shown in Figure A1b. The resistors R_1 & R_2 represent all the individual resistors in the path between the power supply and the Heating Resistor pads – power supply connector resistance to the wire, wire resistance, wire to pcb trace to package connection resistance, pcb trace resistance, pcb trace to package connection resistance, package lead (or ball) resistance, package to chip connection resistance, etc. The same type of resistances will occur on the Sense Voltage measurement side of the circuit, although some of the resistance values will be different; the actual wire may be significantly smaller, hence the wire resistance will be higher. For example purposes, assume the R_H is 7.5 Ω, the V_H is 6 V. Then I_H is 0.8A. If R_1 and R_2 are both 1 Ω each, then each will have a voltage drop of 0.8 V, resulting in an actual applied voltage of 4.4 V [= 6 V - (2 X 0.8 V)]. This lower voltage will significantly understate the power dissipation in the Heating Resistor if V_F is use to calculate power. If the Sense Voltage measurement instrument has a high input resistance, say 1MΩ or more (most typical DMMs have an input resistance ≥10 MΩ), then the 2 Ω associated with the connection circuit has negligible effect on the measured voltage – one part in 500,000 or less – and the V_S reading will be 4.40 V.

Annex A 4-wire Kelvin Connections (cont'd)

The same kind of connection circuit for measuring the Diode Temperature Sensor voltage (V_M) is shown in Figure A2.

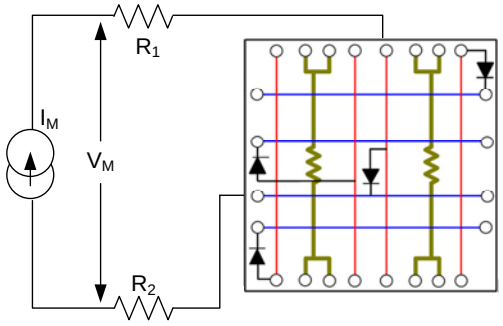


Figure A2
Diode Temperature Sensor Connection Circuit

The V_M measurement is done at the current source IM before R_1 and R_2. VM is equal to the sum of the voltage drops for each resistor plus the diode voltage drop, i.e.,

$$V_M = (R_1 \text{ X } I_M) + V_{Diode} + (R_2 \text{ X } I_M) \quad \text{(A.1)}$$

If R_1 and R_2 are each 1 Ω and I_M is 1 mA, then

$$V_M = V_{Diode} + 2mV \quad \text{(A.2)}$$

The V_{Diode} value is approximately 720mV at ~20 ºC, resulting in a V_M error of just 2 mV or 0.3%. If using V_{Diode} to measure absolute temperature, the resistance-caused offsets corresponds to about a 1 ºC error. The error can be eliminated by measuring V_{Diode} using the pads at the opposite side of the Unit Cell shown in Figure A2.

As most thermal measurements are based on temperature differentials, the voltage offset due to the connection resistors R_1 and R_2 drops out,

$$\Delta V_{Diode} = [V_{Diode2} + I_M(R_{1'} + R_{2'})] - [V_{Diode1} + I_M(R_1 + R_2)] \quad \text{(A.3)}$$

If $R_{1'}$ and $R_{2'}$ at temperature 2 equals R_1 and R_2 at temperature 1, respectively, and I_M remains constant.

The question as to whether the connection resistance are the same at two different temperature can be addressed by using the equation for the temperature coefficient of resistance equation –

$$R' = R[1 + \alpha(T' - T)] \quad \text{(A.4)}$$

where T' is the higher temperature
T is the lower temperature
R' is the resistance at T'
R is the resistance at T
α is the Temperature Coefficient of Resistance

Annex A 4-wire Kelvin Connections (cont'd)

Annex A 4-wire Kelvin Connections (cont'd)

The connection resistors R_1 and R_2 shown in Figure A2 are the result of the same assortment of elements discussed previously for the Heater Resistance – made mostly of Copper and Aluminum, with α values of 0.004041/ºC and 0.004308/ºC respectively. For example purposes, assume that each resistor is divided into half Copper conductor and half Aluminum conductor. Then the average α value is 0.004175/ºC. If T = 20 ºC and T' = 120 ºC, ΔT = 100 ºC. Inserting these values into Equation 4, R' = 1.4175R. However, in most semiconductor thermal measurements, the entire R1 and R2 resistors are not subjected to elevated temperature even when the semiconductor junction is at 120 ºC. Probably less than 20% of the resistance is subject to the higher temperature, thus R' = [1 + (0.4175/5)]R = 1.0835R. Under these conditions, comparing the results with and without correction for R1 and R2 temperature changes shows a difference error of 0.0835%. If this error level is acceptable, as it is in most thermal measurements, then no correction for resistance temperature change is necessary.

The same analysis applies to RTD sensors that may operate at more than 1 mA.

Annex B (informative) Differences between revisions

At time of publication a revision record was not provided.

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