JEDEC STANDARD

2.5 V BiCMOS Logic Device Family Specification with 5 V Tolerant Inputs and Outputs

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2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS

(From JEDEC Board Ballot JCB-98-43, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Purpose

The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use, thus providing compatibility between devices operating between 2.3 V and 2.7 V supply voltages, as well as overvoltage tolerance with devices operating at 3.3 V, or 5 V.

2 Scope

This standard defines dc interface parameters and test loading for digital logic devices based on 2.5 V (nominal) power supply levels.

3 Terms and definitions

prefixes: Prefixes “54” or “74” immediately preceding family name indicate the operating temperature range. For example, 54xxx refers to Military (MIL) version of devices that are specified over the temperature range of -55 °C to +125 °C. 74xxx refers to the Commercial (COM’L) version of devices that are specified over -40 °C to +85 °C.

4 Standard specifications

4.1 Absolute maximum continuous ratings[1, 2]

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{DD}	DC supply voltage		-0.5 to +3.6	V
V_{IN}	DC input voltage		-0.5 to +7.0	V
V_{OUT}	DC output voltage	Output in OFF state	-0.5 to +7.0	V
T_{stg}	Storage temperature range		-65 to +150	°C

NOTE 1 Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under these conditions is not implied.

NOTE 2 Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

4.2 Recommended operating conditions

SYMBOL	PARAMETER	2.5 V RANGE LIMITS		UNIT
		MIN	MAX	
V_{DD}	DC supply voltage	2.3	2.7	V
V_I	Input voltage	0	5.5	V
V_{IH}	High–level input voltage	1.7		V
V_{IL}	Input voltage		0.7	V
I_{OH}	High–level output current		-8	mA
I_{OL}	Low–level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free–air temperature range	-40	+85	°C

4 Standard specifications (cont'd)

4.3 DC specifications

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS		UNIT
				TEMP = –40 °C to +85 °C		
				MIN	MAX	
V_{IK}	Input clamp voltage	V_{DD} = 2.3 V; I_{IK} = -18 mA			-1.2	V
V_{OH}	High–level output voltage	V_{DD} = 2.3 to 2.7 V; I_{OH} = -100 µA		V_{DD} - 0.2		V
		V_{DD} = 2.3 V; I_{OH} = -8 mA		1.8		
		V_{DD} = 2.3 V; I_{OH} = -4 mA		2.0		
V_{OL}	Low–level output voltage	V_{DD} = 2.3 V; I_{OL} = 100 µA			0.2	V
		V_{DD} = 2.3 V; I_{OL} = 24 mA			0.5	
		V_{DD} = 2.3 V; I_{OL} = 8 mA			0.4	
I_I	Input leakage current	V_{DD} = 2.7 V; V_I = V_{DD} or GND	Input pins		±5	µA
		V_{DD} = 0 or 2.7 V; V_I = 5.5 V			10	
$I_{I/O}$	I/O leakage current	V_{DD} = 2.7 V; $V_{I/O}$ = 5.5 V	I/O pins[1]		20	µA
		V_{DD} = 2.7 V; $V_{I/O}$ = V_{DD}			10	
		V_{DD} = 2.7 V; $V_{I/O}$ = 0			-5	
I_{OFF}	Output off current	V_{DD} = 0 V; V_I or V_O = 0 to 5.5 V			±100	µA
I_{OZH}	3–state output HIGH current[2]	V_{DD} = 2.7 V; V_O = 2.3 V; V_I = V_{IL} or V_{IH}			5	µA
		V_{DD} = 2.7 V; V_O = 5.5 V; V_I = V_{IL} or V_{IH}			5	
I_{OZL}	3–state output LOW current[2]	V_{DD} = 2.7 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}			-5	µA
$I_{PU/PD}$	Power up/down 3–State output current[3]	V_{DD} ≤ 1.0 V; V_O = 0.5 V; V_I = GND or V_{DD}			100	µA

NOTE 1 Untested pins at V_{DD} or GND. I/O pins to be configured as inputs.

NOTE 2 This parameter not applicable for I/O pins. See $I_{I/O}$ for leakage currents on I/O pins.

NOTE 3 This parameter is valid for any V_{DD} between 0 V and 1.0 V with a transition time of up to 10 ms. From V_{DD} = 1.0 V to V_{DD} = 2.5 V ± 0.2 V a transition time of 100 µs is permitted.

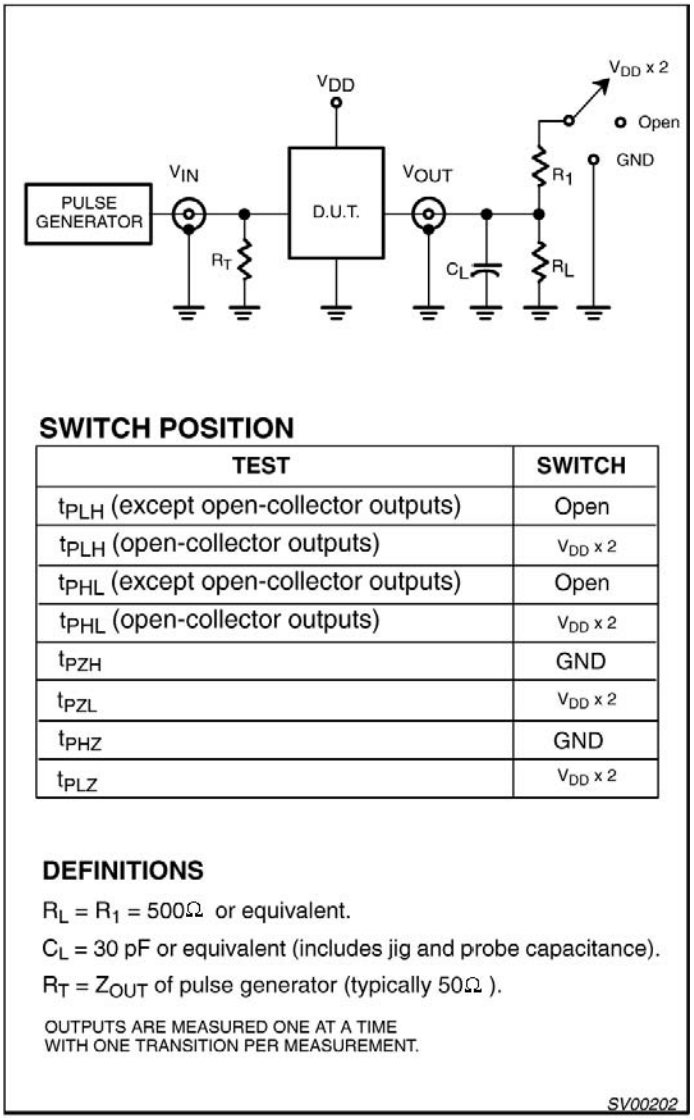
4 Standard specifications (cont'd)

4.4 Power supply characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			TEMP = –40 °C to +85 °C		
			MIN	MAX	
I_{CCH}	Quiescent supply current	V_{DD} = 2.7 V; Outputs High, V_I = GND or V_{DD}, I_O = 0		100	µA
I_{CCL}[1]		V_{DD} = 2.7 V; Outputs Low, V_I = GND or V_{DD}, I_O = 0		300	
I_{CCZ}[2]		V_{DD} = 2.7 V; Outputs Disabled; V_I = GND or V_{DD}, I_O = 0		100	

NOTE 1 The total current for this parameter is the current per output times the number of outputs in this state.
NOTE 2 I_{CCZ} is measured with outputs pulled up to V_{DD} or pulled down to ground.

5 Test circuit and waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLH} (except open-collector outputs)	Open
t_{PLH} (open-collector outputs)	V_{DD} x 2
t_{PHL} (except open-collector outputs)	Open
t_{PHL} (open-collector outputs)	V_{DD} x 2
t_{PZH}	GND
t_{PZL}	V_{DD} x 2
t_{PHZ}	GND
t_{PLZ}	V_{DD} x 2

DEFINITIONS

$R_L = R_1 = 500\Omega$ or equivalent.

C_L = 30 pF or equivalent (includes jig and probe capacitance).

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω).

OUTPUTS ARE MEASURED ONE AT A TIME
WITH ONE TRANSITION PER MEASUREMENT.

SV00202

Figure 1 — Test circuit

5 Test circuit and waveforms (cont'd)

5.1 Switching waveforms

$V_M = V_{DD}/2$, V_{IN} = GND to V_{DD}
$V_X = V_{OL} + 150$ mV
$V_Y = V_{OH} - 150$ mV

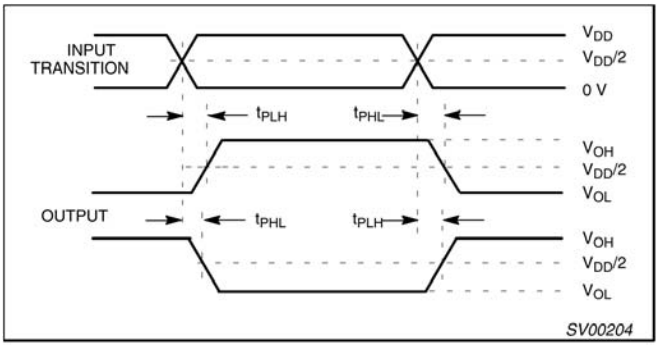


Figure 2 — Propagation Delay Measurements

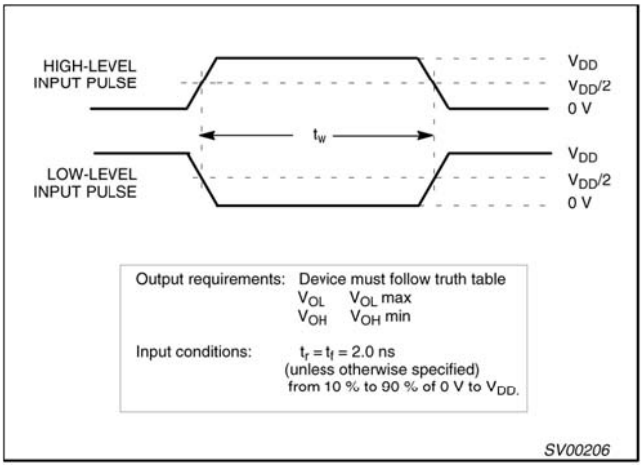


Figure 3 — Pulse Duration (Width) Measurements

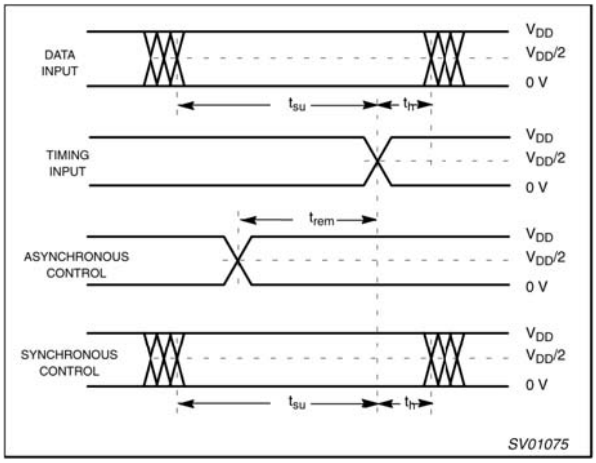


Figure 4 — Setup and Hold Time Measurements

5 Test circuit and waveforms (cont'd)

5.1 Switching waveforms (cont'd)

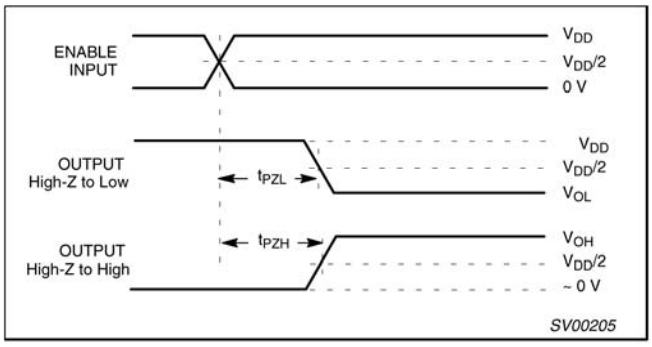


Figure 5 — Enable Time Measurements

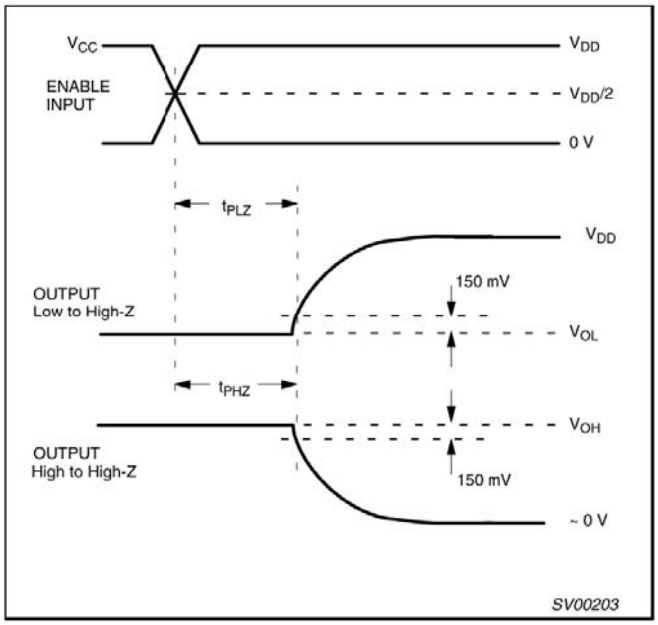
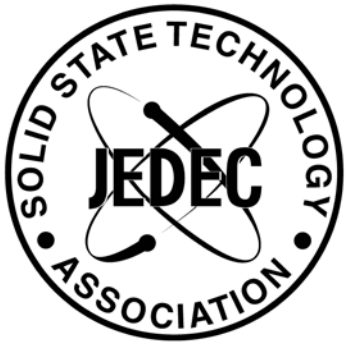


Figure 6 — Disable Time Measurements

6 Reference to other applicable JEDEC standards and publications

JEDEC Standard No. 8–5 2.5 V ± 0.2 V (Normal Range), Power Supply Voltage and Interface Standard for Non–terminated Integrated Circuit. (JESD8–5)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