JEDEC STANDARD

300 mV Interface

JESD8-28

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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300mV Interface Standard

(From JEDEC Board Ballot JCB-15-11, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard is to define and interface with a CMOS rail to rail signal that uses a 300 mV signal swing. This specification defines the maximum signaling rate, the signal levels, overshoot and undershoot limits, and the maximum input capacitance.

This interface is useful in short distance applications, typically of less than 5 mm. An important application of this interface is for in-package, die-to-die interconnection. In-package applications may also take advantage of reduced ESD (Electro-Static Discharge) tolerance requirements.

This interface may be used in both logic to memory and logic to logic applications. The memory used may be either volatile or non-volatile.

This specification only defines interface parameters. The function and interconnection of other parts of the devices is to be defined elsewhere.

2 Standard specifications

2.1 RECOMMENDED DC operation conditions

Table 1 — Recommended DC operation conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for Driver / Receiver	V_{DDQ}	0.285	0.3	0.315	V
Receiver Reference Voltage	V_{REF}	0.45* V_{DDQ}	0.5* V_{DDQ}	0.55* V_{DDQ}	V

2.2 V_{DDQ} tracking with internal logic voltage V_{DD}

At any time, the internal logic voltage V_{DD} should be equal or larger than V_{DDQ}.

2.3 Input capacitance definitions

Table 2 — Input capacitance definitions

Symbol	Parameter	Up to 2 Gbps		Units	Notes
		Min	Max		
C_{in}	Pad Capacitance – for all Input pins	-	0.4	pF	
C_{io}	Pad Capacitance – for BiDi pins	-	0.4	pF	

2.4 Signal levels for input signals[1].

Table 3 — Recommended operational signal voltage level specification

Parameter	Symbol	Min	Max	Unit*
Input High Voltage	V_{IH}	0.70 * V_{DDQ}	V_{DDQ} + 0.2	V
Input Low Voltage	V_{IL}	-0.2	0.30 * V_{DDQ}	V
* ALL SIGNAL LEVELS ARE REFERENCED TO V_{SSQ}.				

[1] Input signals include both Uni and BiDi signals.

2 Standard specifications (cont'd)

2.5 Receiver mask for input signals

Maximum input receiver mask will be a rectangular box shape between V_{IH} and V_{IL} and 45% of UI.

NOTE A UI is *Unit Interval* of time needed to send one data bit, as 1 / (data rate) or 1 / (data frequency *2 for DDR signal).

2.6 Slew rate for input signals

Minimum Input Slew rate when operating up to 2 Gbps will be 1 V/ns.

2.7 Overshoot/Undershoot conditions for input signals

Table 4 — Overshoot/Undershoot conditions for input signals

Parameter	Up to 2 Gbps	Units
	Max	
Maximum peak amplitude allowed for overshoot area (see Figure 1)	0.3	V
Maximum peak amplitude allowed for undershoot area (see Figure 1)	0.3	V
Maximum area above V_{DDQ} (see Figure 1)*	0.1	V-ns
Maximum area below V_{SSQ} (see Figure 1)*	0.1	V-ns
* Max/Min area is only for 2 Gbps		

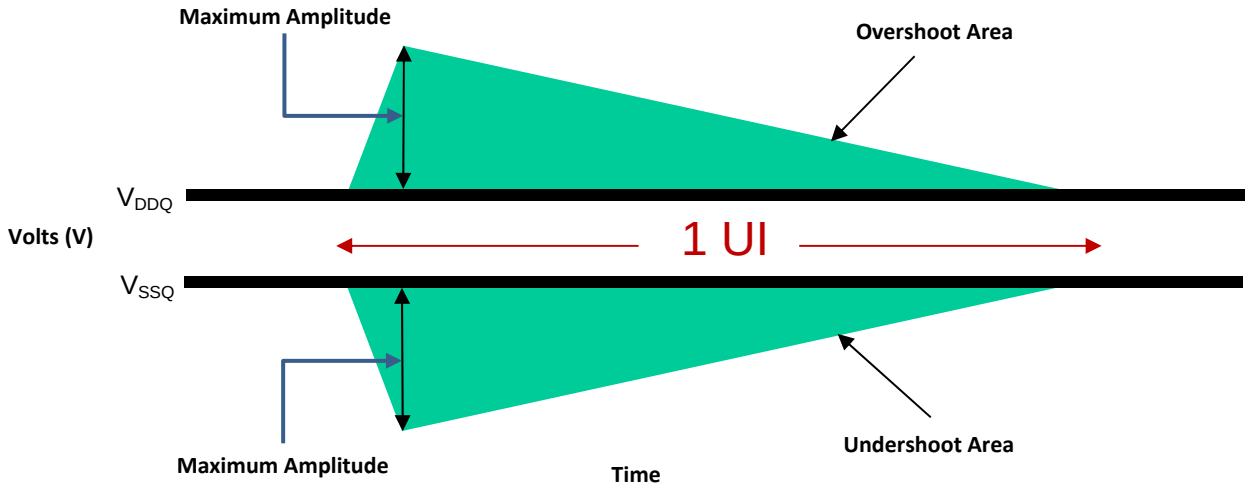

Figure 1 — Overshoot and Undershoot Definition

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