JEDEC STANDARD

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

JESD205

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Product Description

This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/ PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-DIMMs).These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the DIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 DIMM running at 266/333/400 MHz DRAM clock speed and offering 4266/5333/6400 MB/s bandwidth.

DIMM	DRAM	DRAM Clock	Single DIMM Bandwidth	Channel Clock	Channel Transfer Rate
PC2-4200	DDR2-533	266 MHz	4266 MB/s	133 MHz	3.2 GT/s
PC2-5300	DDR2-667	333 MHz	5333 MB/s	166 MHz	4.0 GT/s
PC2-6400	DDR2-800	400 MHz	6400 MB/s	200 MHz	4.8 GT/s

Reference design examples are included which provide an initial basis for Fully Buffered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-4200/PC2-5300/PC2-6400 support. All Fully Buffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design..

Product Family Attributes

DIMM organization	x72 ECC			
DIMM dimensions (nominal)	30.35mm (height) x 133.35mm (width) x 8.2 mm (max thickness) MO-256 variation AB 30.35mm (height) x 133.35mm (width) x 8.8 mm (max thickness) MO-256 variation BB			
Pin count	240			
SDRAMs supported	256Mb, 512Mb, 1Gb, 2Gb, 4Gb			
Capacity	256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB			
Serial PD	Consistent with JC 45			
Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})
Buffer Interface	High-speed Differential Point-to-point Link at 1.5 volt			
DRAM Interface	SSTL_18			

Note 1: Approximate DC values, refer to AMB Component Specification for actual DC and AC values and conditions.
Note 2: Vtt range accomodates measurable offset due to complementary CA bus current paths. (See Vtt section)
An Unloaded system should supply Vtt of 0.48*Vdd/0.52*Vdd to Dimm socket

The reference designs for the DIMM PCBs are called the “raw cards”, abbreviated R/C. After the designs have been verified in working systems, the JEDEC JC-45 committee will post registrations of these R/C designs to the JEDEC web site for use by the industry at large.

Product Family Raw Card Types

Raw Card	DRAM Data Width	# of Ranks	# of DRAM	Z-axis	Width x Height (mm)
A	x8	1	9	planar	133.35 x 30.35
B	x8	2	18	planar	133.35 x 30.35
C	x4	1	18	planar	133.35 x 30.35
D	x4	2	36	stacked / dual die	133.35 x 30.35
E	x4	2	36	planar	133.35 x 30.35
H	x4	2	36	planar	133.35 x 30.35
J	x4	2	36	stacked / dual die	133.35 x 30.35

Environmental Requirements

DDR2 SDRAM Fully Buffered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		1
H_{OPR}	Operating humidity (relative)	10 to 90	%	2
T_{STG}	Storage temperature	-50 to +100	°C	2
H_{STG}	Storage humidity (without condensation)	5 to 95	%	2
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	2

1. The designer must meet the case temperature specifications for individual module components.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Architecture

DIMM Connector Pin Description

Pin Name	Pin Description	Count
SCK	System Clock Input, positive line[1]	1
$\overline{\text{SCK}}$	System Clock Input, negative line[1]	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{\text{PN}}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{\text{PS}}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{\text{SN}}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{\text{SS}}$[9:0]	Secondary Southbound Data, negative lines	10
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is V_{DD} value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is V_{CC} value: OPEN = 1.5 V, GND = 1.2 V	2
$\overline{\text{RESET}}$	AMB reset signal	1
RFU	Reserved for Future Use[2]	16
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	8
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8 Volt)	24
V_{TT}	DRAM Address/Command/Clock Termination Power (V_{DD}/2)	4
V_{DDSPD}	SPD Power	1
V_{SS}	Ground	80
DNU/M_Test	The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time. 1	1
	Total	240

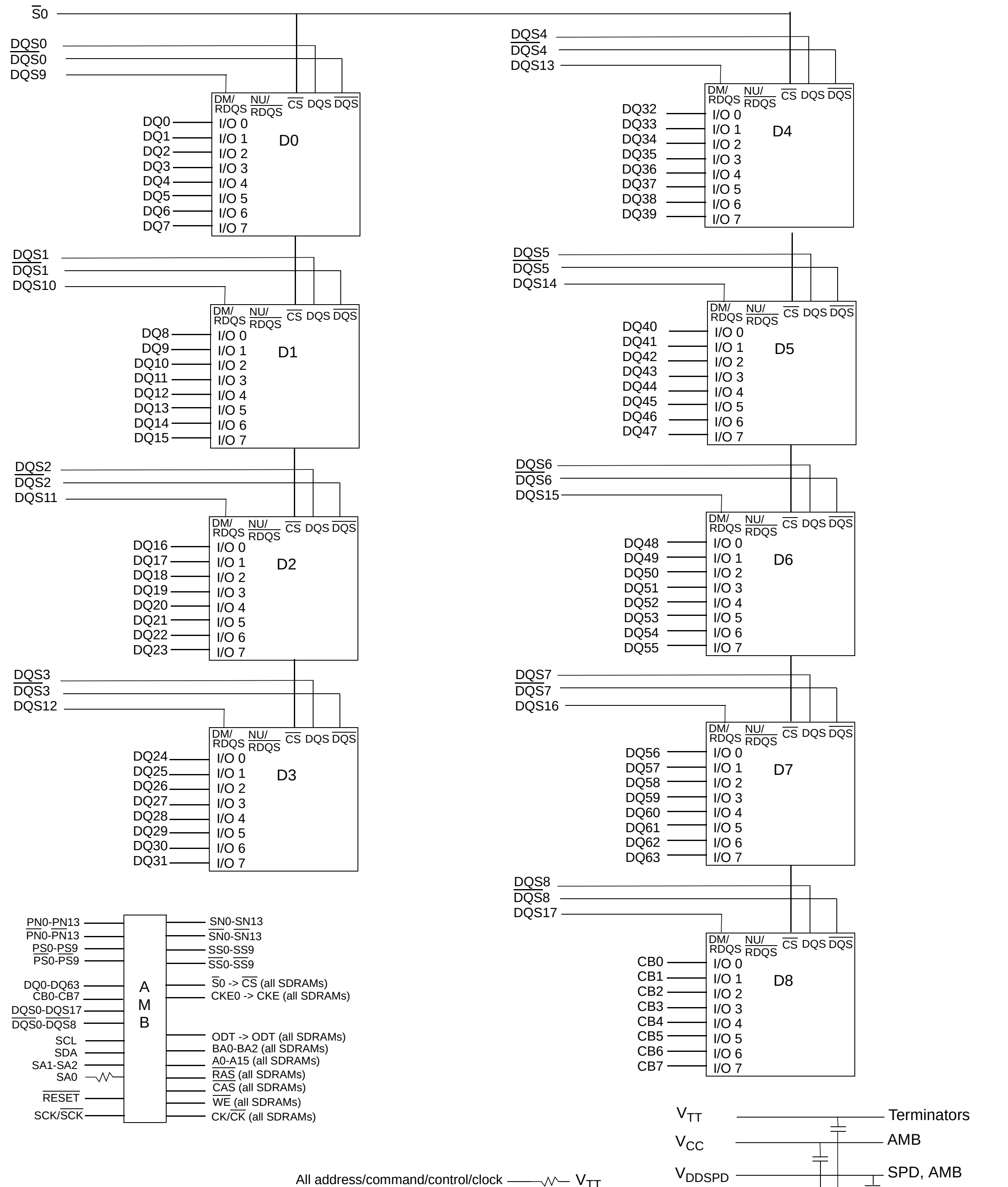
1. System Clock Signals SCK and $\overline{\text{SCK}}$ switch at one half the DRAM CK/$\overline{\text{CK}}$ frequency
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

DDR2 240-pin FBDIMM Pinout

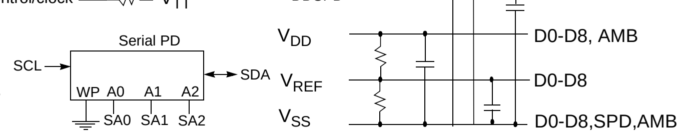
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{DD}	121	V_{DD}	31	PN3	151	SN3	61	$\overline{\text{PN9}}$	181	$\overline{\text{SN9}}$	91	$\overline{\text{PS9}}$	211	$\overline{\text{SS9}}$
2	V_{DD}	122	V_{DD}	32	$\overline{\text{PN3}}$	152	$\overline{\text{SN3}}$	62	V_{SS}	182	V_{SS}	92	V_{SS}	212	V_{SS}
3	V_{DD}	123	V_{DD}	33	V_{SS}	153	V_{SS}	63	PN10	183	SN10	93	PS5	213	SS5
4	V_{SS}	124	V_{SS}	34	PN4	154	SN4	64	$\overline{\text{PN10}}$	184	$\overline{\text{SN10}}$	94	$\overline{\text{PS5}}$	214	$\overline{\text{SS5}}$
5	V_{DD}	125	V_{DD}	35	$\overline{\text{PN4}}$	155	$\overline{\text{SN4}}$	65	V_{SS}	185	V_{SS}	95	V_{SS}	215	V_{SS}
6	V_{DD}	126	V_{DD}	36	V_{SS}	156	V_{SS}	66	PN11	186	SN11	96	PS6	216	SS6
7	V_{DD}	127	V_{DD}	37	PN5	157	SN5	67	$\overline{\text{PN11}}$	187	$\overline{\text{SN11}}$	97	$\overline{\text{PS6}}$	217	$\overline{\text{SS6}}$
8	V_{SS}	128	V_{SS}	38	$\overline{\text{PN5}}$	158	$\overline{\text{SN5}}$	68	V_{SS}	188	V_{SS}	98	V_{SS}	218	V_{SS}
9	V_{CC}	129	V_{CC}	39	V_{SS}	159	V_{SS}	KEY				99	PS7	219	SS7
10	V_{CC}	130	V_{CC}	40	PN13	160	SN13	69	V_{SS}	189	V_{SS}	100	$\overline{\text{PS7}}$	220	$\overline{\text{SS7}}$
11	V_{SS}	131	V_{SS}	41	$\overline{\text{PN13}}$	161	$\overline{\text{SN13}}$	70	PS0	190	SS0	101	V_{SS}	221	V_{SS}
12	V_{CC}	132	V_{CC}	42	V_{SS}	162	V_{SS}	71	$\overline{\text{PS0}}$	191	$\overline{\text{SS0}}$	102	PS8	222	SS8
13	V_{CC}	133	V_{CC}	43	V_{SS}	163	V_{SS}	72	V_{SS}	192	V_{SS}	103	$\overline{\text{PS8}}$	223	$\overline{\text{SS8}}$
14	V_{SS}	134	V_{SS}	44	RFU*	164	RFU*	73	PS1	193	SS1	104	V_{SS}	224	V_{SS}
15	V_{TT}	135	V_{TT}	45	RFU*	165	RFU*	74	$\overline{\text{PS1}}$	194	$\overline{\text{SS1}}$	105	RFU**	225	RFU**
16	VID1	136	VID0	46	V_{SS}	166	V_{SS}	75	V_{SS}	195	V_{SS}	106	RFU**	226	RFU**
17	$\overline{\text{RESET}}$	137	DNU/M_Test	47	V_{SS}	167	V_{SS}	76	PS2	196	SS2	107	V_{SS}	227	V_{SS}
18	V_{SS}	138	V_{SS}	48	PN12	168	SN12	77	$\overline{\text{PS2}}$	197	$\overline{\text{SS2}}$	108	V_{DD}	228	SCK
19	RFU**	139	RFU**	49	$\overline{\text{PN12}}$	169	$\overline{\text{SN12}}$	78	V_{SS}	198	V_{SS}	109	V_{DD}	229	$\overline{\text{SCK}}$
20	RFU**	140	RFU**	50	V_{SS}	170	V_{SS}	79	PS3	199	SS3	110	V_{SS}	230	V_{SS}
21	V_{SS}	141	V_{SS}	51	PN6	171	SN6	80	$\overline{\text{PS3}}$	200	$\overline{\text{SS3}}$	111	V_{DD}	231	V_{DD}
22	PN0	142	SN0	52	$\overline{\text{PN6}}$	172	$\overline{\text{SN6}}$	81	V_{SS}	201	V_{SS}	112	V_{DD}	232	V_{DD}
23	$\overline{\text{PN0}}$	143	$\overline{\text{SN0}}$	53	V_{SS}	173	V_{SS}	82	PS4	202	SS4	113	V_{DD}	233	V_{DD}
24	V_{SS}	144	V_{SS}	54	PN7	174	SN7	83	$\overline{\text{PS4}}$	203	$\overline{\text{SS4}}$	114	V_{SS}	234	V_{SS}
25	PN1	145	SN1	55	$\overline{\text{PN7}}$	175	$\overline{\text{SN7}}$	84	V_{SS}	204	V_{SS}	115	V_{DD}	235	V_{DD}
26	$\overline{\text{PN1}}$	146	$\overline{\text{SN1}}$	56	V_{SS}	176	V_{SS}	85	V_{SS}	205	V_{SS}	116	V_{DD}	236	V_{DD}
27	V_{SS}	147	V_{SS}	57	PN8	177	SN8	86	RFU*	206	RFU*	117	V_{TT}	237	V_{TT}
28	PN2	148	SN2	58	$\overline{\text{PN8}}$	178	$\overline{\text{SN8}}$	87	RFU*	207	RFU*	118	SA2	238	VDDSPD
29	$\overline{\text{PN2}}$	149	$\overline{\text{SN2}}$	59	V_{SS}	179	V_{SS}	88	V_{SS}	208	V_{SS}	119	SDA	239	SA0
30	V_{SS}	150	V_{SS}	60	PN9	180	SN9	89	V_{SS}	209	V_{SS}	120	SCL	240	SA1
								90	PS9	210	SS9				

RFU = Reserved Future Use.
* These pin positions are reserved for forwarded clocks to be used in future module implementations
** These pin positions are reserved for future architecture flexibility
1) The following signals are CRC bits and thus appear out of the normal sequence: PN12/$\overline{\text{PN12}}$, SN12/$\overline{\text{SN12}}$, PN13/$\overline{\text{PN13}}$, SN13/$\overline{\text{SN13}}$, PS9/$\overline{\text{PS9}}$, SS9/$\overline{\text{SS9}}$

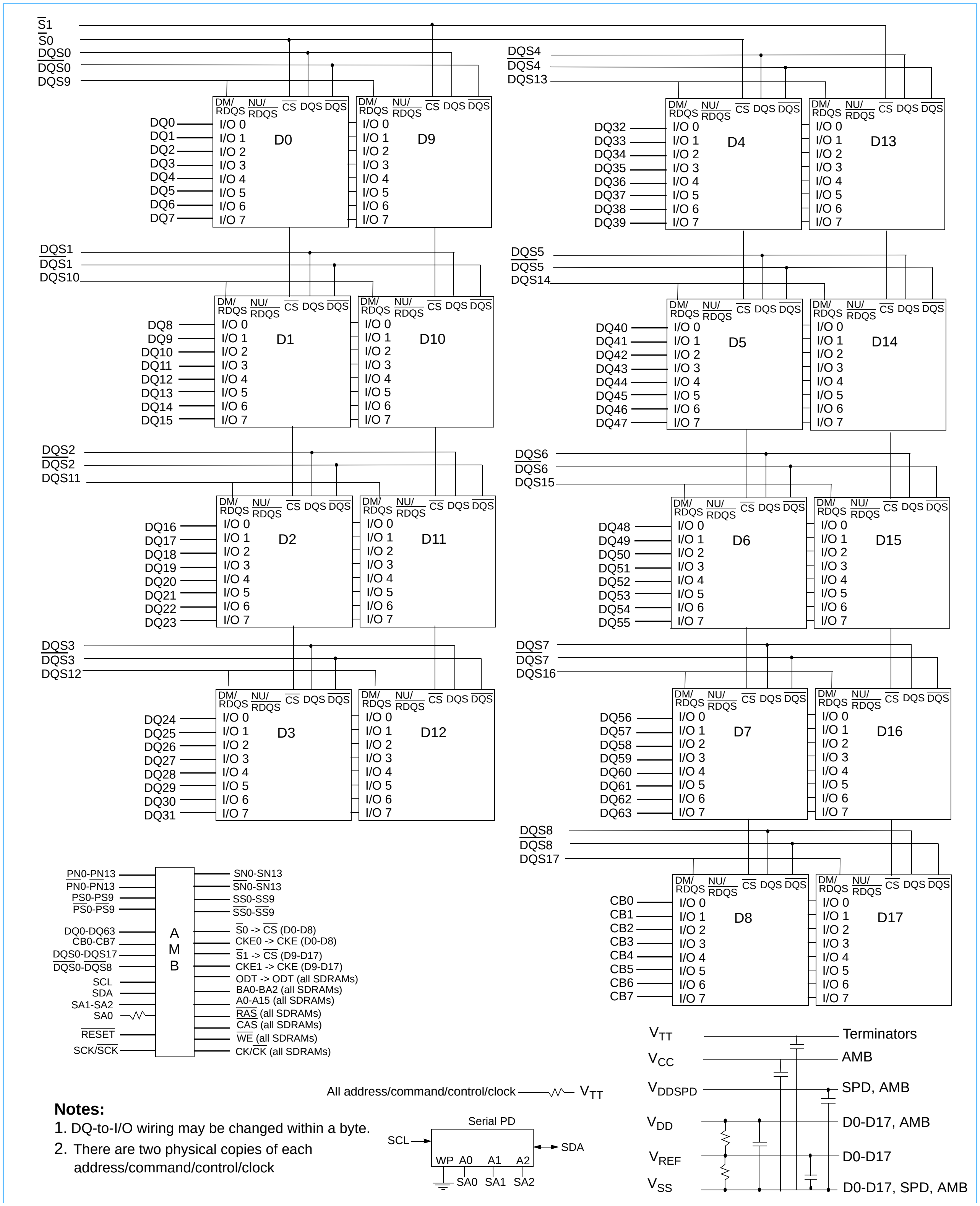
Block Diagram: Raw Card Version A (x72 ECC DIMM, one physical rank of x8 DDR2 SDRAMs)



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock

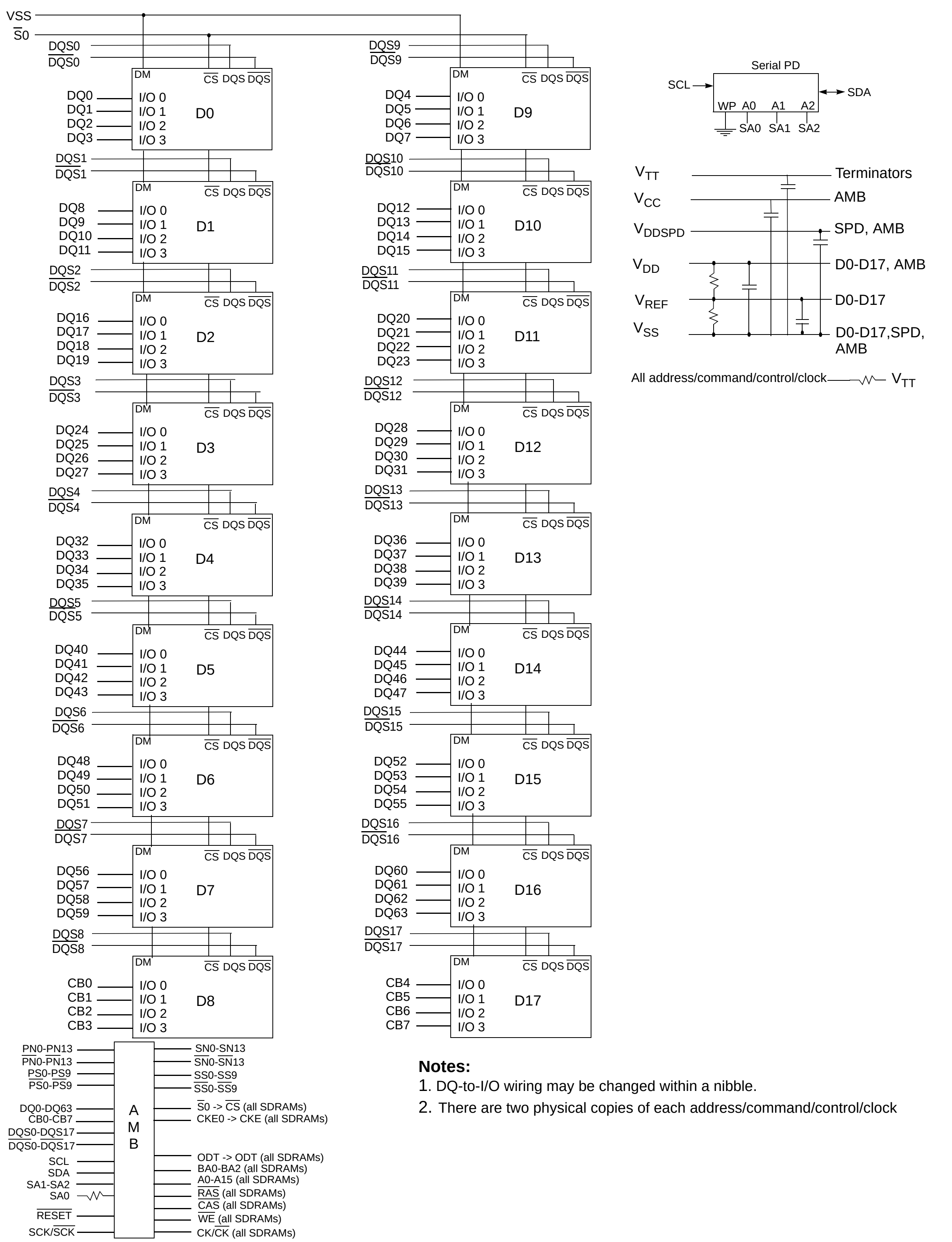


Block Diagram: Raw Card Version B (x72 ECC DIMMs, two physical ranks of x8 DDR2 SDRAMs)



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock

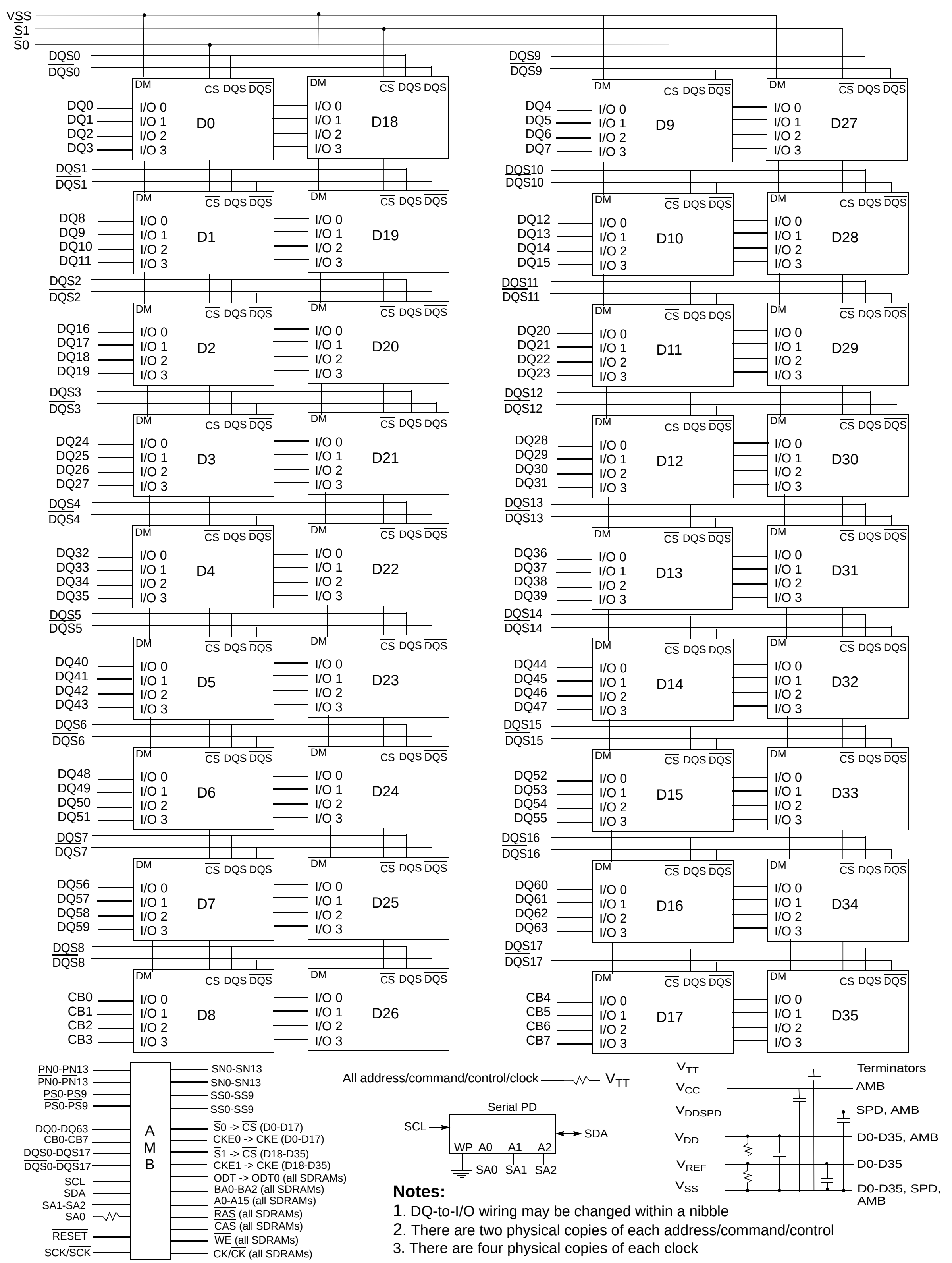
Block Diagram: Raw Card Version C (x72 ECC DIMM, one physical rank of x4 DDR2 SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a nibble.
2. There are two physical copies of each address/command/control/clock

Block Diagram: RC Versions D,E,H,J (x72 ECC DIMMs, 2 physical ranks of x4 DDR2 SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a nibble
2. There are two physical copies of each address/command/control
3. There are four physical copies of each clock

Component Details:

DDR2 SDRAM, 256 Mb to 4 Gb

Raw cards A and B accommodate the x8 ballout with or without support balls, using the x8 common footprint. Raw card C accommodates the x4 ballout with or without support balls, using the x4 common footprint. Raw card D accommodates the stacked x4 ballout with or without support balls, using the stacked x4 common footprint. The tables on the next few pages may include blank rows above the first row with balls, so that all of the tables line up with the common footprints for x4, x8 and stacked x4.

Pin Assignments for x4 and x8 Ballouts without Support Balls (Top View)

(MO-207 variation DJ-z, 60 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
B	NC	VSSQ	DM	DQS	VSSQ	NC
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	NC	VSSQ	DQ3	DQ2	VSSQ	NC
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
G	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
H		A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	
K		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	NU/ $\overline{\text{RDQS}}$	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
B	DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
G	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
H		A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	
K		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball A2 (NU/$\overline{\text{RDQS}}$) will be open on the x8 based DIMMs.

Pin Assignments for Stacked x4 Ballout without Support Balls (Top View)

(MO-242 variation AA, 63 Balls FBGA 0.8mm x 0.8mm pitch

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3		7	8	9
A	VDD	NC	VSS		VSSQ	$\overline{\text{DQS}}$	VDDQ
B	NC	VSSQ	DM		DQS	VSSQ	NC
C	VDDQ	DQ1	VDDQ		VDDQ	DQ0	VDDQ
D	NC	VSSQ	DQ3		DQ2	VSSQ	NC
E	VDDL	VREF	VSS		VSSDL	CK	VDD
F		CKE0	$\overline{\text{WE}}$		$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
G	BA2	BA0	BA1		$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$
H	CKE1	A10	A1		A2	A0	VDD
J	VSS	A3	A5		A6	A4	ODT1
K		A7	A9		A11	A8	VSS
L	VDD	A12	A14,NC		A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

Component Details: **DDR2 SDRAM Fully Buffered DIMM Design Specification**

Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DM-z, 68 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NC	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
F	NC	VSSQ	DM	DQS	VSSQ	NC
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	NC	VSSQ	DQ3	DQ2	VSSQ	NC
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
L	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NU/ $\overline{\text{RDQS}}$	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
F	DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
L	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball E2 (NU/$\overline{\text{RDQS}}$) will be open on the x8 based DIMMs.

Pin Assignments for Stacked x4 Ballout with Support Balls (Top View)

(MO-242 variation AD, 71 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NC	VSS	VSSQ	$\overline{DQS}$	VDDQ
F	NC	VSSQ	DM	DQS	VSSQ	NC
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	NC	VSSQ	DQ3	DQ2	VSSQ	NC
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE0	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT0
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS0}$	$\overline{CS1}$
M	CKE1	A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	ODT1
P		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

Component Details: **DDR2 SDRAM Fully Buffered DIMM Design Specification**

Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DL-z, 92 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D	VDD	NC	VSS	VSS	NC	VDD
E	NC	NC	NC	NC	NC	NC
F	NC	NC	NC	NC	NC	NC
G	NC	NC	NC	NC	NC	NC
H	VDD	NC	VSS	VSS	$\overline{\text{DQS}}$	VDD
J	NC	VSS	DM	DQS	VSS	NC
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NC	VSS	DQ3	DQ2	VSS	NC
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
P	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14,NC	A15,NC	A13,NC	
W						
Y						
AA	NC	NC			NC	NC

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D	VDD	NC	VSS	VSS	NC	VDD
E	NC	NC	NC	NC	NC	NC
F	NC	NC	NC	NC	NC	NC
G	NC	NC	NC	NC	NC	NC
H	VDD	NU/ $\overline{\text{RDQS}}$	VSS	VSS	$\overline{\text{DQS}}$	VDDQ
J	DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	DQ4	VSSQ	DQ3	DQ2	VSS	DQ5
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
P	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14,NC	A15,NC	A13,NC	
W						
Y						
AA	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB Symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball H2 (NU/$\overline{\text{RDQS}}$) will be open on the x8 based DIMMs.

Pin Assignments for Stacked x4 with Support Balls (Top View)

(MO-242 variation AC, 95 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3		7	8	9
A	NC	NC				NC	NC
B							
C							
D	VDD	NC	VSS		VSS	NC	VDD
E	NC	NC	NC		NC	NC	NC
F	NC	NC	NC		NC	NC	NC
G	NC	NC	NC		NC	NC	NC
H	VDD	NC	VSS		VSS	$\overline{\text{DQS}}$	VDD
J	NC	VSS	DM		DQS	VSS	NC
K	VDD	DQ1	VDD		VDD	DQ0	VDD
L	NC	VSS	DQ3		DQ2	VSS	NC
M	VDD	VREF	VSS		VSS	CK	VDD
N		CKE	$\overline{\text{WE}}$		$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
P	BA2	BA0	BA1		$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$
R		A10/AP	A1		A2	A0	VDD
T	VSS	A3	A5		A6	A4	ODT1
U		A7	A9		A11	A8	VSS
V	VDD	A12	A14,NC		A15,NC	A13,NC	
W							
Y							
AA	NC	NC				NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB Symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

Component Details: **DDR2 SDRAM Fully Buffered DIMM Design Specification**

Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DK-z, 84 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view) | x8 Ballout of DDR2 SDRAMs (Top view)

	x4: 1	x4: 2	x4: 3	x4: 7	x4: 8	x4: 9	x8: 1	x8: 2	x8: 3	x8: 7	x8: 8	x8: 9
A	VDD	NC	VSS	VSS	NC	VDD	VDD	NC	VSS	VSS	NC	VDD
B	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
E	VDD	NC	VSS	VSS	$\overline{DQS}$	VDD	VDD	NU/ $\overline{RDQS}$	VSS	VSS	$\overline{DQS}$	VDDQ
F	NC	VSS	DM	DQS	VSS	NC	DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7
G	VDD	DQ1	VDD	VDD	DQ0	VDD	VDD	DQ1	VDD	VDD	DQ0	VDD
H	NC	VSS	DQ3	DQ2	VSS	NC	DQ4	VSSQ	DQ3	DQ2	VSS	DQ5
J	VDD	VREF	VSS	VSS	CK	VDD	VDD	VREF	VSS	VSS	CK	VDD
K		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$		BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
M		A10/AP	A1	A2	A0	VDD		A10/AP	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4		VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC		VDD	A12	A14,NC	A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB Symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball E2 (NU/$\overline{RDQS}$) will be open on the x8 based DIMMs.

Pin Assignments for Stacked x4 Ballouts with Support Balls (Top View)

(MO-242 variation AD, 87 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3		7	8	9
A	VDD	NC	VSS		VSS	NC	VDD
B	NC	NC	NC		NC	NC	NC
C	NC	NC	NC		NC	NC	NC
D	NC	NC	NC		NC	NC	NC
E	VDD	NC	VSS		VSS	$\overline{\text{DQS}}$	VDD
F	NC	VSS	DM		DQS	VSS	NC
G	VDD	DQ1	VDD		VDD	DQ0	VDD
H	NC	VSS	DQ3		DQ2	VSS	NC
J	VDD	VREF	VSS		VSS	CK	VDD
K		CKE	$\overline{\text{WE}}$		$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
L	BA2	BA0	BA1		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	$\overline{\text{CS1}}$
M		A10/AP	A1		A2	A0	VDD
N	VSS	A3	A5		A6	A4	ODT1
P		A7	A9		A11	A8	VSS
R	VDD	A12	A14,NC		A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB Symbol on PCB

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

Pin Assignments for x4 and x8 PCB Symbol (Top View)

x4 Common Symbol on PCB (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NU	VSS	VSS	$\overline{\text{DQS}}$	VDD
J	NU	VSS	DM	DQS	VSS	NU
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NU	VSS	DQ3	DQ2	VSS	NU
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
P	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

x8 Common Symbol on PCB (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NC	VSS	VSS	$\overline{\text{DQS}}$	VDDQ
J	DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	DQ4	VSSQ	DQ3	DQ2	VSS	DQ5
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
P	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

1. Above coordinates of symbol corresponds to x4 and x8 ballouts of the DDR2 SDRAMs.

2. “NC” means that a solder pad is present and is not connected to any signal on the PCB. NC solder pads may be mated with any of the balls of an SDRAM. On the FB-DIMM x8 symbol, only ball H2 is NC.

3. “NU” means that the solder pad is present and may or may not be electrically connected to an active signal on the PCB. NU solder pads may only be mated with the NC ball of an SDRAM. On FB-DIMM, the NU solder pads will be either open, or connected to Vdd/VddQ. The NU pad may be a continuation of a surface plane utilized for power delivery purposes, thus it must only mate to a NC ball on the SDRAM.

Pin Assignments for Stacked x4 PCB Symbol (Top View)

x4 Common Symbol on PCB for Stacked DIMM (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NU	VSS	VSS	$\overline{\text{DQS}}$	VDD
J	NU	VSS	DM	DQS	VSS	NU
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NU	VSS	DQ3	DQ2	VSS	NU
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE0	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
P	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$
R	CKE1	A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	ODT1
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

1. Above coordinates of symbol corresponds to stacked x4 ballout of the DDR2 SDRAMs.

2. “NU” means that the solder pad is present and may or may not be electrically connected to an active signal on the PCB. NU solder pads may only be mated with the NC ball of an SDRAM. On FB-DIMM, the NU solder pads will be either open, or connected to Vdd/VddQ.   The NU pad may be a continuation of a surface plane utilized for power delivery purposes, thus it must only mate to a NC ball on the SDRAM.

Component Details

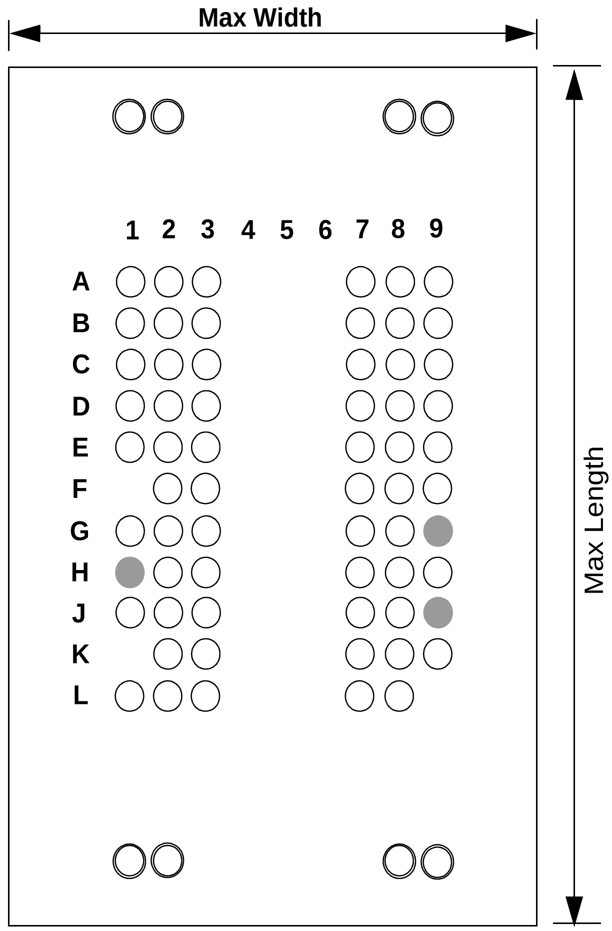
Supported SDRAM Component Maximum size for 256Mb to 4Gb, DDR2 SDRAM

Raw Card	Package Type	Supported DRAM Outline (Width x Length) max. (mm)			
		MO-207 Variation			
		DJ-z (60 pins)	DM-z (68 pins)	DL-z (92 pins)	DK-z (84 pins)
A	Planar	12.4 x 15	12.4 x 18	12.4 x 21	12.4 x 21
B,C	Planar	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21
E	Planar	11 x 11.5	--	--	--
H	Planar	12[4] x 11	--	--	--
		MO-242 Variation			
		AA (63 pins)	AD (71 pins)	AC (95 pins)	AB (87 pins)
D,J	Stacked	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21

1. supported only if no-decoupling capacitor are placed in between the DRAMs
2. 0.4 mm DRAM to DRAM spacing

3 Heat sink attachment may modify the max DRAM length that will fit to 18.6mm

4. Heat sink attachment may modify the max DRAM width that will fit to 11.5mm



Note: Double circles indicate the location of support balls of Variation DM-z
Gray circles indicate the balls for stacked only

Architecture

Advanced Memory Buffer Pin Description

Pin Name	Pin Description	Count
FB-DIMM Channel Signals		**99**
SCK	System Clock Input, positive line	1
$\overline{\text{SCK}}$	System Clock Input, negative line	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{\text{PN}}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{\text{PS}}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{\text{SN}}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{\text{SS}}$[9:0]	Secondary Southbound Data, negative lines	10
FBDRES	To an external precision calibration resistor connected to Vcc	1
DDR2 Interface Signals		**175**
DQS[8:0]	Data Strobes, positive lines	9
$\overline{\text{DQS}}$[8:0]	Data Strobes, negative lines	9
DQS[17:9]/DM[8:0]	Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
$\overline{\text{DQS}}$[17:9]	Data Strobes (x4 DRAM only), negative lines	9
DQ[63:0]	Data	64
CB[7:0]	Checkbits	8
A[15:0]A, A[15:0]B	Addresses. A10 is part of the pre-charge command	32
BA[2:0]A, BA[2:0]B	Bank Addresses	6
$\overline{\text{RASA}}$, $\overline{\text{RASB}}$	Part of command, with $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{CASA}}$, $\overline{\text{CASB}}$	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{WEA}}$, $\overline{\text{WEB}}$	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{CS}}$[1:0].	2
ODTA, ODTB	On-die Termination Enable	2
CKE[1:0]A, CKE[1:0]B	Clock Enable (one per rank)	4
$\overline{\text{CS}}$[1:0]A, $\overline{\text{CS}}$[1:0]B	Chip Select (one per rank)	4
CLK[3:0]	CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
$\overline{\text{CLK}}$[3:0]	Negative lines for CLK[3:0]	4
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_B12	DDR Compensation: Resistor connected to V_{SS}	1
DDRC_C12	DDR Compensation: Resistor connected to V_{DD}	1

Advanced Memory Buffer Pin Description

SPD Bus Interface Signals		5
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
Miscellaneous Signals		**163**
PLLTSTO	PLL Clock Observability Output	1
VCCAPLL	Analog VCC for the PLL. Tied with low pass filter to VCC.	1
VSSAPLL	Analog VSS for the PLL. Tied to ground on the AMB die. Do not tie to ground on the DIMM.	1
TEST_pin#	Leave floating on the DIMM	6
TESTLO_pin#	Tie to ground on the DIMM[2]	5
BFUNC	Tie to ground to set functionality as “buffer on DIMM.”	1
$\overline{\text{RESET}}$	AMB reset signal	1
NC	No connect. Many NC are connected to VDD on the DIMM, to lower the impedance of the VDD power islands.	129
RFU	Reserved for Future Use	18
Power/Ground Signals		**213**
V_{CC}	AMB Core Power (1.5 Volt)	24
V_{CCFBD}	AMB Channel I/O Power (1.5 Volt)	8
V_{DD}	AMB DRAM I/O Power (1.8 Volt)	24
V_{DDSPD}	SPD Power (3.3 Volt)	1
V_{SS}	Ground	156
	Total	**655**

1. System Clock Signals SCK and $\overline{\text{SCK}}$ switch at one half the DRAM CK/$\overline{\text{CK}}$ frequency.
2. TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes on prototype DIMMs: each pin should have a zero ohm resistor pulldown to ground, and an unpopulated resistor pullup to VCC. These resistors can be replaced on production DIMMs with a direct connection to ground.

Pin Assignments for the Advanced Memory Buffer (AMB) (Top View)

655-Ball LFBGA 0.8 mm x 0.8 mm pitch [MO-TBD]

Left Side

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			V_{SS}	DQ26	DQ12	V_{DD}	DQS10	DQ13	V_{DD}	$\overline{DQS1}$	DQ10	V_{DD}	TEST	V_{DD}	V_{DD}
B		V_{DD}	DQS3	$\overline{DQS3}$	V_{SS}	DQ14	$\overline{DQS10}$	V_{SS}	DQ11	DQS1	V_{SS}	DDRC	TESTLO	V_{DD}	V_{SS}
C	V_{SS}	DQS2	DQ18	V_{SS}	DQ4	$\overline{DQS9}$	V_{SS}	DQ15	DQ9	V_{SS}	DQ8	DDRC	V_{SS}	DDRC	DQS17
D	DQ19	$\overline{DQS2}$	V_{SS}	DQ16	DQ24	V_{SS}	DQS9	DQ7	V_{SS}	DQ3	DQS0	V_{SS}	$\overline{DQS8}$	DQS8	V_{DD}
E	DQ21	V_{SS}	DQ17	DQ29	V_{SS}	DQ25	DQ6	V_{SS}	DQ5	DQ1	V_{SS}	DQ0	CB1	V_{SS}	CB2
F	V_{SS}	DQ20	DQ23	V_{SS}	DQ31	DQ27	V_{SS}	TESTLO	TEST	V_{SS}	$\overline{DQS0}$	DQ2	V_{DD}	CB0	CB3
G	$\overline{DQS11}$	DQS11	NC	NC	NC	V_{SS}	DQS12	$\overline{DQS12}$	NC	NC	NC	BFUNC	RFU	RFU	RFU
H	DQ22	V_{SS}	NC	NC	NC	DQ28	DQ30	V_{SS}	NC	NC	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}
J	V_{SS}	CLK2	NC	NC	NC	BA1A	V_{SS}	CKE1A	NC	NC	NC	V_{DD}	V_{SS}	V_{DD}	V_{SS}
K	$\overline{CLK2}$	CLK0	NC	NC	NC	V_{SS}	$\overline{WEA}$	$\overline{RASA}$	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
L	$\overline{CLK0}$	V_{SS}	NC	NC	NC	A0A	CKE0A	V_{SS}	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
M	ODT0A	RFU	NC	NC	NC	$\overline{CASA}$	V_{SS}	BA2A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
N	$\overline{CS1A}$	$\overline{CS0A}$	NC	NC	NC	V_{SS}	BA0A	A10A	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
P	A6A	V_{SS}	NC	NC	NC	A2A	A1A	A3A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
R	V_{SS}	A8A	NC	NC	NC	A11A	V_{SS}	A5A	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
T	A4A	A13A	NC	NC	NC	V_{SS}	A9A	A7A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
U	PN0	$\overline{PN0}$	NC	NC	NC	A15A	A14A	A12A	NC	NC	NC	RFU	V_{CCFBD}	V_{SS}	V_{SS}
V	PN1	$\overline{PN1}$	V_{SS}	SN0	$\overline{SN0}$	V_{CCFBD}	V_{SS}	V_{CCFBD}	V_{SS}	RFU[a]	RFU[a]	V_{CCFBD}	V_{SS}	V_{SS}	V_{SS}
W	PN2	$\overline{PN2}$	V_{SS}	SN1	$\overline{SN1}$	$\overline{SN3}$	$\overline{SN4}$	$\overline{SN5}$	$\overline{SN13}$	$\overline{SN12}$	$\overline{SN6}$	$\overline{SN7}$	$\overline{SN8}$	$\overline{SN9}$	$\overline{SN10}$
Y	PN3	$\overline{PN3}$	V_{SS}	SN2	$\overline{SN2}$	SN3	SN4	SN5	SN13	SN12	SN6	SN7	SN8	SN9	SN10
AA	V_{SS}	PN4	$\overline{PN4}$	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
AB		V_{SS}	$\overline{RESET}$	$\overline{PN5}$	$\overline{PN13}$	RFU[a]	$\overline{PN12}$	$\overline{PN6}$	$\overline{PN7}$	$\overline{PN8}$	$\overline{PN9}$	V_{SSAPLL}	V_{CCAPLL}	$\overline{PN10}$	$\overline{PN11}$
AC			V_{SS}	PN5	PN13	RFU[a]	PN12	PN6	PN7	PN8	PN9	FBDRES	PLL TSTO	PN10	PN11
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

Right Side

	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	V_{DD}	TEST	V_{DD}	DQ52	DQS15	V_{DD}	DQ49	$\overline{DQS6}$	V_{DD}	DQ48	DQ38	V_{DD}		
B	V_{DD}	TEST	DDRC	V_{SS}	$\overline{DQS15}$	DQ53	V_{SS}	DQS6	DQ50	V_{SS}	$\overline{DQS13}$	DQS13	V_{SS}	
C	$\overline{DQS17}$	V_{SS}	DDRC	DQ54	V_{SS}	DQ55	DQ51	V_{SS}	DQS7	DQ56	V_{SS}	DQ46	$\overline{DQS14}$	V_{DD}
D	CB6	CB7	V_{SS}	DQS16	DQ63	V_{SS}	DQ59	$\overline{DQS7}$	V_{SS}	DQ36	DQ44	V_{SS}	DQS14	DQ47
E	V_{SS}	CB5	$\overline{DQS16}$	V_{SS}	DQ61	DQ57	V_{SS}	DQ58	DQ39	V_{SS}	DQ33	DQ45	V_{SS}	DQ41
F	CB4	V_{DD}	DQ62	DQ60	V_{SS}	TEST	TEST	V_{SS}	DQ37	DQ35	V_{SS}	$\overline{DQS5}$	DQ43	V_{SS}
G	TESTLO	RFU	RFU	NC	NC	NC	DQS4	$\overline{DQS4}$	V_{SS}	NC	NC	NC	DQS5	DQ40
H	V_{SS}	V_{DD}	V_{SS}	NC	NC	NC	V_{SS}	DQ34	DQ32	NC	NC	NC	V_{SS}	DQ42
J	V_{DD}	V_{SS}	V_{DD}	NC	NC	NC	$\overline{RASB}$	V_{SS}	RFU	NC	NC	NC	$\overline{CLK3}$	V_{SS}
K	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	ODT0B	$\overline{CS1B}$	V_{SS}	NC	NC	NC	$\overline{CLK1}$	CLK3
L	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	V_{SS}	$\overline{CASB}$	$\overline{WEB}$	NC	NC	NC	V_{SS}	CLK1
M	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	$\overline{CS0B}$	V_{SS}	BA1B	NC	NC	NC	CKE0B	V_{SS}
N	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	A0B	A2B	V_{SS}	NC	NC	NC	BA0B	BA2B
P	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	V_{SS}	A4B	A1B	NC	NC	NC	V_{SS}	CKE1B
R	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	A6B	V_{SS}	A10B	NC	NC	NC	A3B	V_{SS}
T	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	A11B	A9B	V_{SS}	NC	NC	NC	A7B	A5B
U	V_{SS}	V_{CCFBD}	RFU	NC	NC	NC	A8B	A15B	A14B	SA0	SCL	SDA	$\overline{PS8}$	PS8
V	V_{CCFBD}	V_{SS}	V_{CCFBD}	V_{SS}	V_{CCFBD}	RFU[a]	RFU[a]	V_{SS}	A13B	A12 B	SA2	SA1	$\overline{PS7}$	PS7
W	V_{SS}	$\overline{SS0}$	$\overline{SS1}$	$\overline{SS2}$	$\overline{SS3}$	$\overline{SS4}$	$\overline{SS9}$	$\overline{SS5}$	$\overline{SS6}$	$\overline{SS7}$	$\overline{SS8}$	V_{SS}	$\overline{PS6}$	PS6
Y	V_{SS}	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	V_{SS}	$\overline{PS5}$	PS5
AA	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$\overline{PS9}$	PS9	V_{SS}
AB	V_{SS}	$\overline{SN11}$	V_{SS}	SCK	TESTLO	$\overline{PS0}$	$\overline{PS1}$	$\overline{PS2}$	$\overline{PS3}$	$\overline{PS4}$	RFU[a]	V_{DDSPD}	V_{SS}	
AC	RFU	SN11	V_{SS}	$\overline{SCK}$	TESTLO	PS0	PS1	PS2	PS3	PS4	RFU[a]	V_{SS}		
	16	17	18	19	20	21	22	23	24	25	26	27	28	29

a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

Advanced Memory Buffer (AMB) DRAM Interface Specifications

Please refer to the AMB Specification for all technical requirements.

The following specifications for the AMB constitute the subset which is critical for proper operation of the DDR2 SDRAM interface..

Critical AMB Specifications

Symbol	Parameter	Type	V_{DDQ} = 1.8 V ± 0.1 V		Units	Notes
			Min	Max		
t_{SU}	DQ to DQS/$\overline{DQS}$ setup time (read)	Input		-425	ps	1
t_H	DQ to DQS/$\overline{DQS}$ hold time (read)	Input		825	ps	1
tDVBamb	AMB Data Valid Before DQS	Output	470		ps	1
tDVAamb	AMB Data Valid After DQS	Output	470		ps	1
tCVBamb	C/A/CNTL Valid Before Clock	Output	1030		ps	1
tCVAamb	C/A/CNTL Valid After Clock	Output	890		ps	1
$t_{DQSCKamb}$	DQS/$\overline{DQS}$-to-CK/$\overline{CK}$ output skew	Output	-190	190	ps	1
C_{IN}	Input Capacitance (DQ/DQS/$\overline{DQS}$)		2.0	2.5	pF	1

Note 1: The timing numbers are for example only. Design should be based on the latest AMB component specifications

AMB Sourcing

This document is not intended to be an approved vendor list for support components. Although it is recommended that all DDR2 SDRAM FBDIMM AMBs meet the specifications documented above, it is up to each DIMM producer to select the AMB and AMB vendors which meet these requirements.

DDR2 Fully Buffered DIMM Details

DDR2 SDRAM Module Configurations (Reference Designs)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Ranks	# of Banks in SDRAM	# of Address bits row/col/Bank
	Capacity	Organization	Density	Organization					
A	256MB	32Mx72	256Mbit	32Mx8	9	60 Ball FBGA	1	4	13/10/2
	512MB	64Mx72	512Mbit	64Mx8	9	60 Ball FBGA	1	4	14/10/2
	1GB	128Mx72	1Gbit	128Mx8	9	60 Ball FBGA	1	8	14/10/3
	2GB	256Mx72	2Gbit	256Mx8	9	60 Ball FBGA	1	8	15/10/3
	4GB	512Mx72	4Gbit	512Mx8	9	60 Ball FBGA	1	8	16/10/3
B	512MB	64Mx72	256Mbit	32Mx8	18	60 Ball FBGA	2	4	13/10/2
	1GB	128Mx72	512Mbit	64Mx8	18	60 Ball FBGA	2	4	14/10/2
	2GB	256Mx72	1Gbit	128Mx8	18	60 Ball FBGA	2	8	14/10/3
	4GB	512Mx72	2Gbit	256Mx8	18	60 Ball FBGA	2	8	15/10/3
	8GB	1Gx72	4Gbit	512Mx8	18	60 Ball FBGA	2	8	16/10/3
C	512MB	64Mx72	256Mbit	64Mx4	18	60 Ball FBGA	1	4	13/11/2
	1GB	128Mx72	512Mbit	128Mx4	18	60 Ball FBGA	1	4	14/11/2
	2GB	256Mx72	1Gbit	256Mx4	18	60 Ball FBGA	1	8	14/11/3
	4GB	512Mx72	2Gbit	512Mx4	18	60 Ball FBGA	1	8	15/11/3
	8GB	1Gx72	4Gbit	1Gbx4	18	60 Ball FBGA	1	8	16/11/3
D, J, E, H	1GB	64Mx72	256Mbit	64Mx4	36	63 Ball FBGA	2	4	13/11/2
	2GB	128Mx72	512Mbit	128Mx4	36	63 Ball FBGA	2	4	14/11/2
	4GB	256Mx72	1Gbit	256Mx4	36	63 Ball FBGA	2	8	14/11/3
	8GB	512Mx72	2Gbit	512Mx4	36	63 Ball FBGA	2	8	15/11/3
	16GB	1Gx72	4Gbit	1Gbx4	36	63 Ball FBGA	2	8	16/11/3

DDR2 Fully Buffered DIMM Design File Releases

'Reference' design file updates will be released as needed. This Fully Buffered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated. The following table outlines the most recent design file releases.

Raw Card Version	Specification Revision	Applicable Design File	Notes
A	0.5	TBD	TBD
B	0.5	TBD	TBD
C	0.4	TBD	TBD
D	0.4	TBD	TBD
E	0.41	TBD	TBD
H	0.5	TBD	TBD

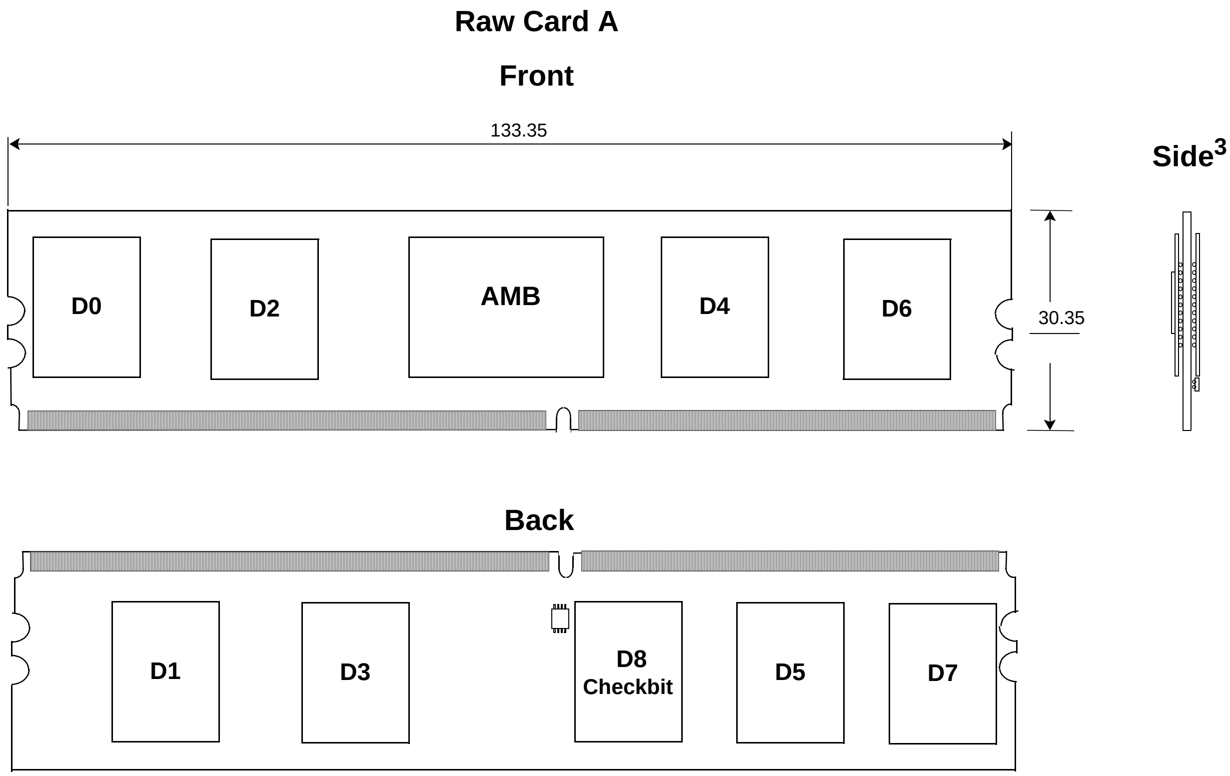
Raw Card Version	Specification Revision	Applicable Design File	Notes
J	0.3	TBD	TBD

Component Types and Placement

Components shall be surface mounted on one or both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR2 SDRAM signals. Bypass capacitors for DDR2 SDRAM devices must be located near the device power pins.

The following layouts suggest placement for the Raw Cards. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

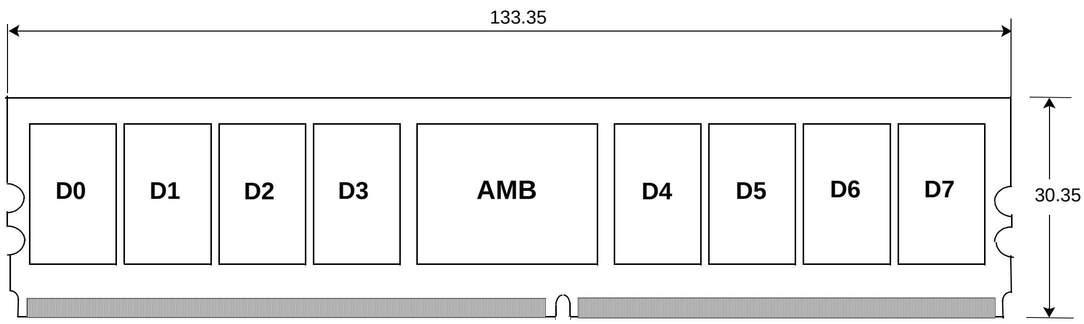
This example is for reference only; please refer to JEDEC standard MO-256 for details.



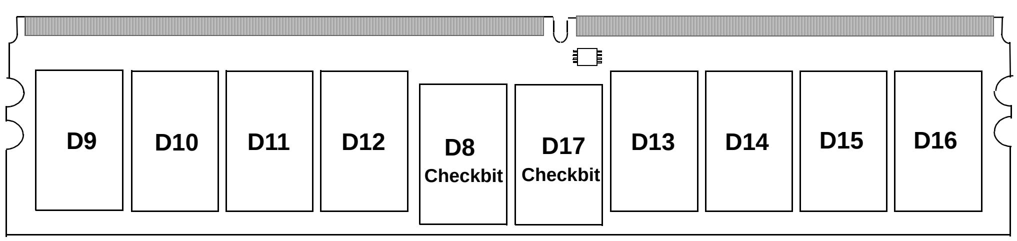
Note 1: All dimensions (in mm) are typical unless otherwise stated.
Note 2: Support for 16.5 mm wide by 21.9 mm tall DRAM footprint.
Note 3: Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

Raw Cards B and C

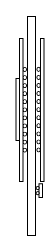
Front



Back



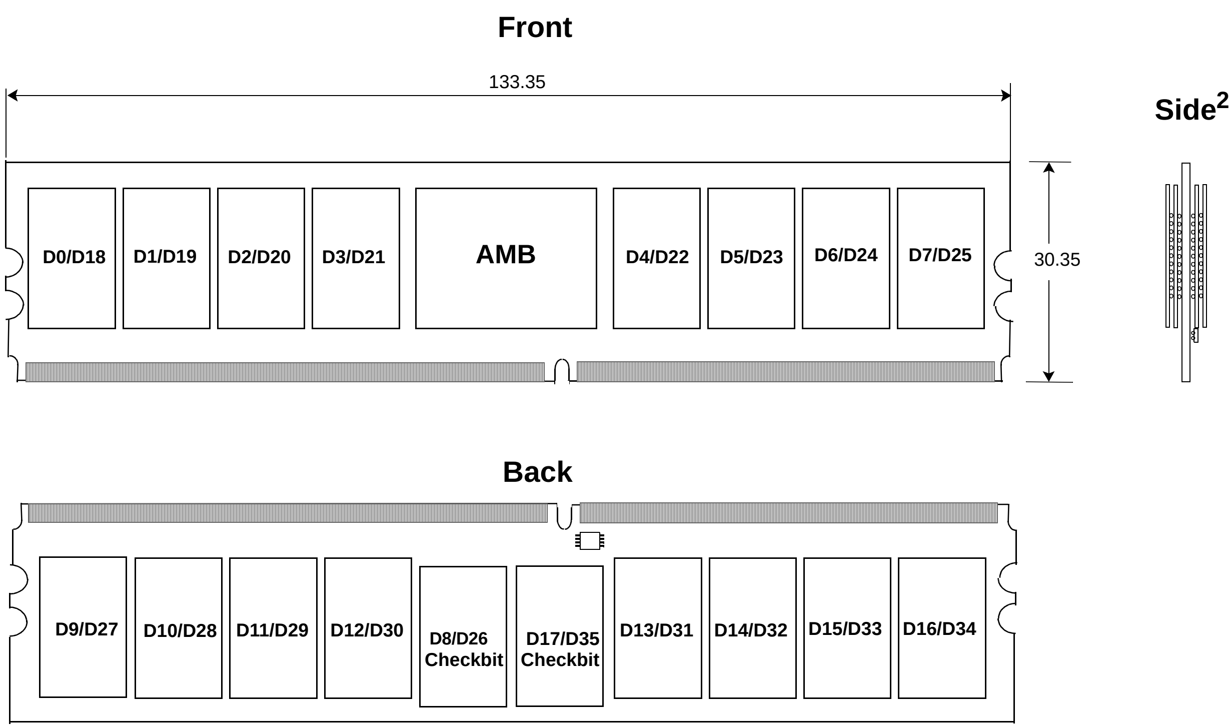
Side[2]



Note 1: All dimensions (in mm) are typical unless otherwise stated.

Note 2: Heat Spreader Assembly not shown,
refer to MO-256 for thickness dimensions.

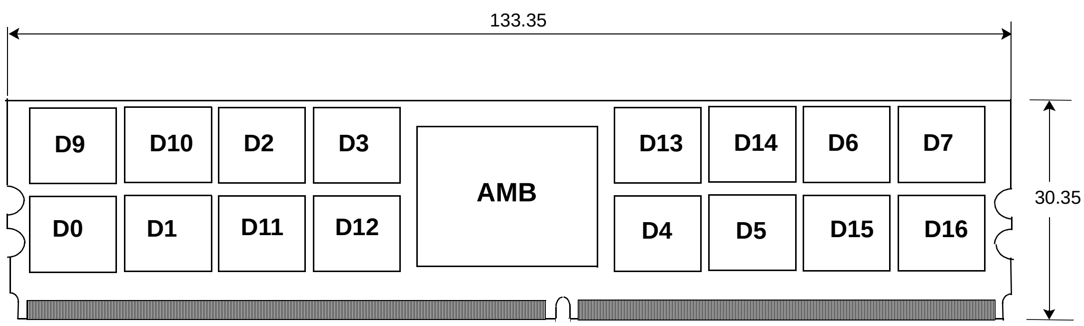
Raw Cards D and J



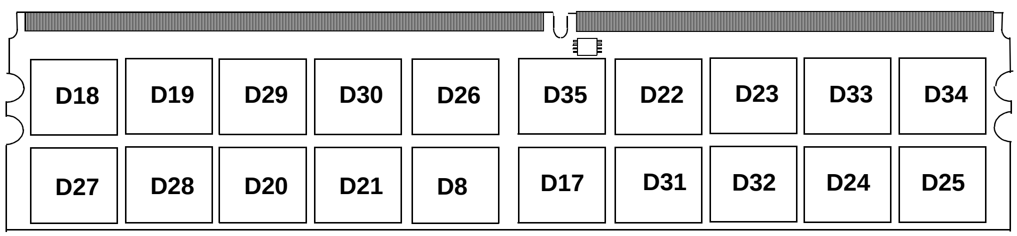
Note 1: All dimensions (in mm) are typical unless otherwise stated.
Note 2: Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

Raw Cards E and H

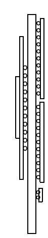
Front



Back



Side[2]



Note 1: All dimensions (in mm) are typical unless otherwise stated.

Note 2: Heat Spreader Assembly not shown,
refer to MO-256 for thickness dimensions.

DDR2 Fully Buffered DIMM Biasing Details

Common AMB Bias Detail

This specification documents the common biasing circuit topology for AMB devices as used on FB-DIMMs. While specific component values are not documented, the circuit topologies are included.

AMBs from different vendors may have specific requirements for BIAS inputs. It is incumbent on users to select correct components to ensure AMB specific requirements are met.

Diagrams are separated by functional groups DDR, PLL, Miscellaneous Explanation of Bias Diagrams.

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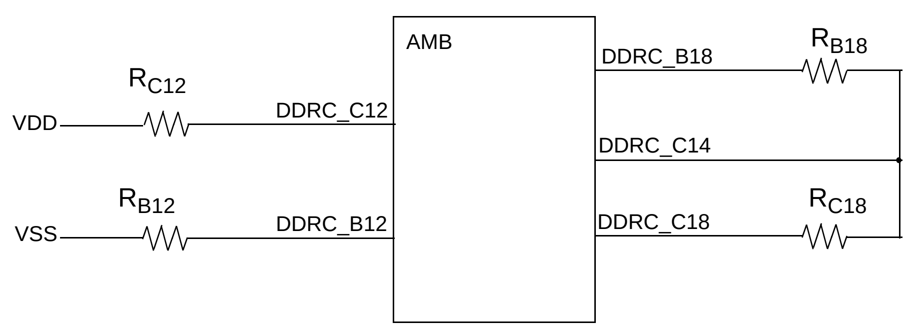
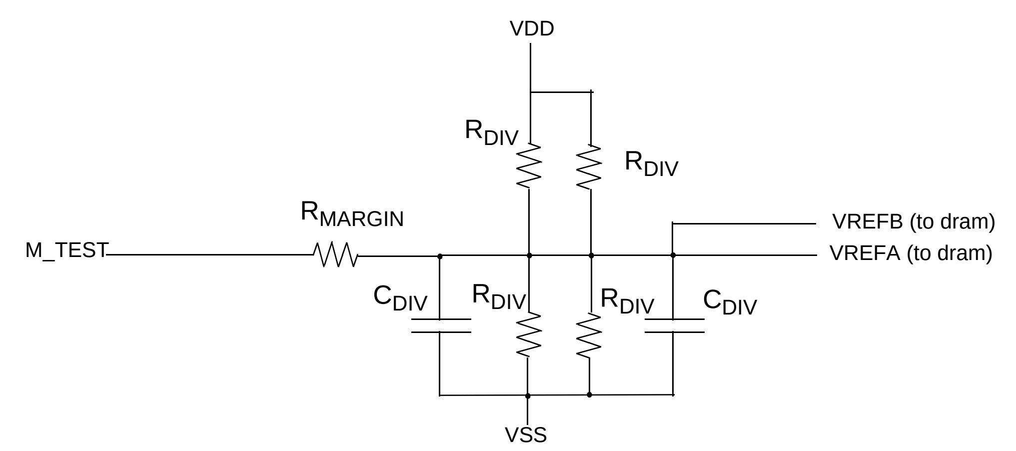
DDR Bias



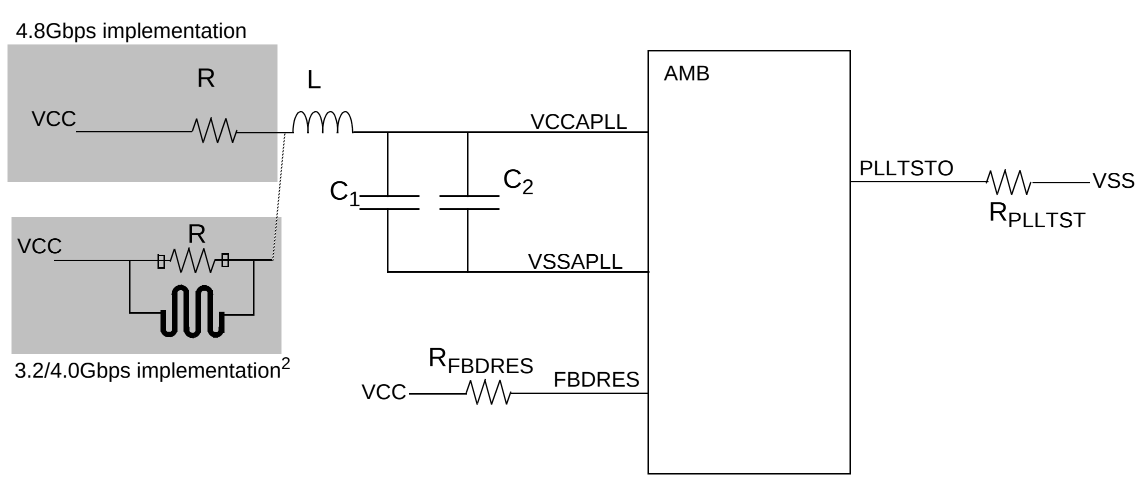
DDR Bias is composed of compensation resistors that implement compensation control of AMB DDR interface. AMB internal implementation details and component values may vary but the topology shown is sufficient for all AMB devices. Some AMB's may not require these components. See following table of Vendor reference material.

DDR VREF BIAS



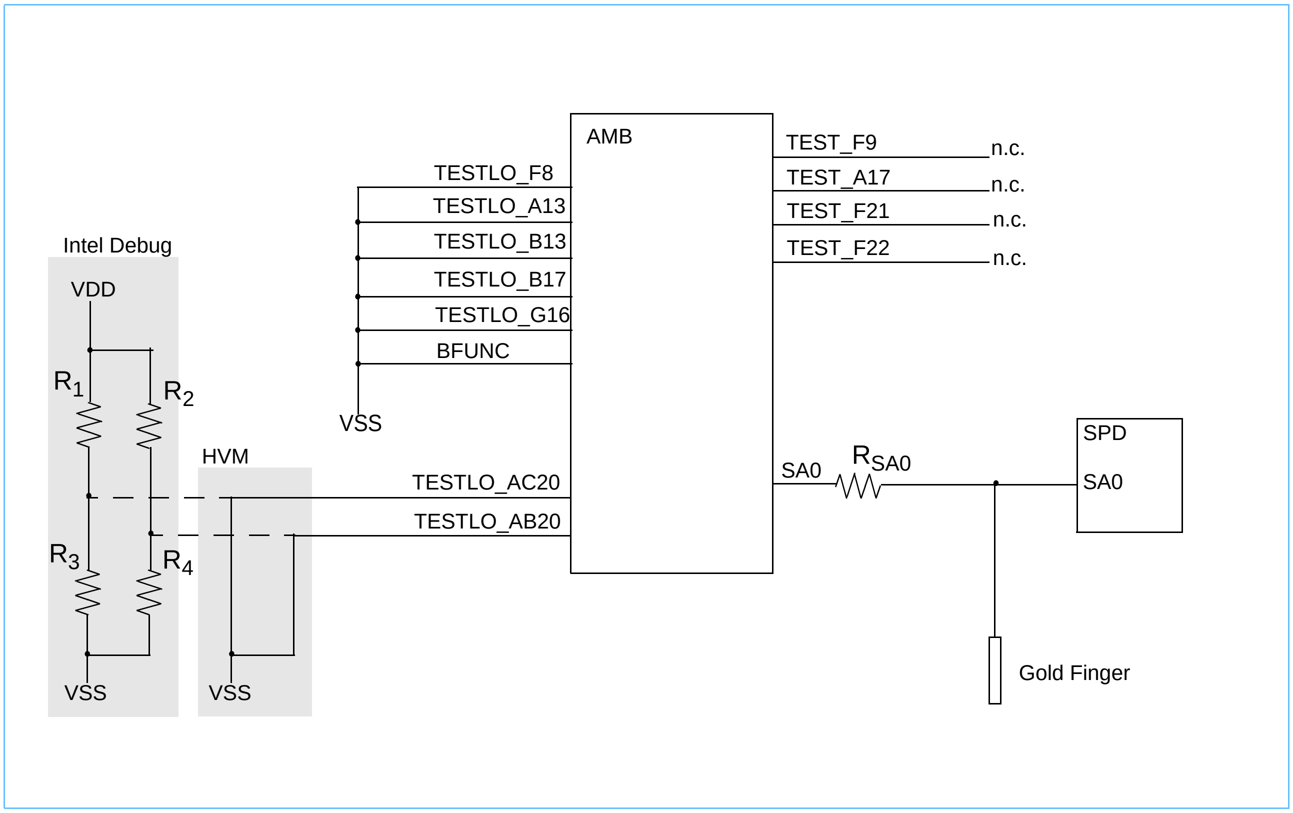
Dram devices require a VREF that tracks VDD/2, Raw Cards generates a trace for each side of the DIMM. Additionally, a test feature M_TEST implements a margin capability to slightly vary VREF for test purposes. While DIMM vendors may utilize their own values, it is recommended that the ratio of Rmargin to Rdiv be 0.015.

PLL and Channel Bias



NOTE 1: There is no connection to ground from VSSAPLL.
NOTE 2: Users must ensure AMB requirements are met by their implementation. Example, in VCCAPLL network, R implemented as copper trace serpentine may not achieve acceptable tolerances for all AMBs.
NOTE 3: VCC power delivery requirements (as specified for VCC balls) are assumed to be met at inputs of VCCAPLL and FBDRES networks, not at VCCAPLL and FBDRES balls.

Miscellaneous Bias



NOTE 1: Intel Debug circuit is optional for proprietary development purposes; Production should use HVM option.

NOTE 2: R_{SA0} protects AMB from overvoltage during SPD programing.

BIAS Components

Diagram	RefDes	Notes	Value
DDR Bias	R1		reference AMB vendor design guide
	R2,		
	R3		
	R4		
DDR VREF Bias	R_{MARGIN}		reference AMB vendor design guide
	R_{DIV}		
	C_{DIV}		
PLL and Channel	R		reference AMB vendor design guide
	L		
	C_1		
	C_2		
	R_{PLLTST}		
	R_{FBDRES}		
Miscellaneous	R_1		reference AMB vendor design guide
	R_2		
	R_3		
	R_4		
	R_{SA0}		

DDR2 Fully Buffered DIMM Wiring Details

Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into four groups. The signals for the high-speed system and SPD interfaces are also included. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Raw Card Version	Notes
System Clock	SCK, $\overline{\text{SCK}}$	A, B, C, D, E, H, J	
System Data Channels	PN[13:0], $\overline{\text{PN}}$[13:0], SN[13:0], $\overline{\text{SN}}$[13:0], PS[9:0], $\overline{\text{PS}}$[9:0], SS[9:0], $\overline{\text{SS}}$[9:0]	A, B, C, D, E, H, J	
DRAM Data, DQS, $\overline{\text{DQS}}$, DM	DQ[63:0],CB[7:0],DQS[17:0],$\overline{\text{DQS}}$[17:0]	A, B, C, D, E, H, J	$\overline{\text{DQS}}$[17:9] not used on R/C A, B $\overline{\text{DQS}}$[8:0] are DM on R/C A, B
DRAM Clock	CK[3:0], $\overline{\text{CK}}$[3:0]	A[1:0], B[1:0], C[1:0], D[3:0], E[3:0], H[3:0], J[3:0]	CK0, CK2 on left CK1, CK3 on right
DRAM Address and Command	A[15:0], BA[2:0], $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, ODT	A, B, C, D, E, H, J	Two sets, one set for left and one set for right
DRAM Control	$\overline{\text{CS}}$[1:0], CKE[1:0]	A (0), B (1:0) C (0), D (1:0), E[1:0], H[1:0], J[1:0]	Two sets, one set for left and one set for right
SPD	SCL, SDA	A, B, C, D, E, H, J	

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows:

- Signals are referenced to Vss layers only

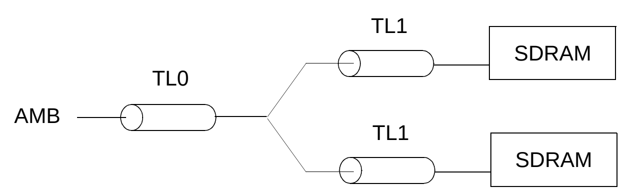
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for Fully Buffered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 1GB dual-rank x72 DIMM using 512Mbit, 64Mx8 SDRAM devices would have a data net structure as shown in the following diagram.



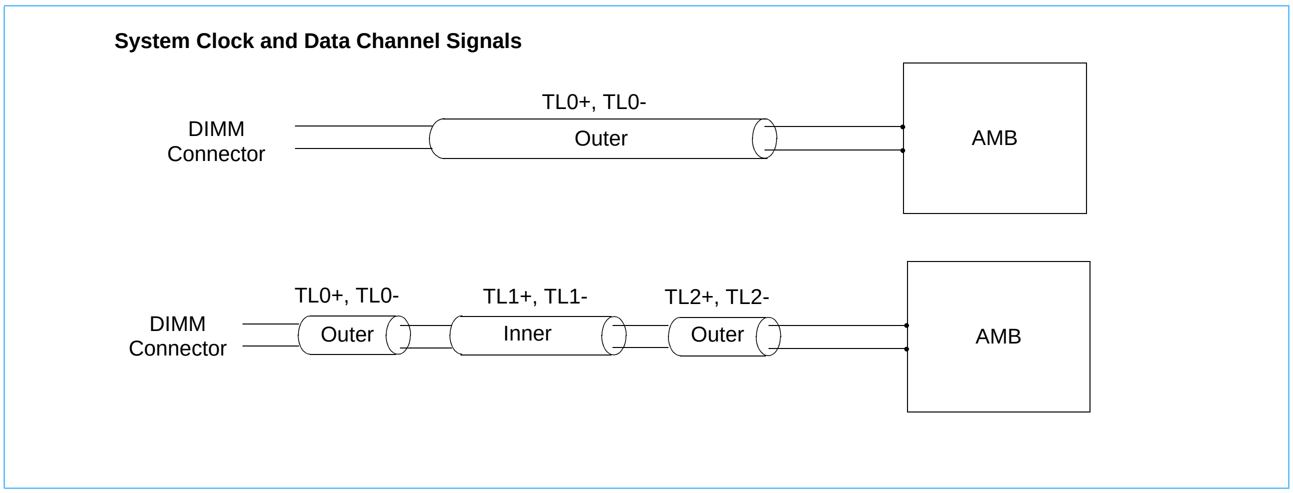
System Clock and Data Channel Net Structures

SCK, $\overline{\text{SCK}}$, PN[13:0], $\overline{\text{PN}}$[13:0], SN[13:0], $\overline{\text{SN}}$[13:0], PS[9:0], $\overline{\text{PS}}$[9:0], SS[9:0], $\overline{\text{SS}}$[9:0]

System Clock and Data Channel traces must be carefully routed to meet the following requirements:

- Signal quality
- Signal loss
- Minimal crosstalk
- Differential signal crosspoint

Net Structure Routing for System Data Channel



Trace Lengths for System Clock Net Structure (SCK, $\overline{\text{SCK}}$)

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B	1.9		50.3	51.0	0.6		52.8	53.5	1, 2
C	1.9		50.3	51.0	0.6		52.8	53.5	1, 2
D, J	1.9		50.3	51.0	0.6		52.8	53.5	1, 2
E	1.8	1.9	50.9		0.5	0.6	53.2	53.3	1, 2
H	1.8	2.2	50.6	51.0	0.5	0.6	52.8	53.5	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. The sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Trace Lengths for Primary Northbound Channel (PN[13:0], $\overline{\text{PN}}$[13:0])

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	8.1	34.4	NA		NA		8.1	34.4	1, 2
D, J	8.1	34.4	NA		NA		8.1	34.4	1, 2
E	1.6	34.4	0.0	23.6	0.0	0.6	9.2	34.4	1, 2
H	1.6	35.2	0.0	20.5	0.0	3.4	9.2	35.2	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. For sum of TL shorter than 12 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.5 mm. For sum of TL longer than 12 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Trace Lengths for Secondary Northbound Channel (SN[13:0], $\overline{\text{SN}}$[13:0])

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	1.8		9.1	34.6	0.6		11.5	37.0	1, 2
D, J	1.8		9.1	34.6	0.6		11.5	37.0	1, 2
E	1.5	2.3	9.1	34.3	0.5	0.6	11.7	37.0	1, 2
H	1.5	2.4	9.1	35.2	0.5	0.6	11.7	37.7	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. For sum of TL shorter than 16 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.5 mm. For sum of TL longer than 16 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Trace Lengths for Primary Southbound Channel (PS[9:0], $\overline{\text{PS}}$[9:0])

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	12.4	40.1	NA		NA		12.4	40.1	1, 2
D, J	12.4	40.1	NA		NA		12.4	40.1	1, 2
E	5.8	40.5	0.0	23.5	0.0	2.4	12.7	40.5	1, 2
H	1.6	41.3	0	24	0.0	4.5	12.4	41.3	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. The sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Trace Lengths for Secondary Southbound Channel (SS[9:0], SS[9:0])

Raw Card	TL0+		TL1+		TL2+		Sum(TL+) / Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	1.8	2.0	17.1	39.1	0.6	1.4	19.5	42.3	1, 2
D, J	1.8	2.0	17.1	39.1	0.6	1.4	19.5	42.3	1, 2
E	1.6	2.0	19.0	40.1	0.5	0.6	21.4	42.3	1, 2
H	1.6	2.1	17.1	40.1	0.5	0.6	21.4	42.3	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. The sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Pair-to-Pair Spacing Rules for System Data Channel Nets

Net Type	Net Length	Minimum Pair-to-Pair Separation	Notes
Microstrip (outer)	< 20 mm	4.25 x Height	1, 2, 3, 4
Microstrip (outer)	> 20 mm	5.25 x Height	1, 2, 3, 4
Stripline (inner)		3.7 x Height	1, 2, 3, 4

1. Pair-to-pair spacing rules are required to guarantee the crosstalk characteristics of the channel.
2. Separation is defined as a multiple of the dielectric height.
3. Separation between two differential pairs is measured between the closest traces, from the center of one trace to the center of the other trace.
4. For traces with a fine serpentine routing (for length matching) the spacing is measured from the average position of the center of the trace.

Minimum Trace Widths for System Data Channel Nets

Net Type	Absolute Minimum Width	Notes
Microstrip (outer)	0.102 mm	1
Stripline (inner)	0.127 mm	1

1. Minimum trace width is required to guarantee the loss characteristics of the channel.

Recommended Minimum Trace and Shape Separation Rules

The following table describes recommended minimum spacing for signals, buses and power isles.

Spacing is represented as ratio AG/D where AG is the air gap measurement from feature edge to feature edge and D is the distance between the signal layer and its reference plane. Ratios are calculated based on values from “Example Six Layer Stackup” section.

Design physical constraints (such as limited routing space in fan-out regions etc.) can cause exceptions. These exceptions should be minimized as much as possible since they can put at risk design integrity.

As table below contains recommended minimum values, designer should try to maximize separation whenever possible. As an example, on 10 layers R/C D designer was able to increase DQ to DQ spacing to 3.3 x dielectric height.

Number represent air gap to dielectric height ratio [#1]		To:						
		DQ	DQS/$\overline{DQS}$	CK	C/A	Power Island	NB Channel	SB Channel
From:	DQ	2.0	2.0	2.4	2.0	2.0	non adj.	non adj.
	DQS/$\overline{DQS}$	na	note #2	non adj.	2.5	non adj.	non adj.	non adj.
	CK	na	na	note #2	2.0	2.0	non adj.	non adj.
	C/A	na	na	na	2.0	2.0	note #4	note #4
	Power Island	na	na	na	na	2.0	3.0	3.0
	NB Channel	na	na	na	na	na	note #2	note #3
	SB Channel	na	na	na	na	na	na	note #2

Notes:

#1 Values in the table represent recommended minimum ratio AG/D where AG is the air gap measurement from feature edge to feature edge and D is the distance between the signal layer and its reference plane. For simplicity, only “From => To” values are shown since the shaded fields contain duplicate values. “non adj.” means that busses are not adjacent on FBDIMM.

#2 For DQS/DQS#, CK and channel information see “Example Trace Geometries” section of this document.

#3 For information see “Pair-to-Pair Spacing Rules for System Data Channel Nets” section.

#4 Primary NB (micro-strip Tx) 5.0 (less or equal than 3.0 is OK for < 2.5 mm parallel run)
Primary SB (micro-strip Rx) 5.0
Secondary SB (strip-line, Tx) 3.0
Secondary NB (strip-line, Rx) 5.0

Example calculations

If the distance between the signal layer and its reference plane (dielectric height) is D=0.127um, the recommended minimum air gap between DQ and DQS/DQS# is: 2.0x0.127=0.254um

Dual Strip-line Differential Pairs Spacing

Noise can be coupled onto to a differential pair from a close-by differential pair running in parallel if a certain width to height ratio is not maintained. This spacing rule provides routing guidelines in the case when two strip-line differential signal pairs are routed in parallel on adjacent strip-line layers. The intra-pair coupling could adversely impact the proper termination and hence spacing rule(s) has to be taken to prevent reflection at the far end of the pairs.

The rules are as follows based on dimensions given in figure below (rules are based on nominal dimensions.)

1.For differential pairs, where signals are opposite direction (RX to TX)

(Xdiff + Ydiff) > 1.7 (S+H)

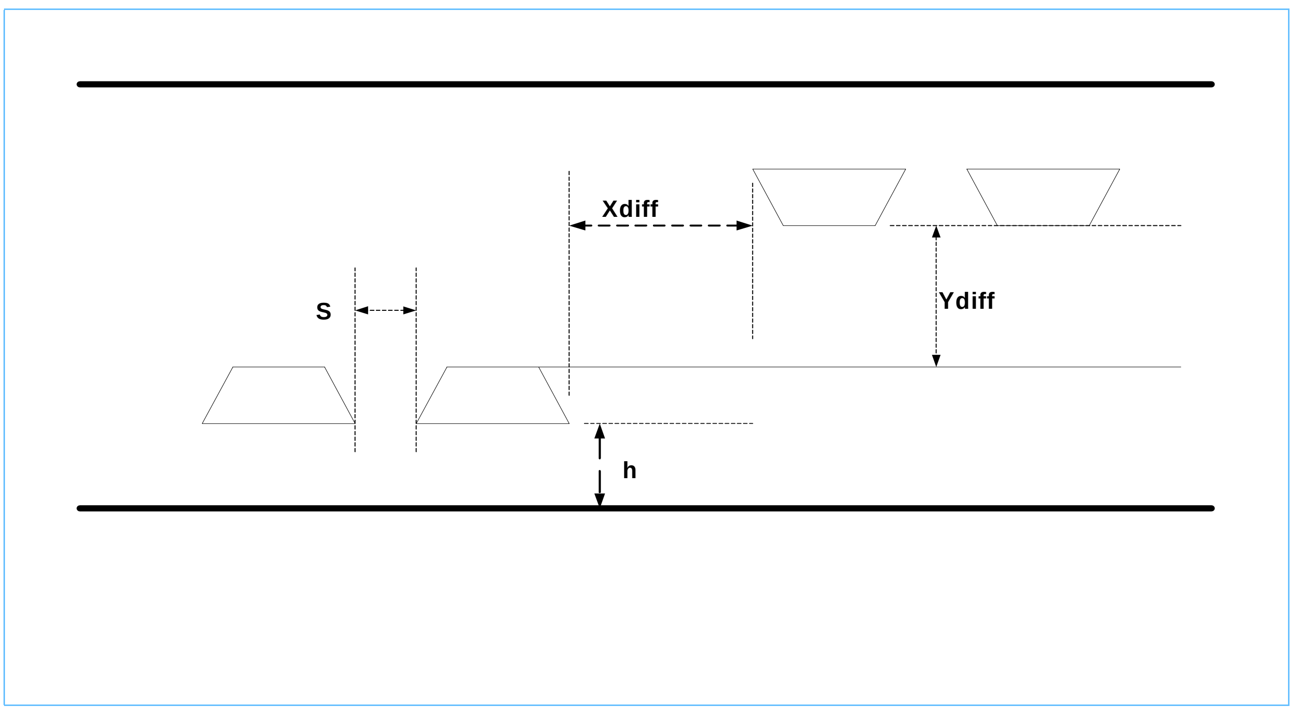
This 1.7 Rule is a MIN spacing requirement for parallel trace segments. While there are no rules precluding pair crossing segments (areas where a pair on one layer crosses over another pair on an adjacent layer), best layout practice should avoid pair crossings whenever possible in order to minimize all forms of crosstalk. Pair crossings should be perpendicular (90 degree intersect), else pair crossings must acheive at least 45 degree intersects.

2.For differential pairs, where signals are same direction (RX to RX or TX to TX)

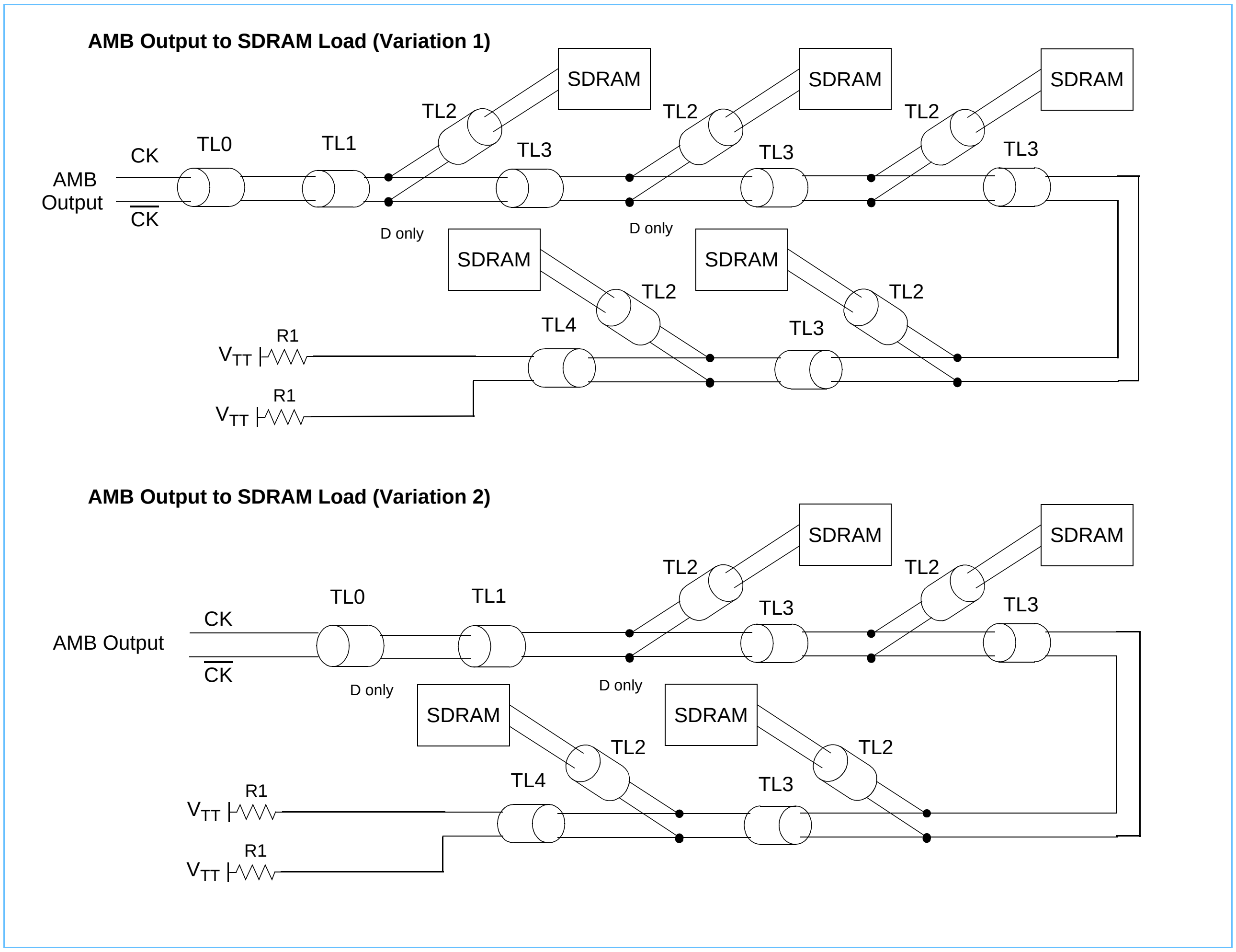
(Xdiff + Ydiff) > 1.3 (S+H)

This 1.3 Rule is a MIN spacing requirement applied in case the signal lines are parallel to possible agressors, and the total length of net segments for that signal is more than 6mm and the aggressor signals run in the same direction. these nets may have some segments with spacing violations and that violation is acceptable so long as the sum of the violating segments is less that 6mm in length.

Dual-strip-line Differential Pairs



Net Structure Routing for AMB Clock Output to SDRAM (Raw Card A)

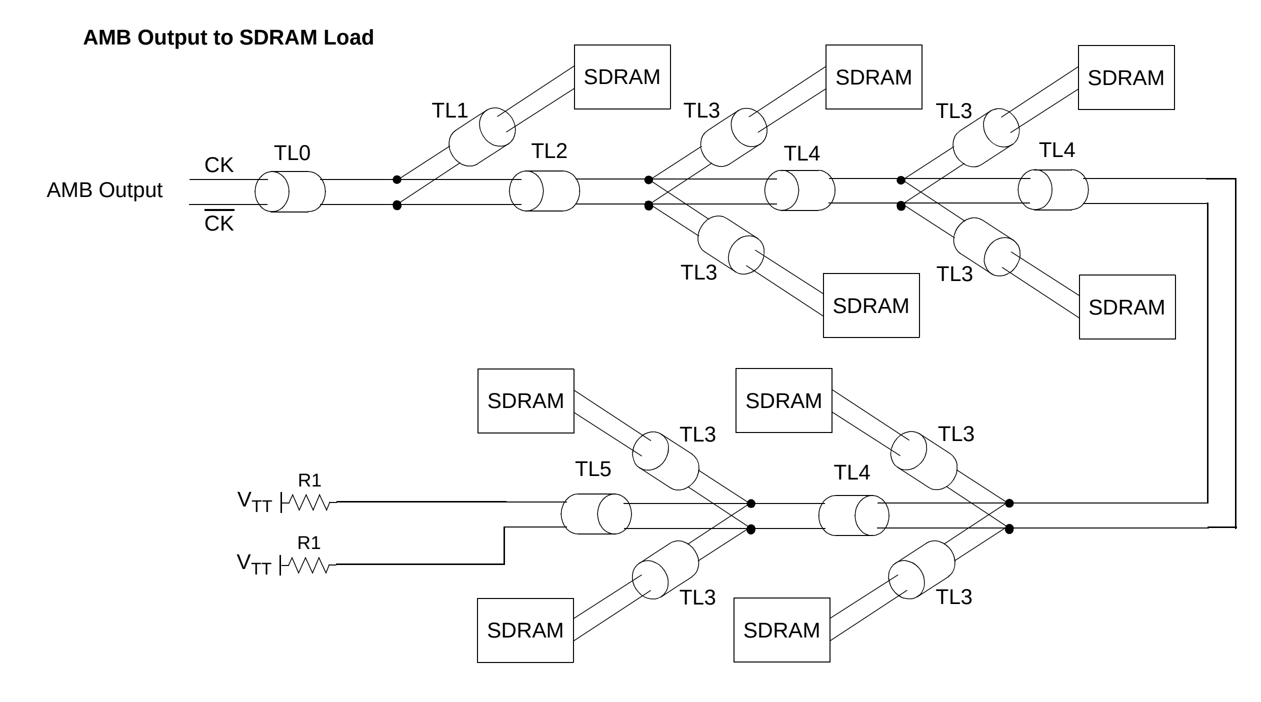


Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card A)

Raw Card	Variation	TL0		TL1		TL2		TL3		TL4		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	1	0.6	0.6	10.0	10.1	2.8	2.8	10.0	10.0	17.6	19.7	30	1, 2, 3, 4
	2	0.6	0.6	14.7	15.0	2.8	2.8	10.0	10.0	19.8	20.3	30	1, 2, 3, 4

1. All distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.50 mm.
3. TL1 and TL3 segments are routed on inner layers only. TL4 is routed on inner layer except for the final 0.9-1.9 mm.
4. On Raw Card A, variation 1 is CK1/$\overline{\text{CK1}}$, variation 2 is CK0/$\overline{\text{CK0}}$.

Net Structure Routing for AMB Clock Output to SDRAM (Raw Cards B,C)



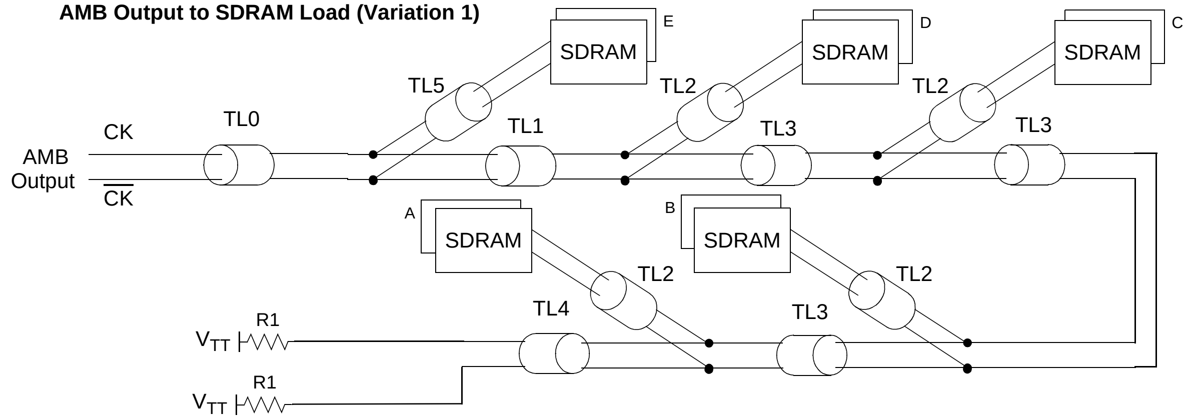
Trace Lengths for AMB Clock Output to SDRAM Net Structure

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B CK0/$\overline{\text{CK0}}$	0.6	1.5	2.1	2.5	12.1	12.2	0.6	4.4	13.3	14.9	16.1	20.8	39	1, 2, 3
B CK1/$\overline{\text{CK1}}$	0.6	1.5	8.6	9.9	7.8	9.3	0.6	3.7						
C CK0/$\overline{\text{CK0}}$	0.6	1.5	2.1	2.5	11.1	11.2	3.1	3.2	13.3	14.9	16.1	20.8	39	1, 2, 3
C CK1/$\overline{\text{CK1}}$	0.6	1.5	9.7	9.9	7.8	9.3	3.1	3.2						

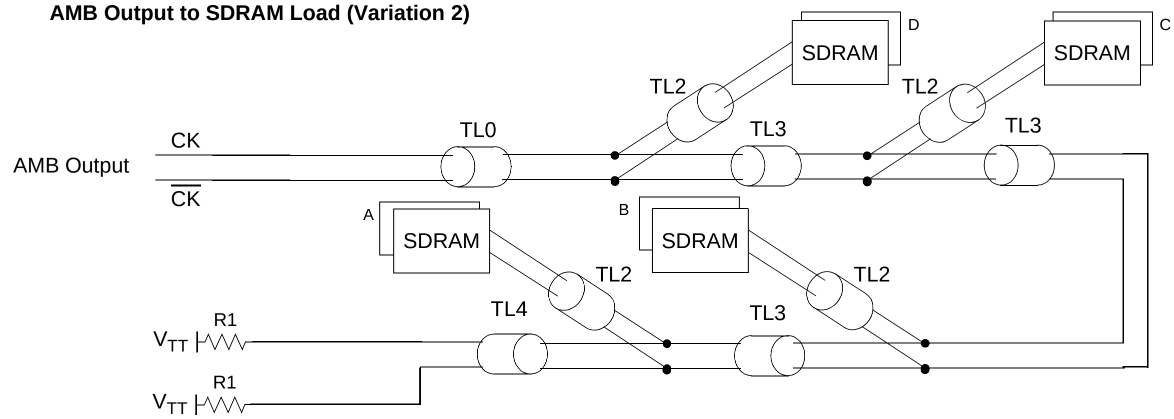
1. CK0/$\overline{\text{CK0}}$ is for the left half of the DIMM, CK1/$\overline{\text{CK1}}$ is for the right half of the DIMM.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.5 mm.
3. TL2 and TL4 segments are routed on inner layers only, TL5 is routed on inner layer except for the final 0.9-1.9 mm.

Net Structure Routing for AMB Clock Output to SDRAM (Raw Card D)

AMB Output to SDRAM Load (Variation 1)



AMB Output to SDRAM Load (Variation 2)

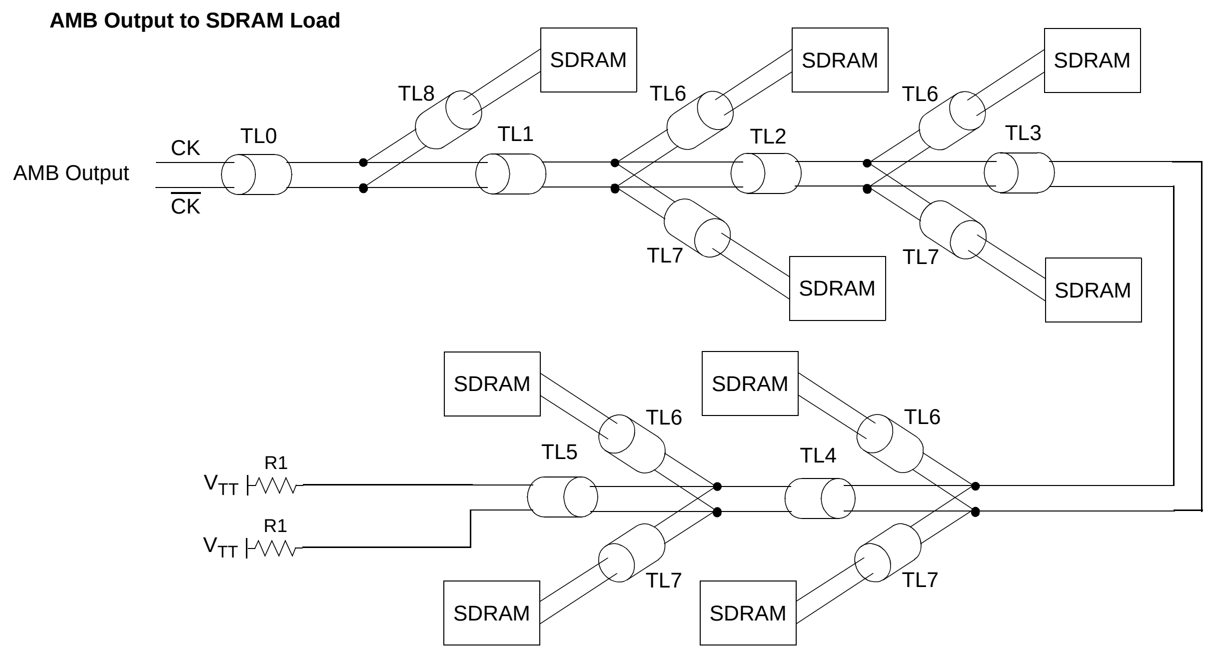


Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card D)

Raw Card	Variation	TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
D	1	0.6	0.6	12.2	12.4	0.6	0.6	15.2	15.4	20.3	20.8	8.2	8.4	33	1, 2, 3, 4
	2	21.2	21.4	NA		0.6	0.6	15.2	15.4	20.3	20.7	NA		33	1, 2, 3, 4

1. All distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.50 mm.
3. TL1 and TL3 segments are routed on inner layers only, TL4 is routed on inner layer except for the final 0.9-1.9 mm.
4. On Raw Card D, variation 1 is CK0/$\overline{\text{CK0}}$ and CK1/$\overline{\text{CK1}}$, variation 2 is CK2/$\overline{\text{CK2}}$ and CK3/$\overline{\text{CK3}}$.

Net Structure Routing for AMB Clock Output to SDRAM (Raw Card E, H)

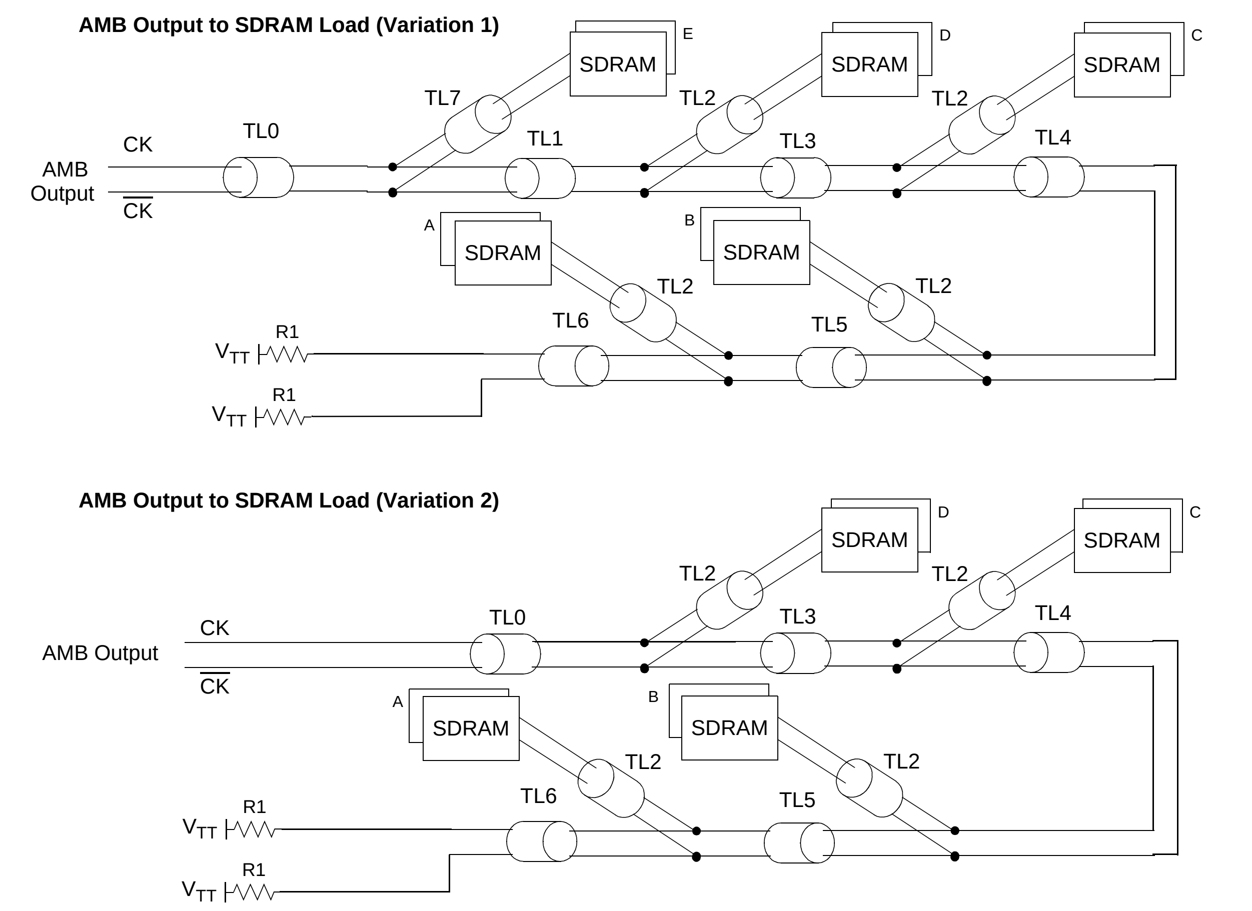


Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card E, H)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E	0.5	10.2	7.5	17.2	13.3	13.6	13.3	13.6	13.3	13.6	17.0	17.6	3.8	3.9	3.8	3.9	10.0	19.6	39	1,2,3
H	0.57	10.1	7.7	17.2	13.3	13.6	13.3	13.6	13.3	13.6	17.0	17.6	3.84	3.86	3.84	3.86	10.6	13.8	39	1,2,3

1. CK0/$\overline{\text{CK0}}$ is for the left half of the DIMM, CK1/$\overline{\text{CK1}}$ is for the right half of the DIMM.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.5 mm.
3. Segments TL0 and TL6 are routed on top layer. Segments TL1, TL2, TL3, TL4 and TL5 are routed on layer S8. Segments TL7 and TL8 are routed on bottom layer.

Net Structure Routing for AMB Clock Output to SDRAM (Raw Card J)



Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card J)

Raw Card	Varia-tion	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7	R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
J	1	0.6	0.6	12.1	12.5	0.6	0.6	19.2	19.3	22.1	22.1	20.7	20.8	20.8	20.9	10.0	30	1, 2, 3, 4
	2	0.6	0.6	12.3	12.5	0.6	0.6	32.6	32.7	23.6	23.7	23.6	23.7	21.8	21.8	--	30	1, 2, 3, 4

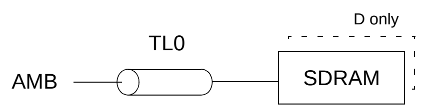
1. All distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.50 mm.
3. TL1, TL3, TL4 and TL5 segments are routed on inner layers only, TL6 is routed on inner layer except for the final 0.9-2.5 mm.
4. On Raw Card J, variation 1 is CK0/$\overline{CK0}$ and CK1/$\overline{CK1}$, variation 2 is CK2/$\overline{CK2}$ and CK3/$\overline{CK3}$.

Data Net Structures

DQ[63:0], CB[7:0], DQS[17:0], $\overline{\text{DQS}}$[17:0]

Special attention must be paid to balancing data nets (including check bits) within a byte lane (Raw Cards A and B) or nibble lane (Raw Cards C and D). Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing.

Net Structure Routing for DQ, CB, DQS, $\overline{\text{DQS}}$ (Raw Cards A, D, J)



Trace Lengths for DQ, CB, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Cards A, D, J)

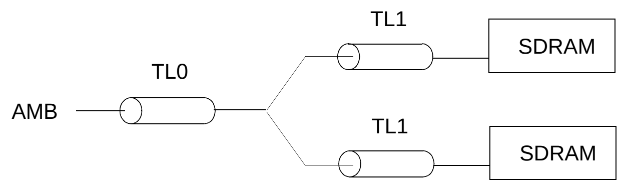
Raw Card	DRAM Position	TL0		Notes
		Min	Max	
A	3,8	21.7	25.3	1, 2, 3, 4
	2,4	30.1	30.5	1, 2, 3, 4
	1,5	40.5	51.6	1, 2, 3, 4
	0,6	57.5	61.7	1, 2, 3, 4
	7	76.8	76.9	1, 2, 3, 4
D (DQ)	8,17	11.9	12.1	1, 2, 3, 4
	3,4,12,13	21.4	21.6	1, 2, 3, 4
	2,5,11,14	37.9	38.1	1, 2, 3, 4
	1,6,10,15	60.9	61.1	1, 2, 3, 4
	0,7,9,16	82.9	83.1	1, 2, 3, 4
D (DQS/$\overline{\text{DQS}}$)	8,17	11.9	12.1	1, 2, 3, 4
	3,4,12,13	21.4	21.6	1, 2, 3, 4
	2,5,11,14	46.9	47.1	1, 2, 3, 4
	1,6,10,15	69.9	70.1	1, 2, 3, 4
	0,7,9,16	91.9	92.1	1, 2, 3, 4
J (DQ)	8,17	12.0	14.2	1, 2, 3, 4
	3,4,12,13	17.5	17.5	1, 2, 3, 4
	2,5,11,14	40.0	40.0	1, 2, 3, 4
	1,6,10,15	80.5	80.5	1, 2, 3, 4
	0,7,9,16	110.0	110.0	1, 2, 3, 4
J (DQS/$\overline{\text{DQS}}$)	8,17	11.7	12.0	1, 2, 3, 4
	3,4,12,13	17.5	17.6	1, 2, 3, 4
	2,5,11,14	41.0	41.2	1, 2, 3, 4
	1,6,10,15	82.5	82.5	1, 2, 3, 4
	0,7,9,16	112.9	113.1	1, 2, 3, 4

Trace Lengths for DQ, CB, DQS, $\overline{DQS}$ Net Structure (Raw Cards A, D, J)

Raw Card	DRAM Position	TL0		Notes
		Min	Max	

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{DQS}$) must not exceed 0.25 mm.
3. Trace length difference between the DQS/$\overline{DQS}$ traces and the DQ traces of a given byte (Raw Card A) or nibble (Raw Cards C, D) must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm. DRAM positions TBD have TBD additional trace on DQS/DQS#.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.

Net Structure Routing for DQ, CB, DQS, $\overline{\text{DQS}}$ (Raw Card B)

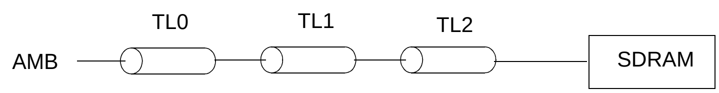


Trace Lengths for DQ, CB, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Card B)

Raw Card	DRAM	TL0		TL1		TL0 + TL1		Notes
		Min	Max	Min	Max	Min	Max	
B (DQ/CB)	8,17	0.6		14.0	14.2	14.6	14.7	1, 2, 3, 4
	3,4,12,13	19.7	24.1	0.6	1.9	21.4	24.7	1, 2, 3, 4
	2,5,11,14	31.0	34.5	0.6	2.7	33,4	35.2	1, 2, 3, 4
	1,6,10,15	56.3	58.1	0.6	1.9	58.0	58.7	1, 2, 3, 4
	0,7,9,16	71.1	75.6	0.6	1.9	73.0	76.2	1, 2, 3, 4
B (DQS/$\overline{\text{DQS}}$)	8,17	0.6		14.0	14.2	14.6	14.7	1, 2, 3, 4
	3,4,12,13	19.7	24.1	0.6	1.9	21.4	24.7	1, 2, 3, 4
	2,5,11,14	31.0	38.5	0.6	2.7	33,4	39.2	1, 2, 3, 4
	1,6,10,15	56.3	61.1	0.6	1.9	58.0	61.7	1, 2, 3, 4
	0,7,9,16	71.1	77.6	0.6	1.9	73.0	78.2	1, 2, 3, 4

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.

Net Structure Routing for DQ, CB, DQS, $\overline{DQS}$ (Raw Card C)



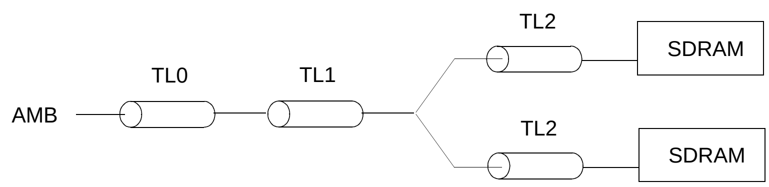
Trace Lengths for DQ, CB, DQS, $\overline{DQS}$ Net Structure (Raw Card C)

Raw Card	DRAM	TL0		TL1		TL2		TL0+TL1+TL2		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
C	8,17	0.6	0.6	13.4	13.6	0.6	0.6	14.6	14.7	1,2,4
	3,4,12,13	0.6	0.6	16.1	19.6	0.6	5.5	21.4	21.7	1,2,4
	2,5,11,14	0.6	0.6	28.0	32.5	0.6	5.5	33,4	35.4	1-4
	1,6,10,15	0.6	0.6	52.0	58.5	0.6	5.5	58.0	58.7	1-4
	0,7,9,16	0.6	0.6	69.0	73.5	0.6	5.5	73.0	76.2	1-4

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{DQS}$) must not exceed 0.25 mm.
3. DRAM positions 2,5,11,14 must have 2mm additional trace on DQS/DQS#.
   DRAM positions 1,6,10,15 must have 3mm additional trace on DQS/DQS#.
   DRAM positions 0,7,9,16 must have 2mm additional trace on DQS/DQS#.

4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.

Net Structure Routing for DQ, DQS, $\overline{\text{DQS}}$ (Raw Cards E, H; excluding DQS8/17, DQS8/17)



Trace Lengths for DQ, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Card E; excluding DQS8/17, DQS8/17)

Raw Card	DRAM	TL0		TL1		TL2		TL0 + TL1 + TL2		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
E	3, 4, 12, 13, 21, 22, 30, 31	0.5	1.4	19.1	20.7	2.1	3.3	22.9	24.2	1-5
	2, 5, 11, 14, 20, 23, 29, 32	0.5	0.6	31.1	34.9	2.1	3.3	33.9	38.8	1-5
	1, 6, 10, 15, 19, 24, 28, 33	0.5	1.4	54.8	58.0	0.5	3.3	57.5	61.9	1-5
	0, 7, 9, 16, 18, 25, 27, 34	0.5	0.6	71.7	73.7	1.3	3.3	74.8	77.6	1-5

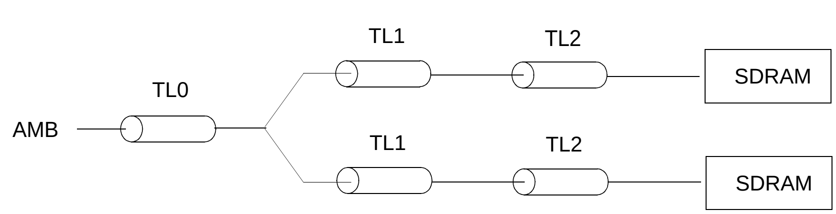
1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1 + TL2) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segment TL1 is routed on layers S3 or S5. Segment TL2 is routed on top or bottom layers..

Trace Lengths for DQ, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Card H; excluding DQS8/17, DQS8/17)

Raw Card	DRAM	Nets	TL0		TL0 + TL1		TL2		TL0 + TL1 + TL2		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
H	0, 7, 9, 16, 18, 25, 27, 34	DQ0 - DQ7, DQ56 - DQ63	0.57	1.37	71.1	75.6	0.6	2.7	73	76.2	1-5
		DQS 0, DQS 9, DQS 7, DQS 16	0.57	1.37	73.1	77.6	2.5	3.3	75	78.2	1-5
	1, 6, 10, 15, 19, 24, 28, 33	DQ8 - DQ15, DQ48 - DQ55	0.57	1.37	56.3	58.1	0.6	2.7	58	58.7	1-5
		DQS 1, DQS 10, DQS 6, DQS 15	0.57	1.37	58.3	61.1	2.5	3.3	61	61.7	1-5
	2, 5, 11, 14, 20, 23, 29, 32	DQ16 - DQ23, DQ40 - DQ47	0.57	1.37	31	35.5	0.6	2.7	33.4	35.2	1-5
		DQS 2, DQS 11, DQS 5, DQS 14	0.57	1.37	35	38.5	2.5	3.3	37.4	39.2	1-5
	3, 4, 12, 13, 21, 22, 30, 31	DQ24 - DQ39	0.57	1.37	19.7	24.1	0.6	2.7	21.4	24.7	1-5
		DQS 3, DQS 12, DQS 4, DQS 13	0.57	1.37	19.7	24.1	2.5	3.3	19.7	24.1	1-5

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1 + TL2) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segment TL1 is routed on layers S3 or S5. Segment TL2 is routed on top or bottom layers..

Net Structure Routing for CB, DQS8/17, $\overline{\text{DQS8/17}}$ (Raw Cards E, H)



Trace Lengths for CB, DQS8/17, $\overline{\text{DQS8/17}}$ (Raw Card E)

Raw Card	DRAM	TL0		TL1		TL2		TL0 + TL1 + TL2		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
E	8, 17, 26, 35	0.5	1.4	17.8	19.2	0.5	1.9	20.2	21.1	1, 2, 3, 4, 5

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segments TL1 and TL2 are routed on top or bottom layers..

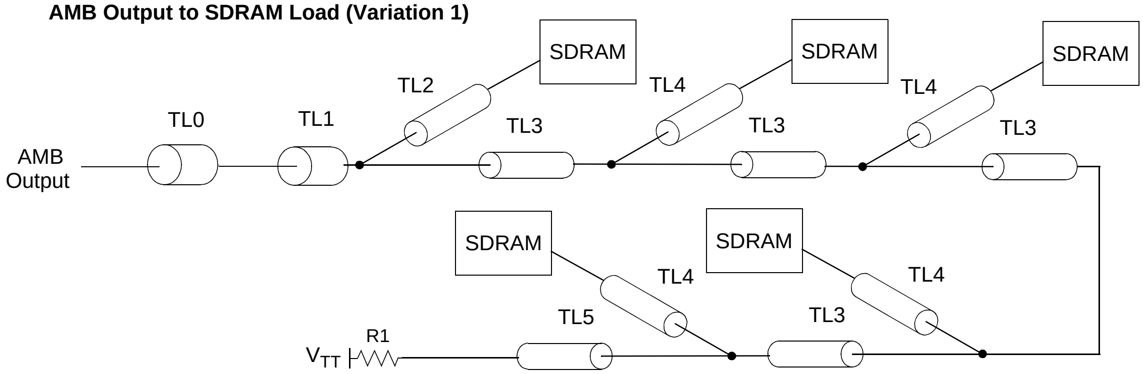
Trace Lengths for CB, DQS8/17, $\overline{\text{DQS8/17}}$ (Raw Card H)

Raw Card	DRAM	Nets	TL0		TL0 + TL1		TL2		TL0 + TL1 + TL2		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
H	8, 17, 26, 35	CB 0 - CB 7	0.57	0.58	19.6	19.8	0.56	1.6	20.1	20.4	1-5
		DQS 8 , DQS 17	0.58	0.58	19.6	19.8	0.58	2.1	20.1	21.7	1-5

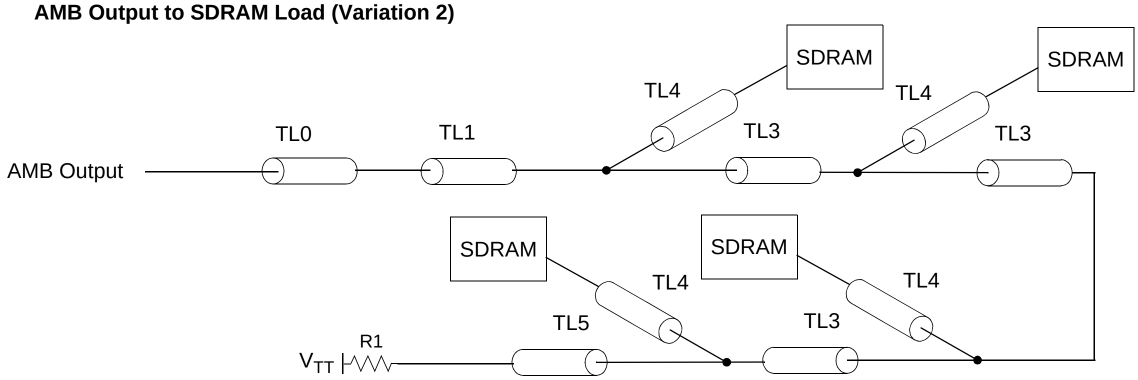
1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segments TL1 and TL2 are routed on top or bottom layers..

Net Structure Routing for Address/Command to SDRAM (Raw Card A)

AMB Output to SDRAM Load (Variation 1)



AMB Output to SDRAM Load (Variation 2)

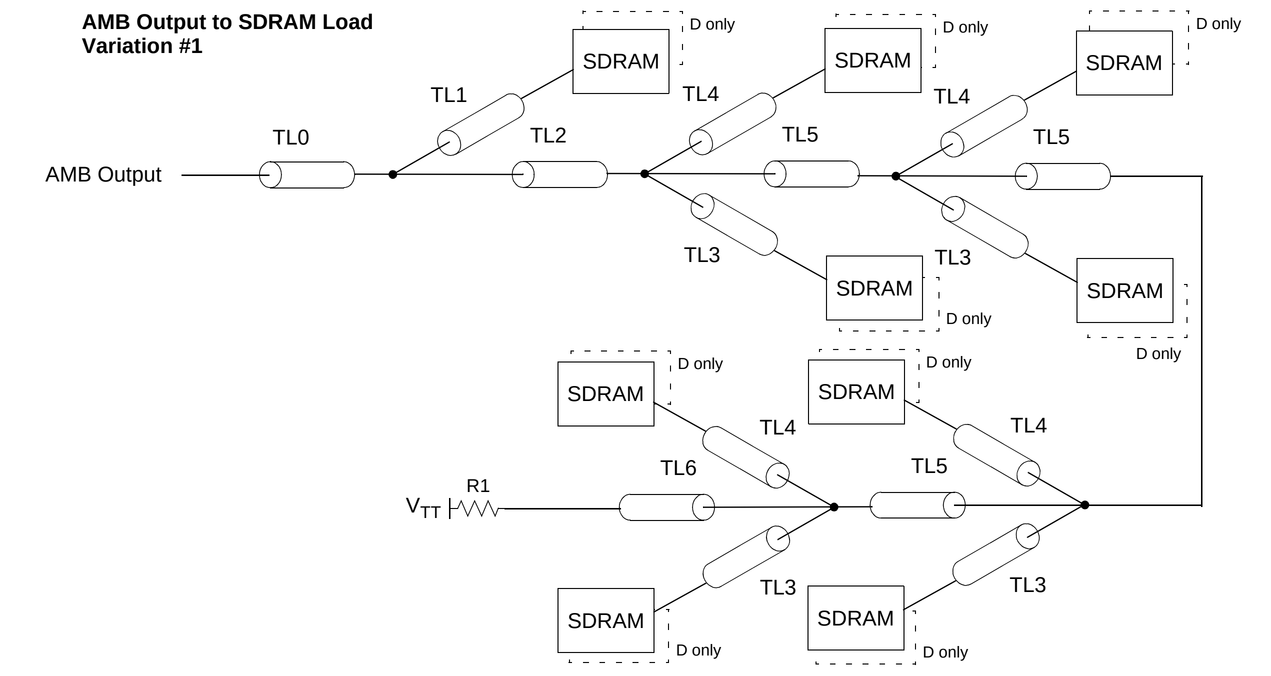


Trace Lengths for Address/Command Net Structure (Raw Card A)

Raw Card	Varia-tion	TL0		TL1		TL2		TL3		TL4		TL5		End-to-End		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	1	0.6	2.0	7.9	16.6	0.6	2.3	1.9	17.4	0.6	2.3	11.7	20.9	74.9	95.9	39	1, 2, 3, 4
	2	0.6	2.0	13.5	21.1	N/A	N/A	2.3	18.7	0.6	2.3	7.0	21.4	52.0	67.3	39	1, 2, 3, 4

1. All distances are given in millimeters.
2. TL1, TL3, and TL5 segments are routed on inner layers only (except for last 0.9-1.9 mm of TL5).
3. End-to-End is the sum of TL0, TL1, all TL3 segments, and TL5, from the AMB output to the pad of the VTT R-pack.
4. Any two adjacent TL3 segments have a sum of between 18.4 and 21.2 mm.

Net Structure Routing for Address/Command to SDRAM (Raw Cards B, C)

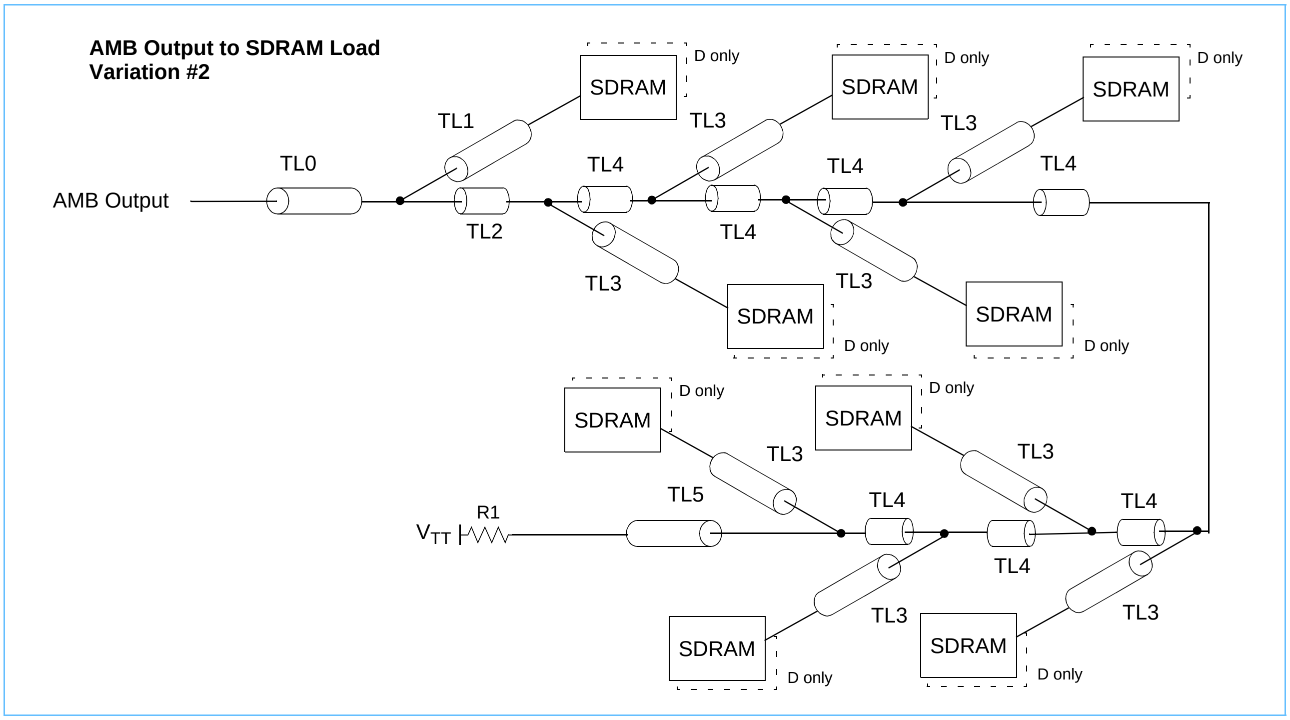


Trace Lengths for Address/Command Net Structure (Raw Cards B, C)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		End-to-End		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	0.6	4.8	0.6	5.1	8.2	22.1	0.9	4.2	0.9	4.8	13.3	15.5	10.4	23.4	67.2	80.8	39	1-4
C	0.6	4.8	0.6	4.4	8.3	22.1	0.9	3.7	0.9	4.8	13.4	15.3	10.8	23.4	67.2	80.8	39	1-4

1. All distances are given in millimeters.
2. TL2, TL5, and TL6 segments are routed on inner layers only (except for last 0.9-1.9 mm of TL6).
3. On Raw Card B & C, all address and command are variation #1, except for A4, A7, A10, BA0, BA2 and ODT.
4. End-to-End is the sum of TL0, TL2, three TL5 segments, and TL6, from the AMB output to the pad of the VTT R-pack.

Net Structure Routing for Address/Command to SDRAM (Raw Cards B, C)

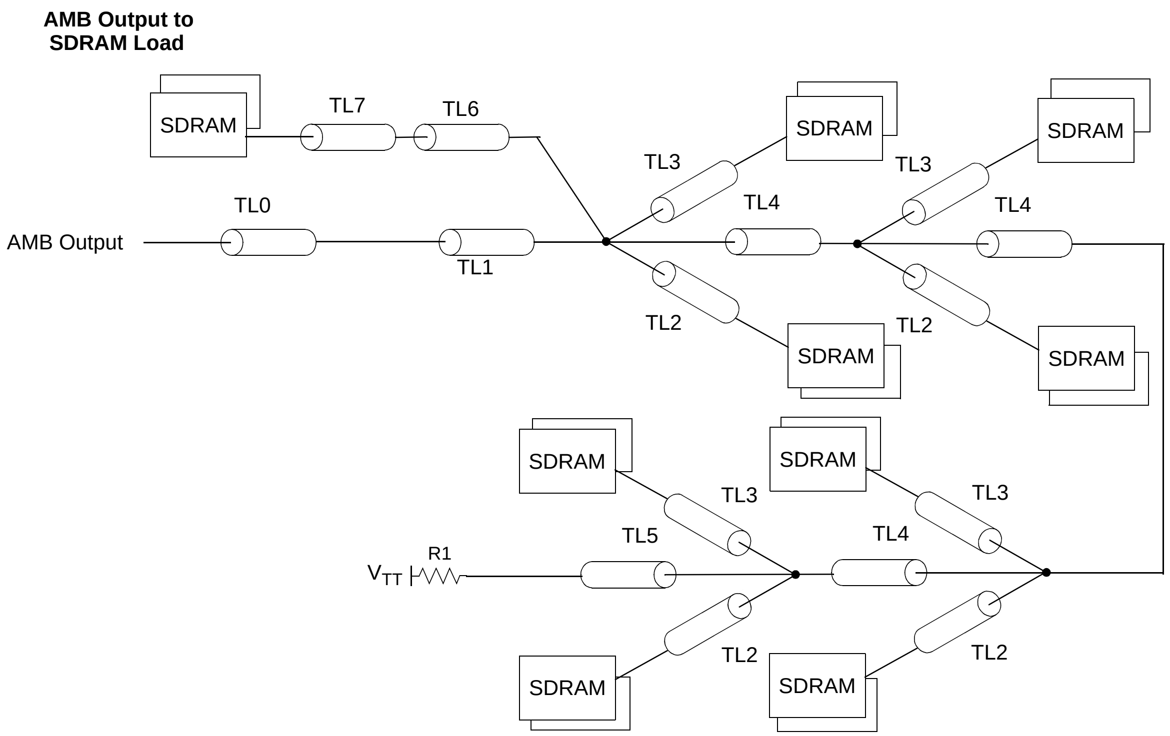


Trace Lengths for Address/Command Net Structure (Raw Cards B, C)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		End-to-end		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	0.6	3.5	0.6	4.8	5.1	14.4	0.6	3.1	3.7	10.9	12.5	22.3	69.9	80.2	39	1-5
C	0.6	3.5	0.6	4.8	5.1	14.0	0.6	3.1	5.3	8.9	12.5	22.3	69.9	80.2	39	1-5

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL2, TL4 and TL5 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL5 segments).
3. On Raw Card B & C, A4, A7, A10, BA0, BA2 and ODT are variation #2.
4. On Raw Card B & C, any two adjacent TL4 segments have a sum of between 11.7 and 16.8 mm.
5. End-to-End is the sum of TL0, TL2, seven TL4 segments, and TL5.

Net Structure Routing for Address/Command to SDRAM (Raw Card D)

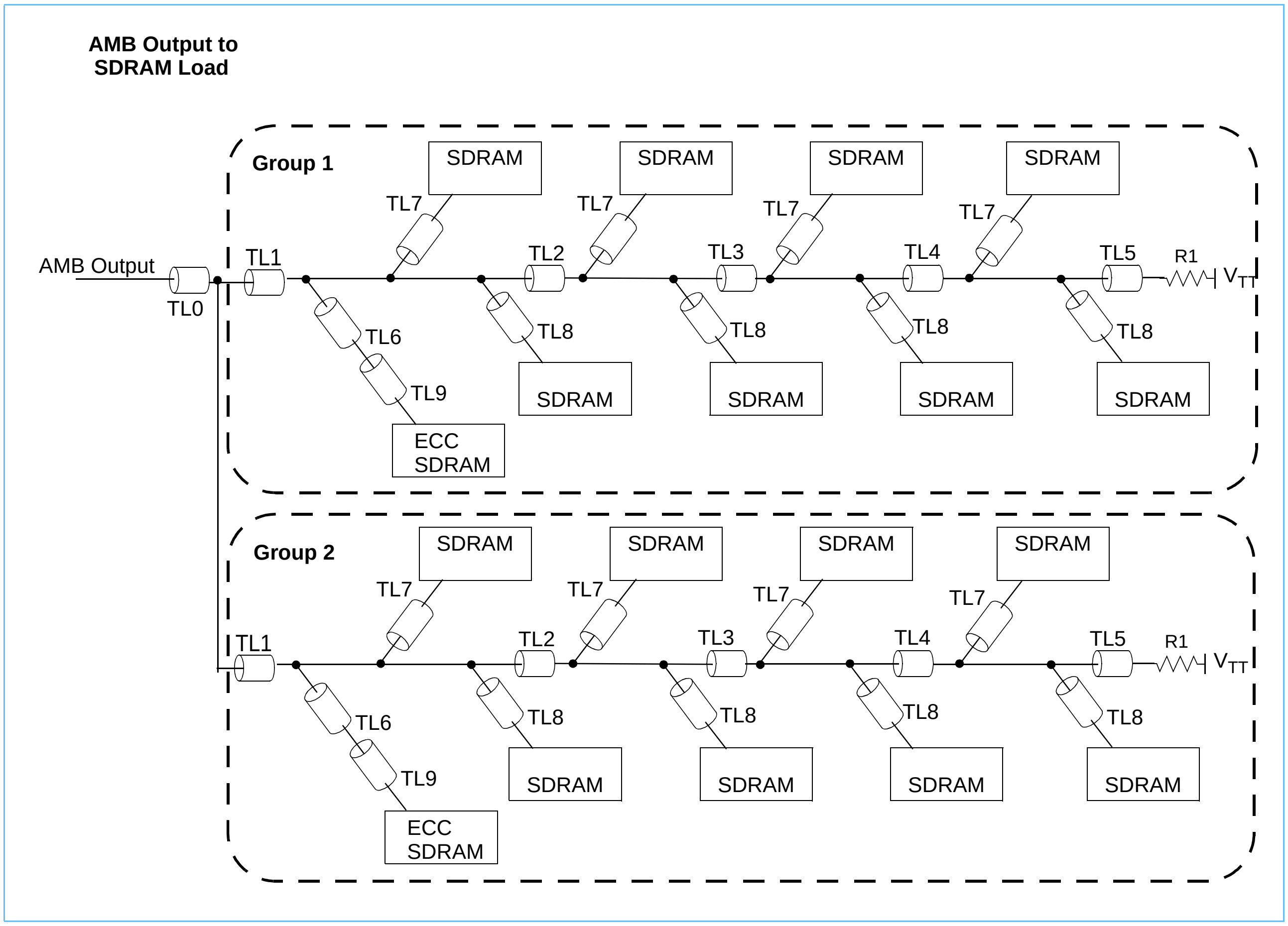


Trace Lengths for Address/Command Net Structure (Raw Card D)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
D (less ODT)	0.6	1.4	26.0	26.1	1.4	6.3	1.0	6.6	13.5	15.1	17.0	18.0	18.2	19.5	0.6	0.6	20	1, 2, 3

1. All distances are given in millimeters.
2. ALL ADDR.CMD except ODT (see separate R/C D ODT wiring detail.
3. 533 MT/s operation can use Normal or Early timing.
   667 MT/s operation requires Early timing.
   800 MT/s operation requires Early timing.

Net Structure Routing for Address/Command to SDRAM (Raw Cards E, H; excluding A4, A7, A10, BA0, BA2 and ODT)

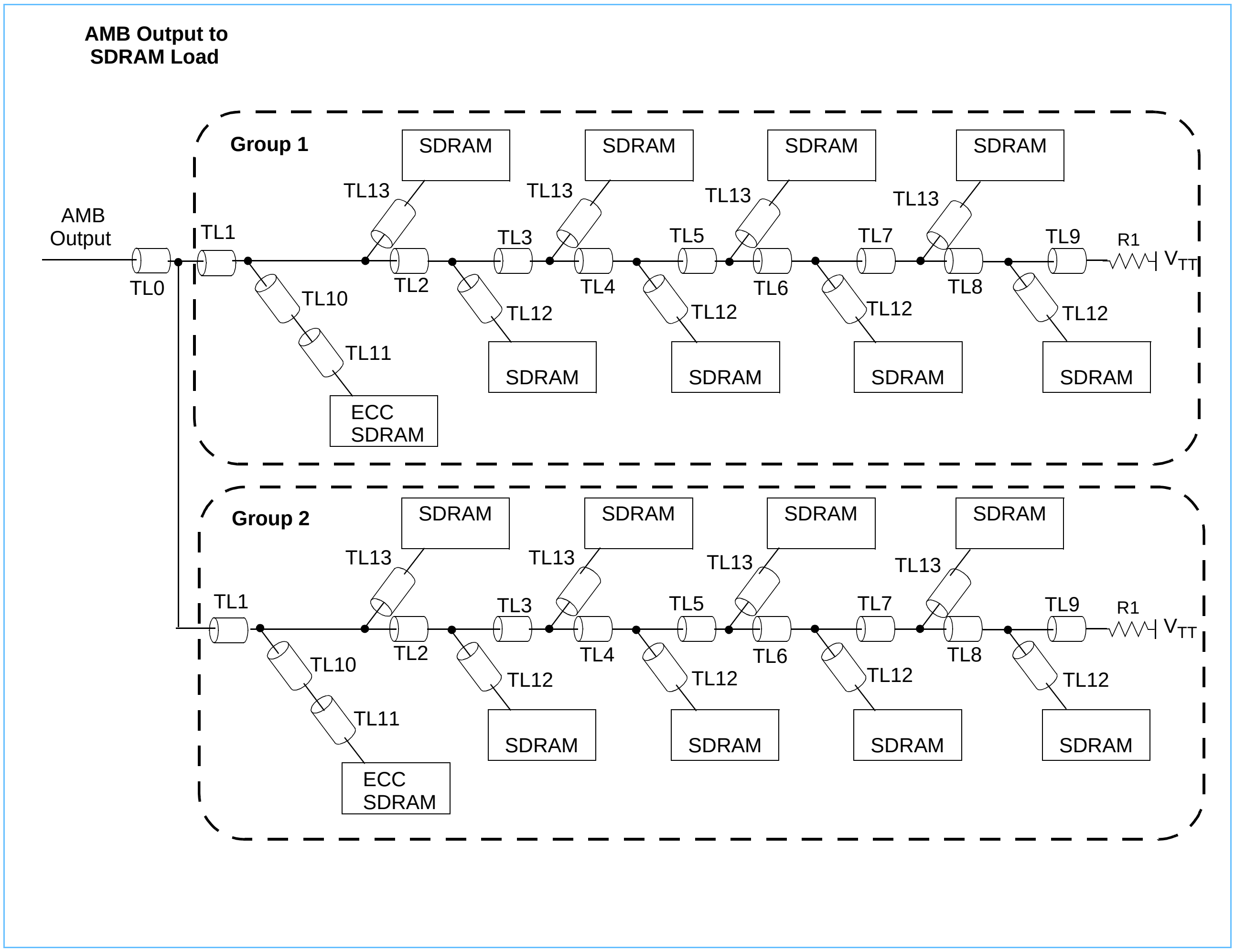


Trace Lengths for Address/Command Net Structure (Raw Cards E, H; excluding A4, A7, A10, BA0, BA2 and ODT)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		TL9		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E Group 1	0.5	4.3	11.8	23	13.3	15.1	12.9	15.3	13.0	15.3	11.4	16.1	7.2	17.1	1.1	4.6	1.0	5.2	0.5	8.0	33	1, 2
E Group 2	0.5	4.3	12.8	22.3	12.9	14.4	13.4	15.3	13.3	14.7	11.5	17.9	9.3	17.4	1.1	4.9	1.0	5.4	0.5	3.9	33	1, 3
H Group 1	0.56	3.6	12.3	22.5	13	15.25	12.9	15.5	13	15.5	11.4	16.2	7.5	18	1	4.6	1	5.3	0.57	9.3	33	1, 2
H Group 2	0.56	3.6	12.3	22.5	12.48	14.35	12.12	15.45	13.15	14.01	11.96	18.04	10.06	16.55	1	4.6	1	5.5	0.59	4.05	33	1, 3

1. All distances are given in millimeters.
2. For R/C E and R/C H, Group 1:TL0 and TL7 are routed on top layer; TL1, TL2, TL3, TL4, TL5 and TL6 are routed on layer S6; TL8 and TL9 are routed on bottom layer.
3. For R/C E and R/C H, Group 2:TL0 and TL7 are routed on top layer; TL1, TL2, TL3, TL4, and TL5 are routed on layer S8; TL6 is routed on layer S6; TL8 and TL9 are routed on bottom layer.

Net Structure Routing for A4, A7, A10, BA0, BA2, ODT to SDRAM (Raw Cards E, H)



Trace Lengths for A4, A7, A10, BA0, BA2 Net Structure (Raw Cards E, H)

Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	R1 [Ohm]	Notes
E Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.5	3.5	9.9	19.2	6.0	8.7	5.2	7.7	6.2	8.2	5.3	7.8	6.2	8.1		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.3	7.8	6.0	8.2	12.6	14.7	4.2	14.5	0.5	3.3	0.5	1.4	0.5	2.8		
E Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.5	3.5	6.3	19.6	5.9	8.6	5.2	11.5	6.1	8.1	5.3	7.7	6.2	8.1		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.3	7.6	5.8	8.1	12.5	18.9	0.0	14.7	0.5	9.4	0.5	1.3	0.5	3.1		
H Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.57	3.6	8.47	19.44	5.94	8.61	5.3	7.66	6.23	8.14	5.29	7.74	6.21	8.09		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.29	7.33	6.1	8.14	12.68	15.58	4.27	14.78	0.57	3.27	0.54	0.58	0.55	3.0		
H Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.57	3.6	5.94	19.4	5.67	8.65	5.24	7.62	6.18	8.39	5.35	7.7	6.23	8.21		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.18	8.35	5.83	8.09	12.49	15.21	7.07	14.51	0.57	2.25	0.55	1.37	0.56	3.0		

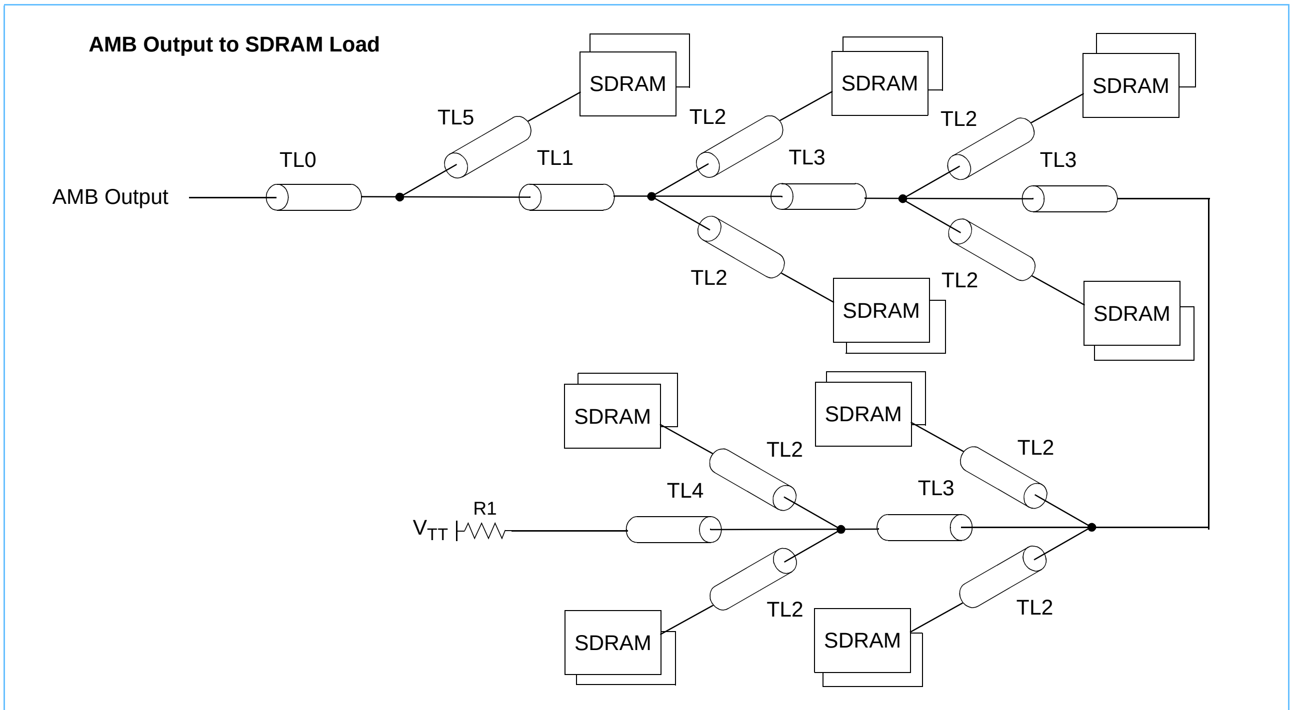
1. All distances are given in millimeters.
2. For R/C E and R/C H, Group 1:TL0 and TL13 are routed on top layer; TL1 is routed on layer S6; TL2 - TL10 are routed on layer.S8; TL11 and TL12 are routed on bottom layer.
3. For R/C E and R/C H, Group 2:TL0 and TL13 are routed on top layer; TL1 is routed on layer S8; TL2 - TL10 are routed on layer.S6; TL11 and TL12 are routed on bottom layer.

Trace Lengths for ODT Net Structure (Raw Cards E, H)

Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	R1 [Ohm]	Notes
E Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.5	0.9	13.3	16.6	9.7	9.9	3.9	4.2	8.8	8.9	4.2	4.3	8.8	8.9		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.2	4.3	8.7	8.9	14.0	14.7	0.0	11.9	0.5	5.1	1.3	2.0	1.0	1.5		
E Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.5	0.9	6.9	16.2	9.5	10.0	4.2	5.6	8.7	8.9	4.2	5.8	8.8	8.9		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.2	5.7	8.8	8.9	12.3	16.0	0.0	15.0	2.2	4.8	1.3	2.0	1.0	1.6		
H Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.57	0.81	13.62	17.56	9.73	9.85	3.94	4.11	8.87	8.89	4.25	4.25	8.89	8.98		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.25	4.25	8.76	8.85	14.37	14.59	5.06	14.09	0.0	0.6	1.38	1.78	0.55	3.0		
H Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.57	0.81	7.0	17.53	9.71	9.96	4.23	5.57	8.85	8.87	4.28	5.73	8.86	8.86		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.34	5.61	8.78	8.87	11.95	15.79	4.72	14.72	0.0	1.94	1.42	1.73	0.56	3.0		

1. All distances are given in millimeters.
2. For R/C E and H, Group 1:TL0 and TL13 are routed on top layer; TL1 is routed on layer S6; TL2 - TL10 are routed on layer.S8; TL11 and TL12 are routed on bottom layer.
3. For R/C E and H, Group 2:TL0 and TL13 are routed on top layer; TL1 is routed on layer S8; TL2 - TL10 are routed on layer.S6; TL11 and TL12 are routed on bottom layer.

Net Structure Routing for Address/Command to SDRAM (Raw Card J; excluding ODT)

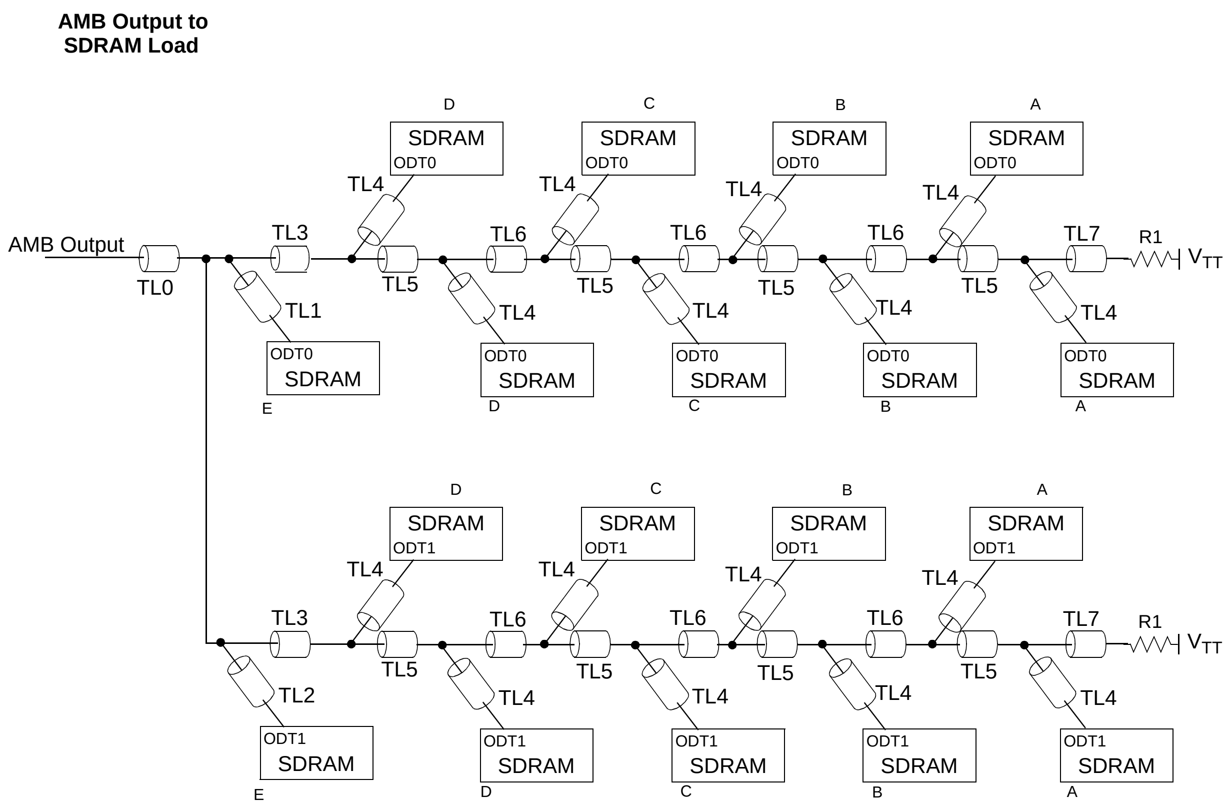


Trace Lengths for Address/Command Net Structure (Raw Card J; excluding ODT)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		End-to-End		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
J	11.2	12.4	14.7	16.0	1.7	6.6	13.3	17.6	12.9	17.1	15.2	16.9	71.5	71.9	20	1, 2, 3

1. All distances are given in millimeters.
2. All Address and Command signals, except ODT (see separate R/C D ODT wiring detail)).
3. No early timing required
4. End-to-End is the sum of TL0, TL1, three TL3 segments, and TL4

Net Structure Routing for ODT to SDRAM (Raw Card D)

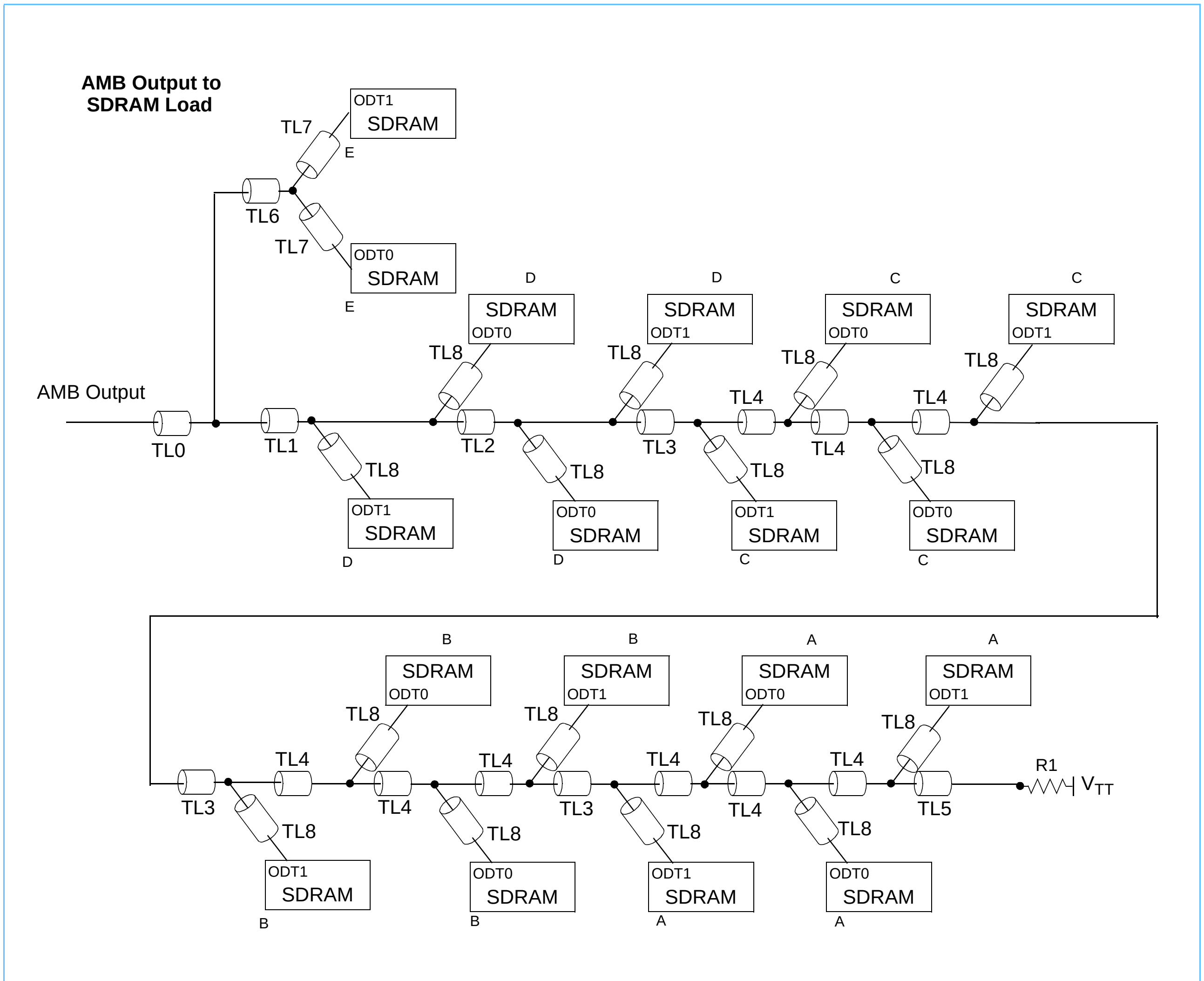


Trace Lengths for ODT Net Structure (Raw Card D)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
ODT	2.3	3.2	4.0	4.1	5.5	5.6	9.9	10.1	1.4	1.5	10.1	10.3	4.2	4.4	13.5	14.5	24	1, 2

1. All distances are given in millimeters.
2. 533 MT/s operation can use Normal or Early timing.
   667 MT/s operation can use Normal or Early timing.
   800 MT/s operation requires Normal timing.

Net Structure Routing for ODT to SDRAM (Raw Card J)

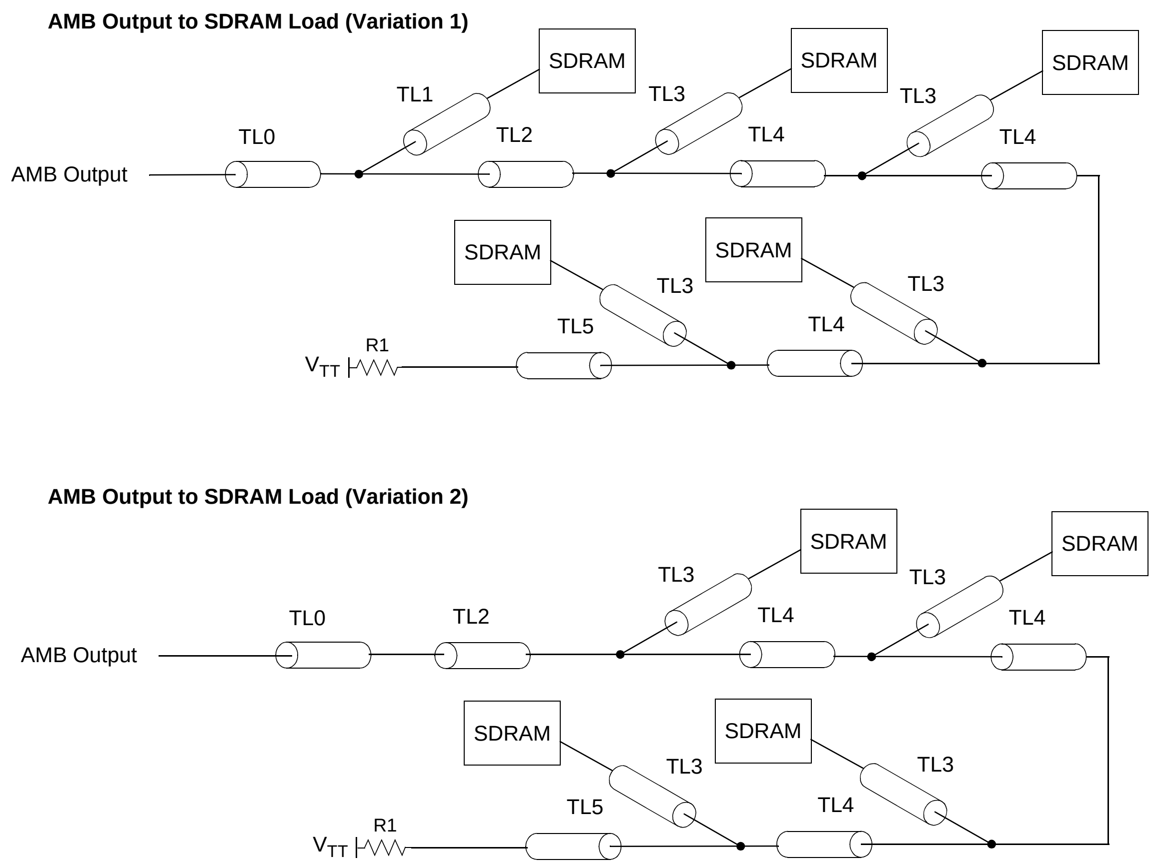


Trace Lengths for ODT Net Structure (Raw Card J)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
J	12.1	13.0	3.8	6.2	2.1	2.6	12.2	12.5	0.2	0.7	10.9	11.5	8.4	10.6	1.7	3.8	3.3	5.5	20	1, 2, 3, 4

1. All distances are given in millimeters.
2. Early timing not required.
3. Segment TL6 is a 0.2 mm wide trace where possible.
4. TL6 + TL7 = 11.7 to 12.2.

Net Structure Routing for Control to SDRAM (Raw Cards A, B)

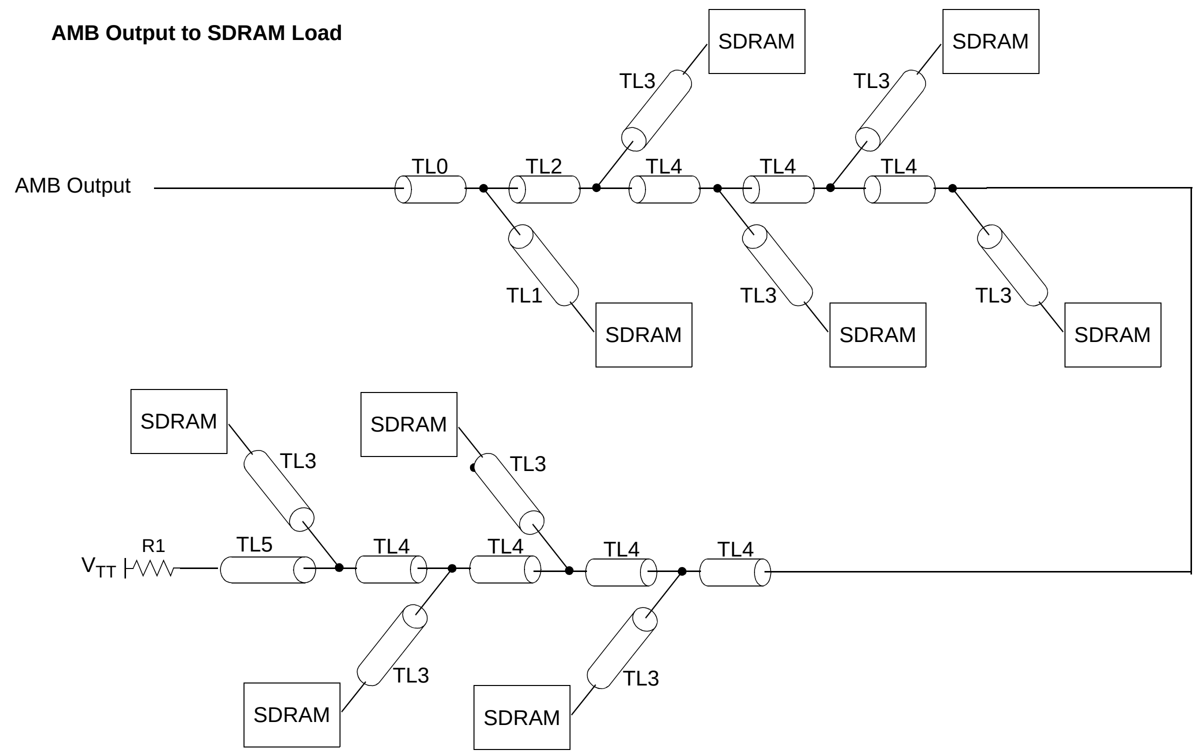


Trace Lengths for Control Net Structure (Raw Cards A, B)

Raw Card	Varia-tion	TL0		TL1		TL2		TL3		TL4		TL5		End-to-end		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	1	11.9	12.7	0.6	0.6	4.6	17.1	0.6	0.6	3.1	16.8	15.3	20.9	81.6	90.5	39	1, 2, 3, 4, 6
	2	0.6	0.6	N/A	N/A	16.2	16.8	0.6	0.6	3.1	16.3	16.9	20.7	58.1	65.8	39	1, 2, 3, 4, 6
B	1	0.6	2.2	0.6	3.2	5.5	21.7	0.6	3.9	3.4	23.9	16.2	31.5	73.4	87.0	47	1, 2, 3, 5, 7
	2	0.6	1.9	N/A	N/A	9.2	14.4	0.6	2.6	3.5	23.9	16.0	26.7	78.3	96.8	47	1, 2, 3, 5, 7

1. All distances are given in millimeters.
2. TL2, TL4, and TL5 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL5).
3. End-to-end is the sum of segments TL0, TL2, three TL4 segments, and TL5.
4. For Raw Card A, variation 1 is for $\overline{CS}$0B and CKE0B, variation 2 is for $\overline{CS}$0A, CKE0A.
5. For Raw Card B, variation 1 is for $\overline{CS}$1A, CKE1A, $\overline{CS}$0B and CKE0B, variation 2 is for $\overline{CS}$0A, CKE0A, $\overline{CS}$1B and CKE1B.
6. On Raw Card A, any two adjacent TL4 segments have a sum of between 19.1 and 19.7 mm.
7. On Raw Card B, any two adjacent TL4 segments have a sum of between 27.0 and 32.3 mm.

Net Structure Routing for Control to SDRAM (Raw Cards C)

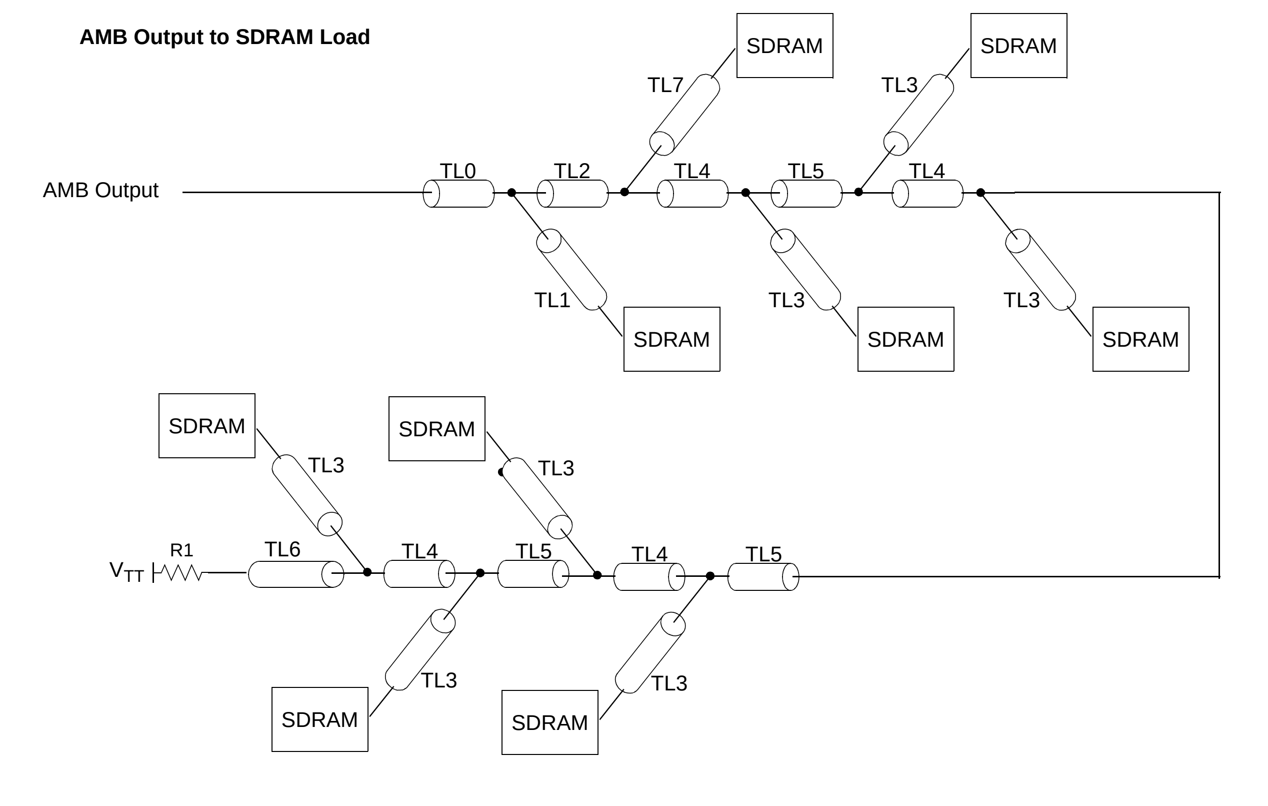


Trace Lengths for Control Net Structure (Raw Cards C)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		End-to-end		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
C	0.6	2.2	0.6	2.2	8.6	13.7	0.6	1.4	5.2	8.7	12.1	15.8	70.6	78.0	39	1-4

1. All distances are given in millimeters.
2. TL2, TL4, and TL5 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL5).
3. End-to-end is the sum of segments TL0, TL2, seven TL4 segments, and TL5.
4. Control nets are CKE(1:0) and $\overline{CS}$(1:0).

Net Structure Routing for Control to SDRAM (Raw Cards D, J)

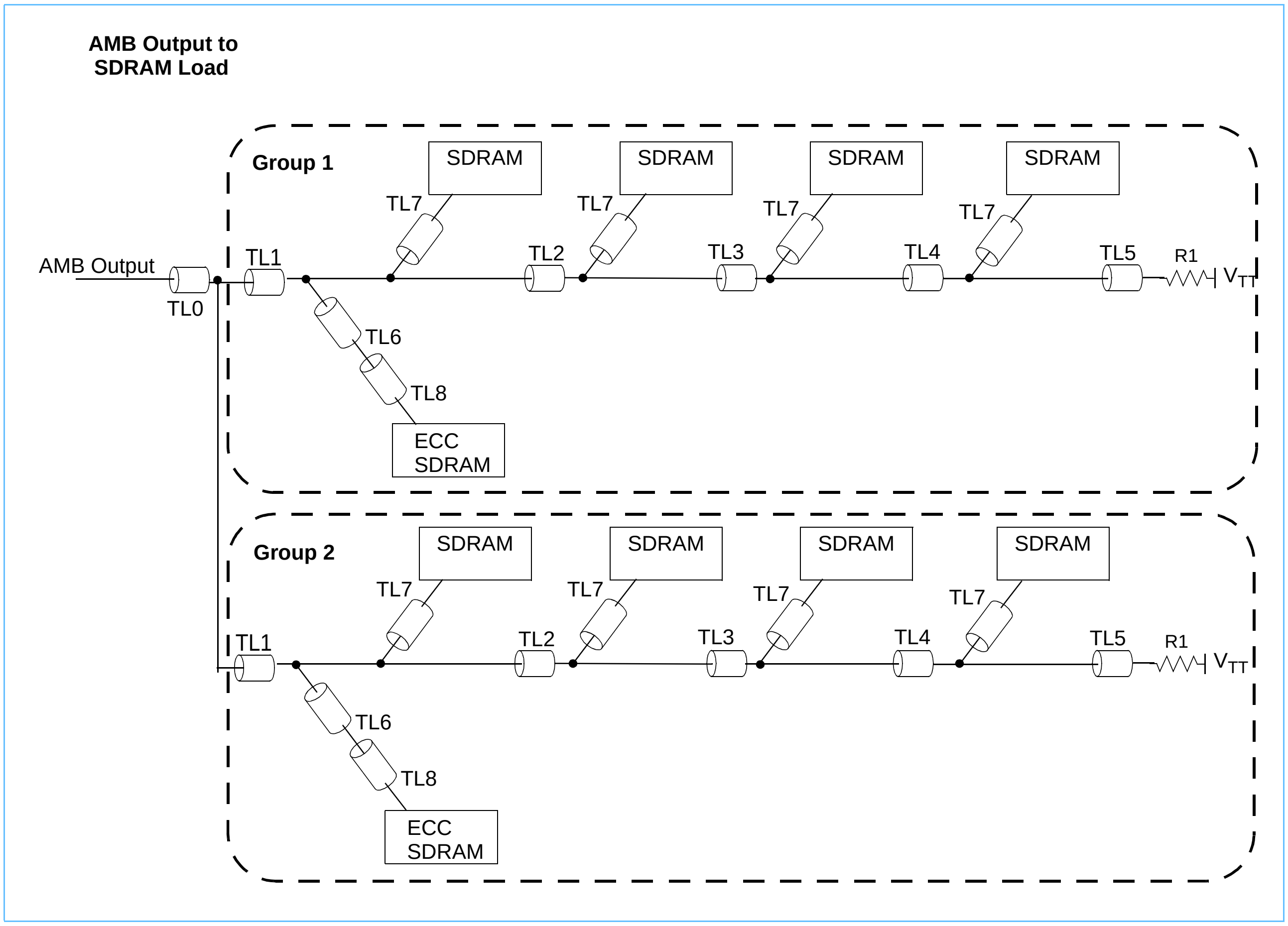


Trace Lengths for Control Net Structure (Raw Cards D, J)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		End-to-end		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
D	0.6	3.5	0.6	6.8	7.0	14.4	0.6	0.6	4.7	8.0	5.6	9.4	17.7	18.3	0.6	0.6	72.5	82.5	24	1, 2, 3, 4, 5
J	13.8	14.1	8.6	8.8	15.6	21.1	3.7	3.8	1.9	2.3	20.0	22.1	15.9	18.8	5.1	5.4	92.5	116.3	20	1, 2, 3, 4, 6, 7

1. All distances are given in millimeters.
2. TL2, TL5, and TL6 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL6).
3. End-to-end is the sum of segments TL0, TL2, four TL4 segments, three TL5 segments and TL6.
4. Control nets are CKE(1:0) and $\overline{CS}$(1:0).
5. 533 MT/s operation can use Normal or Early timing.
   667 MT/s operation can use Normal or Early timing.
   800 MT/s operation requires Normal timing.
6. No early timing required
7. TL4 segment is routed on inner layers only

Net Structure Routing for Control to SDRAM (Raw Card E; excluding S0L and CKE1R)

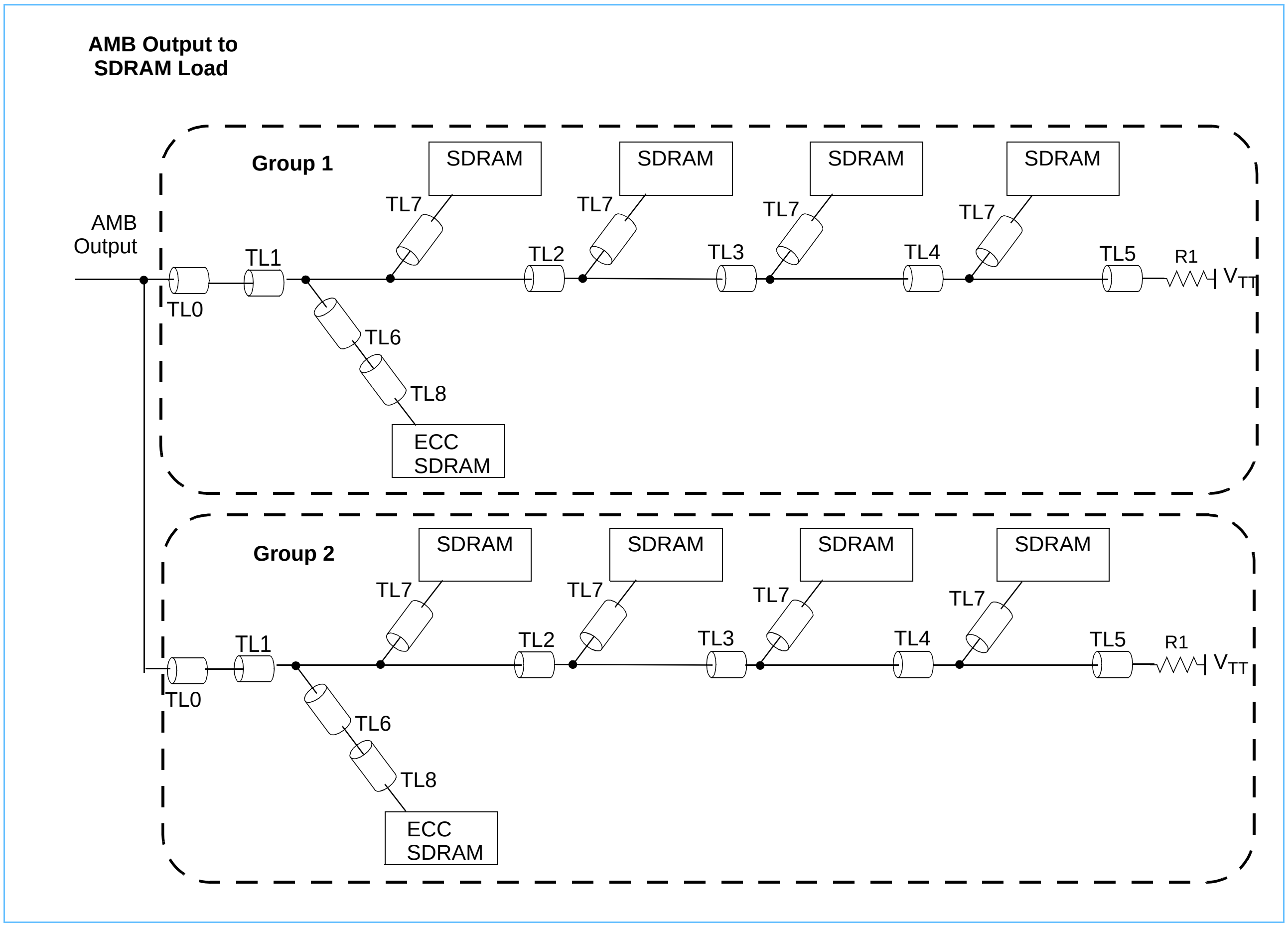


Trace Lengths for Control Net Structure (Raw Card E; excluding S0L and CKE1R)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E Group 1	0.5	11.4	9.0	21.9	12.8	14.4	14.1	14.4	14.1	14.5	17.9	19.2	4.5	21.1	0.5	3.0	0.5	2.3	39	1, 2, 4
E Group 2	0.5	1.4	10.1	22.9	12.1	15.8	14.1	15.5	14.0	16.5	17.3	18.6	11.0	14.1	0.5	3.2	0.5	4.7	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C E Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C E Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C E Group 1 ECC SDRAM with TL6 and TL8 is only for S0R, CKE0R and CKE0L.
5. R/C E Group 2 ECC SDRAM with TL6 and TL8 is only for S1L, S1R and CKE1L.

Net Structure Routing for S0L and CKE1R to SDRAM (Raw Card E)

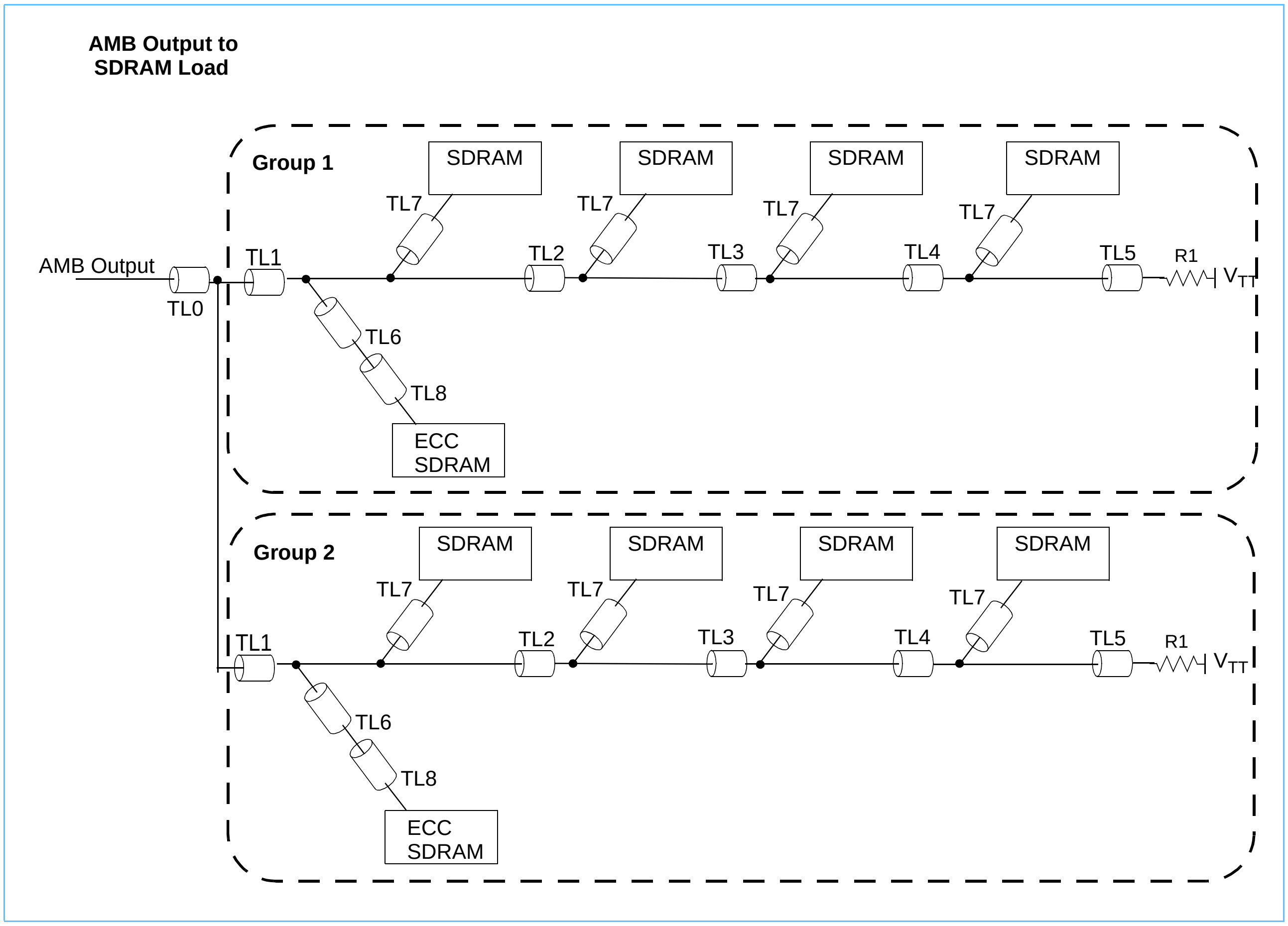


Trace Lengths for S0L and CKE1R Net Structure (Raw Card E)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E Group 1	10.1	12.6	3.6	9.9	13.1	14.3	14.1	14.2	14.0	14.3	16.6	18.0	0.0	0.0	0.5	2.3	8.2	8.2	39	1, 2, 4
E Group 2	5.3	8.3	4.0	11.3	14.0	15.6	14.0	15.0	14.2	15.5	17.1	17.4	7.8	7.8	0.5	2.3	7.6	7.6	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C E Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C E Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C E Group 1 ECC SDRAM with TL6 and TL8 is only for S0L.
5. R/C E Group 2 ECC SDRAM with TL6 and TL8 is only for CKE1R.

Net Structure Routing for Control to SDRAM (Raw Card H; excluding S0L, S1L and CKE1R)

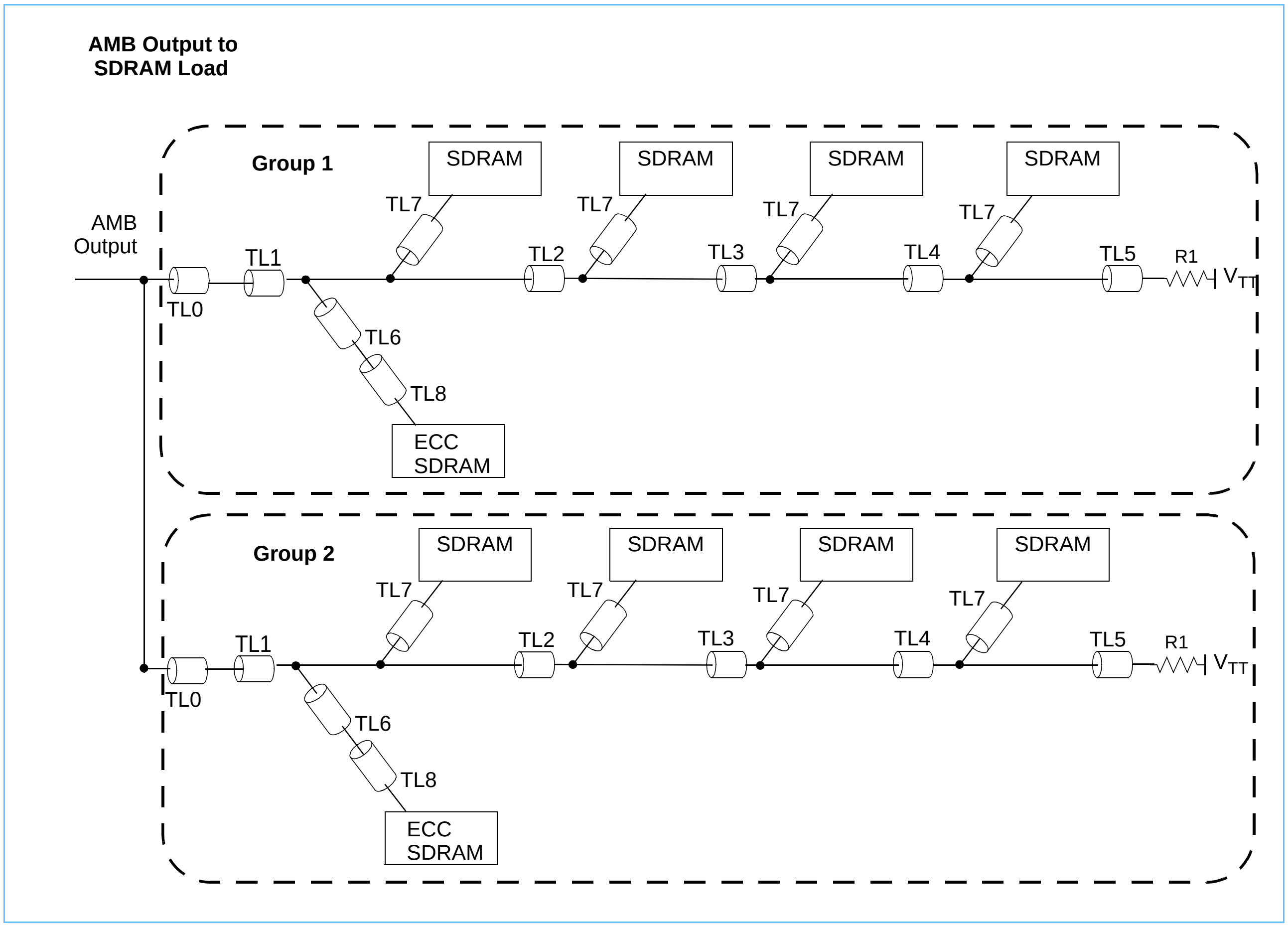


Trace Lengths for Control Net Structure (Raw Card H; excluding S0L, S1L and CKE1R)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
H Group 1	0.57	11.85	3.7	21.83	12.75	14.37	14.13	14.31	14.09	14.43	15.92	18.73	4.51	21.22	0.56	2.9	0.0	2.3	39	1, 2, 4, 6
H Group 2	0.57	7.28	5.2	22.88	13.69	15.77	13.56	15.47	13.6	16.51	16.67	18.51	8.2	13.79	0.56	3.67	0.57	7.64	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C H Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C H Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C H Group 1 ECC SDRAM with TL6 and TL8 is only for S0R, CKE0R and CKE0L.
5. R/C H Group 2 ECC SDRAM with TL6 and TL8 is only for S1R and CKE1L.
6. Group #1 TL6 is directly connected to the DRAM when TL8 = 0.

Net Structure Routing for S0L, S1L and CKE1R to SDRAM (Raw Card H)



Trace Lengths for S0L, S1L and CKE1R Net Structure (Raw Card H)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
H Group 1	0.57	11.85	3.7	21.83	12.75	14.37	14.13	14.31	14.09	14.43	15.92	18.73	4.51	21.22	0.56	2.9	0.0	2.3	39	1, 2, 4, 6
H Group 2	0.57	7.28	5.2	22.88	13.69	15.77	13.56	15.47	13.6	16.51	16.67	18.51	8.2	13.79	0.56	3.67	0.57	7.64	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C H Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C H Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C H Group 1 ECC SDRAM with TL6 and TL8 is only for S0L.
5. R/C H Group 2 ECC SDRAM with TL6 and TL8 is only for S1L and CKE1R.
6. Group #1 TL6 is directly connected to the DRAM when TL8 = 0.

Cross Section Recommendation

The DIMM printed circuit board design uses six, eight or ten layers of glass epoxy material. PCBs should contain solid ground planes. The outside layers typically supply VDD. The inner signal layers supply VDD and VCC.

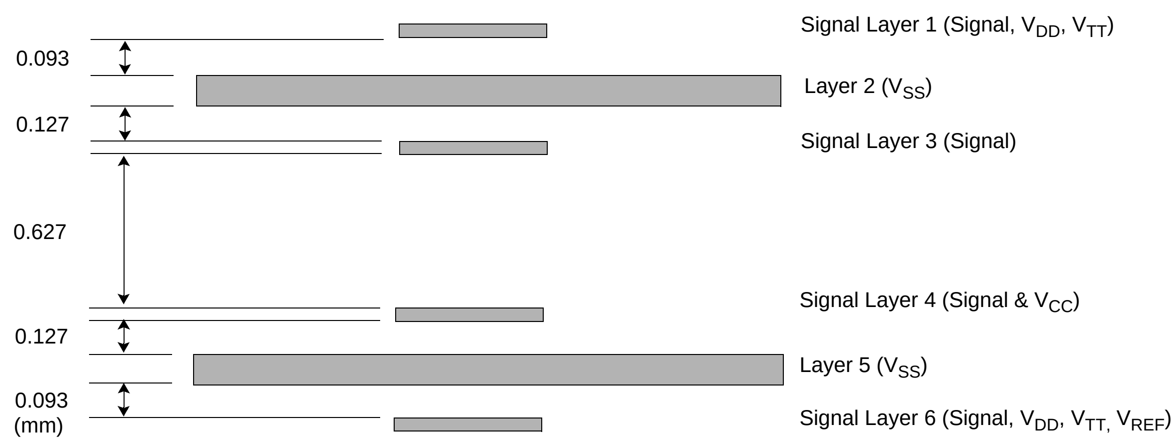
R/C reference design gerber registration collaterial must include stack-up assumptions used to develop the respective gerber. The furnished stack-up information must include core and pre-preg constructions information with dimensional and tolerance details.

Note: The PCB edge connector contacts shall be gold-plated.

PCB Electrical Specifications

Parameter	Min	Nominal	Max	Units
Trace velocity: S0 (outer layers)	5.5		6.7	ps/mm
Trace velocity: S0 (inner layers)	6.5		7.6	ps/mm
Trace impedance: Z_0 (Component break-out pad to via, outer layers)	54	60	66	Ohms
Trace impedance: Z_0 (DQ, inner layer)	50	56	62	Ohms
Trace impedance: Z_0 (Address/Command/Control, inner layer)	56	62	68	Ohms
Differential impedance: Z_{diff} (System Clock)	85	100	115	Ohms
Differential impedance: Z_{diff} (System Data Channel)	72	85	98	Ohms
Differential impedance: Z_{diff} (DRAM Clocks and DRAM DQS/$\overline{DQS}$)	85	100	115	Ohms

Example Six Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Example Trace Geometries, Single Ended

Location	Nominal Z_0	Nominal Trace Width
Outer Layers	60 ohms	0.102 mm
Inner Layers	56 ohms	0.127 mm
	62 ohms	0.102 mm

1.) Trace dimensions assume the example six-layer stackup in the previous diagram.
2.) The designer should maximize trace-to-trace air-gap separation (measuring from trace edge to trace edge) of single-ended signals to reduce signaling noise due to crosstalk.

Example Trace Geometries, Differential

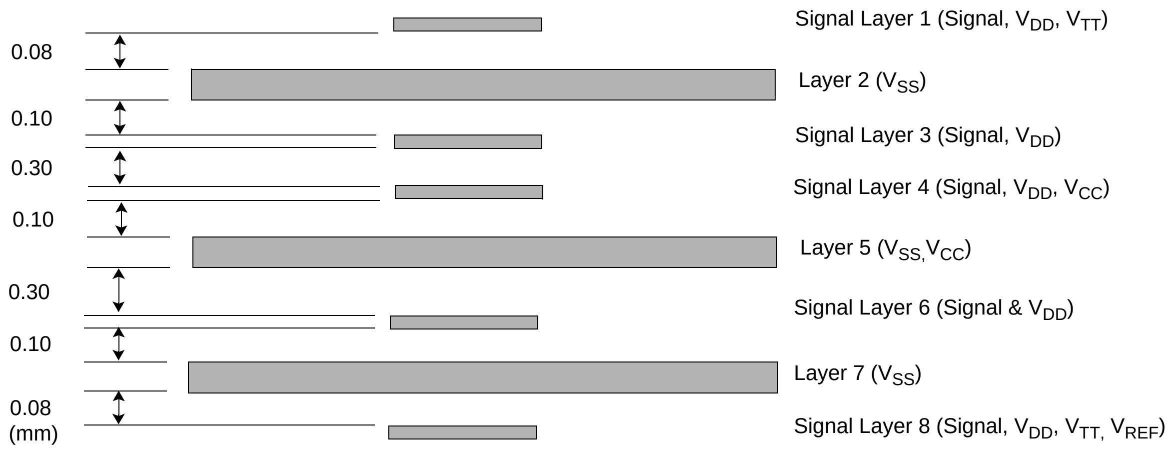
Location	Nominal Z_{diff}	Nominal Trace Width	Nominal Trace Separation [3]
Outer Layers	85	0.127	0.127
Inner Layers	85	0.153	0.127
	100	0.102	0.127

1.) Trace dimensions assume the example six-layer stackup in the previous diagram.
2.) The designer should maximize trace-to-trace air-gap separation between the differential pair and its neighbors (measuring from pair trace edge to neighbor trace edge) to reduce signaling noise due to crosstalk.
3.) Values for Nominal Trace Separation are air-gap distances measuring from pair trace edge to neighbor trace edge.

Impedance Measurement Coupons

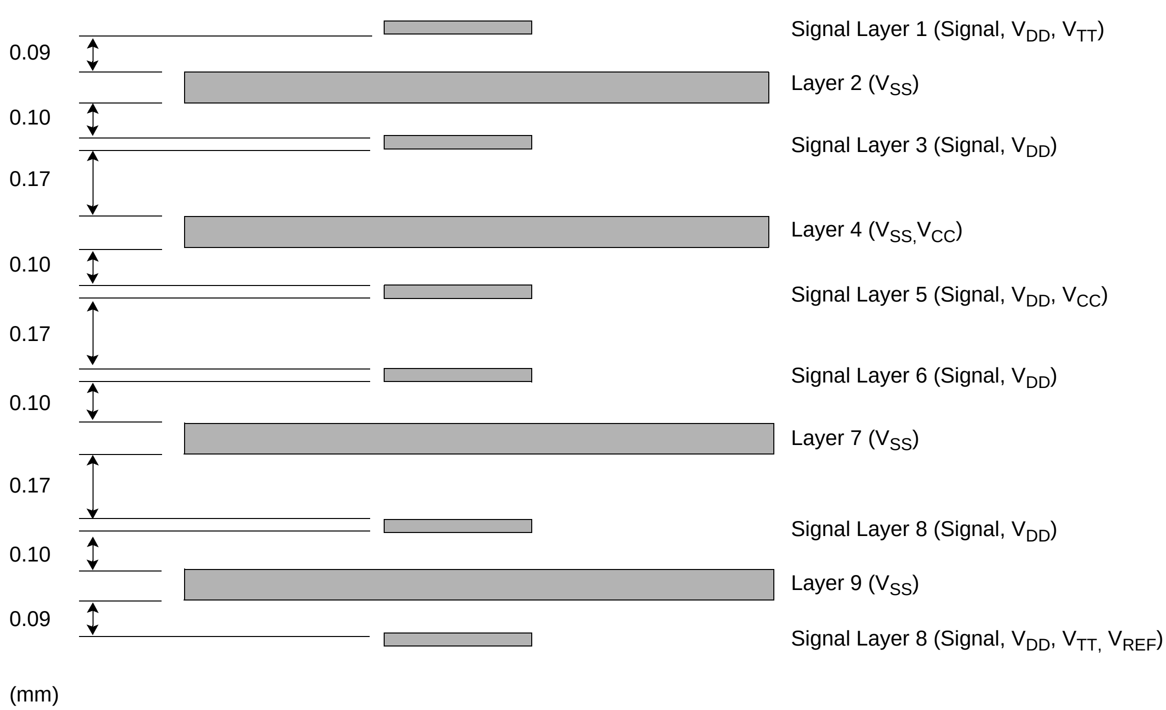
In order to allow DIMM card manufacturers to verify and monitor the trace impedances (Z_0 and Z_{diff}) listed above, measurement coupons have been added to the panels only (not the DIMM raw cards). A Time Domain Reflectometer (TDR) should be used to perform these measurements before DIMM assembly.

Example Eight Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Example Ten Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Example Timing Budget

The post-AMB timings on the Fully Buffered DIMMs are critical. The following tables describes a preliminary post-AMB timing budget for a typical DDR2 PC2-4200/PC2-5300/PC2-6400 Fully Buffered DIMM. Timing analysis is provided for read and write source synchronous data-to-strobe, strobe-to-clock, and address/command-to-clock. All skew budgets shall include the effects of trace length mismatch, crosstalk, inter-symbol interference (ISI) and VREF uncertainty.

The timing numbers used in the tables below are for example only - intention is to illustrate calculation method. Actual timing values should come from respective component specifications and calculated skew budget will differ accordingly.

Example DIMM Post-AMB Read Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCLK	Clock Cycle Time	3750	3000	2500	1
tHPmin	Minimum Clock Half Period at DRAM; tHPmin=min(tCL,tCH); tCL=CK low-level width; tCH=CK low-level width	1688	1315	1100	1
tDQSQ (dram)	DRAM DQS-to-DQ Skew	300	240	200	1
tQHS (dram)	DRAM Hold Skew Factor	400	340	300	1
tVALIDout (dram)	Data valid window at DRAM output tVALIDout = tHP - tDQSQ - tQHS	988	735	600	1
tSU (amb)	DQ and CB Input Setup TIme to DQS Crossing	-700	-530	-425	1
tHD (amb)	DQ and CB Input Hold TIme to DQS Crossing	1180	970	825	1
tSU + tHD (amb)	Sum of AMB Setup and Hold	480	440	400	1
DIMM Skew Budget	System Budget for DQ-to-DQS Skew (setup plus hold combined) = tVALIDout - (tSU + tHD)	508	295	200	1

Note 1: The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB Write Setup Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tDVB (amb)	AMB Data Valid Before DQS	750	575	470	1
tDS (dram)	DRAM Data Setup Time	350	300	250	1
Skew Budget	System DQ-to-DQS Setup Skew = tDVB - tDS	400	275	220	1

Note 1:The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB Write Hold Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tDVA (amb)	AMB Data Valid After DQS	750	575	470	1
tDH (dram)	DRAM Data Hold Time	350	300	250	1
Skew Budget	System Budget for DQ-to-DQS Hold Skew = tDVA - tDH	400	275	220	1

Note 1: The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB CK-to-DQS Timing (PC2-4200/PC2-5300/PC2-6400)[2]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCLK	Clock Cycle Time	3750	3000	2500	2
tDQSCKamb	Clock/DQS Skew at AMB	210	200	190	1, 2
tDQSSmax	tCLK * 1.25	4688	3750	3125	2
tDQSSmin	tCLK * 0.75	2813	2250	1875	2
Skew Budget	System CK-to-DQS Delay Skew (tDQSSmax) = tDQSSmin/max - tCK - tDQSCK	728	550	435	2

Note 1: tDQSCKamb includes allowance for clock output jitter
Note 2: The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB CK-to-C/A/Control Setup Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCVB (amb)	C/A/CNTL Valid before Clock	1615	1260	1030	1
tIS (dram)	DRAM Command/Address/Control Setup	500	400	375	1
Skew Budget	System Budget for DQ-to-C/A/Control Setup Skew (Setup) = tCVB - tIS	1115	860	655	1

Note 1:The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB CK-to-C/A/Control Hold Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCVA (amb)	C/A/CNTL Valid after Clock	1475	1120	890	1
tIH (dram)	DRAM Command/Address/Control Hold	500	400	375	1
Skew Budget	System Budget for DQ-to-C/A/Control Hold Skew (Hold) = tCVA - t IH	975	720	515	1

Note 1:The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Design collateral for specific Raw Cards

Some usage and design information is specific to an individual raw card design. This specification captures collateral information by raw card design.

ODT provides termination to DQ/CB signals and has programmable values that are dynamically turned on in response to ODT signals provided by the AMB. DDR values are programmed via MRS/EMRS settings.

ODT values

Card	Speed	Transaction	AMB[1]	Rank 0 ODT[1]	Rank 1 ODT[1]
R/C A	533/667	Write	OFF	75	N/A
		Read	65	OFF	N/A
	800	Write	OFF	75	N/A
		Read	65	OFF	N/A
R/C B, E, H	533/667	Write	OFF	150	150
		Read	65	OFF	OFF
	800	Write	OFF	75	150
		Read	65	OFF	OFF
R/C C	533/667	Write	OFF	75	N/A
		Read	65	OFF	N/A
	800	Write	OFF	75	N/A
		Read	65	OFF	N/A
R/C D, J	533/667	Write	OFF	150	75
		Read	65	OFF	OFF
	800	Write	OFF	OFF	50
		Read	65	OFF	OFF

Note 1: Recommended values.

Test Mode collateral

AMB devices support a mode that allows transparent access to DRAM interface directly with some special handling to accommodate double data rate data transfers. Details of operation in this mode are available in FB-DIMM AMB DFT Specification. The table documents the transparent DRAM interface signal mapping to the module pinout.

Transparent Mode Pinout

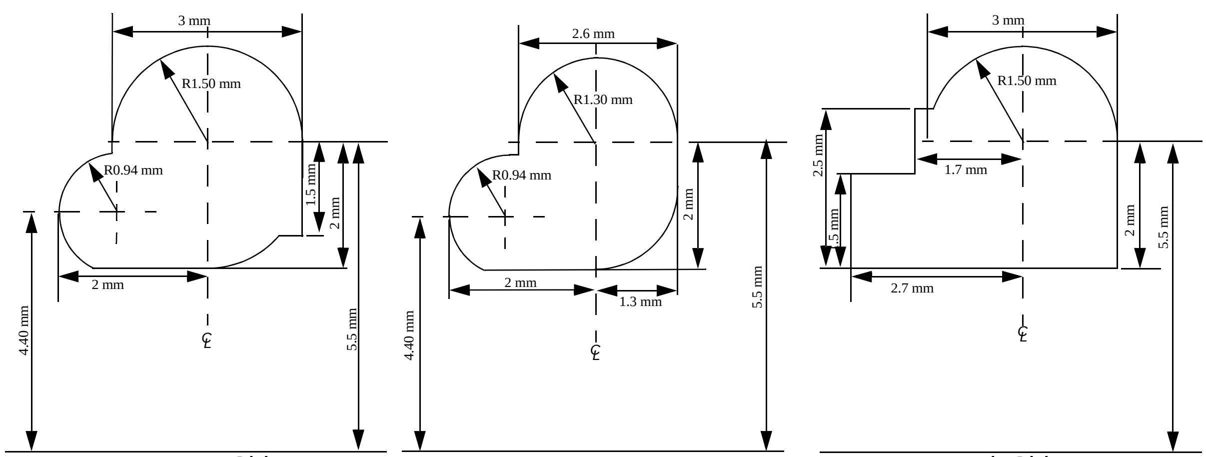
pin	Transparent Mode Signal	pin	Transparent Mode Signal	pin	Transparent Mode Signal
142	CKE[1]	181	A[3]	222	TPF[8]
143	CKE[0]	178	A[2]	219	TPF[7]
145	CS[1]	175	A[1]	216	TPF[6]
146	CS[0]	172	A[0]	213	TPF[5]
148	ODT	102	TDRV	202	TPF[4]
149	RAS#	103	TCMP	199	TPF[3]
151	CAS#	99	TDQ[15]	196	TPF[2]
152	WE#	96	TDQ[14]	193	TPF[1]
154	BA[2]	93	TDQ[13]	190	TPF[0]
155	BA[1]	82	TDQ[12]	40	TDQO[15]
157	BA[0]	79	TDQ[11]	48	TDQO[14]
160	A[15]	76	TDQ[10]	66	TDQO[13]
168	A[14]	73	TDQ[9]	63	TDQO[12]
186	A[13]	70	TDQ[8]	60	TDQO[11]
183	A[12]	100	TDQ[7]	57	TDQO[10]
180	A[11]	97	TDQ[6]	54	TDQO[9]
177	A[10]	94	TDQ[5]	222	TDQO[8]
174	A[9]	83	TDQ[4]	219	TDQO[7]
171	A[8]	80	TDQ[3]	216	TDQO[6]
161	A[7]	77	TDQ[2]	213	TDQO[5]
169	A[6]	74	TDQ[1]	202	TDQO[4]
187	A[5]	71	TDQ[0]	199	TDQO[3]
184	A[4]	--	--	196	TDQO[2]
--	--	--	--	193	TDQO[1]
--	--	--	--	190	TDQO[0]

Recommended trace keepout

AMB components may require some thermal solution that includes a heat spreader attached to AMB device. Heat Spreader attachment methods may require holes or notches for heat spreader retention features.

Below are recommended trace keep out regions that provide for a common keep out area that corresponds to component keep out regions documented in MO-256 details.
Keep-out areas are intended generally for use by AMB buffer Heat Spreader retention features; details are applicable to MO variations AA,AB,AC, BA,BB and BC. Through-holes, notches or associated retention features may be located in these areas.

Trace keep out area in connector area

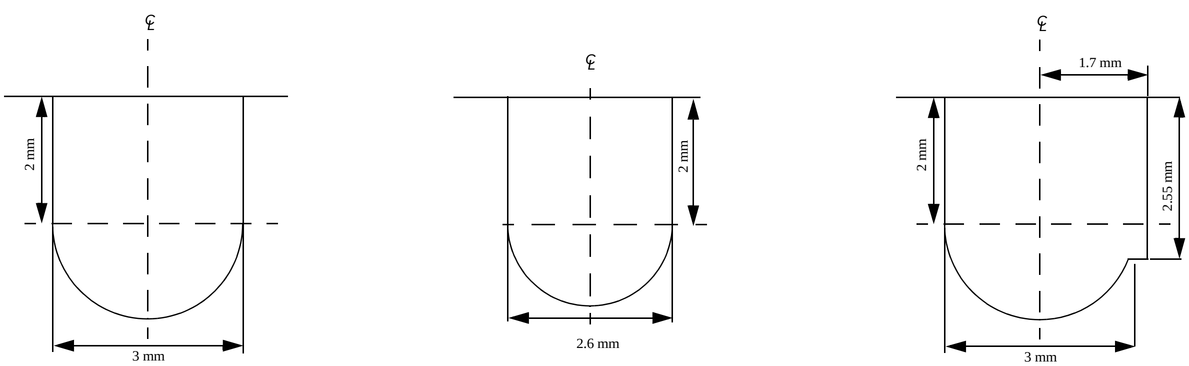


Front Side

Inner Layers
(Perspective from front side)

Back Side
(Perspective from front side)

Trace keep out area in module top edge area



Front Side

Inner Layers
(Perspective from front side)

Back Side
(Perspective from front side)

Vcc Power Delivery

Robust Vcc DC power delivery must be ensured by the FB-DIMM designs. System designers should ensure AMB voltage tolerance is met when these dimm requirements are included in a system analysis.

For purposes of design FB-DIMM designs should target 4.75 mOhm nominal impedance for Vcc DC resistance. Some variation among raw card designs is allowed via a design tolerance.
Additionally, manufactured modules will have some variations and is represented in a manufacturing tolerance. Manufactured modules **should** meet **the** resistance range that incorporates design tolerance and manufacturing tolerances. **Qualification of a design should be by direct resistance measurement. During HVM manufacture, power delivery quality can be verified indirectly by functional tests.**

Effective Resistance Target 4.75 mOhm Nominal @ 23C(room temp)

Tolerance	Min	Max	Min resistance	Max Resistance	Comment
Design	-5%	+5%	4.51	4.99	Design Analysis must meet this range
Manufacturing	-15% Total (Design Min -10%)	+22% Total (Design Max +15%)	4.06	5.74	All manufactured modules must meet this range

Effective Resistance is the Vcc-to-Vss path resistance seen from the module edge fingers, it is comprised of two components: Reffective = Rvcc + Rvss.

Measurement of the effective path resistance is impractical due to multiple paths involved;

A satisfactory approximation is Reffective = Rkelvin + 0.70 mOhm;
where:
Rkelvin is a specific measurable path,
0.70 mOhm accounts for Rvss and residual Rvcc elements not included in Rkelvin path

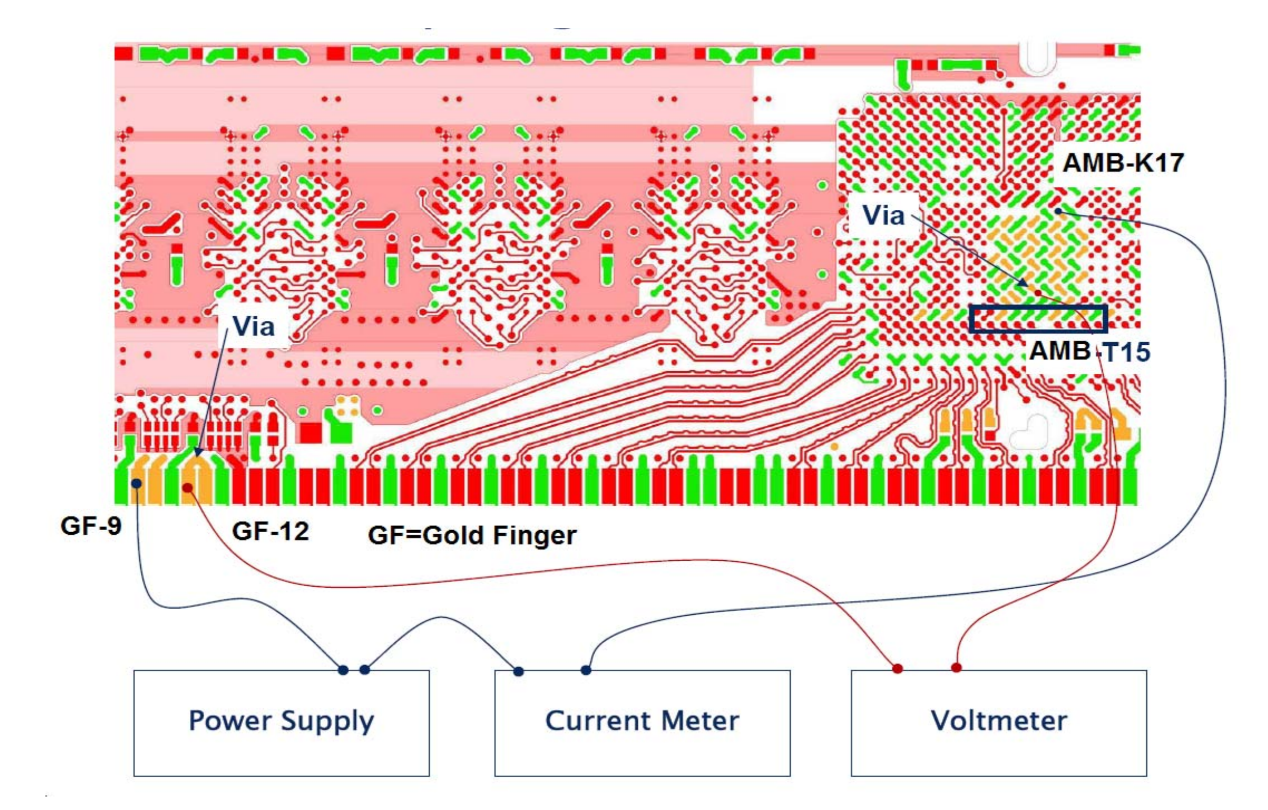
For purposes of standard analysis and measurement, the following measurement points shall be used for measuring Vcc DC resistance in a Kelvin 4-wire measurement. Deriving Vcc Resistance from measurement:

Rkelvin = |Vsense/Isource|

Kelvin Measurement Ports

Port	Adjacent Via of Edge Finger	Adjacent Via of AMB Ball	Function	Comment
A	9	--	Source HI	Current Source
B	12	--	Sense HI	Voltage Sense +
C	--	T15	Sense LO	Voltage Sense -
D	--	K17	Source LO	Current Source return

Rkelvin Measurement Diagram



Injecting 100mA of current with a well regulated power supply, actual current and voltage can be measured with precision to derive Rkelvin.

Suggested equipment requirements for measurements

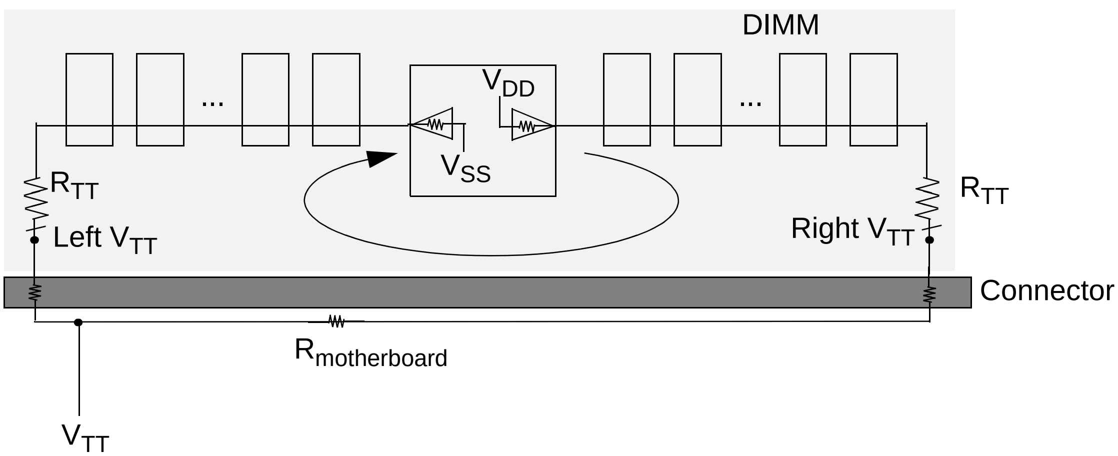
Equipment	Measurement Range	Minimum Resolution	Comment
Power Supply	100mA		current limit set point
Digital Meter	100mA	see note 1	Isource
Digital Meter	20mV	see note 1	Vsense

Note 1: Required tolerance is 1% or better. Designers should ensure analysis method accuracy through correlation to kelvin measurement results. Example analysis:
Rkelvin = 5mOhm; Accuracy 1% (50uOhm); Current set point: Isource = 100mA
Minimum Volt-meter resolution: 100mA x 50uOhm = 5uV
Minimum Current-meter resolution:5uV / 5mOhm = 1mA

V_{TT} Provisions

AMB buffers provide complementary CA bus (between left CA bus and right CA bus). Complementary drivers generate current that travels through the R_{TT} network between the left and right CA buses.

Example Complementary CA Bus Current Path



$$I_{left} = 0.9V/(R_{driver} + R_{TT} + R_{connector})$$
$$I_{right} = 0.9V/(R_{driver} + R_{TT} + R_{connector} + R_{motherboard})$$

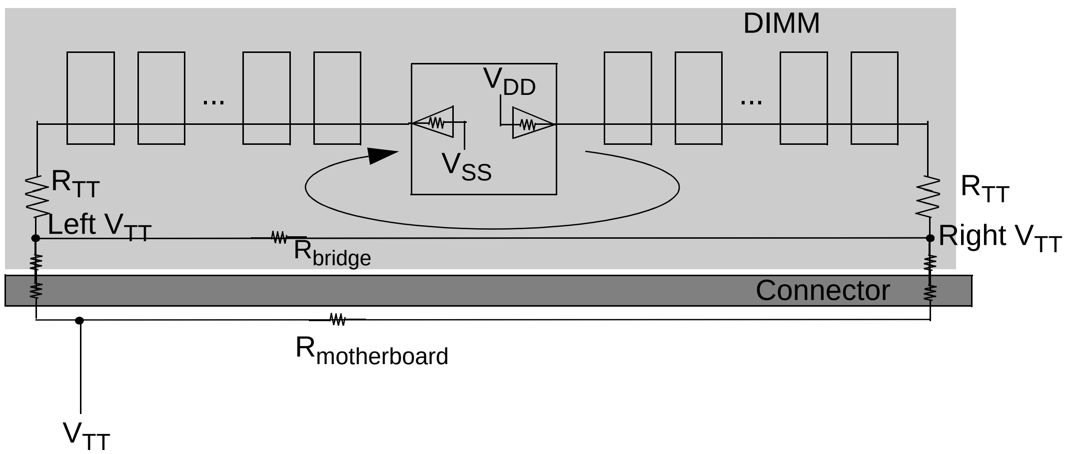
$$\text{Delta} = M(I_{left} \times R_{connector}) + M(I_{right} \times R_{connector}) + MN(I_{right} \times R_{motherboard})$$

where: Delta is difference between Left V_{TT} and Right V_{TT},
N=number of dimms installed in system,
M=number of complementary CA signals

(Complete analysis requires complex summations not shown here)

For purposes to limit V_{TT} voltage difference between left and right R_{TT} networks (due to voltage drop of connector and motherboard) some FB-DIMM designs should provide a connection on the dimm between left and right V_{TT} rails. Requirements of connection are dependent on R_{TT} values and subsequent analysis with system assumptions (complex summations). .

Example FB-DIMM bridge connection requirement



(Complete analysis requires complex summations not shown here)

Based on analysis, the following resistance design requirements were developed to ensure V_{TT} tolerance range is met when complementary CA bus operation is considered. Effort should be spent to minimize effective resistance as low as is feasible. Meeting the max values shown in the table will ensure that induced offset on V_{TT} supply is controlled. System designers need to ensure that baseboard contributions in conjunction with these DIMM assumptions limit induced offset to values shown in Product Family Attributes table earlier in this document.

Effective Resistance (mOhm) Max @ $23°C$ (room temp) for 533/667 FB-DIMMs

Module	Edge Finger to Rtt network	R bridge	Comment
R/C A	6	N/A	No left/right connection needed
R/C B	6	N/A	No left/right connection needed
R/C C	6	N/A	No left/right connection needed
R/C D	10	50	
R/C E	7	52	
R/C H	7	52	
R/C J	10	50	

Effective edge finger to R_{TT} network Resistance is the average path resistance seen from the module edge fingers to local R_{TT} network.

Measurement of the effective path resistance is impractical due to multiple paths involved;

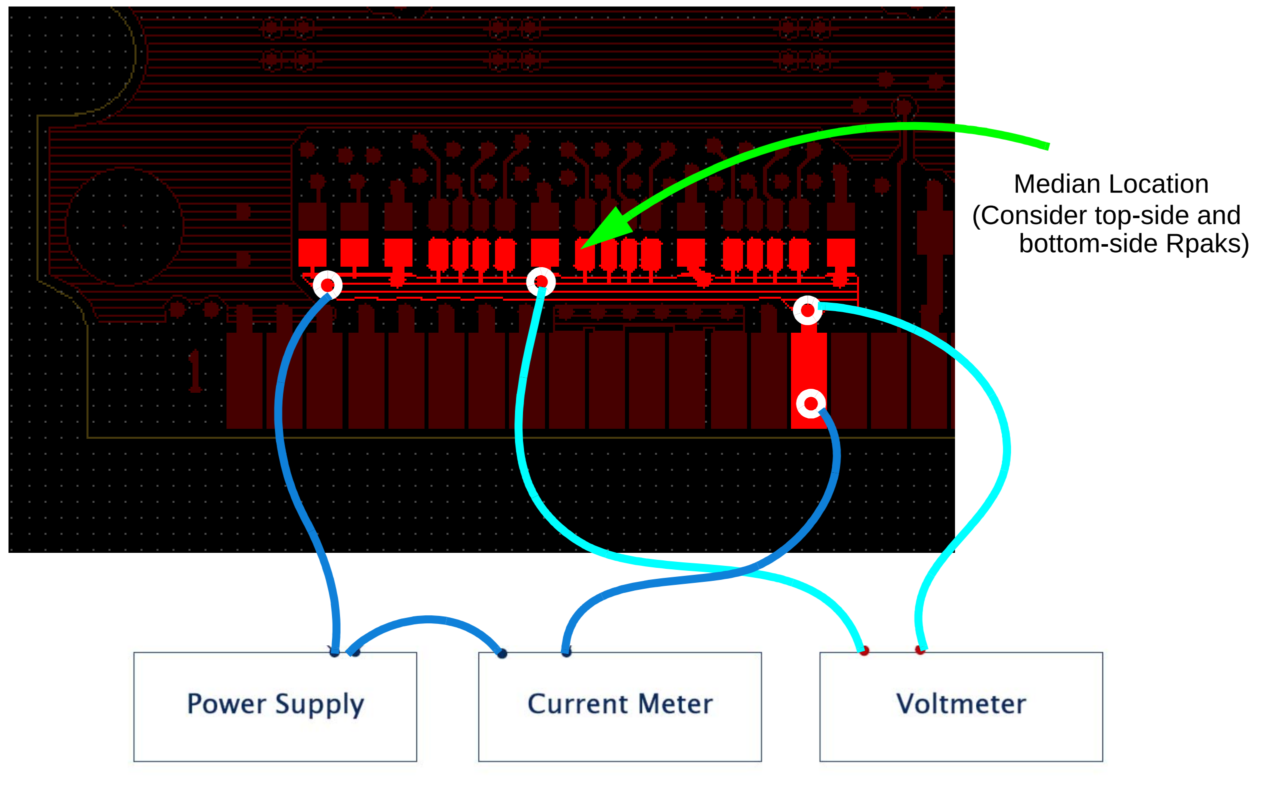
A satisfactory approximation is Reffective = Rkelvin ;
where:
Rkelvin is a specific measurable path representative of the median path,

For purposes of standard analysis and measurement, the following measurement points shall be used for measuring V_{TT} DC resistance in a Kelvin 4-wire measurement. Deriving V_{TT} Resistance from measurement:

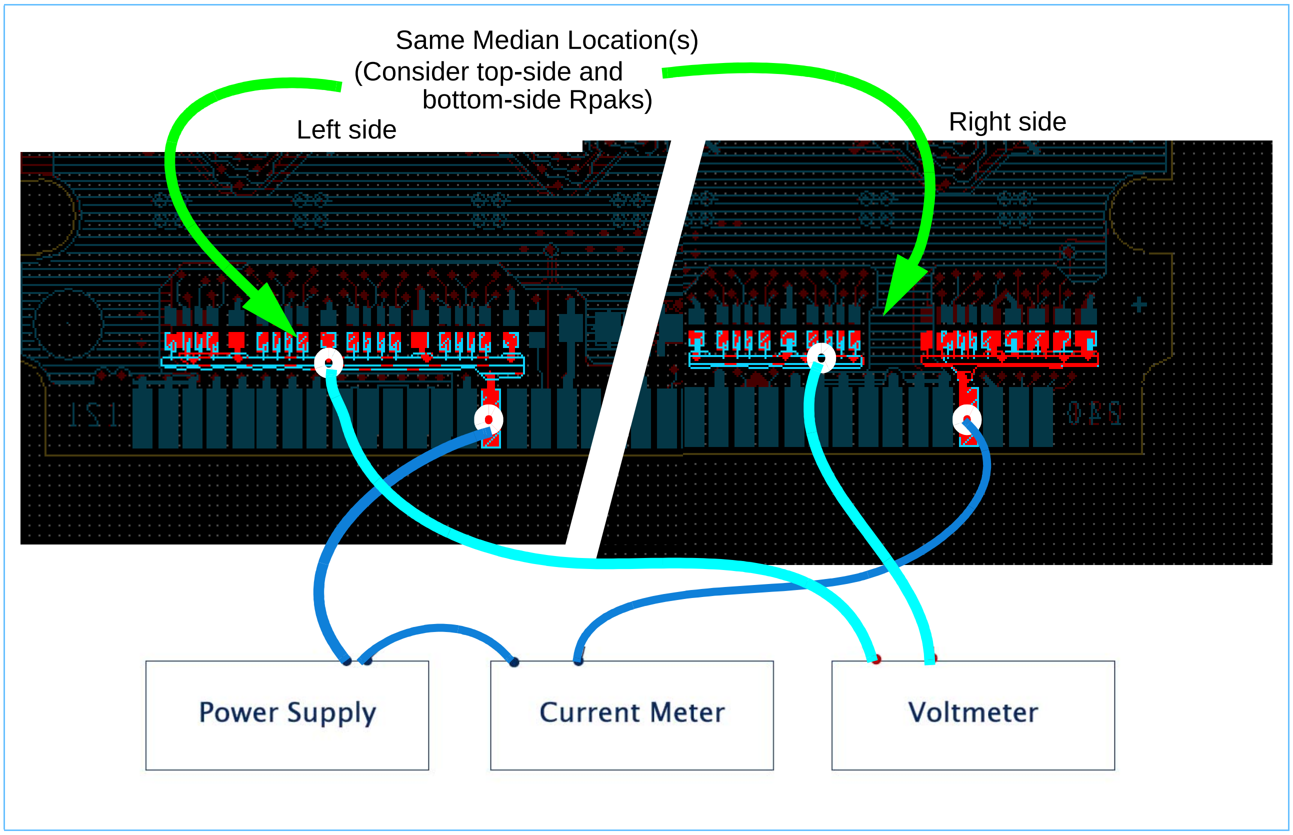
Rkelvin = |Vsense/Isource|

Typical Rkelvin Ports

(Shows typical Left Edge finger to R_{TT}network, use similar ports for right side)



Typical Rkelvin Ports (Shows example R bridge measurement)



Injecting 100mA of current with a well regulated power supply, actual current and voltage can be measured with precision to derive Rkelvin;

Equiment considerations are the same as those specified in Vcc Resistance measurement.

Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the PC2-4200/PC2-5300/PC2-6400 DDR2 SDRAM FB-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC FB-DIMM SPD Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices (Refer to JEDEC ballot JC-45... for SPD field definitions)

The following table is intended to be an **example** of a fast bin PC2-6400 DIMM. SPD values indicating different DIMM characteristics will be utilized based on specific characteristics of the DIMMs. This example assumes:

- Module Organization: 512MB (64Mx72)
- Device Composition: 64Mx8
- Device Package: FBGA
- Module Physical Ranks: 1
- CAS latency: 4

(Editor Note: Table Below is subject to review in SPD TG)

Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
0	Number of Serial PD Bytes in CRC	size=256; CRC = 116; used bytes=128	0x92	
1	SPD Revision	rev 1.0	0x10	
2	Key Byte/ DRAM Device Type	DDR2 FB-DIMM	0x09	
3	Voltage levels of this Assembly	Dram=1.8V; channel=1.5V	0x12	
4	SDRAM Addressing	row=14 col=10 bank=4	0x44	
5	Module Physical Attribues	30~35mm height 8~9mm thick	0x24	
6	Module Type	FB-DIMM 133.35mm nom	0x07	
7	Module Organization	1 rank x8 device width	0x09	
8	Fine Timebase Divend and Divisor	5ps	0x51	
9	Medim Timebase Divident	1(0.25ns)	0x01	
10	Medium Timebase Divisor	4(0.25ns)	0x04	
11	SDRAM Min Cycle TIme (tCKmin)	3.75ns(266MHz)	0x0f	
12	SDRAM Max Cycle Time (tCKmax)	8ns(125MHz)	0x20	
13	SDRAM CAS Latencies Supported	CL=3,4	0x23	
14	SDRAM Min CAS Latency (tAA)	15ns	0x3c	
15	SDRAM Write Recovery Times Supported	WR=3,4	0x23	

Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
16	SDRAM Write Recivery Time (tWR)	15ns	0x3c	
17	SDRAM Write Latencies Supported	WL=4,5,6	0x34	
18	SDRAM Additive Latencies Supported	AL=0,1,2,3	0x40	**
19	SDRAM Min RAS to CAS Delay (tRCD)	15ns	0x3c	
20	SDRAM Min Row Active to Row Active Delay (tRDD)	7.5ns	0x1e	
21	SDRAM Minimum Row Precharge Time (tRP)	15ns	0x3c	
22	SDRAM Upper Nibbles for tRAS and tRC	0	0x00	
23	SDRAM Minimum Active to Precharge Time (tRAS)	45ns	0xb4	
24	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC)	55ns	0xdc	
25	DRAM Minimum Auto-Refresh to Active/Auto-Refresh Command (tRFC)	105ns	0xa4	
26			0x01	
27	SDRAM Internal Write to Read Command Delay (tWTR)	7.5ns	0x1e	
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	7.5ns	0x1e	
29	SDRAM Burst Lengths Supported	BL8,BL4	0x03	
30	SDRAM Terminations Supported	75/150	0x03	
31	SDRAM Weak Drivers Supported	supported	0x01	
32	SDRAM Average Refresh Interval (tREFI) / Double Refresh t / High Temp self-refresh rate support indication	7.8us, 1x hot refresh, no hot self-refresh	0x02	see byte 33
33	Bits 7:4: Tcasemax Delta Bits 3:0: DT4R4W Delta (	Tcasemax=85C DT4R4W case rise=0.8C	0x02	
34	Thermal resistance of SDRAM device package from top (case) to ambient (Psi T-A SDRAM) at still air condition based on JESD51-2 standard.	32C/W	0x40	
35	DT0: Case temperature rise from ambient due to IDD0/activate-precharge operation minus 2.8 ◦C offset temperature.	3.7C	0x20	
36	DT2N/DT2Q: Case temperature rise IDD2N/precharge standby operation and IDD2Q/precharge quiet standby operation	1.6C	0x10	
37	DT2P: Case temperature rise IDD2P/precharge power-down operation.	0.24C	0x10	
38	DT3N: Case temperature rise IDD3N/active standby operation.	2.4C	0x10	
39	DT4R/Mode Bit: Bits 7:1: Case temperature rise IDD4R Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	9.6C 4W > 4R	0x30	
40	DT5B: Case temperature rise IDD5B/burst refresh operation.	10.5C	0x15	
41	DT7: Case temperature rise IDD7/bank interleave read mode operation.	16C	0x20	
42..59	Reserved		0x00	
60..80	Reserved		0x00	

Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
81	FB-DIMM Channel Protocols Supported	ECC Only	0x02	
82			0x00	
83	additional Back-to-Back Access Turnaround Time	r/w 2clk w/r 1clk r/r 1clk	0x25	
84	AMB Read Access Time for DDR2-800 (AMB.LINKPARNXT[1:0] = 11)	(5 + 6/12)* tCK	0x56	
85	AMB Read Access Time for DDR2-667 (AMB.LINKPARNXT[1:0] = 10)	(4 + 4/12)* tCK	0x44	
86	AMB Read Access Time for DDR2-533 (AMB.LINKPARNXT[1:0] = 01)	(3 + 10/12)* tCK	0x3a	
87	Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition based on JESD51-2 standard.	24C/W	0x30	
88	AMB DT Idle_0	53C	0x35	
89	AMB DT Idle_1	77C	0x4d	
90	AMB DT Idle_2	71C	0x47	
91	AMB DT Active_1	98C	0x62	
92	AMB DT Active_2	77C	0x4d	
93	AMB DT L0s	not supported	0x00	
94	Reserved		0x00	
95	Reserved		0x00	
96	Reserved		0x00	
97	Reserved		0x00	
98	Reserved		0x00	
99	Reserved		0x00	
100	Reserved		0x00	
101	AMB Personality Bytes: Pre-Init	GB (rev 0.3)	0xc0	
102			0x00	
103			0x00	
104			0x44	
105			0x00	
106			0x00	

Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
107	AMB Personality Bytes: Post-Init	GB (rev 0.3)	0x40	
108			0x43	
109			0x00	
110			0x00	
111			0x6d	
112			0x04	
113			0x00	
114			0x05	
115	AMB Manufacturer's JEDEC ID Code	Intel ID	0x80	
116			0x89	
117	Module ID: Module Manufacturer's JEDEC ID Code	(TBD)	0x00	
118			0x00	
119	Module ID: Module Manufacturing Location		0x01	
120	Module ID: Module Manufacturing Date	year (2004)	0x04	
121		(week)	0x52	
122	Module ID: Module Serial Number	(TBD)	0x84	
123			0x00	
124			0x03	
125			0xc1	
126	Cyclical Redundancy Code	(TBD)	0x56	
127			0xc3	
128..145	Module Part Number	alpha string(TBD)	0x20	
146	Module Revision Code		0x00	
147			0x01	
148	SDRAM Manufacturer's JEDEC ID Code		0x00	
149			0x2c	
150	Manufacturer's Specific Data	GB SPD rev	0x00	GB SPD rev is example usage
151			0x03	
152..175			0xff	
176..255	Customer Use		0xff	

FBDIMM Label Format

The following label shall be applied to all DDR2 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields.

ggggg eRxff PC2-wwwwm-abc-dd-ef

Where:

- ggggg = Module total capacity, in bytes
  - 256MB, 512MB, 1GB, 2GB, 4GB, etc.
- eR = Number of ranks of memory installed
  - 1R = 1 rank of DDR2 SDRAM installed
  - 2R = 2 ranks
- xff = Device organization (bit width) of DDR2 SDRAMs used on this assembly
  - x4 = x4 organization (4 DQ lines per SDRAM)
  - x8 = x8 organization
  - x16 = x16 organization
- wwww = Module bandwidth in MB/s
  - 3200 = 3.20 GB/s
  - 4200 = 4.26 GB/s
  - 5300 = 5.33 GB/s
  - 6400 = 6.40 GB/s
- m = Module Type
  - E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
  - F = Fully Buffered DIMM ("FB-DIMM")
  - M = Micro-DIMM
  - N = Mini-Registered DIMM ("Mini-RDIMM"), no address/command parity function
  - P = Registered DIMM ("RDIMM"), with address/command parity function
  - R = RDIMM, no address/command parity function
  - S = Small Outline DIMM ("SO-DIMM")
  - U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- a = DDR2 SDRAM CAS Latency, in clocks at maximum operating frequency
- b = DDR2 SDRAM minimum tRCD specification, in clocks at maximum operating frequency
- c = DDR2 SDRAM minimum tRP specification, in clocks at maximum operating frequency
- dd = JEDEC SPD Revision Encoding and Additions level used on this DIMM
- e = Reference design file used for this design (if applicable)
  - A = Reference design for raw card A is used for this assembly
  - B = Reference design for raw card B is used for this assembly
  - Z = None of the reference designs were used for this assembly
- f = Revision number of the reference design used
  - 0 = Initial release
  - 1 = First revision
  - 2 = Second revision
  - P = Pre-release or Engineering sample
  - Z = To be used when field e = Z

Examples, single font:

1GB 1Rx4 PC2-3200F-333-10-C0

is a 1GB DDR2 Fully Buffered DIMM, using 1 rank of x4 SDRAMs operational to PC2-3200 performance with CAS Latency = 3, t_{RCD} = 3, t_{RP} = 3, using JEDEC SPD revision 1.0 (encoding type FB-DIMM), raw card reference design file C initial release used for the assembly

DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to JEDEC official site; http://www.jedec.org.

2. Click on ‘Free Standards ’ and enter the free download area.

3. Search by document number: ‘MO-256’ and download the PDF for this product family.

4. Or search by ‘JEP95’;‘JEDEC Publication 95.’ and open entire document,scroll down and select ‘MO-256’ to download the PDF for this product family.

Within MO-256, several DIMM thickness variations are defined. Variations are denoted by a two letter reference “XX”. The first (MSB) letter position encodes dimm thickness and height attributes . The second(LSB) letter position encodes keying position, three positions are defined(--A,--B,--C)

Note: Maximum DIMM thickness/height can be a measured maximum value, or can be calculated using the maximum component, card, label, and assembly process adders.

FB-DIMMs utilize a single keying position (--B) and can utilize any of the thickness/height variations.
Note: Some system platforms may be designed for a subset of specific variations.

To enable systems to electronically detect DIMM thickness, SPD byte 5 is encoded with the FB-DIMM thickness and height values. When used, in conjunction with other SPD bytes, system operating conditions can be adjusted based on installed modules and projected power consumption.

Supporting Hardware:

Summary of FB-DIMM Support/Development Hardware

Vendor	name	p/n
Agilent Customer Contact Center 800-829-4444 http://www.agilent.com/find/fbd us@agilent.com Agilent Technologies / Perry Keller 1900 Garden of the Gods Rd. Colorado Springs, CO, 80907 perry_keller@agilent.com (719) 590-5651 FuturePlus Systems Corp. / Bill Furch (719) 278-3540 http://www.futureplus.com	4x Resistor Pack Flying Lead Probe	N4234A
	4x/8x BGA DRAM Interposer Probe	N4237A
	Interposer Channel Analysis Probe	FSI-60105 / FS2343
	DIMM Parametric Test Fixture	N4236A
	Slot Channel Analysis Probe	FSI-60097 / FS2338
	Slot Parametric Probe	N4238A
	AMB Parametric Test Fixture	N4235A
	RC/B Validation DIMM Logic Analysis Probe	FSI-60099 / FS2340
Tektronix Customer Support Center 800-833-9200 x3 503-627-2400 Fax: 503-627-5695 www.tek.com/memory Tektronix, Inc. David Haworth PO Box 500, M/S 39-345 Beaverton, OR 97077-0001 503-627-3127 David.A.Haworth@tek.com Nexus Technology, Inc. Bruce Krobusek 877-595-8116 x803 brucekro@busboards.com	12.5GHz Z-Active Differential Probe	P7313
	Serial Data Compliance and Analysis Software	TDSRT-EyeTM v2
	Jitter and Timing Analysis Software	TDSJIT3 v2
	FB-DIMM Interposer Probe & Analysis Software	NEX-FBD-LAI
	FBD Oscilloscope Probing Kit	NEX-TDSFBDP
	FB-DIMM AMB to DDR2 Analysis Probe & Software	NEX-FBD-NEXVu

Summary of FB-DIMM Support/Development Hardware

Vendor	name	p/n
King Tiger Technology Inc., David Jaime 9601 Amberglen Blvd., Suite 120, Austin, TX 78729 512-401-8775 http://www.kingtigertech.com	King Tiger KT-2Pro DIMM Tester	King Tiger KT-2Pro DIMM Tester
Pycon Inc 3301 Leonard Court Santa Clara, CA 05054 Rob Ortega (408) 450-5609 rortega@pycon.com	Channel Test Card (CTC)	FB-DIMM Channel Test Card

Diagnostic Sense Line

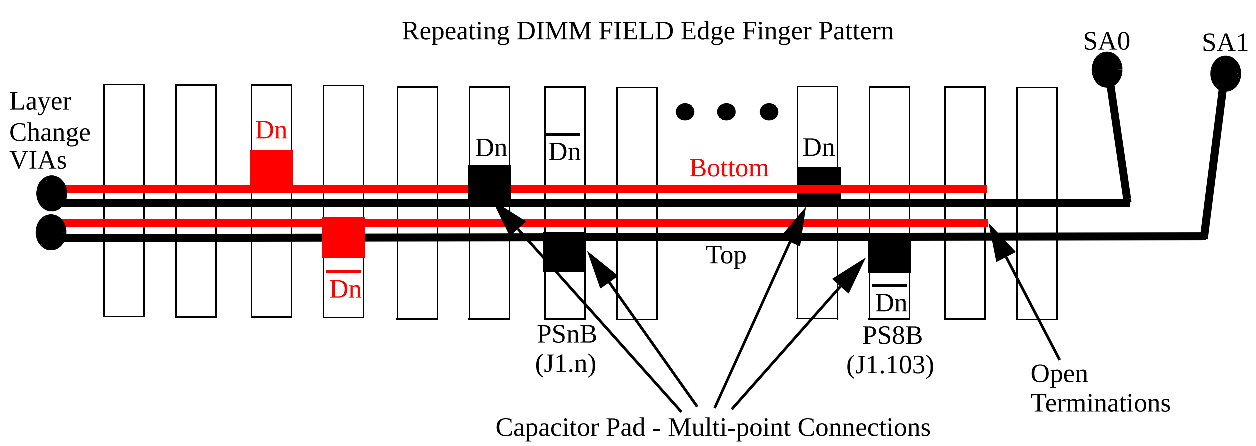
FBDIMM - Diagnostic Sense Line Specification, Introduction

FBDIMM Diagnostic sense lines are by design, ground referenced transmission lines, with specifically placed, routine and regular, capacitor pad multi-point connections. These sense lines couple to the "True" and "Compliment" high speed differential data card edge fingers, by means of proximity capacitive interconnect technology.

In a system that implements sense lines, the connection from the Memory Controller Unit (MCU) to the FBDIMM Hub chip now becomes a multipoint connection connecting the MCU to the Advanced Memory Buffer (AMB) and with diagnostic sense line connections to the Instrumentation Chip. The Instrumentation Chip serves as the diagnostic detection chip, to sense the signal activity or lack of signal activity on the High Speed Link. It does this one side of a differential pair at a time, and thus is capable of diagnosing the electrical continuity between the MCU and the AMB.

Diagnostic sense lines are routed just under the card edge fingers and begin at one end of the DIMM finger field pattern, then travel perpendicularly across the DIMM finger field down to the other end of the DIMM. The test traces then cross over to the other side of the PCB through a pair of layer change VIAs. They then travel back towards the point of origination in the same fashion with an open termination at the end of the line. See General Concept below.

General Concept



Implementation Details

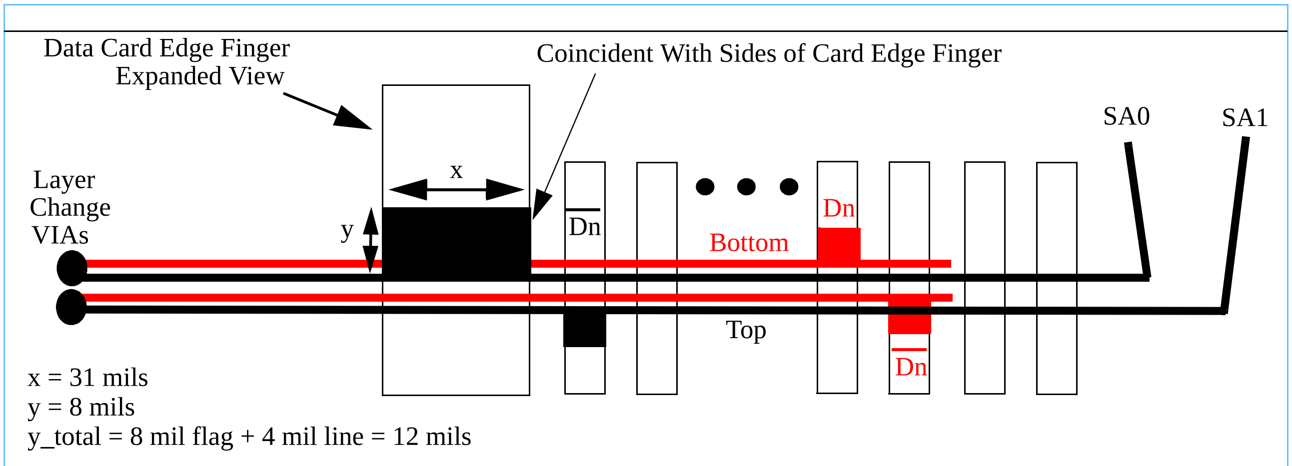
Capacitor Pad Connection Concept

There are one pair of sense line capacitor pad traces per DIMM. Each sense line shall originate at the right side of the DIMM (oriented card edge finger down and top side up). One sense line capacitor pad capacitively connects to the North and Southbound high-speed TX/RX "True" card edge fingers starting at PS8 (J1.102) then, PS7 (J1.99), then PS6 (J1.96), and continuing on. The other capacitively connects to the corresponding North and Southbound high-speed TX/RX "Compliment" card edge fingers starting at PS8B (J1.103) then, PS7B (J1.100), then PS6B (J1.97), and continuing on. See General Concept.

Capacitor Connection Pad Size and Placement

The capacitor connection pad is designed to be 31 mils x 12 mils. Each Flag extends off of the transmission line width is 8 mils. Adding the transmission line width (4 mils) results in the 12 mil pad height. The pads are placed as shown below.

Capacitor Connection Pad



Diagnostic Sense Line Routing Line Width and Spacing

Diagnostic sense lines shall have a line width of 4 mils and a edge to edge spacing of 4 mils.

Diagnostic Sense Line Same Layer Isolation

Diagnostic sense lines shall be isolated from any other active route or shape on the same layer by greater than or equal to 20 mils.

Diagnostic Sense Line Adjacent Layer Isolation

Diagnostic sense lines shall be isolated from any other active route or shape on the adjacent signal layer by greater than or equal to 20 mils. Crossing the diagnostic sense lines in any way with routes or shapes on the adjacent signal layers is not allowed.

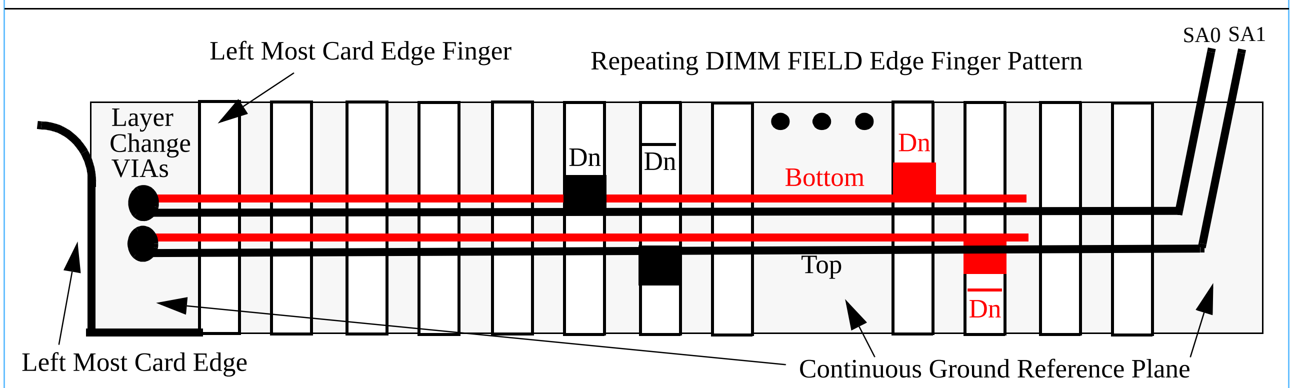
Diagnostic Sense Line Reference Planes

Diagnostic sense lines shall be referenced to ground. Ground shapes shall be placed on layers 3 and 4, or 3 and 6, or 3 and 8 of a 6, 8, or 10 layer board respectively. They shall shadow the card edge finger field all along the card edge of the DIMM. The width of the shape is essentially set to be the height of the rectangular card edge finger shape height.

There are two approved topologies shown in **Diagnostic Sense Line Topologies, Segment Lengths, and Terminations** section later in this text. Both of these topologies must be implemented with a uniform and continuous ground reference plane. See example of preferred topology with a uniform and continuous ground reference plane shown in the figure below.

Note – Uniform and continuous ground plane is required to follow the sense line routes around the notch. This is not shown in figure below but is implied.

Diagnostic Sense Line Reference Plane Shape and Location



Layer change transition VIAs are designed with the following parameters:

1. VIA Type = Plated Through Hole
2. VIA Drill Hole Size = 12 mils +0.002/-0.006
3. VIA Land (Internal) = 18 mils
4. VIA Land (Outer) = 20 mils
5. VIA Antipad (Internal) = 30 mils
6. VIA Finished Hole Size = 12 mils

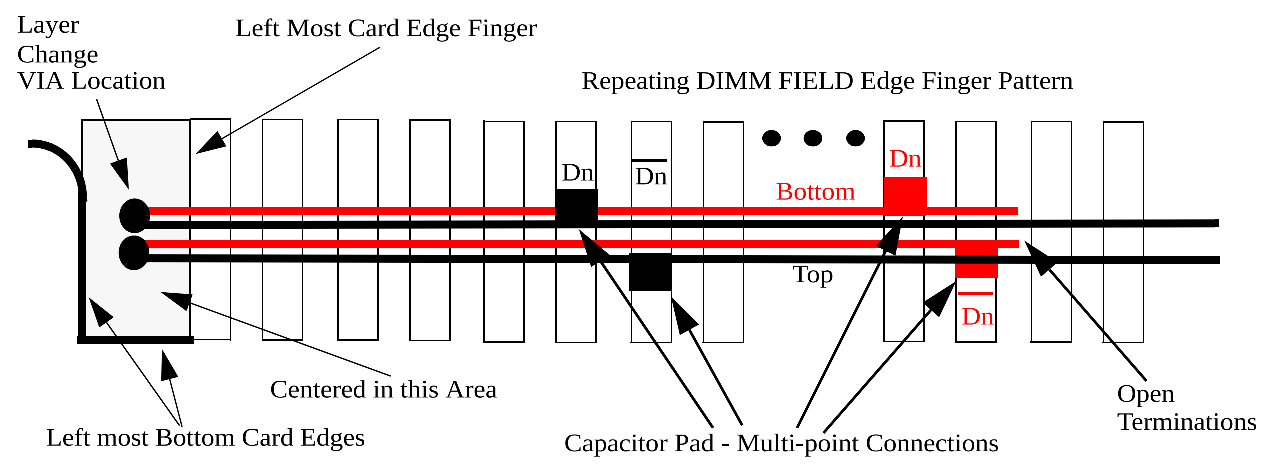
Note – Remove the pads from unconnected layers

Diagnostic Sense Line Layer Change VIA location

Layer change transition VIAs are to be placed at the left side of the board and centered in the region bounded in the "X" direction by the left card edge and the left most edge of the last card edge finger. They are bounded in "Y" direction by the bottom card edge and the top of the card edge finger shape. See figure below.

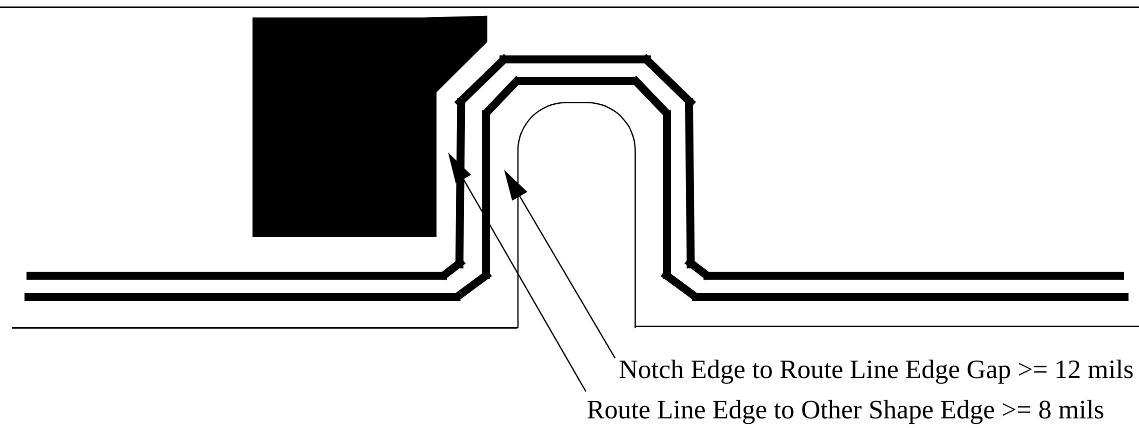
Routing around the DIMM Key Notch

Layer Change Transition VIA Location



When routing around the DIMM key notch, care must be taken to maintain the 4 mil line width and 4 mil spacing. Use 45 degree angle turns as shown below.

Routing Around the DIMM Key Notch



Diagnostic Sense Line Topologies, Segment Lengths, and Terminations

There are two acceptable diagnostic sense line topologies. The first is the preferred topology. The second is a less than optimal alternate, but approved topology.

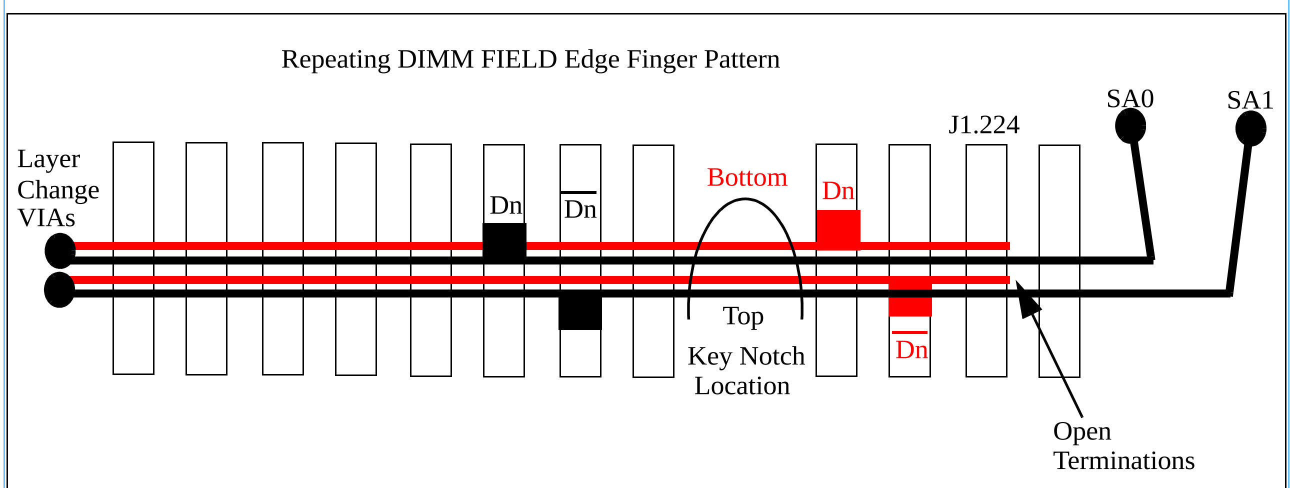
Preferred Topology

A pair of diagnostic sense lines shall travel from the right side of the card (oriented card edge finger down and top side up). They originate at a pair of VIAs connected to address bits SA0 and SA1. They run horizontally under the card edge fingers towards the left side of the card. The route travels on layer 2 of either a 6, 8, or 10 layer board. This leg of the sense line route is to be approximately 5.2 inches long.

The sense line pair then crosses over to the opposite side of the PCB through a pair of layer change vias. Once on the opposite side, they are to travel back towards the point of origination on layer 5, 7, or 9 of a 6, 8, or 10 layer board respectively.

The route is to then terminate at the right most edge of card edge finger J1.224 as an open termination at the end of the line. This leg of the route is to be approximately 4.5 inches long. See Preferred Topology shown below.

Diagnostic Sense Line - Preferred Topology



Alternate Topology (Forked Topology)

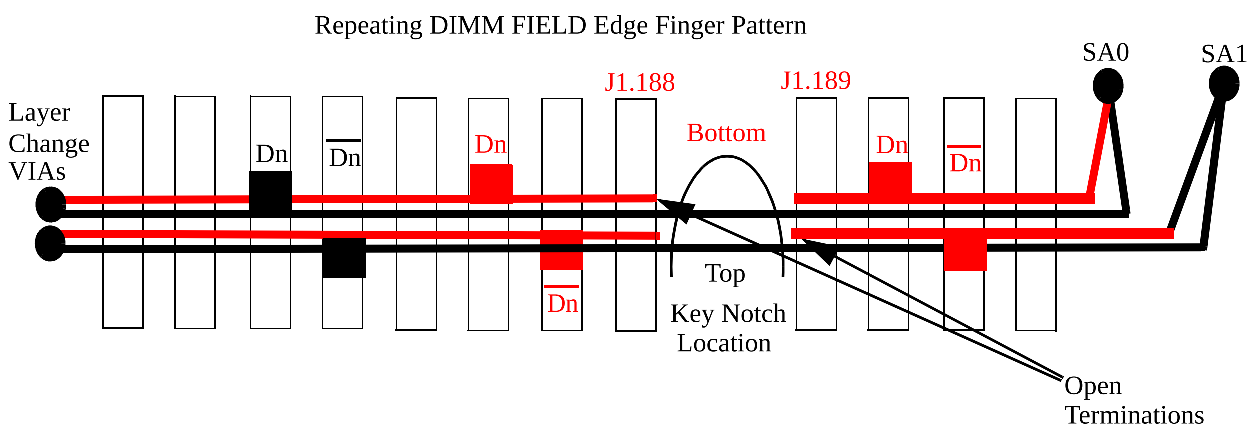
A pair of diagnostic sense lines shall travel from the right side of the card (oriented card edge finger down and top side up). They originate at a pair of VIAs connected to address bits SA0 and SA1. They run horizontally under the card edge fingers towards the left side of the card. The route travels on layer 2 of a 6, 8, or 10 layer board. This leg of the sense line route is to be approximately 5.2 inches long.

The sense line pair then crosses over to the opposite side of the PCB through a pair of layer change vias. Once on the opposite side, they travel back towards the point of origination on layer 5, 7, or 9 of a 6, 8, or 10 layer board respectively.

This back side segment terminates at the right most edge of card edge finger J1.188 as an open termination at the end of this line segment. This leg of the route is to be approximately 2.7 inches long.

A second back side sense line segment originates and forks off of the same VIAs connected to address bits SA0 and SA1 (right side of the card) and then travels right to left on layer 5, 7, or 9 of a 6, 8, or 10 layer board respectively. This back side segment terminates at the left most edge of card edge finger J1.189 as an open termination at the end of this line segment. This leg of the route is to be approximately 2.2 inches long. See Alternate Topology below.

Diagnostic Sense Line - Alternate Topology



Conclusion

While both the Alternate and the Preferred Topologies are designed to provide adequate diagnostic sense line signal strength to the input of the Instrumentation Chip, the implementation of the Preferred Topology will produce the highest signal power possible for any given system implementation.

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DDR2 SDRAM Fully Buffered DIMM Design Specification

Revision Log

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Revision	Pages	Changes
Intel 0.55b	all	Initial content
Intel 0.60a		Removed all references to raw cards E and F Updated net topologies and lengths for channel Added pair-to-pair spacing rules for channel Updated net lengths for DRAM data Added pin descriptions and pinout for AMB Showed DM connection on x8 DIMMs Changed AMB on block diagram to show channel flow through NC pins on DRAM may be connected to VDD on DIMM Updated R/C A picture to show support for wider DRAM Removed example SPD values
	all	Added "JEDEC Confidential -- For Internal Use Only"
	5	Removed "also used to select DIMM number in AMB" from SDA, really belongs on SA(2:0)
	18	Added note 2, TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes
	23	Added note on DRAM size for R/C A
	30	For pair-to-pair spacings, separation is a multiple of dielectric height only
	32	Updated clock trace lengths
	34	Replaced "byte spread" with |DQ - DQS|
Intel 0.60b	5	Added "also used to select DIMM number in AMB" to SA(2:0)‘
	6	Changed pin 117, 237 to VTT
	8,10	Removed ‘s’
	9,10	changed ‘byte’ to ‘nibble’
	11-14	changed notes concerning NC pins
	15-16	added language on footprint NC/NU pins from registered DIMM spec
	18	added ‘also used to select DIMM number in AMB” to SA[2:0]
	24	added side view
	32	add note about CK0 on left, CK1 on right
	43	change FB- to PC2-
Intel 0.60c	3	Added table including channel clock and transfer rate, added "DRAM" to clock in text
	4	Added Introductory table of raw cards. Re-ordered notes on environmental table
	5	Added "DIMM connector" to title.

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	11	Added introduction to the DRAM component and common footprint details
	28-39	Removed references to trace impedance, Removed offset skew in AMB package and DIMM, increased max on SB signals by 2.2 mm Updated R/C B Command/Address bus trace lengths, renumbered segments Updated R/C B Control bus trace lengths, renumbered segments
	40	Indicated that power is typically delivered on outer layer power islands
	42	Re-calculated timing budgets using skew budgets, instead of margins
	43	Added calculations for CK-to-DQS and CK-to-C/A/Control
	44	Added note that table is temporarily removed
Intel 0.60d	12,14	changed 60 to 63 balls
	13	changed A1 reference to E2
	15	Changed A2 reference to H2. Changed H2, L1 and L9 in x4 package from NC to NU
	16	Changed 68 to 71 balls. Changed H2, L1 and L9 in stacked x4 package from NC to NU
	28-30	Replaced TL1 with TL- in the notes
	29	Changed 8.4 to 9.1 mm. For matching tolerance on northbound primary channel, distinguish between nets shorter and longer than 12 mm (this is especially for PN10/PN10#)
	38	Organized control into variation 1 and 2, updated lengths, changed R1 back to TBD
	40	Clarified component breakout, changed 0.100 to 0.102
0.20a		Changed to JEDEC rev 0.20 from Intel rev 0.60e
	5	non-stacked variations called out as MO-256 variation AB stated variations called out as MO-256 variation BB
	7	RFU pin count was reduced DNU/M_Test was added Note 2 was updated to reflect correct RFO accounting
	8	FBDIMM Pinout diagram updated for DNU/M_Test
	9~12	Power connectivity adjusted to include SPD
	24	Module Configuration table updated to reflect 4Gb page size change to be the same as 1Gb and 2Gb page sizes
	25~27	updated component placement diagrams and associated side-views
	29	added notes to indicate $\overline{DQS}$ usage on R/C's A & B added noes to indicate left and right copies of DRAM Addr/cmd/ctrl
	31	added R/C's A & C to trace length table TL1 and SUM changed to unique min and max values
	32	added R/C's A & C to trace length tables PN TL1 and SUM Max values changed to 34.4 SN TL1 max changed to 34.6; SUM max changed to 37.0 Notes updated short pair matching from TBD to +/- 0.5 mm

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	33	SS TL1 max changed to 39.1 SS SUM max changed to 42.3 Pair-to-Pair changes: microstrip outer < 20mm changed to 4.25xheight microstrip outer > 20mm changed to 5.25xheight stripline changed to 3.7xheight added 4 notes Added Minimum Trace Widths table for System Data Channel Nets
	34	changed “Copy A” to “Variation 1” In variation 1, changed TL1 segment to TL3, added new TL1 in series with TL0 added specific values to trace length table for R/C A split note 1 into notes 1 & 2 added note 4
	35	changed B CK1 TL1 min to 8.6 changed note 2 to “Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.5 mm”
	36	R/C A DQ/CB/DQS/$\overline{\text{DQS}}$ TL0 updated separate min/max values Note 1 dropped tolerance reference Note 3 changed to “Trace length difference between the DQS/DQS traces and the DQ traces of a given byte (Raw Card A) or nibble (Raw Cards C, D) must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm. DRAM positions TBD have TBD additional trace on DQS/DQS#
	37	In DQ diagram changed “DIMM Connector” to “AMB” Note 3 changed to “Trace length difference between the DQS/DQS traces and the DQ traces of a given byte (Raw Card A) or nibble (Raw Cards C, D) must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm. DRAM positions TBD have TBD additional trace on DQS/DQS#
	38	added separate R/C C DQ diagram and table
	39	added separate R/C A Address/Command diagram and table
	40	updated R/C B and C Address/Command Trace lengths added R1 value of 39 ohms Note 5 dropped “from the AMB output to the pad of the VTT R-pack”
	41	added R/C A Control Trace Lengths added R/C A R1 value of 39 added R/C B R1 value of 47 changed notes 4~6 to: 4. For Raw Card A, variation 1 is for CS0B and CKE0B, variation 2 is for CS0A, CKE0A. 5. For Raw Card B, variation 1 is for CS1A, CKE1A, CS0B and CKE0B, variation 2 is for CS0A, CKE0A, CS1B and CKE1B. 6. On Raw Card A, any two adjacent TL4 segments have a sum of between 19.1 and 19.7 mm. 7. On Raw Card B, any two adjacent TL4 segments have a sum of between 27.0 and 32.3 mm.
	42	added R/C C Control diagram and table
	45	On Cross Section Recommendation, Note in edge connector dropped “and not chamfered” PCB Electrical Specs changed to include nom 60 Ohm for single ended, w/adjustments to min/max nom 85 for Zdiff DRAM clocks and DQS/DQS# w/adjustments to min/max
	46	added trace geometry examples to single-ended table removed 100 Ohm example from outer layer differential example.

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	47~48	Footnoted unofficial AMB/DRAM timing values as unapproved estimates.
	51	changed 4.26 GB/sec to 4.27 GB/sec changed 5.34 GB/sec to 5.33 GB/sec
0.21	global	changed PC2-4300 to PC2-4200
	5	added min/max values 1.7/1.9 for DRAM added min/max values 1.46/1.54 fro AMB; footnoted as estimate added min/max values 0.48*VDD/0.52*VDD for VTT added min/max values 3.0/3.6 for VDDSPD
	7	updated editorial wording of M_test description
	9~12	added “control” to Rtt terminated groups in block diagrams changed ‘banks’ to ‘ranks’ in R/C Block Diagram titles page 11: changed ‘72’ to ‘x72’ in diagram title
	19	(new page) added Early 2Gb x4 and x8 Ballout with support balls; note calls out x4 differences
	27~29	updated side-view dimensions to reflect proposed JC-11 MO-256 base values w/o HS
	31	changed Dram Address/Command/Control Notes: “one set for left, one set for right”
	33	updated R/C C System Clock Trace Lengths as per Infineon: TL0 1.9; TL2 0.6;
	36	updated R/C A AMB CLK Output to SDRAM Trace Lengths: R/C A Variation 2 TL1min from 14.6 to 14.7; TL4min/max from 18.2/18.4 to 19.8/20.2 R/C A Variation 1 TL3max from 10.7 to 10.0; TL4min form 18.5 to 18.4
	37	added AMB Clock Output to SDRAM Trace Lengths for R/C C values as per Infineon
	40	(new page) added unique R/C C DQ/C/DQS/DQS# diagram and table
	41	added unique R/C C to Address/Command diagram (R/C B,C,D; variation #1) and table
	42	added unique R/C C to Address/Command diagram (R/C B,C,D; variation #2) and table
	45	updated R/C C Control Net Trace Length: TL0max fro m2.7 to 2.2; End-to-End max from 79.8 to 78.0 removed reference to R/C F
	49	(new page) added Example Eight layer Stackup diagram
	53	changed ‘Module Physical Banks’ to ‘Module Physical Ranks’
	55	In labeling spec, changed 4300 to 4200 for module bandwidth
0.5	global	removed multiple footer references to approved/passed ballots as well as bars that indicate changes to previous document revisions
	6	clarified explanation of R/C
	25	timing parameters in table were changed to be consistent with the rest of document added note 1
	26	added the latest specification numbers
	34, 35, 36	updated trace lengths for R/C A, B and C added trace lengths for R/C D
	39	added diagram for R/C D net structure routing for AMB Clock Output to SDRAM added table with trace lengths for AMB Clock Output to SDRAM net structure

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	40	added R/C D trace lengths for DQ, CB, DQS, DQS# net structure and changed note 4
	41	updated R/C B DQS/DQS# trace lengths and changed note 4
	42	changed note 4
	46	added diagram that describes R/C D net structure routing for Address/Command to SDRAM added table with R/C D trace lengths for Address/Command net structure
	47	added diagram that describes R/C D net structure routing for ODT to SDRAM added table with R/C D trace lengths for ODT net structure
	50	added diagram that describes R/C D net structure routing for Control to SDRAM added table with R/C D trace lengths for Control net structure
	51-54	added chapter DDR2 Fully Buffered DIMM Biasing Details with diagrams/tables
	55	clarified cross-section recommendation
	57	added example 10 layer stackup
	59, 60, 61	multiple changes in paragraphs/tables: clarified that timing numbers used in the timing tables are for example only; multiple changes in description column and in timing values; added note 1
	63	added chapter “Design collateral for specific Raw Cards” including table with ODT values
	65	added “Test Mode collateral” chapter with table that describes transparent mode pinout
	69-70	label format updated
1.0	65	added trace KO page
	44,45,48	modified R/C B net lengths/Rterm as per review in TG
	23,58,59, 60	updated example timing values for amb and dram contributions
	37,40,45, 48	modified R/C A net lengths as per review in TG
	9,10,11,12	added SA0 resistors
	25	strike out TBD Note for additional ctritical AMB params; clarified table footnote to reference AMB spec
	74	Lifted Mechanical wording from RDIMM Spec.
	67..70	added SPD table
	75	added Supporting Hardware information
	25,26,27	on R/C A device placement drawing adjusted position of SPD device to match gerber; removed thickness dimensions, added reference to MO-256
	17,18	replaced “footprint” with “landing pattern”
1.0 BoD	8	PBAR param consistent with RDIMM Spec.
	16,18,19, 20	corrected reference to DRAM MO-XXX for ballouts with support balls
	15-20	made terminology consistent to “landing pattern” (table titles and notes)

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	17,18	corrected actual ball counts
	21	added Dram max outline by raw card
	79	revised HW List
2.0	Global	Introduced R/C E, H and J to spec. Multiple addition in different sections, mostly focusing on topologies
3.0	7	Product Faminly Attributes table was updated (MO256 variations; AMB Vcc voltage)
	15~25	SDRAM Component details and Dram Size Table updated
	97~98	Vcc power delivery section added
	65~68	R/C E and H CA termination value change.
	91	ODT Table corrected typographiocal error by numbering rank 0,1 (was numbered rank1,2)
	99~104	Vtt delivery
	47	dual stripline rule
	53~55,69, 70,73	R/C J adjustments
	80	VCC PLL Filter figure updated