ARM® CoreLink™ DMC-520 Dynamic Memory Controller

Revision: r0p0

Technical Reference Manual

ARM 100000_0000_00_en

ARM® CoreLink™ DMC-520 Dynamic Memory Controller

Technical Reference Manual

Release information

Document History

Issue	Date	Confidentiality	Change
00	07 March 2014	Non-Confidential	First release for r0p0.

Proprietary notice

Confidentiality status

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Product status

The information in this document is Final, that is for a developed product.

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Contents
ARM® CoreLink™ DMC-520 Dynamic Memory Controller Technical Reference Manual

Preface

This preface introduces the *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Technical Reference Manual*.

It contains the following:

About this book

This book is for the ARM CoreLink DMC-520 Dynamic Memory Controller.

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n*
: Identifies the major revision of the product.

p*n*
: Identifies the minor revision or modification status of the product.

Intended audience

This book is written for experienced engineers who want to integrate the delivered ARM DMC-520 product in a *System on Chip* (SoC) design.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter describes the DMC-520.

Chapter 2 Functional Description

This chapter describes how the DMC-520 operates.

Chapter 3 Programmers Model

This chapter describes the programmers model of the DMC-520.

Appendix A Signal Descriptions

This appendix describes the DMC-520 signals.

Appendix B Revisions

This appendix describes the technical changes between released issues of this book.

Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM Glossary* for more information.

Typographic conventions

italic
: Introduces special terminology, denotes cross-references, and citations.

bold
: Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
: Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space
: Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

monospace italic
: Denotes arguments to monospace text where the argument is to be replaced by a specific value.

monospace bold
: Denotes language keywords when used outside example code.

<and>
: Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

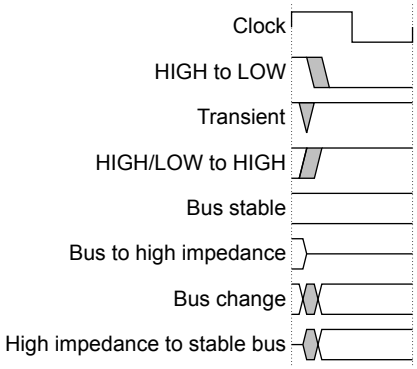

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
: The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n
: At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

ARM publications

The following confidential books are only available to licensees:

- *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Design Manual* (ARM 100001).
- *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Integration Manual* (ARM 100003).
- *ARM® CoreLink™ DMC-520 Dynamic Memory Controller Implementation Guide* (ARM 100002).
- *ARM® AMBA® 5 CHI Protocol Specification* (ARM IHI 0050).
- *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* (ARM IHI 0068).
- *ARM® AMBA® APB Protocol Specification* (ARM IHI 0024).

Other publications

- *JEDEC STANDARD DDR3 SDRAM Specification*, JESD79-3D, *http://www.jedec.org*.
- *JEDEC STANDARD DDR3L SDRAM Specification*, JESD79-3-1A, *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 SDRAM Specification*, JESD79-4, *http://www.jedec.org*.
- *JEDEC STANDARD DDR3 RDIMM Specification*, JESD82-29, *http://www.jedec.org*.
- *JEDEC STANDARD DDR3 LRDIMM Specification*, (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR3 3DS Addendum Specification*, JESD79-3 Addendum (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 RDIMM Common Design Specification*, (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 LRDIMM Common Design Specification*, (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 RCD Specification*, (pre-release), *http://www.jedec.org*.
- *JEDEC STANDARD DDR4 DB Specification*, (pre-release), *http://www.jedec.org*.
- *DDR PHY Interface DFI 3.0 Specification*, *http://ddr-phy.org/*.

——— **Note** ———

See the *ARM®CoreLink™ DMC-520 Dynamic Memory Controller Release Note* for the actual versions of the specifications that ARM used when designing the device.

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Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title.
- The number ARM 100000_0000_00_en.
- The page number(s) to which your comments refer.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

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Chapter 1
Introduction

This chapter describes the DMC-520.
It contains the following sections:

1.1 About the product

This is a high-level overview of the DMC-520.

The DMC-520 is an ARM AMBA 5 CHI SoC peripheral developed, tested, and licensed by ARM. It is a high-performance, area-optimized memory controller that is compatible with the AMBA 5 CHI protocol. It supports the following memory devices:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

The following figure shows an example system.

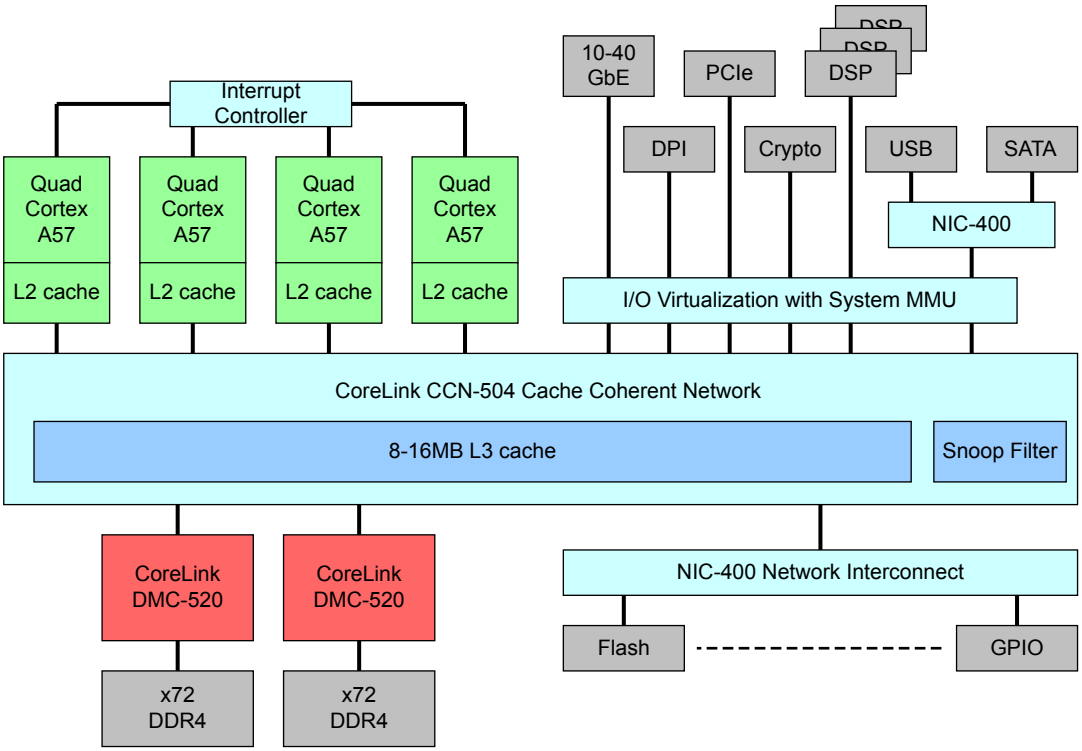

Figure 1-1 Example system

The DMC-520 enables data transfer between the SoC and the SDRAM devices external to the chip. It connects to the on-chip system through a single CHI interface and to a processor through the programmers APB3™ interface to program the DMC-520. It connects to the SDRAM devices through its memory interface block and the *DDR PHY Interface* (DFI).

1.2 DMC-520 compliance

The DMC-520 is compatible with the following protocol specifications and standards:

- AMBA 5 CHI protocol.
- AMBA 3 APB protocol.
- JEDEC DDR4 JESD79-4 standard.
- JEDEC DDR3 JESD79-3 standard.
- JEDEC DDR3L JESD79-3-1 standard.
- JEDEC JESD82-29 standard.
- JEDEC LRDIMM DDR3 Memory Buffer Spec Proposal.
- DDR4 SDRAM Registered DIMM Design Specification.
- DDR4 SDRAM Load Reduced DIMM Design Specification.
- DFI 3.0.

1.3 Features

The DMC-520 supports DDR3 and DDR4 SDRAMs. It also supports error checking, reliability, availability, and serviceability features. In addition, *Quality of Service* (QoS) features and ARM TrustZone® architecture security extensions are built in throughout the controller.

The system interface provides a CHI interface for connection to a CoreLink *Cache Coherent Network* (CCN), an APB3 interface for configuration and initialization purposes, and an external performance event interface for connecting to CoreSight™ on-chip debug and trace technology.

The DMC-520 has the following features:

- Profiling signals that enable performance profiling to be performed in the system.
- TrustZone architecture security extensions.
- Buffering to optimize read and write turnaround and to maximize bandwidth.
- A system interface that provides:
  - A CHI interface to connect to a CCN.
  - An APB3 interface for configuration and initialization purposes.
- A *Memory Interface* (MI) that provides:
  - A DFI 3.0 interface to a PHY that supports DDR3, DDR3L, and DDR4.
- Low power operation through programmable SDRAM power modes.
- *Reliability, Availability, Serviceability* (RAS):
  - *Single Error Correcting, Double Error Detecting* (SEC-DED) ECC for off-chip DRAM.
  - Symbol-based ECC, to correct memory chip and data-lane failures.
  - SEC-DED ECC for on-chip RAM protection.
  - Hardware *Read-Modify-Write* (RMW) for systems supporting sparse writes.
  - Link protection for DDR4 link errors.
  - CRC write-data protection for DDR4 devices.
- A programmable mechanism for automated SDRAM scrubbing.
- Error handling.
- Refresh Control Logic for memory banks.
- Power Control Logic. This generates power down requests to the SDRAM, and manages power enables for the PHY logic.

1.4 Interfaces

This section lists the interfaces in the DMC-520.

The DMC-520 has the following external interfaces:

- A system interface to provide read and write access to or from a master. It uses the CHI protocol.
- An APB3 programmers interface to program and control the DMC-520.
- A DFI3.0 compatible PHY interface to transfer data to and from the external memory.
- A profile and debug interface.
- A low-power clock control interface that uses the Q-channel protocol. See *Q-channel interface* on page 2-26.
- An abort interface that is a 4-phase request and acknowledge handshake that you can use to recover from a livelock caused by DRAM or PHY failure.
- User I/O ports.
- A set of interrupts used to detect some operational events or handle errors for example.

1.5 Configurable options

There are no configurable options in the DMC-520.

1.6 Test features

The DMC-520 provides the following test features:

- Integration test logic for integration testing.
- A debug and profile interface to enable you to monitor transaction events.

1.7 Product documentation and design flow

This section describes the DMC books and how they relate to the design flow.

Documentation

The DMC documentation is as follows:

Technical Reference Manual
The *Technical Reference Manual* (TRM) summarizes the functionality of the DMC, and describes its pins.

Design Manual
The *Design Manual* (DM) describes the functionality and the effects of functional options on the behavior of the DMC. It is required at all stages of the design flow. The choices made in the design flow can mean that some behavior described in the DM is not relevant. If you are programming the DMC then contact:

- The implementer to determine what integration, if any, was performed before implementing the DMC.
- The integrator to determine the pin configuration of the device that you are using.

The DM is a confidential book that is only available to licensees.

Implementation Guide
The *Implementation Guide* (IG) describes:

- How to synthesize the *Register Transfer Level* (RTL).
- How to integrate RAM arrays.
- How to run test patterns.
- The processes to sign off the configured design.

The ARM product deliverables include reference scripts and information about using them to implement your design. Reference methodology flows supplied by ARM are example reference implementations. Contact your EDA vendor for EDA tool support.

The IG is a confidential book that is only available to licensees.

Integration Manual
The *Integration Manual* (IM) describes how to integrate the DMC into a SoC. It includes a description of the pins that the integrator must tie off to connect the DMC into an SoC design or to other IP..

The IM is a confidential book that is only available to licensees.

Design flow

The DMC is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation
The implementer synthesizes the RTL to produce a hard macrocell. This includes integrating RAMs into the design.

Integration
The integrator connects the implemented design into a SoC. This includes connecting it to a memory system.

Programming
This is the last process. The system programmer develops the software required to initialize the DMC, and tests the required application software.

Each process:

- Can be performed by a different party.

- Can include implementation and integration choices that affect the behavior and features of the DMC.

The operation of the final device depends on:

Configuration inputs
: The integrator configures some features of the DMC by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software programming
: The programmer configures the DMC by programming particular values into registers. This affects the behavior of the DMC.

——— **Note** ———

This manual refers to implementation-defined features. Reference to a feature that is included means that the appropriate pin configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

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1.8 Product revisions

This section describes the differences in functionality between product revisions of the DMC-520.

r0p0

First release.

Chapter 2
Functional Description

This chapter describes how the DMC-520 operates.
It contains the following sections:

2.1 About the functions

This section gives a brief description of all of the functions of the device.

The following figure shows a block diagram of the functions of the DMC-520. The colors show the different categories of functions:

- Blue indicates the blocks that are associated with data flow. The System interface is an example.
- Green indicates the blocks that are associated with programming. The Programming interface is an example.
- Orange indicates the blocks that are associated with the quality and efficiency of the communication to its external memory. The QoS engine is an example.

The arrows indicate the direction from master to slave for the CHI, APB , and DFI interfaces. For the PMU interface the arrow indicates the direction of information flow.

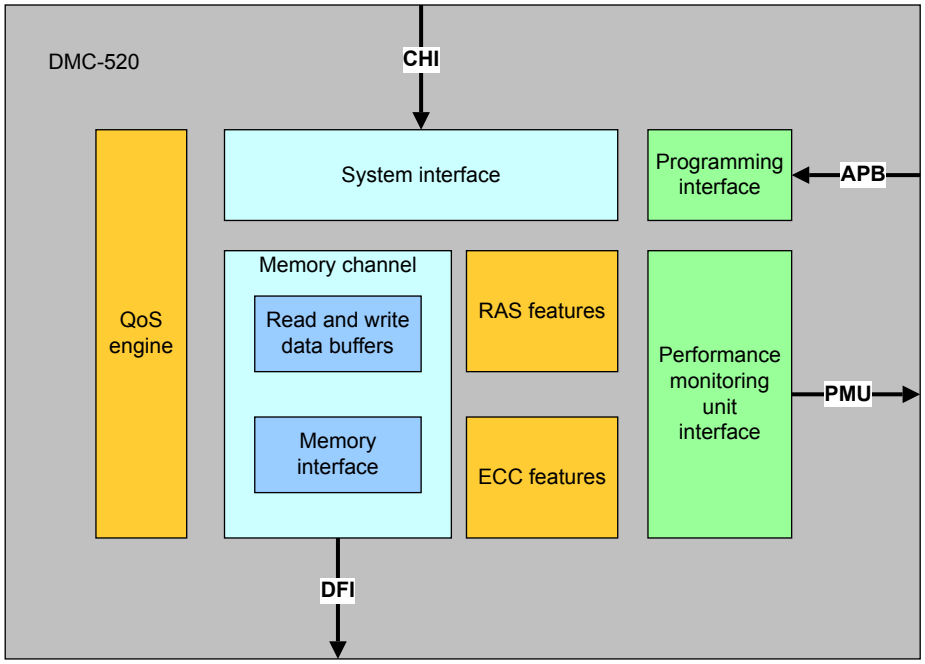

Figure 2-1 Functional block diagram

System interface

The DMC-520 interfaces to the rest of the SoC through this interface. This is a standard CHI interface that connects to a CHI *Slave Node Interface* (SNF). For any attempted accesses that the system makes outside of the programmed address range of the DMC-520, the system interface responds with a non-data error response. According to how you program the DMC-520, it converts the system access information to the correct rank, bank, column, and row access of the external SDRAM that connects to it. The system interface supports TrustZone features to regulate Secure and Non-secure accesses to both Secure and Non-secure regions of memory

The DMC monitors queue occupancies and dictates whether system requests of any given QoS is to be accepted. Prefetched and Dynamic P-Credit requests are allocated based on a threshold setting, derived from register settings.

Memory channel

Through this interface the DMC-520 conducts its data transactions with the SDRAM and regulates the power consumption of the SDRAM. The DMC-520 uses the ECC information that it receives from the SDRAM to maximize the quality of information that it receives from these devices.

Programming interface

Through this interface a master in the system programs the DMC-520. You can define the Secure and Non-secure regions of external memory and also define how the DMC-520 addresses the external memory from the address that the system provides on its system interface. You can also make direct accesses to the SDRAM, for example to initialize it.

Performance monitoring unit interface

You can use the *Performance Monitoring Unit* (PMU) interface to monitor the performance and power settings for your specific application. This interface allows you to monitor the inner workings of the device and so enables additional information to be viewed.

QoS engine

The DMC-520 provides controls to enable you to adjust its arbitration scheme for your system to maximize the availability of your external memory devices. It provides buffers to re-order system transaction requests. It uses an advanced scheduling algorithm to ensure that traffic going to one memory bank causes minimal disruption to traffic going to a different memory bank. It also schedules transaction requests according to the availability of the destination memory bank. For system access requests to different available memory banks the DMC-520 arbitrates these requests based on the QoS priority initially then on the temporal priority. These memory access requests all compete for control of the external SDRAM bus and SDRAM bank availability.

RAS

RAS features include support for the following:

- SECDED ECC and symbol-based ECC for external DRAM. The symbol-based ECC performs quad symbol correct and multi-symbol detect.
- SECDED ECC of on-chip SRAM buffers within the DMC-520.
- An automated retry of failed read transactions.
- Write-back of corrected errors.
- To reduce memory errors, the DMC-520 supports:
  - Link error protection for the memory interface.
  - Programmable data scrubbing where the DMC-520 periodically detects and corrects data errors in the memory itself.

2.2 Clocking and resets

The DMC-520 normally operates as one synchronous clock domain between the interconnect and the external DDR interface. However, the programming interface can operate asynchronously to this.

This section shows the clock and reset signals that the DMC-520 requires.

Clocks

The following requirements, with respect to the APB and refresh controller clocks, apply:

- **clk** must run synchronously with, and at the same speed as, the PHY and SDRAM and with the interfacing system interconnect.
- **pclk** and **clk** can run asynchronously to each other.

Reset

Resets must be applied for a minimum duration of two clock cycles for each clock domain.

There is one reset per clock domain. The **pclk** domain must be brought out of reset prior to the **clk** domain.

——— **Note** ———

- To assert any DMC-520 reset signal, you must set it LOW.
- To perform a DMC-520 reset, you must assert both reset signals.

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Related references

Signals list.

2.3 Interfaces

This section describes the interfaces of the DMC-520, as the following figure shows.

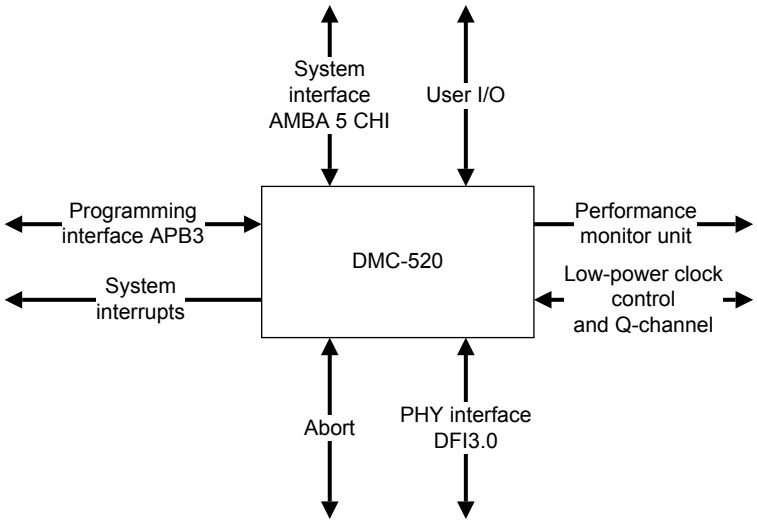

Figure 2-2 Interfaces of the DMC-520

This section contains the following subsections:

- *2.3.1 System Interface* on page 2-24.
- *2.3.2 Programming Interface* on page 2-24.
- *2.3.3 PHY interface* on page 2-24.
- *2.3.4 Profile and Debug interface* on page 2-25.
- *2.3.5 Low-power Clock Control interface* on page 2-25.
- *2.3.6 Abort interface* on page 2-27.

2.3.1 System Interface

This section describes the function of the System interface.

The System Interface provides protocol conversion between CHI and internal read/write requests. Because CHI is packet-based and a slave node only supports read and write semantics, this translation is straightforward at a transaction level because no transformation function is performed.

2.3.2 Programming Interface

This section describes the APB3 interface, used for programming the DMC-520.

The AMBA APB3 slave interface allows software to configure the controller and to initialize the memory devices. The APB3 programming interface also provides a means of performing architectural state transitions in addition to querying certain debug and profile information. The interface is a memory-mapped register interface.

2.3.3 PHY interface

The PHY interface provides command scheduling and arbitration, including the generation of any required SDRAM prepare commands, for example, ACTIVATE and PRECHARGE. This section describes the PHY interface in the DMC-520.

The PHY interface is a DFI3.0 interface compatible with the DDR standards for DDR4 and DDR3 (including DDR3L). It provides:

- Command scheduling and arbitration, including generation of any required SDRAM prepare commands, for example, ACTIVATE, or PRECHARGE.
- Automated AUTOREFRESH command generation.
- SDRAM interface link protection including automated retries for failed commands to ensure the correct ordering of those retried commands to SDRAM.
- Automated SDRAM and PHY logic power control.
- Profile and debug information.

2.3.4 Profile and Debug interface

This section describes the profile and debug interface in the DMC-520.

The DMC-520 provides programmable features that allow system designers and software developers to fine-tune performance and power settings for their applications. A number of events can be monitored and the statistics used to fine-tune the performance of the controller by statically, or dynamically, altering the programmed state.

The information is made available through output pins that the system integrator must connect to an external monitoring unit.

The following events are monitored:

- Channel utilization.
- Channel and chip power state information.
- Bank utilization.
- Bank distribution.
- Activation rate.
- Read and write turnaround frequency.
- Read and write buffer fill status and the frequency of full events.
- Thresholding asserting back pressure.
- Arbitration decisions made where QoS is prioritized over efficiency.
- *Read-Modify-Write* (RMW) frequency.
- Timeouts and deadline events.

Each event is implemented as a pair of signals, VALID, and either PAYLOAD or a permanently valid PAYLOAD signal.

The Profile and Debug event interface can be connected to a generic event counter block, where any combination of the signals can be logged and tracked, depending on your system requirements.

2.3.5 Low-power Clock Control interface

This section describes the clock requirements for the DMC-520.

The DMC-520 provides a low-power control interface using the Q-channel protocol. This is used to place the DMC into its low-power state, in which state the clock can be removed. The system can use the APB interface to put the DMC into its low-power state, and take it out of its low-power state.

SDRAM provides a number of power-saving states, as distinct from those of the DMC-520:

1. Idle-ready.
2. Clock stop.
3. Active power down.
4. Precharge power down.
5. *Self-Refresh* (SR).
6. *Maximum Power Down* (MPD) for DDR4.

All states prohibit commands apart from Idle-ready. From states 2-6, the energy saving increases, but so does the exit latency from that state. Some SDRAMs do not support dynamic clock stopping or MPD. Specific commands, together with the clock-enable **CKE** signal, are used to control states 2-5. Individual **CKE** pins are required for each chip that requires separate power control.

The features of the DMC-520 include:

- Separate clock and **CKE** controls for each chip select, with a set of multiplexer options to support standard DIMM configurations.
- Automated power control of SDRAM power modes based on an enable and timer. See *3.3.7 low_power_control_next* on page 3-51.
- Clock stop functionality that differs between memory devices. A programmable register controls this behavior. See *3.3.7 low_power_control_next* on page 3-51.
- Auto powerdown with minimal or no latency penalty on wake up.
- Auto self-refresh functionality. The time delay before entry to self-refresh can be timed in refresh periods. When in self-refresh, a chip only comes out of self-refresh in response to system commands.
- Software-controlled low-power entry through the APB programming interface.
- A Q-channel interface for hardware to control entry into the SR states. See *Q-channel interface* on page 2-26.
- A separate low-power interface to allow clock stopping of the programming interface.

——— **Note** ———

The DMC-520 does not allow multiple methods of low power entry, either software or hardware, that is used at the same time. This is a restriction imposed on the system design.

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The PHY logic consumes power in standby mode. If the controller is using SDRAM low-power modes, then it indicates to the PHY that it can power down. The wake-up value that the DMC signals to the PHY with the powerdown request determines the level of power state that the PHY enters. The wake-up value is determined from a programmed value that is associated with each SDRAM power-saving state. These states are:

- Idle.
- Power-down.
- Configuration.
- Self-refresh.
- MPD.

——— **Note** ———

The DMC can also indicate that the PHY must power down in the following ways:

- As a direct command from software, with a software-defined wake-up value.
- As part of a Q-channel sequence, with a tie-off defined wake-up value.

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Q-channel interface

The DMC has a Q-channel interface that allows an external power controller to place the DMC into a low-power state.

It is a standard Q-channel interface as defined in the *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces* using the following 4 signals.

- **qactive**.
- **qreqn**.
- **qacceptn**.
- **qdeny**.

When the DMC receives a request itl puts the DRAM into self_refresh before asserting **qacceptn** to accept the request that indicates the clk can be stopped.

DMC denies requests to power down using the Q-Channel when geardown_mode is enabled. In this case low-power mode can still be entered using the APB interface.

There is a separate Q-channel interface for the **pclk** using the following signals:

- **qactive_apb**.
- **qreqn_apb**.
- **qacceptn_apb**.
- **qdeny_apb**.

The DMC never denies a request to power down the APB clock although it might be delayed based on APB activity.

——— **Note** ———

These two interfaces are interrelated and a change on one can cause **qactive** on the other to be asserted. If this occurs then the power up request must be responded to straight away to allow the request to be serviced.

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See *ARM® Low Power Interface Specification, Q-Channel and P-Channel Interfaces*.

2.3.6 Abort interface

The abort interface is a 4-phase request and acknowledge handshake that the DMC can use to recover from a livelock caused by a DRAM failure or a PHY failure. When a failure happens, it causes repeated retries of commands on the memory interface.

The following diagram shows the request, acknowledge handshake.

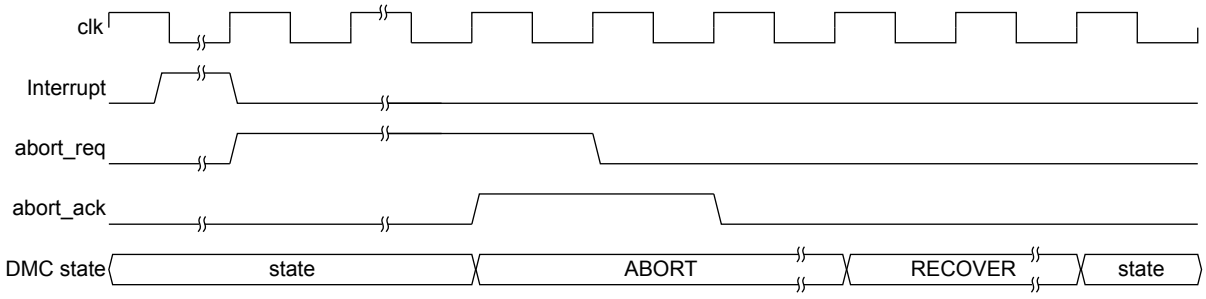

Figure 2-3 Abort interface timing diagram

The system can issue an abort at any time that puts the DMC into the ABORT architectural state. Software must then restore the memory state. All current system transactions are retried when instructed by software.

2.4 Constraints and limitations of use

The constraints and limitations of the DMC-520 depend on the SDRAMS used, and the interoperability within the PHYs. This, in turn, depends on the *DDR Physical Interface* (DFI) parameters.

The SDRAMs supported by the DMC-520 are:

- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

——— **Note** ———

These devices are described in the JEDEC specifications that are global standards for the microelectronics industry.

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The DIMMs supported by the DMC-520 are:

- DDR3 UDIMM.
- DDR3 RDIMM.
- DDR3 LRDIMM.
- DDR3 3DS.
- DDR4 UDIMM.
- DDR4 RDIMM.
- DDR4 LRDIMM.

2.5 System address conversion

This section describes how the DMC-520 transforms the system address to the SDRAM address.

The following figure shows the functions that the DMC-520 uses to transform the address that it receives from the system to the address it presents to the SDRAM.

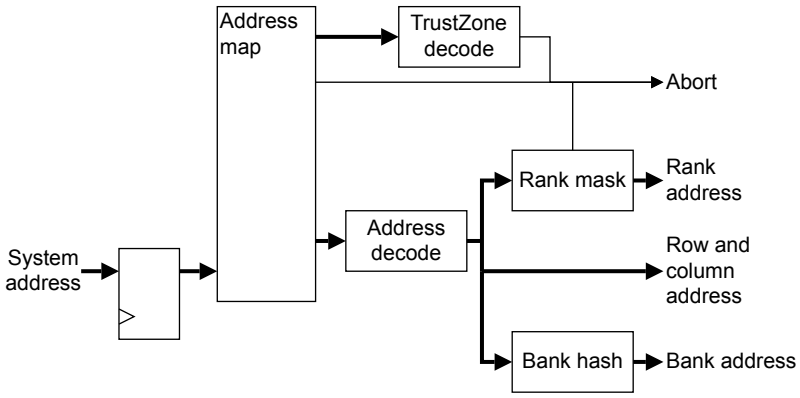

Figure 2-4 System address conversion

The following describes the function of the boxes:

Address map
Receives the system address and converts it to a suitable form for the Address decode function.

TrustZone decode
Decodes invalid address regions.

Address decode
Translates its input address to row, rank, bank, and column addresses.

Chapter 3
Programmers Model

This chapter describes the programmers model of the DMC-520.
It contains the following sections:

3.1 About this programmers model

The following information applies to the DMC-520 registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to the reset value specified in the *3.2 Register summary* on page 3-32.
- Access type is described as follows:

  RW Read and write.

  RO Read only.

  WO Write only.

3.2 Register summary

The following table shows the registers in offset order from the base memory address.

Table 3-1 Register summary

Offset	Name	Type	Reset	Width	Description
0x000	memc_status	RO	0x00000000	32	*3.3.1 memc_status* on page 3-46
0x004	memc_config	RO	0x00000000	32	*3.3.2 memc_config* on page 3-47
0x008	memc_cmd	WO	0x00000000	32	*3.3.3 memc_cmd* on page 3-48
0x010	address_control_next	RW	0x00030202	32	*3.3.4 address_control_next* on page 3-49
0x014	decode_control_next	RW	0x00000000	32	*3.3.5 decode_control_next* on page 3-50
0x01C	address_map_next	RW	0x00000000	32	*3.3.6 address_map_next* on page 3-51
0x020	low_power_control_next	RW	0x00000020	32	*3.3.7 low_power_control_next* on page 3-51
0x028	turnaround_control_next	RW	0x0F0F0F0F	32	*3.3.8 turnaround_control_next* on page 3-52
0x02C	hit_turnaround_control_next	RW	0x08101F1F	32	*3.3.9 hit_turnaround_control_next* on page 3-53
0x030	qos_class_control_next	RW	0x00000FC8	32	*3.3.10 qos_class_control_next* on page 3-54
0x034	escalation_control_next	RW	0x00080000	32	*3.3.11 escalation_control_next* on page 3-55
0x038	qv_control_31_00_next	RW	0x76543210	32	*3.3.12 qv_control_31_00_next* on page 3-56
0x03C	qv_control_63_32_next	RW	0xFEDCBA98	32	*3.3.13 qv_control_63_32_next* on page 3-57
0x040	rt_control_31_00_next	RW	0x00000000	32	*3.3.14 rt_control_31_00_next* on page 3-58
0x044	rt_control_63_32_next	RW	0x00000000	32	*3.3.15 rt_control_63_32_next* on page 3-59
0x048	timeout_control_next	RW	0x00000001	32	*3.3.16 timeout_control_next* on page 3-60
0x04C	credit_control_next	RW	0x00000000	32	*3.3.17 credit_control_next* on page 3-61
0x050	write_priority_control_31_00_next	RW	0x00000000	32	*3.3.18 write_priority_control_31_00_next* on page 3-62
0x054	write_priority_control_63_32_next	RW	0x00000000	32	*3.3.19 write_priority_control_63_32_next* on page 3-63
0x060	queue_threshold_control_31_00_next	RW	0x00000000	32	*3.3.20 queue_threshold_control_31_00_next* on page 3-64
0x064	queue_threshold_control_63_32_next	RW	0x00000000	32	*3.3.21 queue_threshold_control_63_32_next* on page 3-65
0x078	memory_address_max_31_00_next	RW	0x00000010	32	*3.3.22 memory_address_max_31_00_next* on page 3-66

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x07C	memory_address_max_43_32_next	RW	0x00000000	32	*3.3.23 memory_address_max_43_32_next* on page 3-66
0x080	access_address_min0_31_00_next	RW	0x00000000	32	*3.3.24 access_address_min0_31_00_next* on page 3-67
0x084	access_address_min0_43_32_next	RW	0x00000000	32	*3.3.25 access_address_min0_43_32_next* on page 3-68
0x088	access_address_max0_31_00_next	RW	0x00000000	32	*3.3.26 access_address_max0_31_00_next* on page 3-68
0x08C	access_address_max0_43_32_next	RW	0x00000000	32	*3.3.27 access_address_max0_43_32_next* on page 3-69
0x090	access_address_min1_31_00_next	RW	0x00000000	32	*3.3.28 access_address_min1_31_00_next* on page 3-69
0x094	access_address_min1_43_32_next	RW	0x00000000	32	*3.3.29 access_address_min1_43_32_next* on page 3-70
0x098	access_address_max1_31_00_next	RW	0x00000000	32	*3.3.30 access_address_max1_31_00_next* on page 3-71
0x09C	access_address_max1_43_32_next	RW	0x00000000	32	*3.3.31 access_address_max1_43_32_next* on page 3-71
0x0A0	access_address_min2_31_00_next	RW	0x00000000	32	*3.3.32 access_address_min2_31_00_next* on page 3-72
0x0A4	access_address_min2_43_32_next	RW	0x00000000	32	*3.3.33 access_address_min2_43_32_next* on page 3-73
0x0A8	access_address_max2_31_00_next	RW	0x00000000	32	*3.3.34 access_address_max2_31_00_next* on page 3-73
0x0AC	access_address_max2_43_32_next	RW	0x00000000	32	*3.3.35 access_address_max2_43_32_next* on page 3-74
0x0B0	access_address_min3_31_00_next	RW	0x00000000	32	*3.3.36 access_address_min3_31_00_next* on page 3-74
0x0B4	access_address_min3_43_32_next	RW	0x00000000	32	*3.3.37 access_address_min3_43_32_next* on page 3-75
0x0B8	access_address_max3_31_00_next	RW	0x00000000	32	*3.3.38 access_address_max3_31_00_next* on page 3-76
0x0BC	access_address_max3_43_32_next	RW	0x00000000	32	*3.3.39 access_address_max3_43_32_next* on page 3-76
0x0C0	access_address_min4_31_00_next	RW	0x00000000	32	*3.3.40 access_address_min4_31_00_next* on page 3-77
0x0C4	access_address_min4_43_32_next	RW	0x00000000	32	*3.3.41 access_address_min4_43_32_next* on page 3-78
0x0C8	access_address_max4_31_00_next	RW	0x00000000	32	*3.3.42 access_address_max4_31_00_next* on page 3-78
0x0CC	access_address_max4_43_32_next	RW	0x00000000	32	*3.3.43 access_address_max4_43_32_next* on page 3-79

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0D0	access_address_min5_31_00_next	RW	0x00000000	32	*3.3.44 access_address_min5_31_00_next* on page 3-79
0x0D4	access_address_min5_43_32_next	RW	0x00000000	32	*3.3.45 access_address_min5_43_32_next* on page 3-80
0x0D8	access_address_max5_31_00_next	RW	0x00000000	32	*3.3.46 access_address_max5_31_00_next* on page 3-81
0x0DC	access_address_max5_43_32_next	RW	0x00000000	32	*3.3.47 access_address_max5_43_32_next* on page 3-81
0x0E0	access_address_min6_31_00_next	RW	0x00000000	32	*3.3.48 access_address_min6_31_00_next* on page 3-82
0x0E4	access_address_min6_43_32_next	RW	0x00000000	32	*3.3.49 access_address_min6_43_32_next* on page 3-82
0x0E8	access_address_max6_31_00_next	RW	0x00000000	32	*3.3.50 access_address_max6_31_00_next* on page 3-83
0x0EC	access_address_max6_43_32_next	RW	0x00000000	32	*3.3.51 access_address_max6_43_32_next* on page 3-83
0x0F0	access_address_min7_31_00_next	RW	0x00000000	32	*3.3.52 access_address_min7_31_00_next* on page 3-84
0x0F4	access_address_min7_43_32_next	RW	0x00000000	32	*3.3.53 access_address_min7_43_32_next* on page 3-85
0x0F8	access_address_max7_31_00_next	RW	0x00000000	32	*3.3.54 access_address_max7_31_00_next* on page 3-85
0x0FC	access_address_max7_43_32_next	RW	0x00000000	32	*3.3.55 access_address_max7_43_32_next* on page 3-86
0x100	channel_status	RO	0x00000003	32	*3.3.56 channel_status* on page 3-86
0x108	direct_addr	RW	0x00000000	32	*3.3.57 direct_addr* on page 3-88
0x10C	direct_cmd	WO	0x00000000	32	*3.3.58 direct_cmd* on page 3-88
0x110	dci_replay_type_next	RW	0x00000002	32	*3.3.59 dci_replay_type_next* on page 3-89
0x118	dci_strb	RW	0x0000000F	32	*3.3.60 dci_strb* on page 3-90
0x11C	dci_data	RW	0x00000000	32	*3.3.61 dci_data* on page 3-90
0x120	refresh_control_next	RW	0x00000000	32	*3.3.62 refresh_control_next* on page 3-91
0x128	memory_type_next	RW	0x00000101	32	*3.3.63 memory_type_next* on page 3-92
0x130	feature_config	RW	0x000000F0	32	*3.3.64 feature_config* on page 3-92
0x138	nibble_failed_031_000	RW	0x00000000	32	*3.3.65 nibble_failed_031_000* on page 3-93
0x13C	nibble_failed_063_032	RW	0x00000000	32	*3.3.66 nibble_failed_063_032* on page 3-94
0x140	nibble_failed_095_064	RW	0x00000000	32	*3.3.67 nibble_failed_095_064* on page 3-95

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x144	nibble_failed_127_096	RW	0x00000000	32	*3.3.68 nibble_failed_127_096* on page 3-96
0x148	queue_allocate_control_031_000	RW	0xFFFFFFFF	32	*3.3.69 queue_allocate_control_031_000* on page 3-97
0x14C	queue_allocate_control_063_032	RW	0xFFFFFFFF	32	*3.3.70 queue_allocate_control_063_032* on page 3-98
0x150	queue_allocate_control_095_064	RW	0xFFFFFFFF	32	*3.3.71 queue_allocate_control_095_064* on page 3-98
0x154	queue_allocate_control_127_096	RW	0xFFFFFFFF	32	*3.3.72 queue_allocate_control_127_096* on page 3-99
0x158	ecc_errc_count_31_00	RW	0x00000000	32	*3.3.73 ecc_errc_count_31_00* on page 3-99
0x15C	ecc_errc_count_63_32	RW	0x00000000	32	*3.3.74 ecc_errc_count_63_32* on page 3-100
0x160	ecc_errd_count_31_00	RW	0x00000000	32	*3.3.75 ecc_errd_count_31_00* on page 3-100
0x164	ecc_errd_count_63_32	RW	0x00000000	32	*3.3.76 ecc_errd_count_63_32* on page 3-101
0x168	ram_err_count	RW	0x00000000	32	*3.3.77 ram_err_count* on page 3-102
0x16C	link_err_count	RW	0x00000000	32	*3.3.78 link_err_count* on page 3-102
0x170	scrub_control0_next	RW	0x00000000	32	*3.3.79 scrub_control0_next* on page 3-103
0x174	scrub_address_min0_next	RW	0x00000000	32	*3.3.80 scrub_address_min0_next* on page 3-104
0x178	scrub_address_max0_next	RW	0x00000000	32	*3.3.81 scrub_address_max0_next* on page 3-104
0x180	scrub_control1_next	RW	0x00000000	32	*3.3.82 scrub_control1_next* on page 3-105
0x184	scrub_address_min1_next	RW	0x00000000	32	*3.3.83 scrub_address_min1_next* on page 3-106
0x188	scrub_address_max1_next	RW	0x00000000	32	*3.3.84 scrub_address_max1_next* on page 3-106
0x190	scrub_control2_next	RW	0x00000000	32	*3.3.85 scrub_control2_next* on page 3-107
0x194	scrub_address_min2_next	RW	0x00000000	32	*3.3.86 scrub_address_min2_next* on page 3-108
0x198	scrub_address_max2_next	RW	0x00000000	32	*3.3.87 scrub_address_max2_next* on page 3-108
0x1A0	scrub_control3_next	RW	0x00000000	32	*3.3.88 scrub_control3_next* on page 3-109
0x1A4	scrub_address_min3_next	RW	0x00000000	32	*3.3.89 scrub_address_min3_next* on page 3-110
0x1A8	scrub_address_max3_next	RW	0x00000000	32	*3.3.90 scrub_address_max3_next* on page 3-110

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1B0	scrub_control4_next	RW	0x00000000	32	*3.3.91 scrub_control4_next* on page 3-111
0x1B4	scrub_address_min4_next	RW	0x00000000	32	*3.3.92 scrub_address_min4_next* on page 3-112
0x1B8	scrub_address_max4_next	RW	0x00000000	32	*3.3.93 scrub_address_max4_next* on page 3-112
0x1C0	scrub_control5_next	RW	0x00000000	32	*3.3.94 scrub_control5_next* on page 3-113
0x1C4	scrub_address_min5_next	RW	0x00000000	32	*3.3.95 scrub_address_min5_next* on page 3-114
0x1C8	scrub_address_max5_next	RW	0x00000000	32	*3.3.96 scrub_address_max5_next* on page 3-114
0x1D0	scrub_control6_next	RW	0x00000000	32	*3.3.97 scrub_control6_next* on page 3-115
0x1D4	scrub_address_min6_next	RW	0x00000000	32	*3.3.98 scrub_address_min6_next* on page 3-116
0x1D8	scrub_address_max6_next	RW	0x00000000	32	*3.3.99 scrub_address_max6_next* on page 3-116
0x1E0	scrub_control7_next	RW	0x00000000	32	*3.3.100 scrub_control7_next* on page 3-117
0x1E4	scrub_address_min7_next	RW	0x00000000	32	*3.3.101 scrub_address_min7_next* on page 3-118
0x1E8	scrub_address_max7_next	RW	0x00000000	32	*3.3.102 scrub_address_max7_next* on page 3-118
0x1F0	feature_control_next	RW	0x0AA00000	32	*3.3.103 feature_control_next* on page 3-119
0x1F4	mux_control_next	RW	0x00000000	32	*3.3.104 mux_control_next* on page 3-120
0x1F8	rank_remap_control_next	RW	0x76543210	32	*3.3.105 rank_remap_control_next* on page 3-121
0x200	t_refi_next	RW	0x00090100	32	*3.3.106 t_refi_next* on page 3-123
0x204	t_rfc_next	RW	0x00008C23	32	*3.3.107 t_rfc_next* on page 3-123
0x208	t_mrr_next	RW	0x00000002	32	*3.3.108 t_mrr_next* on page 3-124
0x20C	t_mrw_next	RW	0x0000000C	32	*3.3.109 t_mrw_next* on page 3-125
0x210	t_rdpden_next	RW	0x00000002	32	*3.3.110 t_rdpden_next* on page 3-125
0x218	t_rcd_next	RW	0x00000005	32	*3.3.111 t_rcd_next* on page 3-126
0x21C	t_ras_next	RW	0x0000000E	32	*3.3.112 t_ras_next* on page 3-127
0x220	t_rp_next	RW	0x00000005	32	*3.3.113 t_rp_next* on page 3-127
0x224	t_rpall_next	RW	0x00000005	32	*3.3.114 t_rpall_next* on page 3-128
0x228	t_rrd_next	RW	0x00000404	32	*3.3.115 t_rrd_next* on page 3-128
0x22C	t_act_window_next	RW	0x03560014	32	*3.3.116 t_act_window_next* on page 3-129
0x234	t_rtr_next	RW	0x00040404	32	*3.3.117 t_rtr_next* on page 3-130
0x238	t_rtw_next	RW	0x00060606	32	*3.3.118 t_rtw_next* on page 3-130
0x23C	t_rtp_next	RW	0x00000004	32	*3.3.119 t_rtp_next* on page 3-131

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x244	t_wr_next	RW	0x00000005	32	*3.3.120 t_wr_next* on page 3-132
0x248	t_wtr_next	RW	0x00040404	32	*3.3.121 t_wtr_next* on page 3-132
0x24C	t_wtw_next	RW	0x00040404	32	*3.3.122 t_wtw_next* on page 3-133
0x254	t_xmpd_next	RW	0x000003FF	32	*3.3.123 t_xmpd_next* on page 3-134
0x258	t_ep_next	RW	0x00000002	32	*3.3.124 t_ep_next* on page 3-135
0x25C	t_xp_next	RW	0x00060002	32	*3.3.125 t_xp_next* on page 3-135
0x260	t_esr_next	RW	0x0000000E	32	*3.3.126 t_esr_next* on page 3-136
0x264	t_xsr_next	RW	0x05120100	32	*3.3.127 t_xsr_next* on page 3-136
0x268	t_esrck_next	RW	0x00000005	32	*3.3.128 t_esrck_next* on page 3-137
0x26C	t_ckxsr_next	RW	0x00000001	32	*3.3.129 t_ckxsr_next* on page 3-138
0x270	t_cmd_next	RW	0x00000000	32	*3.3.130 t_cmd_next* on page 3-138
0x274	t_parity_next	RW	0x00000900	32	*3.3.131 t_parity_next* on page 3-139
0x278	t_zqcs_next	RW	0x00000040	32	*3.3.132 t_zqcs_next* on page 3-140
0x300	t_rddata_en_next	RW	0x00000001	32	*3.3.133 t_rddata_en_next* on page 3-140
0x304	t_phyrdlat_next	RW	0x00000000	32	*3.3.134 t_phyrdlat_next* on page 3-141
0x308	t_phywrlat_next	RW	0x00000001	32	*3.3.135 t_phywrlat_next* on page 3-142
0x310	rdlvl_control_next	RW	0x00001080	32	*3.3.136 rdlvl_control_next* on page 3-143
0x314	rdlvl_mrs_next	RW	0x00000004	32	*3.3.137 rdlvl_mrs_next* on page 3-144
0x318	t_rdlvl_en_next	RW	0x00000000	32	*3.3.138 t_rdlvl_en_next* on page 3-144
0x31C	t_rdlvl_rr_next	RW	0x00000000	32	*3.3.139 t_rdlvl_rr_next* on page 3-145
0x320	wrlvl_control_next	RW	0x00001000	32	*3.3.140 wrlvl_control_next* on page 3-146
0x324	wrlvl_mrs_next	RW	0x00000086	32	*3.3.141 wrlvl_mrs_next* on page 3-147
0x328	t_wrlvl_en_next	RW	0x00000000	32	*3.3.142 t_wrlvl_en_next* on page 3-147
0x32C	t_wrlvl_ww_next	RW	0x00000000	32	*3.3.143 t_wrlvl_ww_next* on page 3-148
0x348	phy_power_control_next	RW	0x00000000	32	*3.3.144 phy_power_control_next* on page 3-149
0x34C	t_lpresp_next	RW	0x00000000	32	*3.3.145 t_lpresp_next* on page 3-150
0x350	phy_update_control_next	RW	0x0FE00000	32	*3.3.146 phy_update_control_next* on page 3-150
0x358	odt_timing_next	RW	0x06000600	32	*3.3.147 odt_timing_next* on page 3-152
0x360	odt_wr_control_31_00_next	RW	0x08040201	32	*3.3.148 odt_wr_control_31_00_next* on page 3-153
0x364	odt_wr_control_63_32_next	RW	0x80402010	32	*3.3.149 odt_wr_control_63_32_next* on page 3-153
0x368	odt_rd_control_31_00_next	RW	0x00000000	32	*3.3.150 odt_rd_control_31_00_next* on page 3-154

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x36C	odt_rd_control_63_32_next	RW	0x00000000	32	*3.3.151 odt_rd_control_63_32_next* on page 3-155
0x370	temperature_readout	RO	0x00000000	32	*3.3.152 temperature_readout* on page 3-156
0x378	training_status	RO	0x00000000	32	*3.3.153 training_status* on page 3-157
0x380	dq_map_control_15_00_next	RW	0x00000000	32	*3.3.154 dq_map_control_15_00_next* on page 3-158
0x384	dq_map_control_31_16_next	RW	0x00000000	32	*3.3.155 dq_map_control_31_16_next* on page 3-159
0x388	dq_map_control_47_32_next	RW	0x00000000	32	*3.3.156 dq_map_control_47_32_next* on page 3-160
0x38C	dq_map_control_63_48_next	RW	0x00000000	32	*3.3.157 dq_map_control_63_48_next* on page 3-161
0x390	dq_map_control_71_64_next	RW	0x00000000	32	*3.3.158 dq_map_control_71_64_next* on page 3-162
0x398	rank_status	RO	0x00000000	32	*3.3.159 rank_status* on page 3-163
0x39C	mode_change_status	RO	0x00000000	32	*3.3.160 mode_change_status* on page 3-164
0x400	user_status	RO	0x00000000	32	*3.3.161 user_status* on page 3-164
0x408	user_config0_next	RW	0x00000000	32	*3.3.162 user_config0_next* on page 3-165
0x40C	user_config1_next	RW	0x00000000	32	*3.3.163 user_config1_next* on page 3-165
0x410	user_config2	RW	0x00000000	32	*3.3.164 user_config2* on page 3-166
0x414	user_config3	RW	0x00000000	32	*3.3.165 user_config3* on page 3-166
0x500	interrupt_control	RW	0x00000000	32	*3.3.166 interrupt_control* on page 3-167
0x508	interrupt_clr	WO	0x00000000	32	*3.3.167 interrupt_clr* on page 3-168
0x510	interrupt_status	RO	0x00000000	32	*3.3.168 interrupt_status* on page 3-169
0x518	ram_ecc_errc_int_info_31_00	RO	0x00000000	32	*3.3.169 ram_ecc_errc_int_info_31_00* on page 3-171
0x51C	ram_ecc_errc_int_info_63_32	RO	0x00000000	32	*3.3.170 ram_ecc_errc_int_info_63_32* on page 3-172
0x520	ram_ecc_errd_int_info_31_00	RO	0x00000000	32	*3.3.171 ram_ecc_errd_int_info_31_00* on page 3-172
0x524	ram_ecc_errd_int_info_63_32	RO	0x00000000	32	*3.3.172 ram_ecc_errd_int_info_63_32* on page 3-173
0x528	dram_ecc_errc_int_info_31_00	RO	0x00000000	32	*3.3.173 dram_ecc_errc_int_info_31_00* on page 3-174
0x52C	dram_ecc_errc_int_info_63_32	RO	0x00000000	32	*3.3.174 dram_ecc_errc_int_info_63_32* on page 3-174
0x530	dram_ecc_errd_int_info_31_00	RO	0x00000000	32	*3.3.175 dram_ecc_errd_int_info_31_00* on page 3-175

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x534	dram_ecc_errd_int_info_63_32	RO	0x00000000	32	*3.3.176 dram_ecc_errd_int_info_63_32* on page 3-176
0x538	failed_access_int_info_31_00	RO	0x00000000	32	*3.3.177 failed_access_int_info_31_00* on page 3-176
0x53C	failed_access_int_info_63_32	RO	0x00000000	32	*3.3.178 failed_access_int_info_63_32* on page 3-177
0x540	failed_prog_int_info_31_00	RO	0x00000000	32	*3.3.179 failed_prog_int_info_31_00* on page 3-178
0x544	failed_prog_int_info_63_32	RO	0x00000000	32	*3.3.180 failed_prog_int_info_63_32* on page 3-179
0x548	link_err_int_info_31_00	RO	0x00000000	32	*3.3.181 link_err_int_info_31_00* on page 3-179
0x54C	link_err_int_info_63_32	RO	0x00000000	32	*3.3.182 link_err_int_info_63_32* on page 3-180
0x550	arch_fsm_int_info_31_00	RO	0x00000000	32	*3.3.183 arch_fsm_int_info_31_00* on page 3-181
0x554	arch_fsm_int_info_63_32	RO	0x00000000	32	*3.3.184 arch_fsm_int_info_63_32* on page 3-181
0xE00	integ_cfg	RW	0x00000000	32	*3.3.185 integ_cfg* on page 3-182
0xE08	integ_outputs	WO	0x00000000	32	*3.3.186 integ_outputs* on page 3-182
0x1010	address_control_now	RO	0x00030202	32	*3.3.187 address_control_now* on page 3-185
0x1014	decode_control_now	RO	0x00000000	32	*3.3.188 decode_control_now* on page 3-186
0x101C	address_map_now	RO	0x00000000	32	*3.3.189 address_map_now* on page 3-186
0x1020	low_power_control_now	RO	0x00000020	32	*3.3.190 low_power_control_now* on page 3-187
0x1028	turnaround_control_now	RO	0x0F0F0F0F	32	*3.3.191 turnaround_control_now* on page 3-188
0x102C	hit_turnaround_control_now	RO	0x08101F1F	32	*3.3.192 hit_turnaround_control_now* on page 3-189
0x1030	qos_class_control_now	RO	0x00000FC8	32	*3.3.193 qos_class_control_now* on page 3-190
0x1034	escalation_control_now	RO	0x00080000	32	*3.3.194 escalation_control_now* on page 3-191
0x1038	qv_control_31_00_now	RO	0x76543210	32	*3.3.195 qv_control_31_00_now* on page 3-192
0x103C	qv_control_63_32_now	RO	0xFEDCBA98	32	*3.3.196 qv_control_63_32_now* on page 3-193
0x1040	rt_control_31_00_now	RO	0x00000000	32	*3.3.197 rt_control_31_00_now* on page 3-194

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1044	rt_control_63_32_now	RO	0x00000000	32	*3.3.198 rt_control_63_32_now* on page 3-195
0x1048	timeout_control_now	RO	0x00000001	32	*3.3.199 timeout_control_now* on page 3-196
0x104C	credit_control_now	RO	0x00000000	32	*3.3.200 credit_control_now* on page 3-197
0x1050	write_priority_control_31_00_now	RO	0x00000000	32	*3.3.201 write_priority_control_31_00_now* on page 3-198
0x1054	write_priority_control_63_32_now	RO	0x00000000	32	*3.3.202 write_priority_control_63_32_now* on page 3-199
0x1060	queue_threshold_control_31_00_now	RO	0x00000000	32	*3.3.203 queue_threshold_control_31_00_now* on page 3-200
0x1064	queue_threshold_control_63_32_now	RO	0x00000000	32	*3.3.204 queue_threshold_control_63_32_now* on page 3-201
0x1078	memory_address_max_31_00_now	RO	0x00000010	32	*3.3.205 memory_address_max_31_00_now* on page 3-202
0x107C	memory_address_max_43_32_now	RO	0x00000000	32	*3.3.206 memory_address_max_43_32_now* on page 3-203
0x1080	access_address_min0_31_00_now	RO	0x00000000	32	*3.3.207 access_address_min0_31_00_now* on page 3-203
0x1084	access_address_min0_43_32_now	RO	0x00000000	32	*3.3.208 access_address_min0_43_32_now* on page 3-204
0x1088	access_address_max0_31_00_now	RO	0x00000000	32	*3.3.209 access_address_max0_31_00_now* on page 3-205
0x108C	access_address_max0_43_32_now	RO	0x00000000	32	*3.3.210 access_address_max0_43_32_now* on page 3-205
0x1090	access_address_min1_31_00_now	RO	0x00000000	32	*3.3.211 access_address_min1_31_00_now* on page 3-206
0x1094	access_address_min1_43_32_now	RO	0x00000000	32	*3.3.212 access_address_min1_43_32_now* on page 3-207
0x1098	access_address_max1_31_00_now	RO	0x00000000	32	*3.3.213 access_address_max1_31_00_now* on page 3-207
0x109C	access_address_max1_43_32_now	RO	0x00000000	32	*3.3.214 access_address_max1_43_32_now* on page 3-208
0x10A0	access_address_min2_31_00_now	RO	0x00000000	32	*3.3.215 access_address_min2_31_00_now* on page 3-208
0x10A4	access_address_min2_43_32_now	RO	0x00000000	32	*3.3.216 access_address_min2_43_32_now* on page 3-209
0x10A8	access_address_max2_31_00_now	RO	0x00000000	32	*3.3.217 access_address_max2_31_00_now* on page 3-210
0x10AC	access_address_max2_43_32_now	RO	0x00000000	32	*3.3.218 access_address_max2_43_32_now* on page 3-210

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x10B0	access_address_min3_31_00_now	RO	0x00000000	32	*3.3.219 access_address_min3_31_00_now* on page 3-211
0x10B4	access_address_min3_43_32_now	RO	0x00000000	32	*3.3.220 access_address_min3_43_32_now* on page 3-211
0x10B8	access_address_max3_31_00_now	RO	0x00000000	32	*3.3.221 access_address_max3_31_00_now* on page 3-212
0x10BC	access_address_max3_43_32_now	RO	0x00000000	32	*3.3.222 access_address_max3_43_32_now* on page 3-212
0x10C0	access_address_min4_31_00_now	RO	0x00000000	32	*3.3.223 access_address_min4_31_00_now* on page 3-213
0x10C4	access_address_min4_43_32_now	RO	0x00000000	32	*3.3.224 access_address_min4_43_32_now* on page 3-214
0x10C8	access_address_max4_31_00_now	RO	0x00000000	32	*3.3.225 access_address_max4_31_00_now* on page 3-214
0x10CC	access_address_max4_43_32_now	RO	0x00000000	32	*3.3.226 access_address_max4_43_32_now* on page 3-215
0x10D0	access_address_min5_31_00_now	RO	0x00000000	32	*3.3.227 access_address_min5_31_00_now* on page 3-215
0x10D4	access_address_min5_43_32_now	RO	0x00000000	32	*3.3.228 access_address_min5_43_32_now* on page 3-216
0x10D8	access_address_max5_31_00_now	RO	0x00000000	32	*3.3.229 access_address_max5_31_00_now* on page 3-217
0x10DC	access_address_max5_43_32_now	RO	0x00000000	32	*3.3.230 access_address_max5_43_32_now* on page 3-217
0x10E0	access_address_min6_31_00_now	RO	0x00000000	32	*3.3.231 access_address_min6_31_00_now* on page 3-218
0x10E4	access_address_min6_43_32_now	RO	0x00000000	32	*3.3.232 access_address_min6_43_32_now* on page 3-219
0x10E8	access_address_max6_31_00_now	RO	0x00000000	32	*3.3.233 access_address_max6_31_00_now* on page 3-219
0x10EC	access_address_max6_43_32_now	RO	0x00000000	32	*3.3.234 access_address_max6_43_32_now* on page 3-220
0x10F0	access_address_min7_31_00_now	RO	0x00000000	32	*3.3.235 access_address_min7_31_00_now* on page 3-220
0x10F4	access_address_min7_43_32_now	RO	0x00000000	32	*3.3.236 access_address_min7_43_32_now* on page 3-221
0x10F8	access_address_max7_31_00_now	RO	0x00000000	32	*3.3.237 access_address_max7_31_00_now* on page 3-222
0x10FC	access_address_max7_43_32_now	RO	0x00000000	32	*3.3.238 access_address_max7_43_32_now* on page 3-222
0x1110	dci_replay_type_now	RO	0x00000002	32	*3.3.239 dci_replay_type_now* on page 3-223

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1120	refresh_control_now	RO	0x00000000	32	*3.3.240 refresh_control_now* on page 3-223
0x1128	memory_type_now	RO	0x00000101	32	*3.3.241 memory_type_now* on page 3-224
0x1170	scrub_control0_now	RO	0x00000000	32	*3.3.242 scrub_control0_now* on page 3-225
0x1174	scrub_address_min0_now	RO	0x00000000	32	*3.3.243 scrub_address_min0_now* on page 3-226
0x1178	scrub_address_max0_now	RO	0x00000000	32	*3.3.244 scrub_address_max0_now* on page 3-226
0x1180	scrub_control1_now	RO	0x00000000	32	*3.3.245 scrub_control1_now* on page 3-227
0x1184	scrub_address_min1_now	RO	0x00000000	32	*3.3.246 scrub_address_min1_now* on page 3-228
0x1188	scrub_address_max1_now	RO	0x00000000	32	*3.3.247 scrub_address_max1_now* on page 3-228
0x1190	scrub_control2_now	RO	0x00000000	32	*3.3.248 scrub_control2_now* on page 3-229
0x1194	scrub_address_min2_now	RO	0x00000000	32	*3.3.249 scrub_address_min2_now* on page 3-230
0x1198	scrub_address_max2_now	RO	0x00000000	32	*3.3.250 scrub_address_max2_now* on page 3-230
0x11A0	scrub_control3_now	RO	0x00000000	32	*3.3.251 scrub_control3_now* on page 3-231
0x11A4	scrub_address_min3_now	RO	0x00000000	32	*3.3.252 scrub_address_min3_now* on page 3-232
0x11A8	scrub_address_max3_now	RO	0x00000000	32	*3.3.253 scrub_address_max3_now* on page 3-232
0x11B0	scrub_control4_now	RO	0x00000000	32	*3.3.254 scrub_control4_now* on page 3-233
0x11B4	scrub_address_min4_now	RO	0x00000000	32	*3.3.255 scrub_address_min4_now* on page 3-234
0x11B8	scrub_address_max4_now	RO	0x00000000	32	*3.3.256 scrub_address_max4_now* on page 3-234
0x11C0	scrub_control5_now	RO	0x00000000	32	*3.3.257 scrub_control5_now* on page 3-235
0x11C4	scrub_address_min5_now	RO	0x00000000	32	*3.3.258 scrub_address_min5_now* on page 3-236
0x11C8	scrub_address_max5_now	RO	0x00000000	32	*3.3.259 scrub_address_max5_now* on page 3-236
0x11D0	scrub_control6_now	RO	0x00000000	32	*3.3.260 scrub_control6_now* on page 3-237
0x11D4	scrub_address_min6_now	RO	0x00000000	32	*3.3.261 scrub_address_min6_now* on page 3-238
0x11D8	scrub_address_max6_now	RO	0x00000000	32	*3.3.262 scrub_address_max6_now* on page 3-238
0x11E0	scrub_control7_now	RO	0x00000000	32	*3.3.263 scrub_control7_now* on page 3-239
0x11E4	scrub_address_min7_now	RO	0x00000000	32	*3.3.264 scrub_address_min7_now* on page 3-240

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x11E8	scrub_address_max7_now	RO	0x00000000	32	*3.3.265 scrub_address_max7_now* on page 3-240
0x11F0	feature_control_now	RO	0x0AA00000	32	*3.3.266 feature_control_now* on page 3-241
0x11F4	mux_control_now	RO	0x00000000	32	*3.3.267 mux_control_now* on page 3-243
0x11F8	rank_remap_control_now	RO	0x76543210	32	*3.3.268 rank_remap_control_now* on page 3-244
0x1200	t_refi_now	RO	0x00090100	32	*3.3.269 t_refi_now* on page 3-245
0x1204	t_rfc_now	RO	0x00008C23	32	*3.3.270 t_rfc_now* on page 3-246
0x1208	t_mrr_now	RO	0x00000002	32	*3.3.271 t_mrr_now* on page 3-247
0x120C	t_mrw_now	RO	0x0000000C	32	*3.3.272 t_mrw_now* on page 3-247
0x1210	t_rdpden_now	RO	0x00000002	32	*3.3.273 t_rdpden_now* on page 3-248
0x1218	t_rcd_now	RO	0x00000005	32	*3.3.274 t_rcd_now* on page 3-248
0x121C	t_ras_now	RO	0x0000000E	32	*3.3.275 t_ras_now* on page 3-249
0x1220	t_rp_now	RO	0x00000005	32	*3.3.276 t_rp_now* on page 3-249
0x1224	t_rpall_now	RO	0x00000005	32	*3.3.277 t_rpall_now* on page 3-250
0x1228	t_rrd_now	RO	0x00000404	32	*3.3.278 t_rrd_now* on page 3-251
0x122C	t_act_window_now	RO	0x03560014	32	*3.3.279 t_act_window_now* on page 3-251
0x1234	t_rtr_now	RO	0x00040404	32	*3.3.280 t_rtr_now* on page 3-252
0x1238	t_rtw_now	RO	0x00060606	32	*3.3.281 t_rtw_now* on page 3-253
0x123C	t_rtp_now	RO	0x00000004	32	*3.3.282 t_rtp_now* on page 3-254
0x1244	t_wr_now	RO	0x00000005	32	*3.3.283 t_wr_now* on page 3-254
0x1248	t_wtr_now	RO	0x00040404	32	*3.3.284 t_wtr_now* on page 3-255
0x124C	t_wtw_now	RO	0x00040404	32	*3.3.285 t_wtw_now* on page 3-256
0x1254	t_xmpd_now	RO	0x000003FF	32	*3.3.286 t_xmpd_now* on page 3-256
0x1258	t_ep_now	RO	0x00000002	32	*3.3.287 t_ep_now* on page 3-257
0x125C	t_xp_now	RO	0x00060002	32	*3.3.288 t_xp_now* on page 3-257
0x1260	t_esr_now	RO	0x0000000E	32	*3.3.289 t_esr_now* on page 3-258
0x1264	t_xsr_now	RO	0x05120100	32	*3.3.290 t_xsr_now* on page 3-259
0x1268	t_esrck_now	RO	0x00000005	32	*3.3.291 t_esrck_now* on page 3-259
0x126C	t_ckxsr_now	RO	0x00000001	32	*3.3.292 t_ckxsr_now* on page 3-260
0x1270	t_cmd_now	RO	0x00000000	32	*3.3.293 t_cmd_now* on page 3-261
0x1274	t_parity_now	RO	0x00000900	32	*3.3.294 t_parity_now* on page 3-261
0x1278	t_zqcs_now	RO	0x00000040	32	*3.3.295 t_zqcs_now* on page 3-262
0x1300	t_rddata_en_now	RO	0x00000001	32	*3.3.296 t_rddata_en_now* on page 3-263
0x1304	t_phyrdlat_now	RO	0x00000000	32	*3.3.297 t_phyrdlat_now* on page 3-264

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1308	t_phywrlat_now	RO	0x00000001	32	*3.3.298 t_phywrlat_now* on page 3-264
0x1310	rdlvl_control_now	RO	0x00001080	32	*3.3.299 rdlvl_control_now* on page 3-265
0x1314	rdlvl_mrs_now	RO	0x00000004	32	*3.3.300 rdlvl_mrs_now* on page 3-267
0x1318	t_rdlvl_en_now	RO	0x00000000	32	*3.3.301 t_rdlvl_en_now* on page 3-267
0x131C	t_rdlvl_rr_now	RO	0x00000000	32	*3.3.302 t_rdlvl_rr_now* on page 3-268
0x1320	wrlvl_control_now	RO	0x00001000	32	*3.3.303 wrlvl_control_now* on page 3-268
0x1324	wrlvl_mrs_now	RO	0x00000086	32	*3.3.304 wrlvl_mrs_now* on page 3-270
0x1328	t_wrlvl_en_now	RO	0x00000000	32	*3.3.305 t_wrlvl_en_now* on page 3-270
0x132C	t_wrlvl_ww_now	RO	0x00000000	32	*3.3.306 t_wrlvl_ww_now* on page 3-271
0x1348	phy_power_control_now	RO	0x00000000	32	*3.3.307 phy_power_control_now* on page 3-271
0x134C	t_lpresp_now	RO	0x00000000	32	*3.3.308 t_lpresp_now* on page 3-273
0x1350	phy_update_control_now	RO	0x0FE00000	32	*3.3.309 phy_update_control_now* on page 3-273
0x1358	odt_timing_now	RO	0x06000600	32	*3.3.310 odt_timing_now* on page 3-274
0x1360	odt_wr_control_31_00_now	RO	0x08040201	32	*3.3.311 odt_wr_control_31_00_now* on page 3-275
0x1364	odt_wr_control_63_32_now	RO	0x80402010	32	*3.3.312 odt_wr_control_63_32_now* on page 3-276
0x1368	odt_rd_control_31_00_now	RO	0x00000000	32	*3.3.313 odt_rd_control_31_00_now* on page 3-277
0x136C	odt_rd_control_63_32_now	RO	0x00000000	32	*3.3.314 odt_rd_control_63_32_now* on page 3-278
0x1380	dq_map_control_15_00_now	RO	0x00000000	32	*3.3.315 dq_map_control_15_00_now* on page 3-279
0x1384	dq_map_control_31_16_now	RO	0x00000000	32	*3.3.316 dq_map_control_31_16_now* on page 3-279
0x1388	dq_map_control_47_32_now	RO	0x00000000	32	*3.3.317 dq_map_control_47_32_now* on page 3-280
0x138C	dq_map_control_63_48_now	RO	0x00000000	32	*3.3.318 dq_map_control_63_48_now* on page 3-281
0x1390	dq_map_control_71_64_now	RO	0x00000000	32	*3.3.319 dq_map_control_71_64_now* on page 3-282
0x1408	user_config0_now	RO	0x00000000	32	*3.3.320 user_config0_now* on page 3-283
0x140C	user_config1_now	RO	0x00000000	32	*3.3.321 user_config1_now* on page 3-284
0x1FD0	periph_id_4	RO	0x00000014	32	*3.3.322 periph_id_4* on page 3-284
0x1FE0	periph_id_0	RO	0x00000052	32	*3.3.323 periph_id_0* on page 3-285
0x1FE4	periph_id_1	RO	0x000000B4	32	*3.3.324 periph_id_1* on page 3-285

Table 3-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x1FE8	periph_id_2	RO	0x0000000B	32	*3.3.325 periph_id_2* on page 3-286
0x1FEC	periph_id_3	RO	0x00000000	32	*3.3.326 periph_id_3* on page 3-287
0x1FF0	component_id_0	RO	0x0000000D	32	*3.3.327 component_id_0* on page 3-287
0x1FF4	component_id_1	RO	0x000000F0	32	*3.3.328 component_id_1* on page 3-288
0x1FF8	component_id_2	RO	0x00000005	32	*3.3.329 component_id_2* on page 3-288
0x1FFC	component_id_3	RO	0x000000B1	32	*3.3.330 component_id_3* on page 3-289

3.3 Register descriptions

This section describes the DMC-520 registers.

3.2 Register summary on page 3-32 provides cross references to individual registers.

3.3.1 memc_status

This register holds the architectural status of the DMC.

The memc_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x000`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

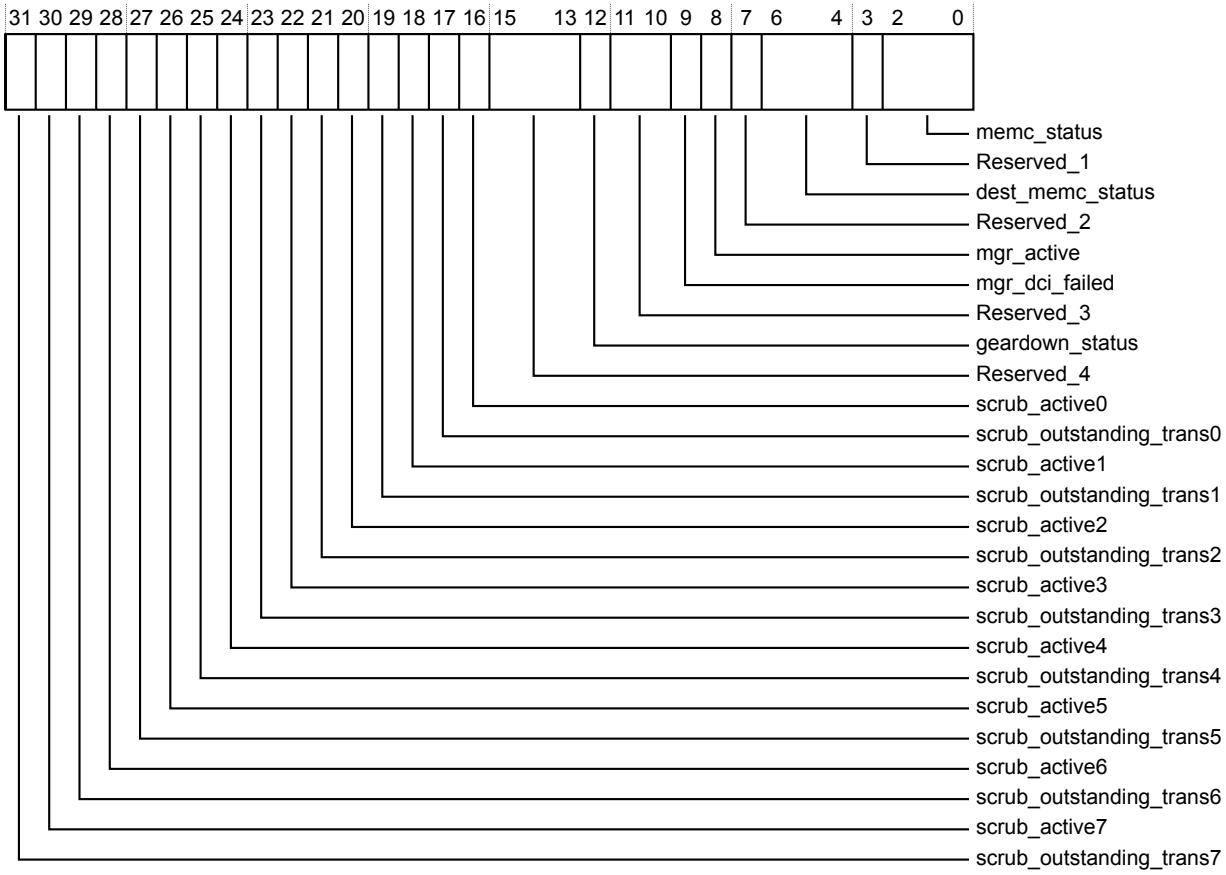

Figure 3-1 memc_status register bit assignments

The following shows the bit assignments.

[31] scrub_outstanding_trans7
scrub_outstanding_trans7 bitfield.

[30] scrub_active7
scrub_active7 bitfield.
[29] scrub_outstanding_trans6
scrub_outstanding_trans6 bitfield.
[28] scrub_active6
scrub_active6 bitfield.
[27] scrub_outstanding_trans5
scrub_outstanding_trans5 bitfield.
[26] scrub_active5
scrub_active5 bitfield.
[25] scrub_outstanding_trans4
scrub_outstanding_trans4 bitfield.
[24] scrub_active4
scrub_active4 bitfield.
[23] scrub_outstanding_trans3
scrub_outstanding_trans3 bitfield.
[22] scrub_active3
scrub_active3 bitfield.
[21] scrub_outstanding_trans2
scrub_outstanding_trans2 bitfield.
[20] scrub_active2
scrub_active2 bitfield.
[19] scrub_outstanding_trans1
scrub_outstanding_trans1 bitfield.
[18] scrub_active1
scrub_active1 bitfield.
[17] scrub_outstanding_trans0
scrub_outstanding_trans0 bitfield.
[16] scrub_active0
scrub_active0 bitfield.
[15:13] Reserved_4
Unused bits
[12] geardown_status
Indicates if the DMC is operating in Geardown mode for DDR4 accesses.
[11:10] Reserved_3
Unused bits
[9] mgr_dci_failed
A direct command in a previous sequence has failed.
[8] mgr_active
mgr_active bitfield.
[7] Reserved_2
Unused bits
[6:4] dest_memc_status
The intended destination state of the DMC during an active transition, or when in the ABORTED or RECOVER state.
[3] Reserved_1
Unused bits
[2:0] memc_status
The current state of the DMC.

3.3.2 memc_config

This register holds the configuration data for the DMC.

The memc_config register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0x004`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

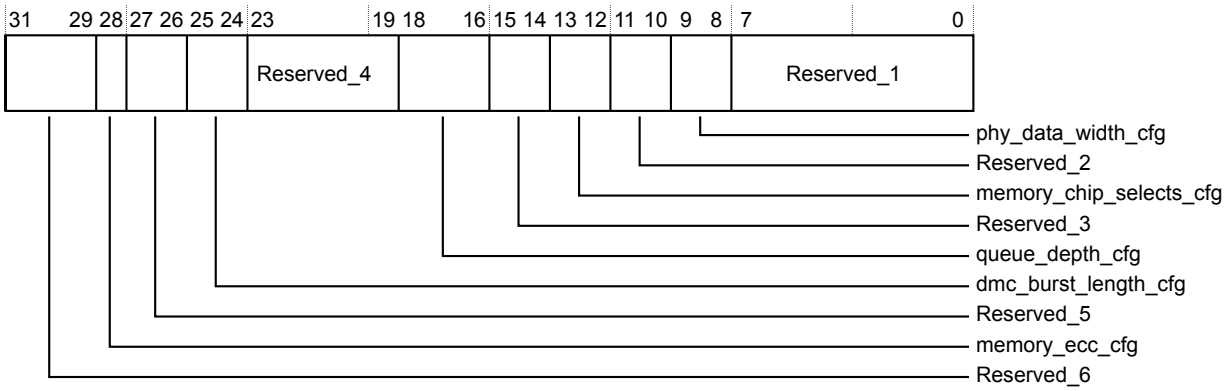

Figure 3-2 memc_config register bit assignments

The following shows the bit assignments.

[31:29] Reserved_6

Unused bits

[28] memory_ecc_cfg

Indicates presence of error correction code logic

[27:26] Reserved_5

Unused bits

[25:24] dmc_burst_length_cfg

Configured DMC burst length, expressed in beats of phy_data_width_cfg width

[23:19] Reserved_4

Unused bits

[18:16] queue_depth_cfg

Configured depth of the request queue, in units of DMC bursts

[15:14] Reserved_3

Unused bits

[13:12] memory_chip_selects_cfg

Configured number of memory chip (rank) selects per interface

[11:10] Reserved_2

Unused bits

[9:8] phy_data_width_cfg

Configured effective memory width, PHY interface width

[7:0] Reserved_1

Unused bits

3.3.3 memc_cmd

This register changes the architectural state of the DMC, or executes queued manager operations.

The memc_cmd register characteristics are:

Usage constraints

Cannot be read from. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.
Attributes

Offset	0x008
Type	Write-only
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

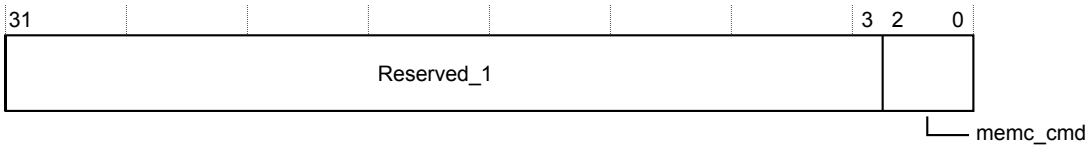

Figure 3-3 memc_cmd register bit assignments

The following shows the bit assignments.

[31:3] Reserved_1
Unused bits
[2:0] memc_cmd
memc_cmd bitfield.

3.3.4 address_control_next

This register configures the DRAM address parameters. Use the DRAM device data sheet or *Serial Presence Detect* (SPD)-derived values to assist in programming these values.

The address_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	0x010
Type	Read-write
Reset	0x00030202
Width	32

The following figure shows the bit assignments.

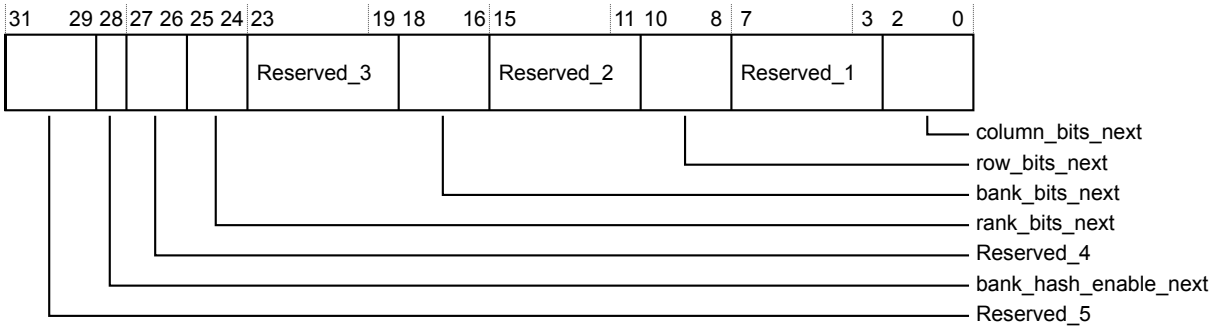

Figure 3-4 address_control_next register bit assignments

The following shows the bit assignments.

[31:29] Reserved_5
Unused bits

[28] bank_hash_enable_next
Configures the bank hash function used in system address decode. Used to alter traffic distribution across banks.

[27:26] Reserved_4
Unused bits

[25:24] rank_bits_next
Program to match the number of active ranks to be addressed.

[23:19] Reserved_3
Unused bits

[18:16] bank_bits_next
Program to match the number of banks per chip-select (rank) on the attached DRAM device. Note: this number correspond to the sum total of all banks in all bank groups (where applicable) on a device.

[15:11] Reserved_2
Unused bits

[10:8] row_bits_next
Program to match the number of row bits on the attached DRAM device.

[7:3] Reserved_1
Unused bits

[2:0] column_bits_next
Program to match the number of column address bits present on the DRAM device.

3.3.5 decode_control_next

This register configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, bank, row address, and the column address.

The decode_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x014`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

Figure 3-5 decode_control_next register bit assignments

The following shows the bit assignments.

[31:7] Reserved_2
Unused bits

[6:4] stripe_decode_next
Determines the address boundary on which to stripe system requests across DRAM pages. The DMC decodes the bottom two page address bits from a programmable slice within the lowest 14 bits of the system address. To disable sub-page striping you must program this value to the DRAM page size (or use the default value 0). Note: you must not program the DMC to stripe at a higher boundary than the DRAM page size.

[3:2] Reserved_1
Unused bits

[1:0] address_decode_next
Determines in which pattern the DRAM address components are decoded from the system address.

3.3.6 address_map_next

This register configures the system address mapping options.

The address_map_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x01C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

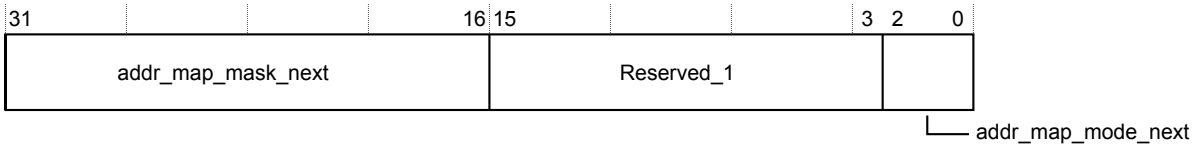

Figure 3-6 address_map_next register bit assignments

The following shows the bit assignments.

[31:16] addr_map_mask_next
Configures the mask applied to system address bits [43:28]. The system address map uses upper address bits to select from multiple DMC instances in a system. The DMC must discard these address bits that fall outside physical memory to decode correctly.

[15:3] Reserved_1
Unused bits

[2:0] addr_map_mode_next
Selects the address translation mode. See the System Address Conversion section of the Design Manual for more information on address translation options.

3.3.7 low_power_control_next

This register configures the low-power features of the DMC.

The low_power_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x020
Type Read-write
Reset 0x00000020
Width 32

The following figure shows the bit assignments.

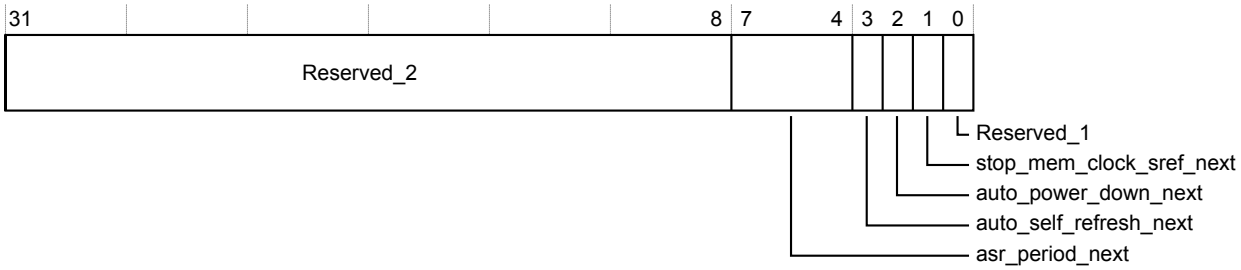

Figure 3-7 low_power_control_next register bit assignments

The following shows the bit assignments.

[31:8] Reserved_2
Unused bits

[7:4] asr_period_next
Program the number of tREFI intervals to wait without activity before placing the DRAM into a self-refresh state when auto_self_refresh is enabled. The supported range for this bitfield is 1-15.

[3] auto_self_refresh_next
Program to enable or disable placing a DRAM rank into a self-refresh state when the rank has been idle for the amount of time that asr_period defines.

[2] auto_power_down_next
Program to enable or disable placing the DRAM into a power-down state when idle.

[1] stop_mem_clock_sref_next
Program to enable or disable stopping the DRAM clock when the memory device is in self-refresh, reset, or maximum power down.

[0] Reserved_1
Unused bits

3.3.8 turnaround_control_next

This register configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus.

The turnaround_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x028
Type Read-write
Reset 0x0F0F0F0F
Width 32

The following figure shows the bit assignments.

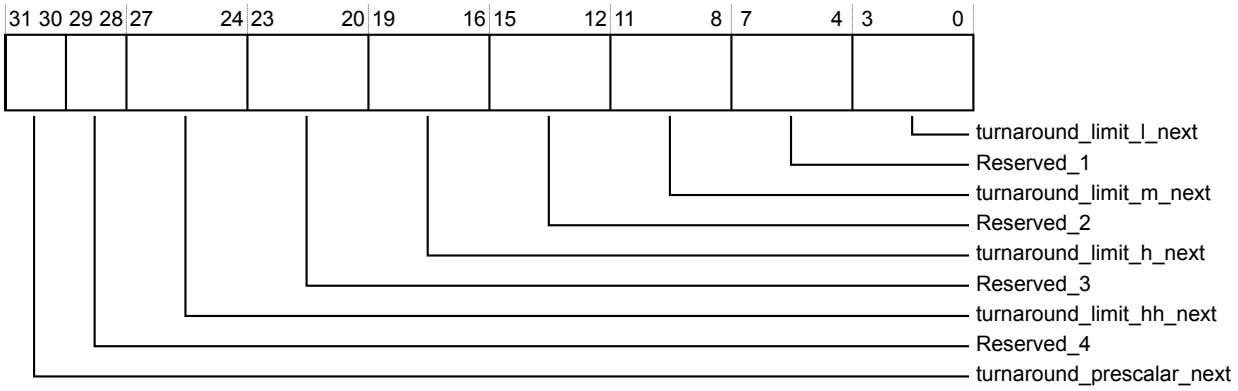

Figure 3-8 turnaround_control_next register bit assignments

The following shows the bit assignments.

[31:30] turnaround_prescalar_next
Turnaround counter prescaler.

[29:28] Reserved_4
Unused bits

[27:24] turnaround_limit_hh_next
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of HIGH-HIGH class requests. The supported range for this bitfield is 0-15.

[23:20] Reserved_3
Unused bits

[19:16] turnaround_limit_h_next
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of HIGH class requests. The supported range for this bitfield is 0-15.

[15:12] Reserved_2
Unused bits

[11:8] turnaround_limit_m_next
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of MEDIUM class requests. The supported range for this bitfield is 0-15.

[7:4] Reserved_1
Unused bits

[3:0] turnaround_limit_l_next
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of LOW class requests. The supported range for this bitfield is 0-15.

3.3.9 hit_turnaround_control_next

This register configures the settings for preventing starvation of non-hits in the presence of in-row hit streams.

The hit_turnaround_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x02C`
Type	Read-write
Reset	`0x08101F1F`
Width	32

The following figure shows the bit assignments.

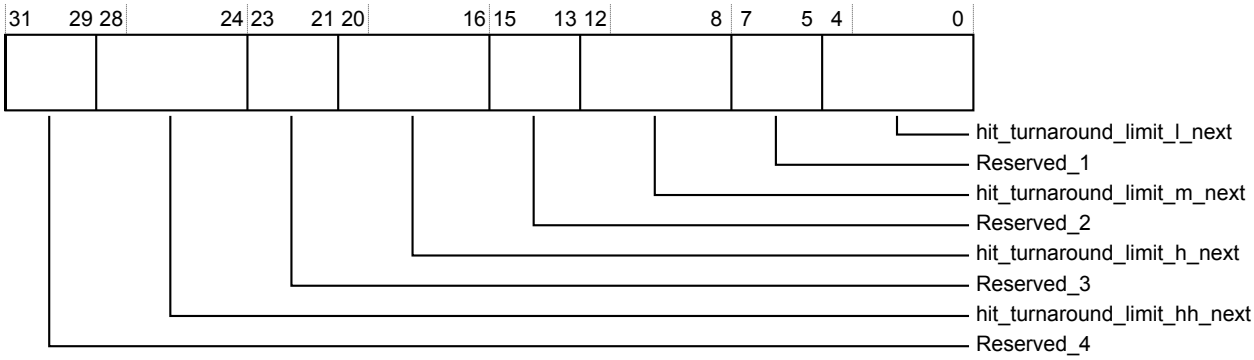

Figure 3-9 hit_turnaround_control_next register bit assignments

The following shows the bit assignments.

[31:29] Reserved_4
Unused bits

[28:24] hit_turnaround_limit_hh_next
Program the maximum number of consecutive in-row hits in the presence of HIGH-HIGH class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

[23:21] Reserved_3
Unused bits

[20:16] hit_turnaround_limit_h_next
Program the maximum number of consecutive in-row hits in the presence of HIGH class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

[15:13] Reserved_2
Unused bits

[12:8] hit_turnaround_limit_m_next
Program the maximum number of consecutive in-row hits in the presence of MEDIUM class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

[7:5] Reserved_1
Unused bits

[4:0] hit_turnaround_limit_l_next
Program the maximum number of consecutive in-row hits in the presence of LOW class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

3.3.10 qos_class_control_next

This register configures the priority class for each QoS encoding.

The qos_class_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x030`
Type	Read-write
Reset	`0x00000FC8`
Width	32

The following figure shows the bit assignments.

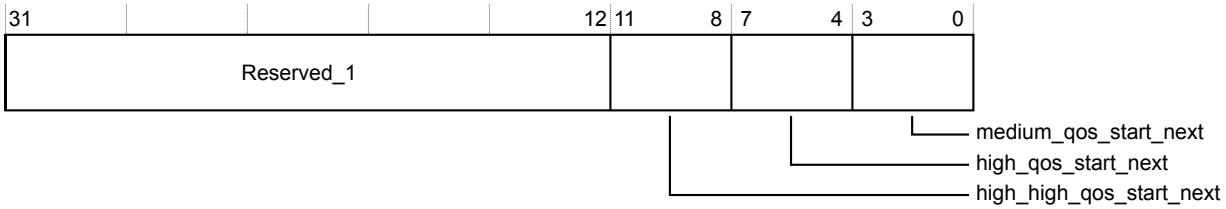

Figure 3-10 qos_class_control_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:8] high_high_qos_start_next
Determines the minimum Qv value mapped onto the HIGH-HIGH QoS class. The supported range for this bitfield is 0-15.

[7:4] high_qos_start_next
Determines the minimum Qv value mapped onto the HIGH QoS class. The supported range for this bitfield is 0-15.

[3:0] medium_qos_start_next
Determines the minimum Qv value mapped onto the MEDIUM QoS class. The supported range for this bitfield is 0-15.

3.3.11 escalation_control_next

This register configures the settings for escalating the priority of entries in the queue.

The escalation_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x034`
Type	Read-write
Reset	`0x00080000`
Width	32

The following figure shows the bit assignments.

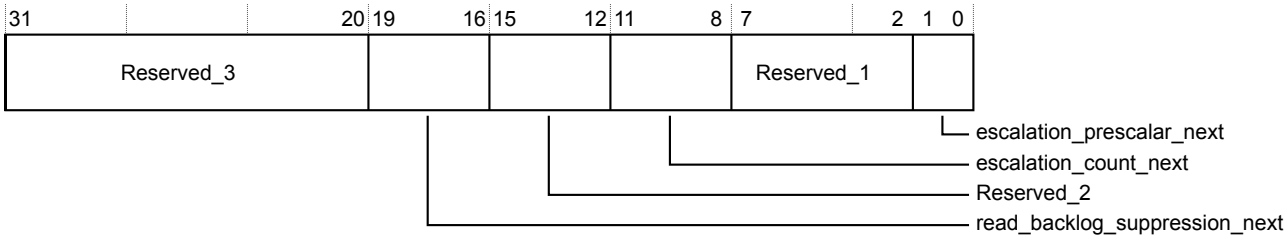

Figure 3-11 escalation_control_next register bit assignments

The following shows the bit assignments.

[31:20] Reserved_3
Unused bits

[19:16] read_backlog_suppression_next
Configures the number of completed reads (as a proportion in 16ths of the queue depth) at which to stop arbitrating more reads until the system drains the fetched read data. Zero disables this feature. The supported range for this bitfield is 0-15.

[15:12] Reserved_2
Unused bits

[11:8] escalation_count_next
Program the number of escalation prescaler periods between applying escalation. Zero disables priority escalation in the queue. The supported range for this bitfield is 0-15.

[7:2] Reserved_1
Unused bits

[1:0] escalation_prescalar_next
Escalation counter prescaler.

3.3.12 qv_control_31_00_next

This register configures the priority settings for each QoS encoding.

The qv_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x038`
Type	Read-write
Reset	`0x76543210`
Width	32

The following figure shows the bit assignments.

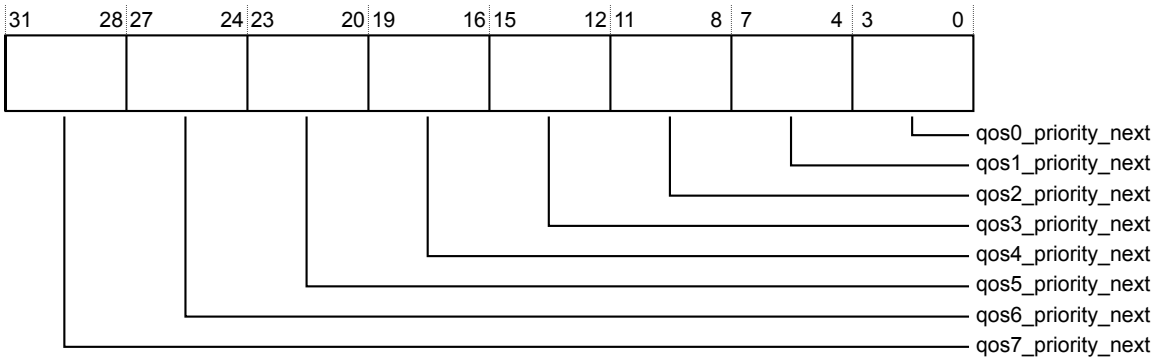

Figure 3-12 qv_control_31_00_next register bit assignments

The following shows the bit assignments.

[31:28] qos7_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos6_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos5_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos4_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos3_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos2_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos1_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos0_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

3.3.13 qv_control_63_32_next

This register configures the priority settings for each QoS encoding.

The qv_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x03C`
Type	Read-write
Reset	`0xFEDCBA98`
Width	32

The following figure shows the bit assignments.

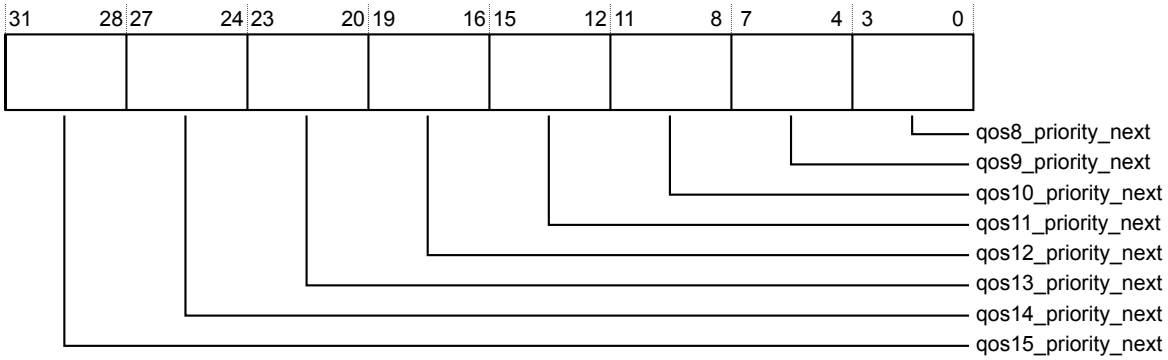

Figure 3-13 qv_control_63_32_next register bit assignments

The following shows the bit assignments.

[31:28] qos15_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos14_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos13_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos12_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos11_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos10_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos9_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos8_priority_next
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

3.3.14 rt_control_31_00_next

This register configures the timeout settings for each QoS encoding.

The rt_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x040`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

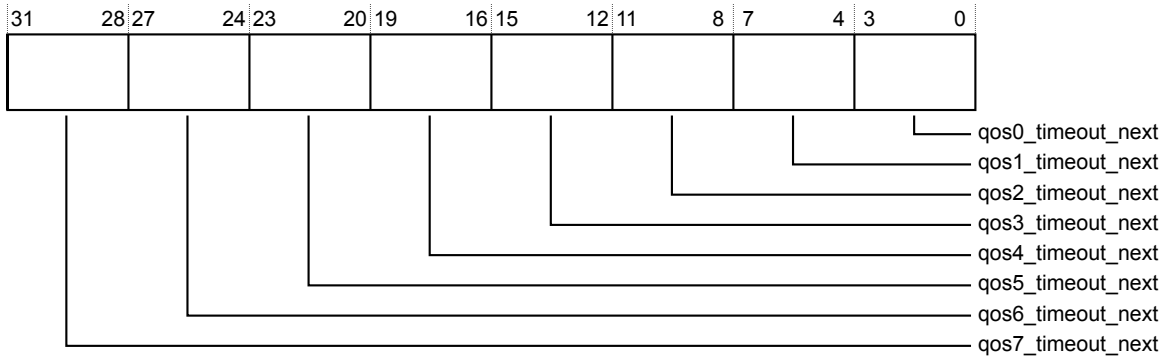

Figure 3-14 rt_control_31_00_next register bit assignments

The following shows the bit assignments.

[31:28] qos7_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos6_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos5_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos4_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos3_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos2_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos1_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos0_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

3.3.15 rt_control_63_32_next

This register configures the timeout settings for each QoS encoding.

The rt_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x044`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

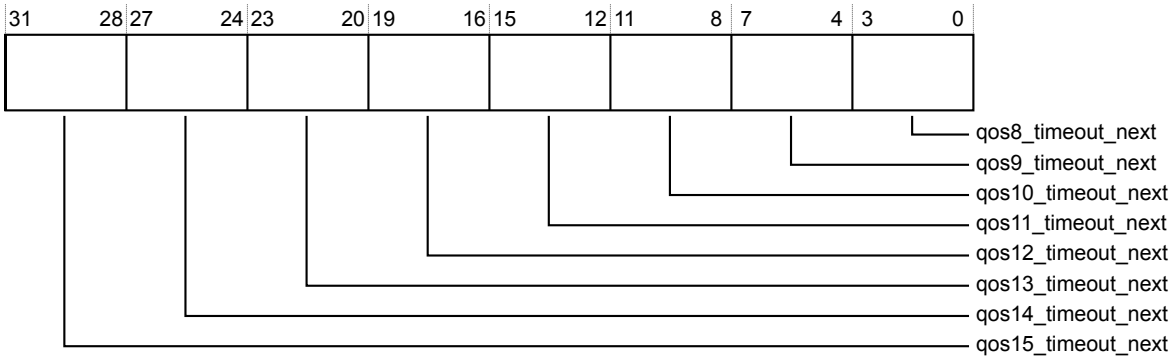

Figure 3-15 rt_control_63_32_next register bit assignments

The following shows the bit assignments.

[31:28] qos15_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos14_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos13_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos12_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos11_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos10_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos9_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos8_timeout_next
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

3.3.16 timeout_control_next

This register configures the prescaler applied to timeout values.

The timeout_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x048
Type Read-write
Reset 0x00000001
Width 32

The following figure shows the bit assignments.

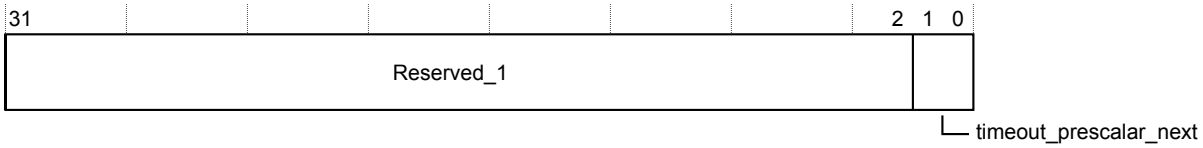

Figure 3-16 timeout_control_next register bit assignments

The following shows the bit assignments.

[31:2] Reserved_1
Unused bits
[1:0] timeout_prescalar_next
timeout_prescalar_next bitfield.

3.3.17 credit_control_next

This register configures the settings for preventing starvation of CHI protocol retries.

The credit_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x04C
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

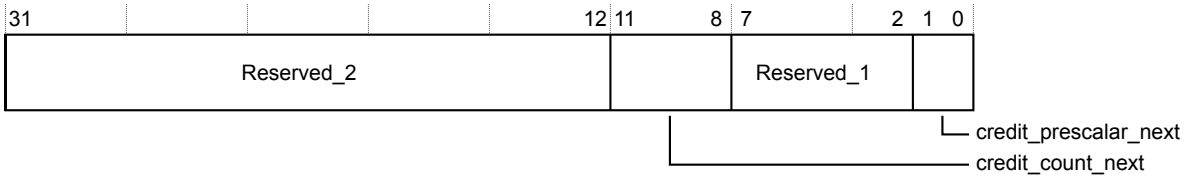

Figure 3-17 credit_control_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_2
Unused bits
[11:8] credit_count_next
Program the number of P-credit prescaler periods between applying escalation. 0 disables this feature. The supported range for this bitfield is 0-15.
[7:2] Reserved_1
Unused bits

[1:0] credit_prescalar_next
P-credit counter prescaler.

3.3.18 write_priority_control_31_00_next

This register configures the priority settings for write requests within the DMC.

The write_priority_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x050`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

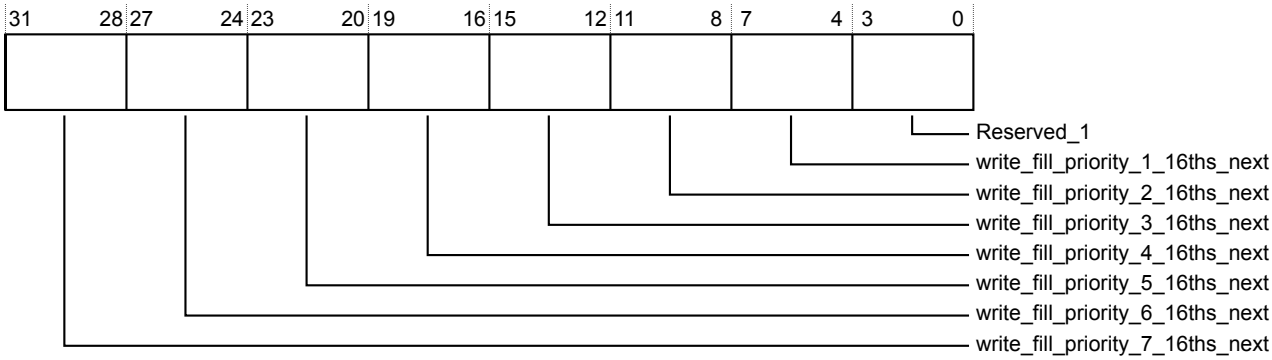

Figure 3-18 write_priority_control_31_00_next register bit assignments

The following shows the bit assignments.

[31:28] write_fill_priority_7_16ths_next
Program the priority of write requests when write requests occupy 7/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[27:24] write_fill_priority_6_16ths_next
Program the priority of write requests when write requests occupy 6/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[23:20] write_fill_priority_5_16ths_next
Program the priority of write requests when write requests occupy 5/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[19:16] write_fill_priority_4_16ths_next
Program the priority of write requests when write requests occupy 4/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[15:12] write_fill_priority_3_16ths_next
Program the priority of write requests when write requests occupy 3/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[11:8] write_fill_priority_2_16ths_next
Program the priority of write requests when write requests occupy 2/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[7:4] write_fill_priority_1_16ths_next
Program the priority of write requests when write requests occupy 1/16th of the DMC queue. The supported range for this bitfield is 0-15.

[3:0] Reserved_1
Unused bits

3.3.19 write_priority_control_63_32_next

This register configures the priority settings for write requests within the DMC.

The write_priority_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x054`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

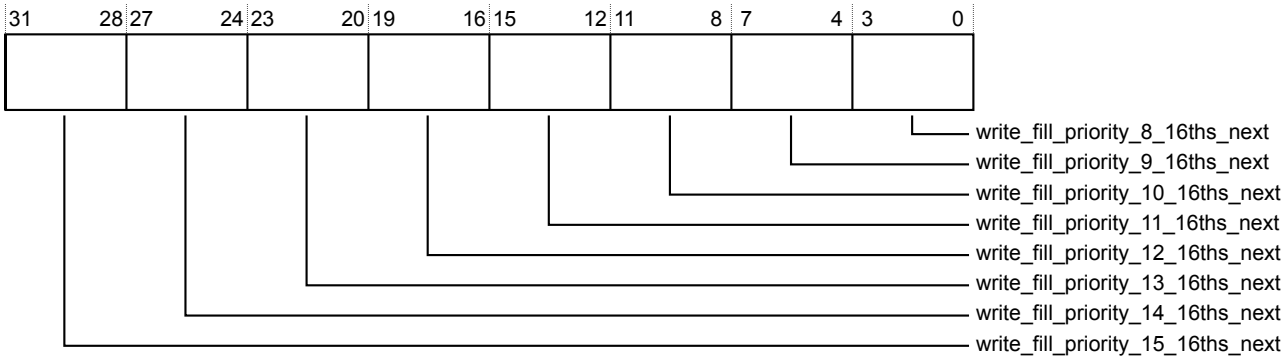

Figure 3-19 write_priority_control_63_32_next register bit assignments

The following shows the bit assignments.

[31:28] write_fill_priority_15_16ths_next
Program the priority of write requests when write requests occupy 15/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[27:24] write_fill_priority_14_16ths_next
Program the priority of write requests when write requests occupy 14/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[23:20] write_fill_priority_13_16ths_next
Program the priority of write requests when write requests occupy 13/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[19:16] write_fill_priority_12_16ths_next
Program the priority of write requests when write requests occupy 12/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[15:12] write_fill_priority_11_16ths_next
Program the priority of write requests when write requests occupy 11/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[11:8] write_fill_priority_10_16ths_next
Program the priority of write requests when write requests occupy 10/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[7:4] write_fill_priority_9_16ths_next
Program the priority of write requests when write requests occupy 9/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[3:0] write_fill_priority_8_16ths_next
Program the priority of write requests when write requests occupy 8/16ths of the DMC queue. The supported range for this bitfield is 0-15.

3.3.20 queue_threshold_control_31_00_next

This register configures the threshold settings for requests in the DMC.

The queue_threshold_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x060`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

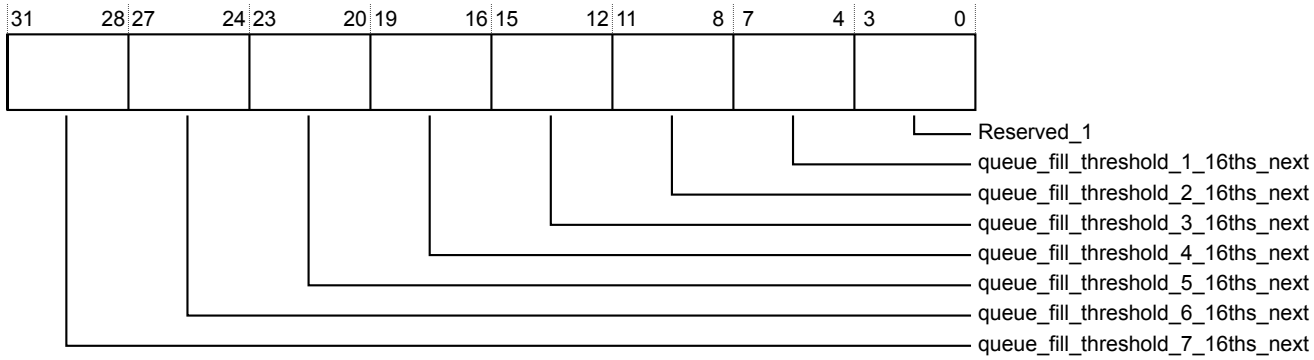

Figure 3-20 queue_threshold_control_31_00_next register bit assignments

The following shows the bit assignments.

[31:28] queue_fill_threshold_7_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 7/16ths full. The supported range for this bitfield is 0-15.

[27:24] queue_fill_threshold_6_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 6/16ths full. The supported range for this bitfield is 0-15.

[23:20] queue_fill_threshold_5_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 5/16ths full. The supported range for this bitfield is 0-15.

[19:16] queue_fill_threshold_4_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 4/16ths full. The supported range for this bitfield is 0-15.

[15:12] queue_fill_threshold_3_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 3/16ths full. The supported range for this bitfield is 0-15.

[11:8] queue_fill_threshold_2_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 2/16ths full. The supported range for this bitfield is 0-15.

[7:4] queue_fill_threshold_1_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 1/16ths full. The supported range for this bitfield is 0-15.

[3:0] Reserved_1
Unused bits

3.3.21 queue_threshold_control_63_32_next

This register configures the threshold settings for requests in the DMC.

The queue_threshold_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x064`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

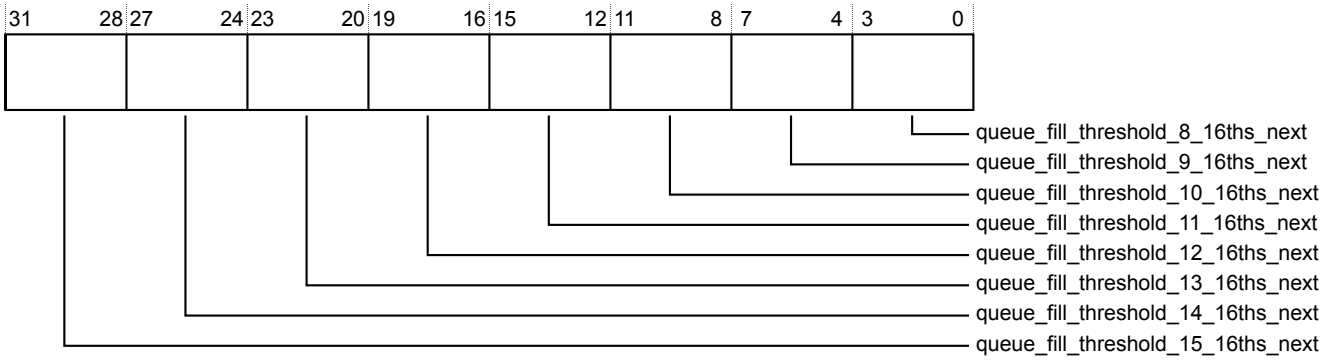

Figure 3-21 queue_threshold_control_63_32_next register bit assignments

The following shows the bit assignments.

[31:28] queue_fill_threshold_15_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 15/16ths full. The supported range for this bitfield is 0-15.

[27:24] queue_fill_threshold_14_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 14/16ths full. The supported range for this bitfield is 0-15.

[23:20] queue_fill_threshold_13_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 13/16ths full. The supported range for this bitfield is 0-15.

[19:16] queue_fill_threshold_12_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 12/16ths full. The supported range for this bitfield is 0-15.

[15:12] queue_fill_threshold_11_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 11/16ths full. The supported range for this bitfield is 0-15.

[11:8] queue_fill_threshold_10_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 10/16ths full. The supported range for this bitfield is 0-15.

[7:4] queue_fill_threshold_9_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 9/16ths full. The supported range for this bitfield is 0-15.

[3:0] queue_fill_threshold_8_16ths_next
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 8/16ths full. The supported range for this bitfield is 0-15.

3.3.22 memory_address_max_31_00_next

This register configures the address space control for the DMC default region.

The memory_address_max_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x078`
Type	Read-write
Reset	`0x00000010`
Width	32

The following figure shows the bit assignments.

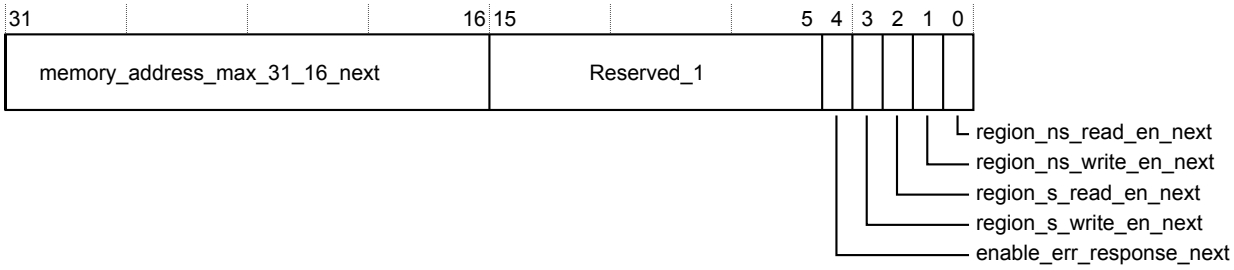

Figure 3-22 memory_address_max_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] memory_address_max_31_16_next
Program to set bits[31:16] of the maximum memory address. Note that this is the address value after address translation has been applied (if applicable).

[15:5] Reserved_1
Unused bits

[4] enable_err_response_next
Configures the response used for a request that fails address access checks.

[3] region_s_write_en_next
Enables Secure writes to the default region

[2] region_s_read_en_next
Enables Secure reads to the default region

[1] region_ns_write_en_next
Enables Non-secure writes to the default region

[0] region_ns_read_en_next
Enables Non-secure reads to the default region

3.3.23 memory_address_max_43_32_next

This register configures the address space control for the DMC default region.

The memory_address_max_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x07C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

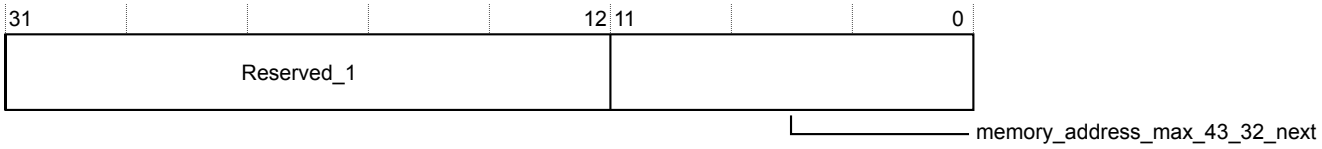

Figure 3-23 memory_address_max_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] memory_address_max_43_32_next
Program to set bits[43:32] of the maximum memory address. Note that this is the address value after address translation has been applied (if applicable).

3.3.24 access_address_min0_31_00_next

This register configures the address space control for address region 0.

The access_address_min0_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x080`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

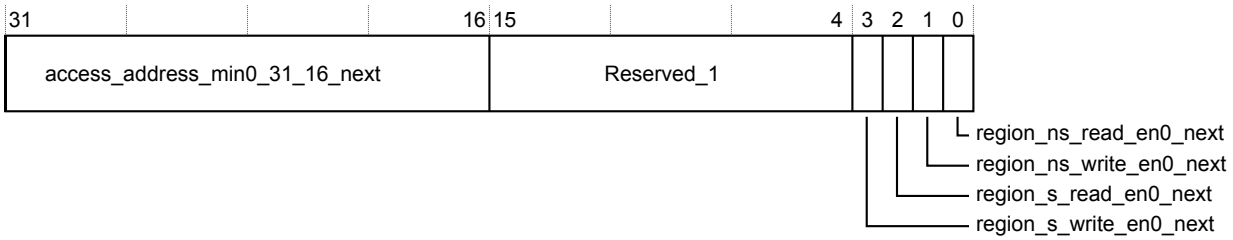

Figure 3-24 access_address_min0_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min0_31_16_next
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en0_next
Enables Secure writes to the region
[2] region_s_read_en0_next
Enables Secure reads to the region
[1] region_ns_write_en0_next
Enables Non-secure writes to the region
[0] region_ns_read_en0_next
Enables Non-secure reads to the region

3.3.25 access_address_min0_43_32_next

This register configures the address space control for address region 0.

The access_address_min0_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x084`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

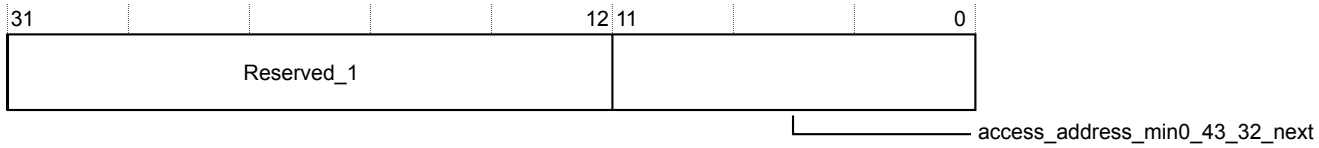

Figure 3-25 access_address_min0_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min0_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.26 access_address_max0_31_00_next

This register configures the address space control for address region 0.

The access_address_max0_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x088`
Type	Read-write

Reset 0x00000000
Width 32

The following figure shows the bit assignments.

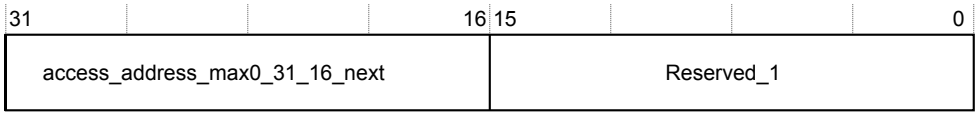

Figure 3-26 access_address_max0_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max0_31_16_next
Program to set bits[31:16] of the maximum address in the region
[15:0] Reserved_1
Unused bits

3.3.27 access_address_max0_43_32_next

This register configures the address space control for address region 0.

The access_address_max0_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x08C
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

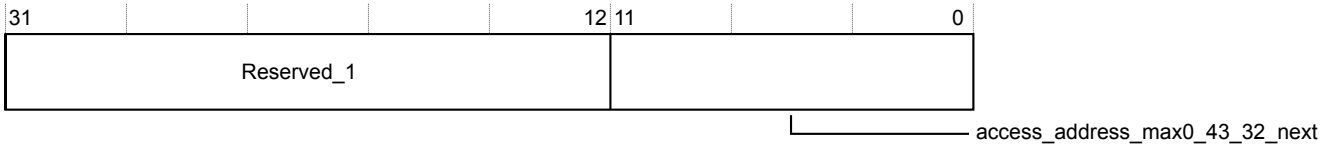

Figure 3-27 access_address_max0_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_max0_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.28 access_address_min1_31_00_next

This register configures the address space control for address region 1.

The access_address_min1_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.

Attributes

Offset 0x090
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

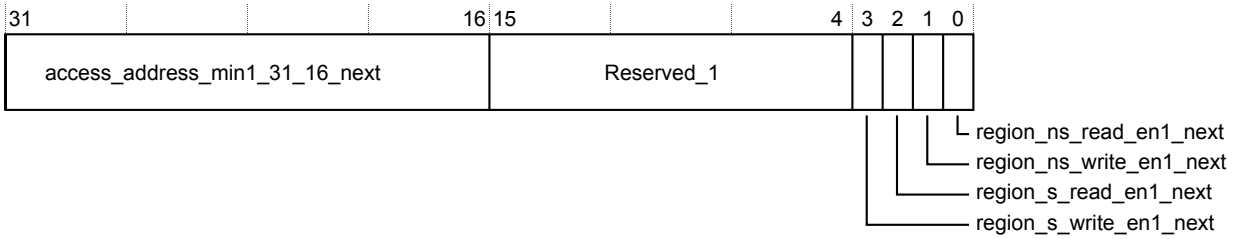

Figure 3-28 access_address_min1_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min1_31_16_next
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en1_next
Enables Secure writes to the region
[2] region_s_read_en1_next
Enables Secure reads to the region
[1] region_ns_write_en1_next
Enables Non-secure writes to the region
[0] region_ns_read_en1_next
Enables Non-secure reads to the region

3.3.29 access_address_min1_43_32_next

This register configures the address space control for address region 1.

The access_address_min1_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x094
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

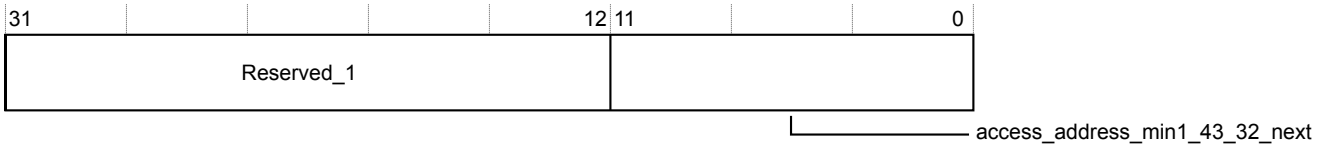

Figure 3-29 access_address_min1_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_min1_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.30 access_address_max1_31_00_next

This register configures the address space control for address region 1.

The access_address_max1_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x098`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

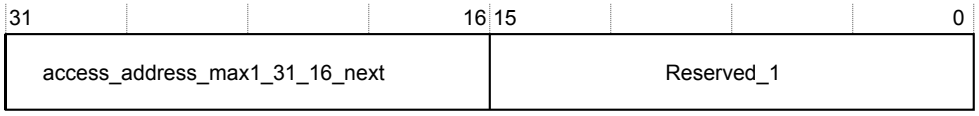

Figure 3-30 access_address_max1_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max1_31_16_next
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.31 access_address_max1_43_32_next

This register configures the address space control for address region 1.

The access_address_max1_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x09C`
Type	Read-write
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

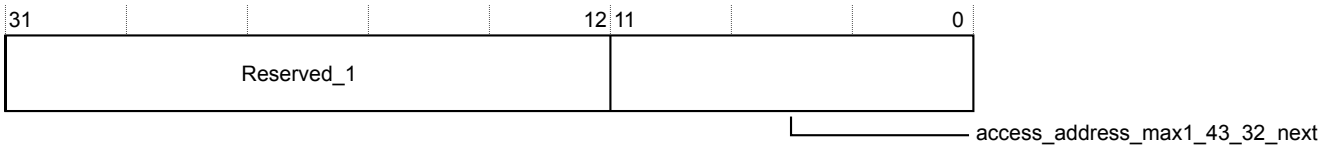

Figure 3-31 access_address_max1_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max1_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.32 access_address_min2_31_00_next

This register configures the address space control for address region 2.

The access_address_min2_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x0A0`

Type Read-write

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

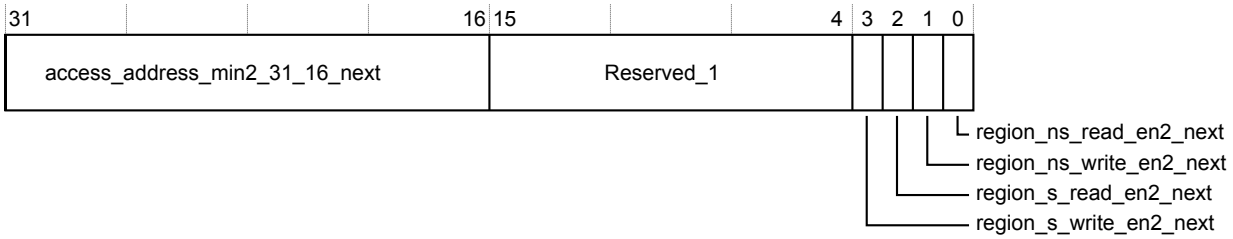

Figure 3-32 access_address_min2_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min2_31_16_next
Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1
Unused bits

[3] region_s_write_en2_next
Enables Secure writes to the region

[2] region_s_read_en2_next
Enables Secure reads to the region

[1] region_ns_write_en2_next
Enables Non-secure writes to the region

[0] region_ns_read_en2_next
Enables Non-secure reads to the region

3.3.33 access_address_min2_43_32_next

This register configures the address space control for address region 2.

The access_address_min2_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0A4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

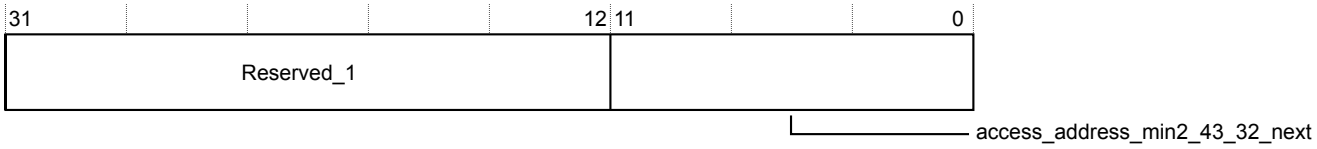

Figure 3-33 access_address_min2_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_min2_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.34 access_address_max2_31_00_next

This register configures the address space control for address region 2.

The access_address_max2_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0A8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

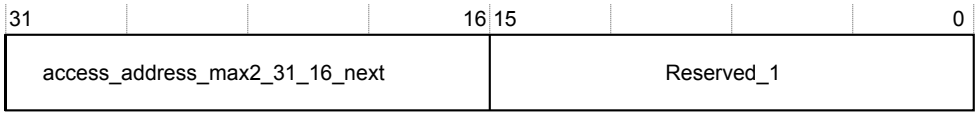

Figure 3-34 access_address_max2_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max2_31_16_next
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.35 access_address_max2_43_32_next

This register configures the address space control for address region 2.

The access_address_max2_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0AC`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

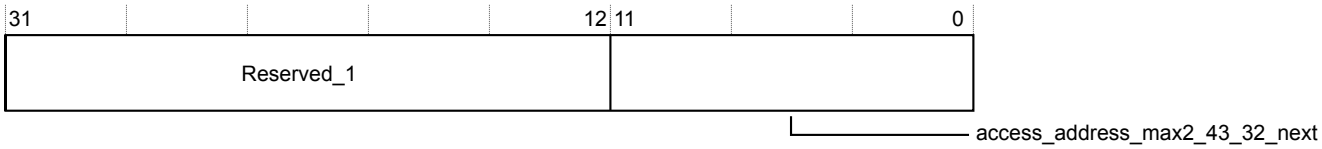

Figure 3-35 access_address_max2_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max2_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.36 access_address_min3_31_00_next

This register configures the address space control for address region 3.

The access_address_min3_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0B0`
Type	Read-write
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

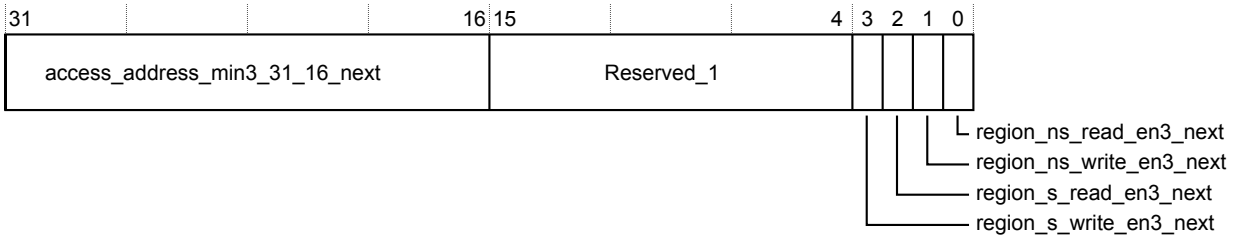

Figure 3-36 access_address_min3_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min3_31_16_next
Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1
Unused bits

[3] region_s_write_en3_next
Enables Secure writes to the region

[2] region_s_read_en3_next
Enables Secure reads to the region

[1] region_ns_write_en3_next
Enables Non-secure writes to the region

[0] region_ns_read_en3_next
Enables Non-secure reads to the region

3.3.37 access_address_min3_43_32_next

This register configures the address space control for address region 3.

The access_address_min3_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x0B4`

Type Read-write

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

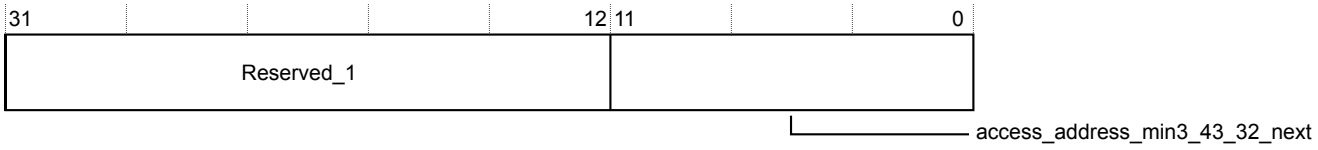

Figure 3-37 access_address_min3_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_min3_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.38 access_address_max3_31_00_next

This register configures the address space control for address region 3.

The access_address_max3_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0B8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

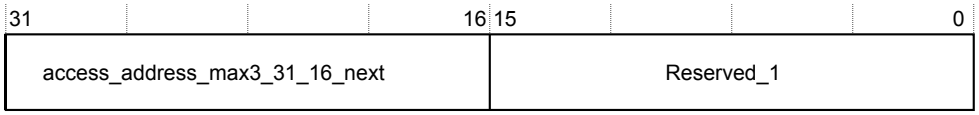

Figure 3-38 access_address_max3_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max3_31_16_next
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.39 access_address_max3_43_32_next

This register configures the address space control for address region 3.

The access_address_max3_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0BC`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

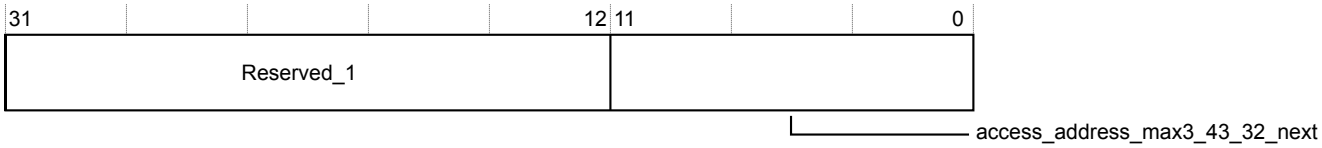

Figure 3-39 access_address_max3_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max3_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.40 access_address_min4_31_00_next

This register configures the address space control for address region 4.

The access_address_min4_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0C0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

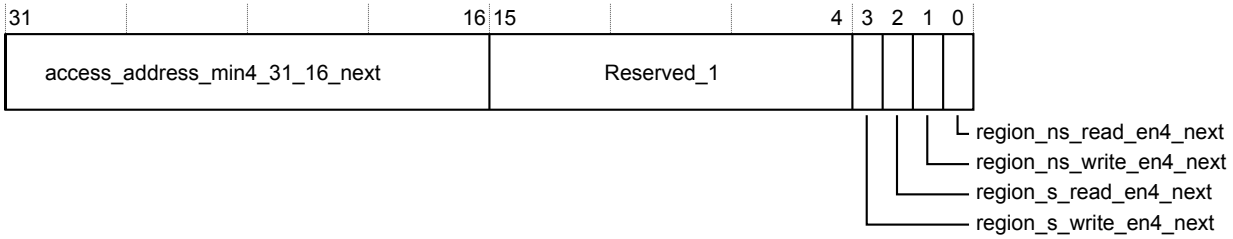

Figure 3-40 access_address_min4_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min4_31_16_next
Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1
Unused bits

[3] region_s_write_en4_next
Enables Secure writes to the region

[2] region_s_read_en4_next
Enables Secure reads to the region

[1] region_ns_write_en4_next
Enables Non-secure writes to the region

[0] region_ns_read_en4_next
Enables Non-secure reads to the region

3.3.41 access_address_min4_43_32_next

This register configures the address space control for address region 4.

The access_address_min4_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0C4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

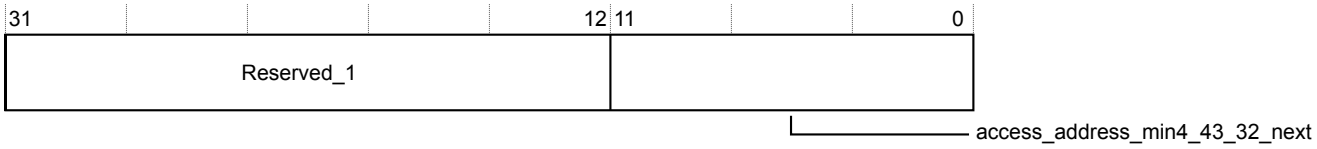

Figure 3-41 access_address_min4_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_min4_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.42 access_address_max4_31_00_next

This register configures the address space control for address region 4.

The access_address_max4_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0C8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

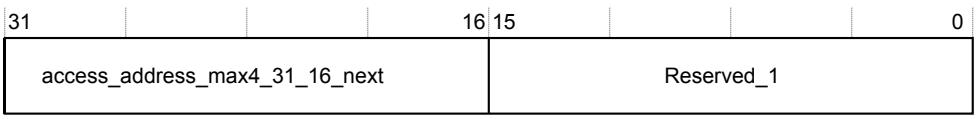

Figure 3-42 access_address_max4_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max4_31_16_next
Program to set bits[31:16] of the maximum address in the region
[15:0] Reserved_1
Unused bits

3.3.43 access_address_max4_43_32_next

This register configures the address space control for address region 4.

The access_address_max4_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x0CC`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

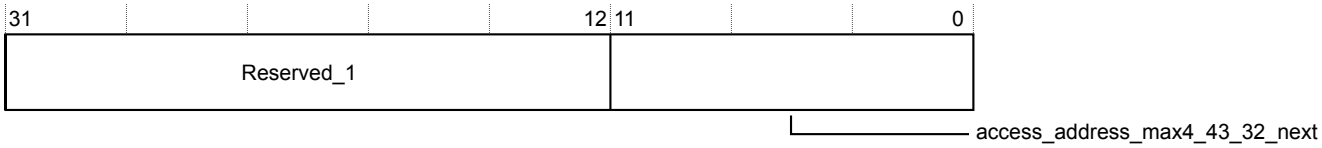

Figure 3-43 access_address_max4_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_max4_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.44 access_address_min5_31_00_next

This register configures the address space control for address region 5.

The access_address_min5_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x0D0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

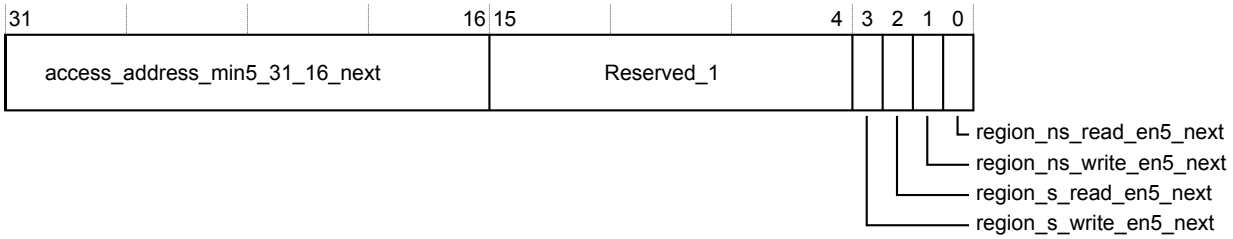

Figure 3-44 access_address_min5_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min5_31_16_next
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en5_next
Enables Secure writes to the region
[2] region_s_read_en5_next
Enables Secure reads to the region
[1] region_ns_write_en5_next
Enables Non-secure writes to the region
[0] region_ns_read_en5_next
Enables Non-secure reads to the region

3.3.45 access_address_min5_43_32_next

This register configures the address space control for address region 5.

The access_address_min5_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x0D4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

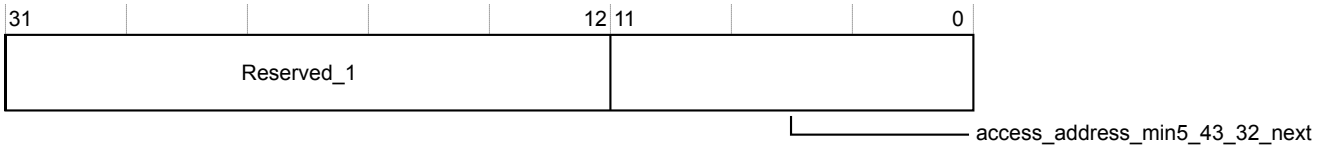

Figure 3-45 access_address_min5_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min5_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.46 access_address_max5_31_00_next

This register configures the address space control for address region 5.

The access_address_max5_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0D8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

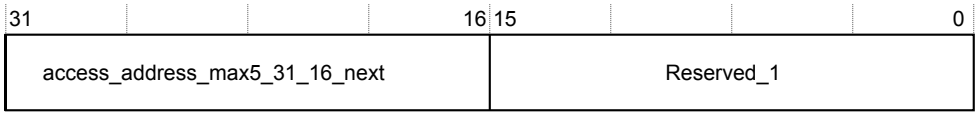

Figure 3-46 access_address_max5_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max5_31_16_next
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.47 access_address_max5_43_32_next

This register configures the address space control for address region 5.

The access_address_max5_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0DC`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

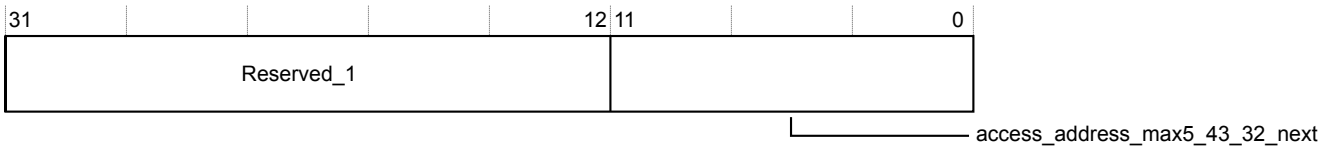

Figure 3-47 access_address_max5_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_max5_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.48 access_address_min6_31_00_next

This register configures the address space control for address region 6.

The access_address_min6_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x0E0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

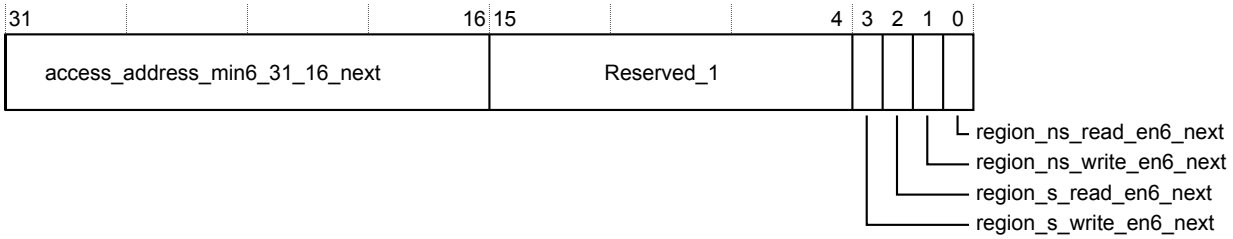

Figure 3-48 access_address_min6_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min6_31_16_next
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en6_next
Enables Secure writes to the region
[2] region_s_read_en6_next
Enables Secure reads to the region
[1] region_ns_write_en6_next
Enables Non-secure writes to the region
[0] region_ns_read_en6_next
Enables Non-secure reads to the region

3.3.49 access_address_min6_43_32_next

This register configures the address space control for address region 6.

The access_address_min6_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x0E4
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

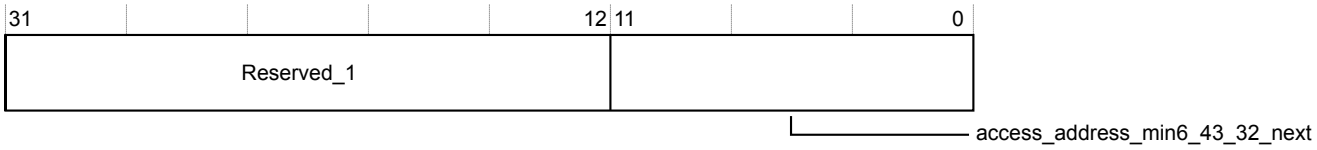

Figure 3-49 access_address_min6_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min6_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.50 access_address_max6_31_00_next

This register configures the address space control for address region 6.

The access_address_max6_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x0E8
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

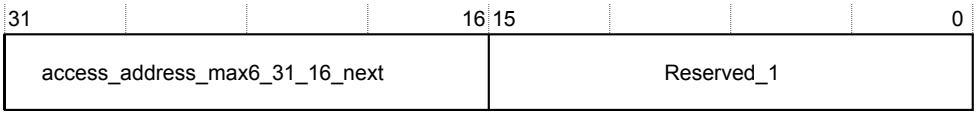

Figure 3-50 access_address_max6_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max6_31_16_next
Program to set bits[31:16] of the maximum address in the region
[15:0] Reserved_1
Unused bits

3.3.51 access_address_max6_43_32_next

This register configures the address space control for address region 6.

The access_address_max6_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x0EC
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

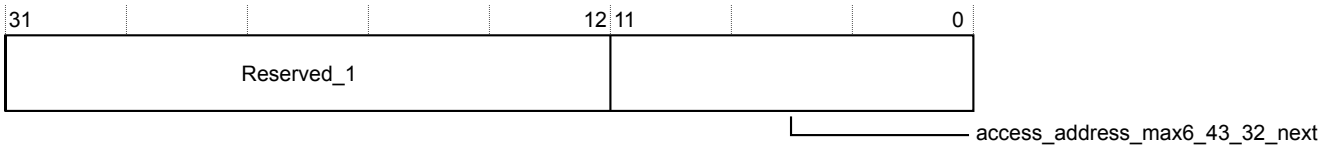

Figure 3-51 access_address_max6_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max6_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.52 access_address_min7_31_00_next

This register configures the address space control for address region 7.

The access_address_min7_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x0F0
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

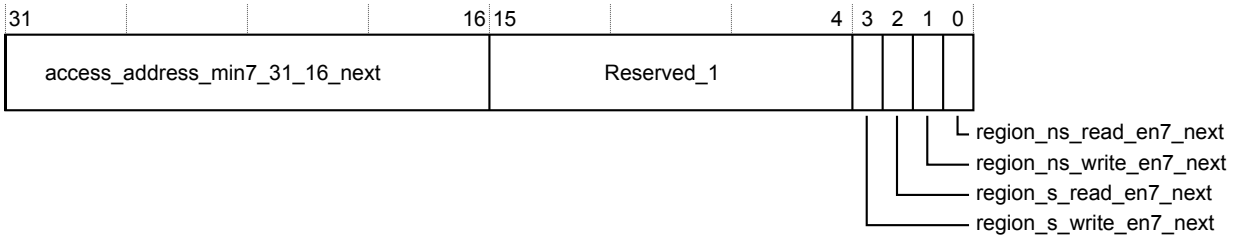

Figure 3-52 access_address_min7_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_min7_31_16_next
Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1
Unused bits
[3] region_s_write_en7_next
Enables Secure writes to the region
[2] region_s_read_en7_next
Enables Secure reads to the region
[1] region_ns_write_en7_next
Enables Non-secure writes to the region
[0] region_ns_read_en7_next
Enables Non-secure reads to the region

3.3.53 access_address_min7_43_32_next

This register configures the address space control for address region 7.

The access_address_min7_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x0F4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

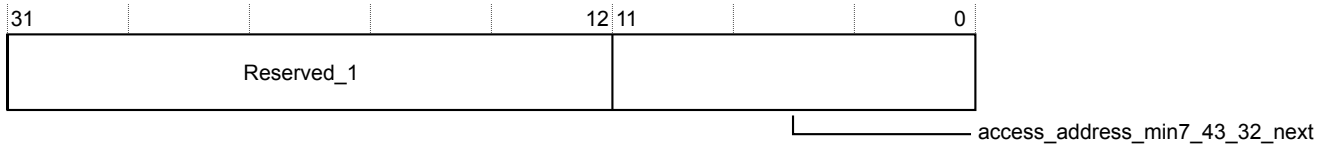

Figure 3-53 access_address_min7_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min7_43_32_next
Program to set bits[43:32] of the minimum address in the region

3.3.54 access_address_max7_31_00_next

This register configures the address space control for address region 7.

The access_address_max7_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x0F8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

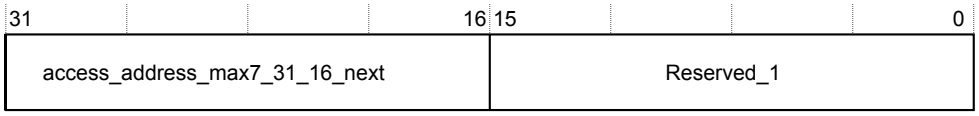

Figure 3-54 access_address_max7_31_00_next register bit assignments

The following shows the bit assignments.

[31:16] access_address_max7_31_16_next
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.55 access_address_max7_43_32_next

This register configures the address space control for the address region 7.

The access_address_max7_43_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x0FC`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

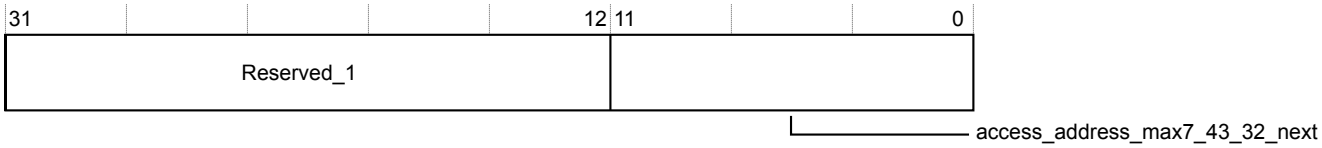

Figure 3-55 access_address_max7_43_32_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max7_43_32_next
Program to set bits[43:32] of the maximum address in the region

3.3.56 channel_status

This register holds the current status of the memory channel.

The channel_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x100`

Type Read-only
Reset 0x00000003
Width 32

The following figure shows the bit assignments.

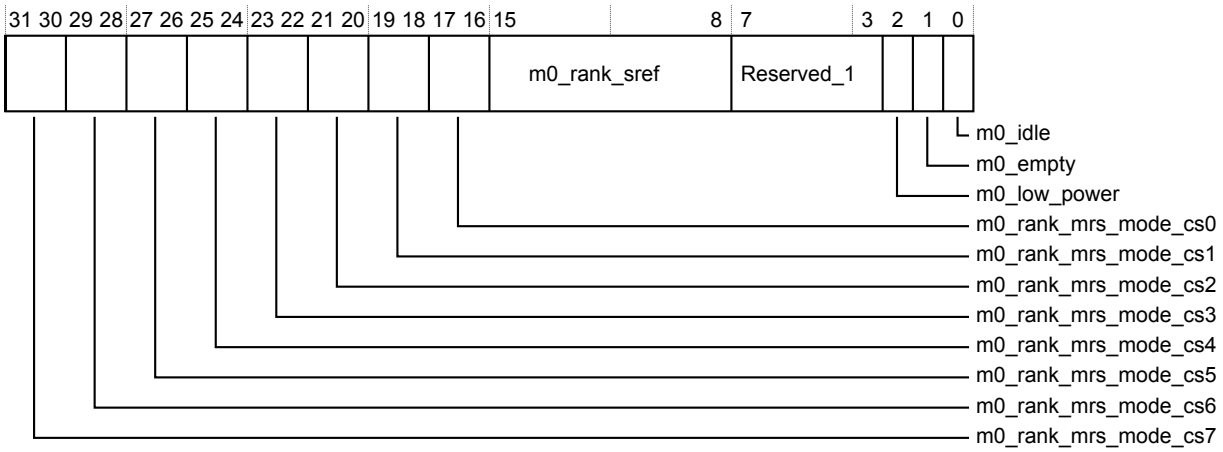

Figure 3-56 channel_status register bit assignments

The following shows the bit assignments.

[31:30] m0_rank_mrs_mode_cs7
m0_rank_mrs_mode_cs7 bitfield.
[29:28] m0_rank_mrs_mode_cs6
m0_rank_mrs_mode_cs6 bitfield.
[27:26] m0_rank_mrs_mode_cs5
m0_rank_mrs_mode_cs5 bitfield.
[25:24] m0_rank_mrs_mode_cs4
m0_rank_mrs_mode_cs4 bitfield.
[23:22] m0_rank_mrs_mode_cs3
m0_rank_mrs_mode_cs3 bitfield.
[21:20] m0_rank_mrs_mode_cs2
m0_rank_mrs_mode_cs2 bitfield.
[19:18] m0_rank_mrs_mode_cs1
m0_rank_mrs_mode_cs1 bitfield.
[17:16] m0_rank_mrs_mode_cs0
Holds state information for this rank.
[15:8] m0_rank_sref
One-bit per rank indicating that the rank does not require the DMC to issue AUTOREFRESH commands
[7:3] Reserved_1
Unused bits
[2] m0_low_power
Indicates if all the DRAM ranks on this channel are in a state not requiring AUTOREFRESH commands
[1] m0_empty
Indicates if the interface is empty, that is, there are no outstanding requests. Note that this value might go non-empty at any time when in the READY state.
[0] m0_idle
Indicates if the interface is idle, that is, there are no outstanding requests and no outstanding activity, including delays, associated with previous commands. Note that this value might go non-idle at any time when in the READY state.

3.3.57 direct_addr

This register sets the direct command address field for direct commands.

The direct_addr register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x108`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

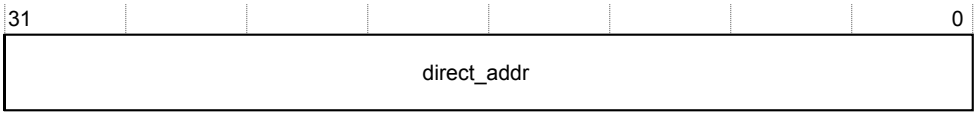

Figure 3-57 direct_addr register bit assignments

The following shows the bit assignments.

[31:0] direct_addr
For more information see direct_cmd command descriptions.

3.3.58 direct_cmd

This register generates direct commands from the manager.

The direct_cmd register characteristics are:

Usage constraints
Cannot be read from. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x10C`
Type	Write-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

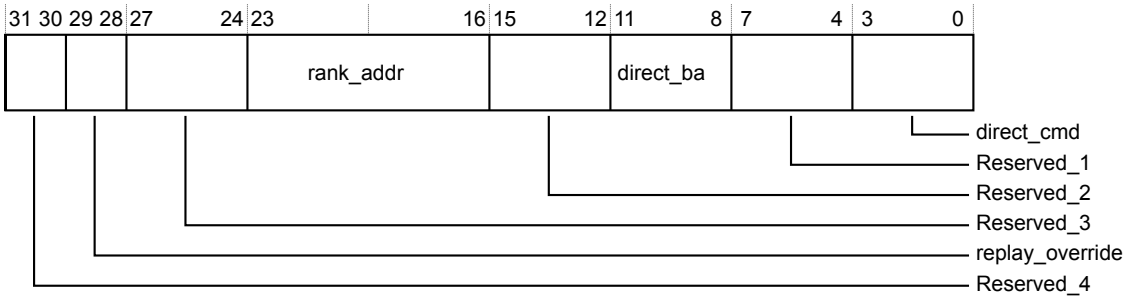

Figure 3-58 direct_cmd register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4
Unused bits

[29:28] replay_override
Defines the replay behavior for this particular command.

[27:24] Reserved_3
Unused bits

[23:16] rank_addr
Determines the target rank, each bit corresponding to a rank. If multiple ranks are selected then the command is sent to each rank in turn.

[15:12] Reserved_2
Unused bits

[11:8] direct_ba
Determines the value to be driven on the external bank group and bank address pins. For MRS commands, it is the mode register number. For all other commands, bank group (if programmed) is taken from the least significant bits, bank address is taken from the bits directly above the bank group bits.

[7:4] Reserved_1
Unused bits

[3:0] direct_cmd
Determines the command to be performed.

3.3.59 dci_replay_type_next

This register configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command.

The dci_replay_type_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x110`
Type	Read-write
Reset	`0x00000002`
Width	32

The following figure shows the bit assignments.

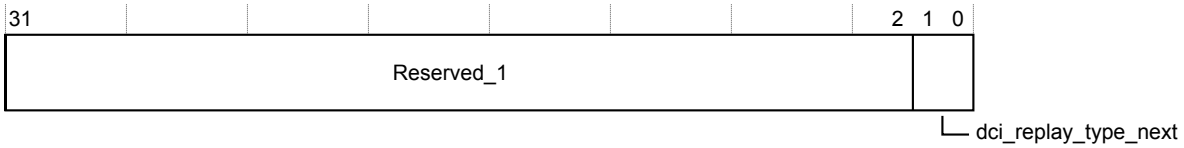

Figure 3-59 dci_replay_type_next register bit assignments

The following shows the bit assignments.

[31:2] Reserved_1
Unused bits

[1:0] dci_replay_type_next
dci_replay_type_next bitfield.

3.3.60 dci_strb

This register configures the write data strobe values used during direct_cmd WRITE operations.

The dci_strb register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x118`
Type	Read-write
Reset	`0x0000000F`
Width	32

The following figure shows the bit assignments.

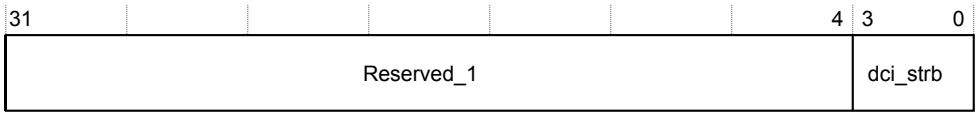

Figure 3-60 dci_strb register bit assignments

The following shows the bit assignments.

[31:4] Reserved_1
Unused bits

[3:0] dci_strb
For write operations, provides the value used to drive DQM, where a value of 1 indicates data must be committed to DRAM. You must write once for each 32-bit data word to write as part of a DRAM burst. Defaults to 4'b1111.

3.3.61 dci_data

Reading from this register location returns read data received as a result of a READ command. Writing to this register location sets the data to be used for direct_cmd WRITE commands. You must read or write once for each 32-bit data word of a DRAM burst.

The dci_data register characteristics are:

Usage constraints
Can be read from when in CONFIG, PAUSED or READY states. Can be written to when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x11C
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

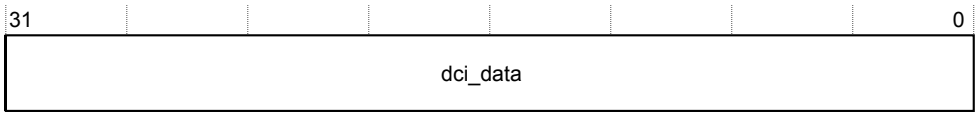

Figure 3-61 dci_data register bit assignments

The following shows the bit assignments.

[31:0] dci_data
dci_data bitfield.

3.3.62 refresh_control_next

This register configures the type of refresh commands issued by the DMC.

The refresh_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x120
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

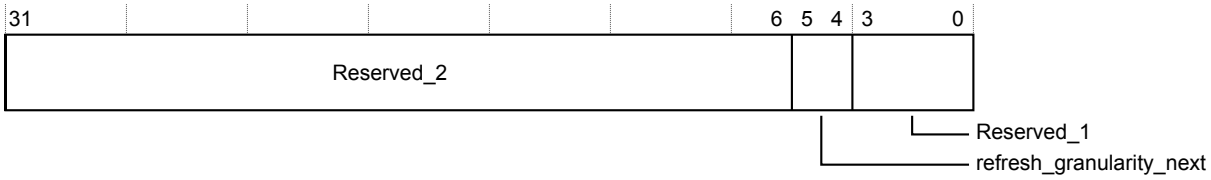

Figure 3-62 refresh_control_next register bit assignments

The following shows the bit assignments.

[31:6] Reserved_2
Unused bits

[5:4] refresh_granularity_next
Configures the refresh rate mode of the DMC. You must program this to match the mode of the DRAM. All DRAMs requiring refresh must use the same refresh rate.

[3:0] Reserved_1
Unused bits

3.3.63 memory_type_next

This register configures the DMC for the attached memory type.

The memory_type_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x128`
Type	Read-write
Reset	`0x00000101`
Width	32

The following figure shows the bit assignments.

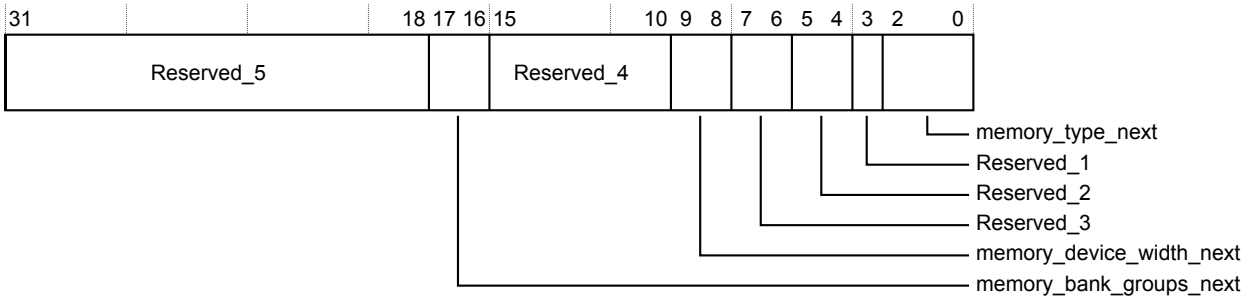

Figure 3-63 memory_type_next register bit assignments

The following shows the bit assignments.

[31:18] Reserved_5
Unused bits

[17:16] memory_bank_groups_next
Program to configure the number of bank groups in the attached memory device

[15:10] Reserved_4
Unused bits

[9:8] memory_device_width_next
Program to configure the device widths.

[7:6] Reserved_3
Unused bits

[5:4] Reserved_2
Unused bits

[3] Reserved_1
Unused bits

[2:0] memory_type_next
Program to configure the attached memory type

3.3.64 feature_config

This register controls DMC features.

The feature_config register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x130`
Type	Read-write
Reset	`0x000000F0`
Width	32

The following figure shows the bit assignments.

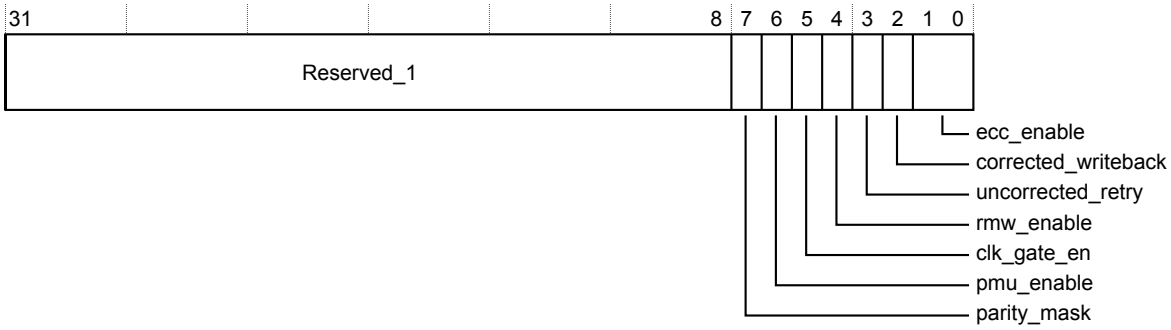

Figure 3-64 feature_config register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7] parity_mask
Program to include a[17] in parity calculation.

[6] pmu_enable
Enable performance monitoring unit outputs.

[5] clk_gate_en
Enable clock gating for DMC.

[4] rmw_enable
Enable read-modify-write operations. Must be enabled if Write DBI or ECC is enabled.

[3] uncorrected_retry
Program to enable or disable retry of ECC-uncorrectable data operations.

[2] corrected_writeback
Program to enable or disable write-back of ECC-corrected data.

[1:0] ecc_enable
Program to enable or disable ECC functionality.

3.3.65 nibble_failed_031_000

This register informs the DMC that a particular nibble has failed.

The nibble_failed_031_000 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x138`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

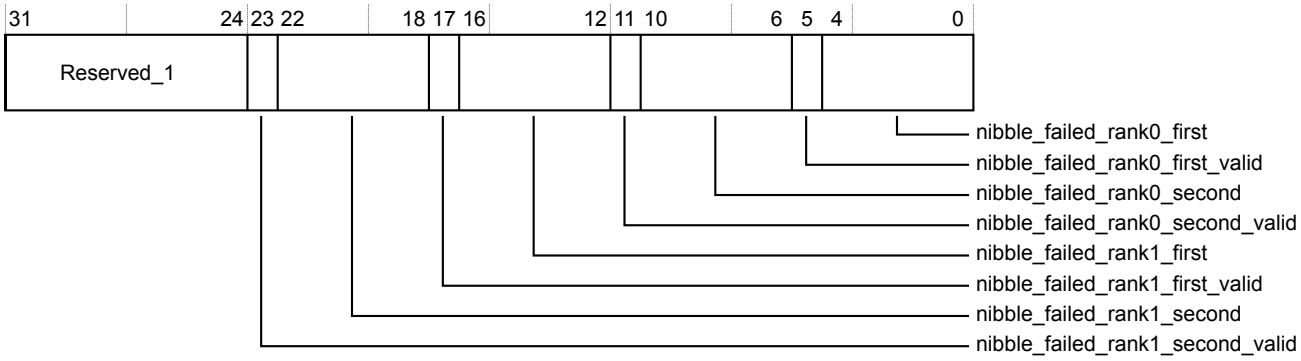

Figure 3-65 nibble_failed_031_000 register bit assignments

The following shows the bit assignments.

[31:24] Reserved_1
Unused bits

[23] nibble_failed_rank1_second_valid
Indicates if the second location is valid.

[22:18] nibble_failed_rank1_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[17] nibble_failed_rank1_first_valid
Indicates if the first location is valid.

[16:12] nibble_failed_rank1_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

[11] nibble_failed_rank0_second_valid
Indicates if the second location is valid.

[10:6] nibble_failed_rank0_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[5] nibble_failed_rank0_first_valid
Indicates if the first location is valid.

[4:0] nibble_failed_rank0_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

3.3.66 nibble_failed_063_032

This register informs the DMC that a particular nibble has failed.

The nibble_failed_063_032 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x13C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

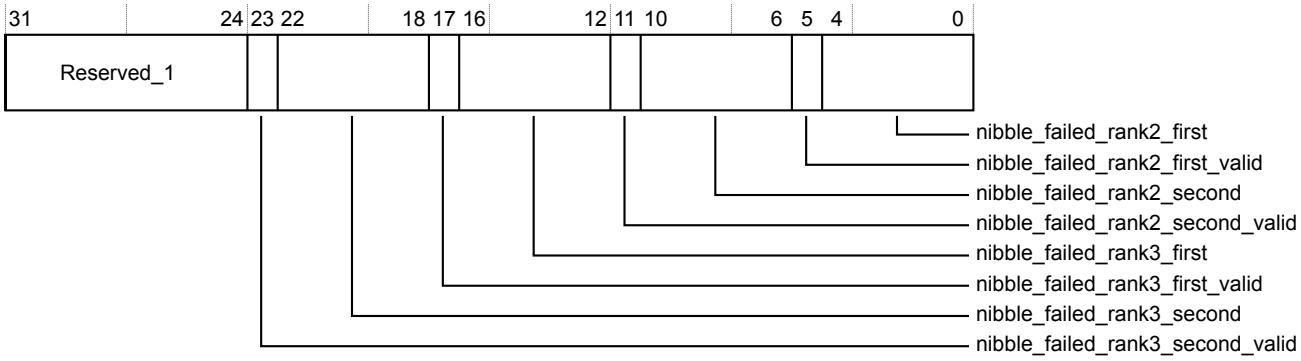

Figure 3-66 nibble_failed_063_032 register bit assignments

The following shows the bit assignments.

[31:24] Reserved_1
Unused bits

[23] nibble_failed_rank3_second_valid
Indicates if the second location is valid.

[22:18] nibble_failed_rank3_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[17] nibble_failed_rank3_first_valid
Indicates if the first location is valid.

[16:12] nibble_failed_rank3_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

[11] nibble_failed_rank2_second_valid
Indicates if the second location is valid.

[10:6] nibble_failed_rank2_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[5] nibble_failed_rank2_first_valid
Indicates if the first location is valid.

[4:0] nibble_failed_rank2_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

3.3.67 nibble_failed_095_064

This register informs the DMC that a particular nibble has failed.

The nibble_failed_095_064 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x140`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

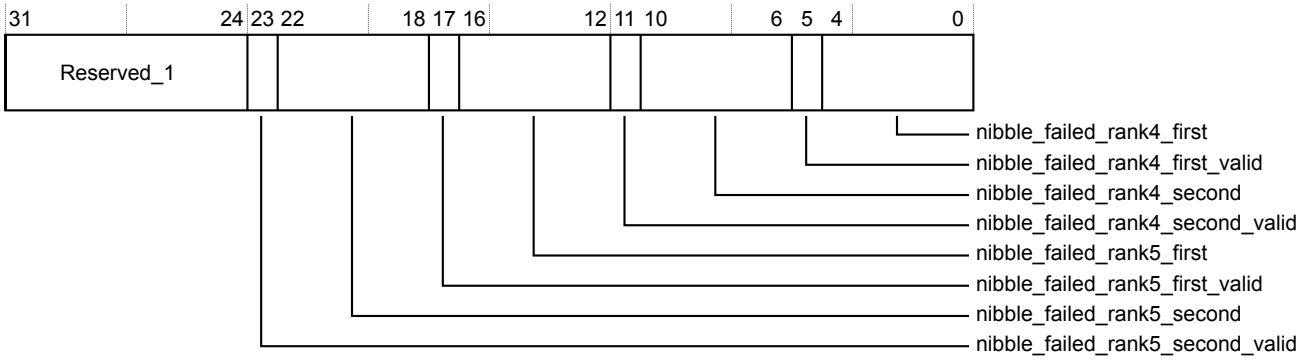

Figure 3-67 nibble_failed_095_064 register bit assignments

The following shows the bit assignments.

[31:24] Reserved_1
Unused bits

[23] nibble_failed_rank5_second_valid
Indicates if the second location is valid.

[22:18] nibble_failed_rank5_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[17] nibble_failed_rank5_first_valid
Indicates if the first location is valid.

[16:12] nibble_failed_rank5_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

[11] nibble_failed_rank4_second_valid
Indicates if the second location is valid.

[10:6] nibble_failed_rank4_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[5] nibble_failed_rank4_first_valid
Indicates if the first location is valid.

[4:0] nibble_failed_rank4_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

3.3.68 nibble_failed_127_096

Used to inform the DMC that a particular nibble has failed.

The nibble_failed_127_096 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x144`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

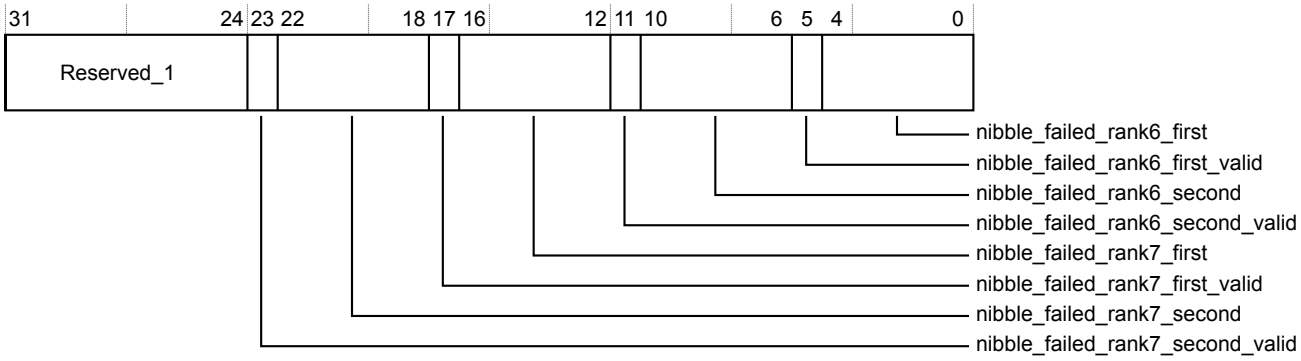

Figure 3-68 nibble_failed_127_096 register bit assignments

The following shows the bit assignments.

[31:24] Reserved_1
Unused bits

[23] nibble_failed_rank7_second_valid
Indicates if the second location is valid.

[22:18] nibble_failed_rank7_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[17] nibble_failed_rank7_first_valid
Indicates if the first location is valid.

[16:12] nibble_failed_rank7_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

[11] nibble_failed_rank6_second_valid
Indicates if the second location is valid.

[10:6] nibble_failed_rank6_second
Used to inform the DMC of the second location that has failed. The supported range for this bitfield is 0-17.

[5] nibble_failed_rank6_first_valid
Indicates if the first location is valid.

[4:0] nibble_failed_rank6_first
Used to inform the DMC of the first location that has failed. The supported range for this bitfield is 0-17.

3.3.69 queue_allocate_control_031_000

Used to inform the DMC that a particular queue (RAM) entry has failed, where 0 means failed and not included for allocation.

The queue_allocate_control_031_000 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x148`
Type	Read-write
Reset	`0xFFFFFFFF`
Width	32

The following figure shows the bit assignments.

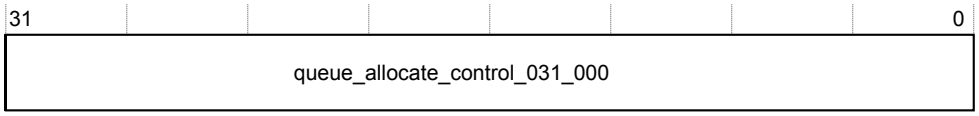

Figure 3-69 queue_allocate_control_031_000 register bit assignments

The following shows the bit assignments.

[31:0] queue_allocate_control_031_000
Used to inform the DMC that a particular queue (RAM) entry has failed, where 0 means failed and not included for allocation.

3.3.70 queue_allocate_control_063_032

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations.

The queue_allocate_control_063_032 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x14C`
Type	Read-write
Reset	`0xFFFFFFFF`
Width	32

The following figure shows the bit assignments.

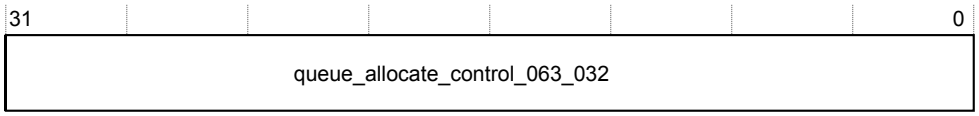

Figure 3-70 queue_allocate_control_063_032 register bit assignments

The following shows the bit assignments.

[31:0] queue_allocate_control_063_032
queue_allocate_control_063_032 bitfield.

3.3.71 queue_allocate_control_095_064

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations.

The queue_allocate_control_095_064 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x150`
Type	Read-write
Reset	`0xFFFFFFFF`
Width	32

The following figure shows the bit assignments.

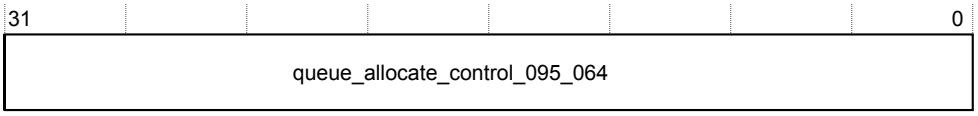

Figure 3-71 queue_allocate_control_095_064 register bit assignments

The following shows the bit assignments.

[31:0] queue_allocate_control_095_064
queue_allocate_control_095_064 bitfield.

3.3.72 queue_allocate_control_127_096

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations.

The queue_allocate_control_127_096 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x154`
Type	Read-write
Reset	`0xFFFFFFFF`
Width	32

The following figure shows the bit assignments.

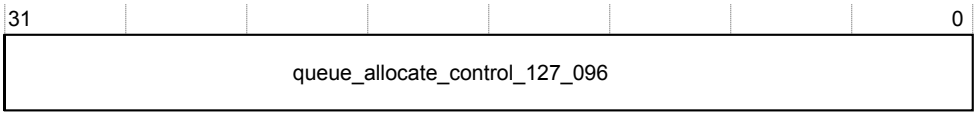

Figure 3-72 queue_allocate_control_127_096 register bit assignments

The following shows the bit assignments.

[31:0] queue_allocate_control_127_096
queue_allocate_control_127_096 bitfield.

3.3.73 ecc_errc_count_31_00

Counter register for the DRAM ECC functionality.

The ecc_errc_count_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x158`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

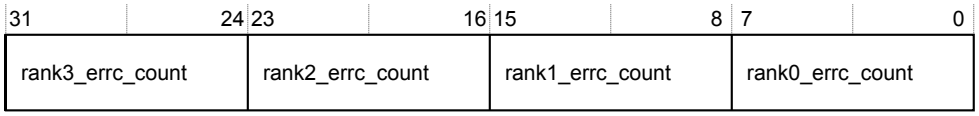

Figure 3-73 ecc_errc_count_31_00 register bit assignments

The following shows the bit assignments.

[31:24] rank3_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.
[23:16] rank2_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.
[15:8] rank1_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.
[7:0] rank0_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.

3.3.74 ecc_errc_count_63_32

Counter register for the DRAM ECC functionality.

The ecc_errc_count_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x15C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

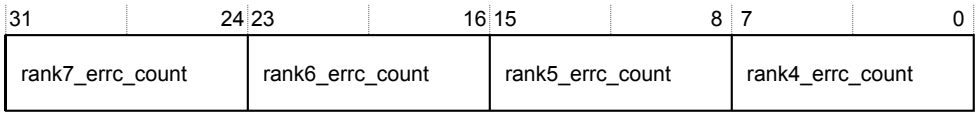

Figure 3-74 ecc_errc_count_63_32 register bit assignments

The following shows the bit assignments.

[31:24] rank7_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.
[23:16] rank6_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.
[15:8] rank5_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.
[7:0] rank4_errc_count
Corrected error count. A write to the bitfield resets the counter to the written value.

3.3.75 ecc_errd_count_31_00

Counter register for the DRAM ECC functionality.

The ecc_errd_count_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x160

Type Read-write

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

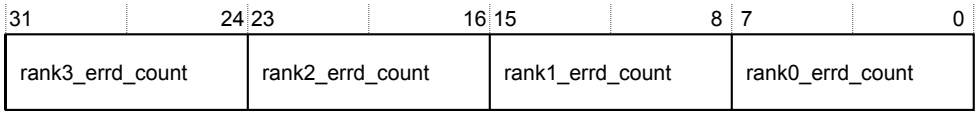

Figure 3-75 ecc_errd_count_31_00 register bit assignments

The following shows the bit assignments.

[31:24] rank3_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

[23:16] rank2_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

[15:8] rank1_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

[7:0] rank0_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

3.3.76 ecc_errd_count_63_32

Counter register for the DRAM ECC functionality.

The ecc_errd_count_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x164

Type Read-write

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

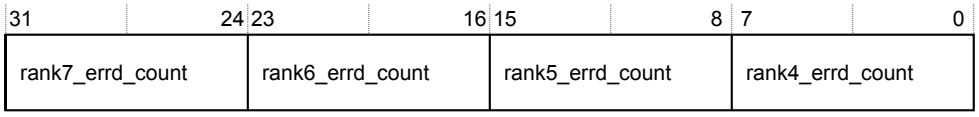

Figure 3-76 ecc_errd_count_63_32 register bit assignments

The following shows the bit assignments.

[31:24] rank7_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

[23:16] rank6_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

[15:8] rank5_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

[7:0] rank4_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

3.3.77 ram_err_count

Counter register for the RAM ECC functionality.

The ram_err_count register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x168`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

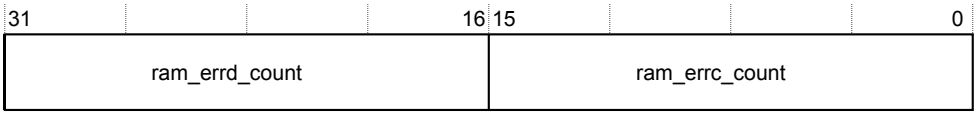

Figure 3-77 ram_err_count register bit assignments

The following shows the bit assignments.

[31:16] ram_errd_count
Uncorrected error count. A write to the bitfield resets the counter to the written value.

[15:0] ram_errc_count
Corrected error count. A write to this bitfield resets the counter to the written value.

3.3.78 link_err_count

Counter register for link errors. The counter increments on detection of a new link error (dfi_alert_n or dfi_err).

The link_err_count register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x16C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

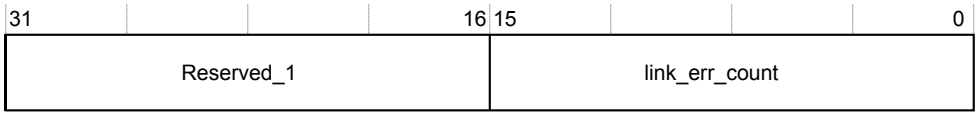

Figure 3-78 link_err_count register bit assignments

The following shows the bit assignments.

[31:16] Reserved_1
Unused bits

[15:0] link_err_count
Link error count. A write to this bitfield resets the counter to the written value.

3.3.79 scrub_control0_next

Scrub engine channel control register.

The scrub_control0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x170`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

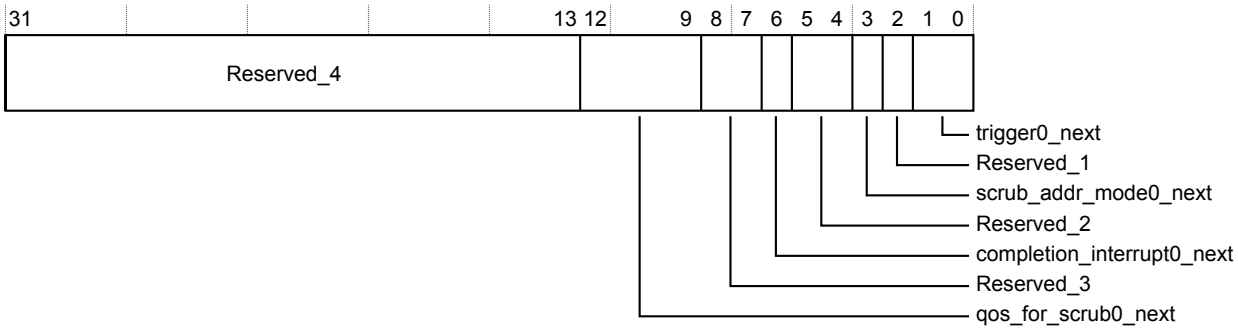

Figure 3-79 scrub_control0_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub0_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt0_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode0_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger0_next
Controls the trigger event associated with the channel operation.

3.3.80 scrub_address_min0_next

Configures the address space control for the scrub engine channel.

The scrub_address_min0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x174`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

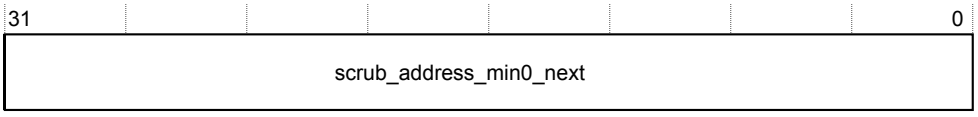

Figure 3-80 scrub_address_min0_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min0_next
Program to set the starting address for the scrub engine. When scrub_addr_mode0 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode0 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.81 scrub_address_max0_next

Configures the address space control for the scrub engine channel.

The scrub_address_max0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x178`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

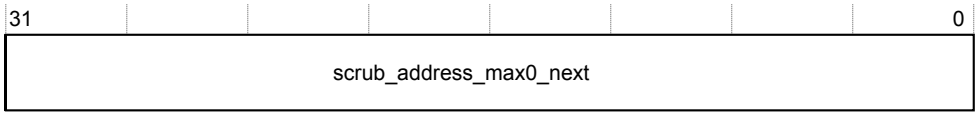

Figure 3-81 scrub_address_max0_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max0_next
Program to set the ending address for the scrub engine. When scrub_addr_mode0 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode0 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.82 scrub_control1_next

Scrub engine channel control register.

The scrub_control1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x180`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

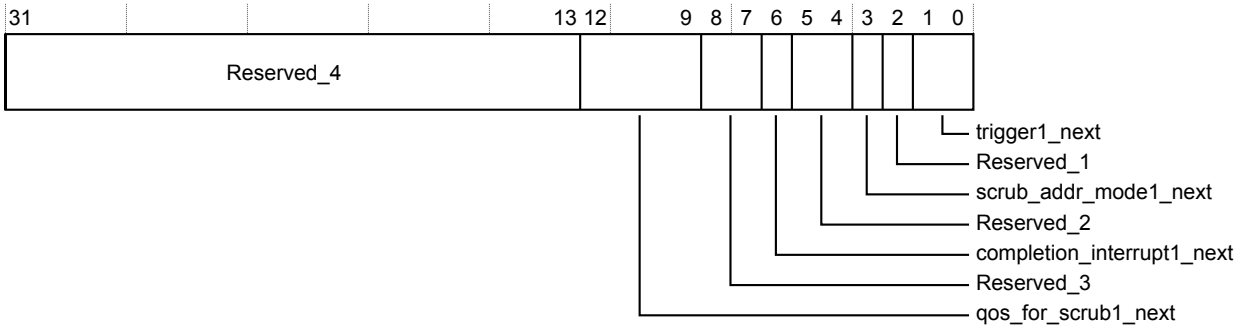

Figure 3-82 scrub_control1_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub1_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt1_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode1_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger1_next
Controls the trigger event associated with the channel operation.

3.3.83 scrub_address_min1_next

Configures the address space control for the scrub engine channel.

The scrub_address_min1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x184`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

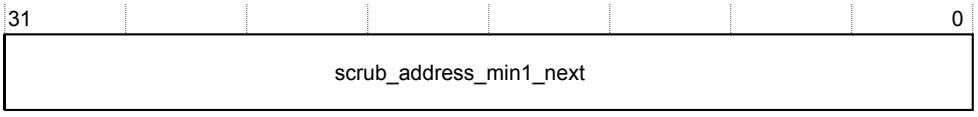

Figure 3-83 scrub_address_min1_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min1_next
Program to set the starting address for the scrub engine. When scrub_addr_mode1 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode1 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.84 scrub_address_max1_next

Configures the address space control for the scrub engine channel.

The scrub_address_max1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x188`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

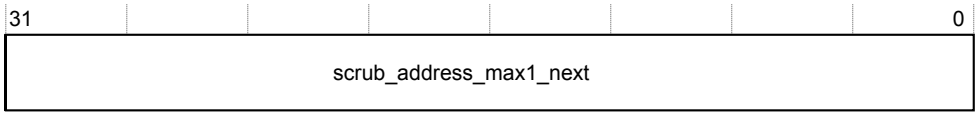

Figure 3-84 scrub_address_max1_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max1_next
Program to set the ending address for the scrub engine. When scrub_addr_mode1 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode1 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.85 scrub_control2_next

Scrub engine channel control register.

The scrub_control2_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x190`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

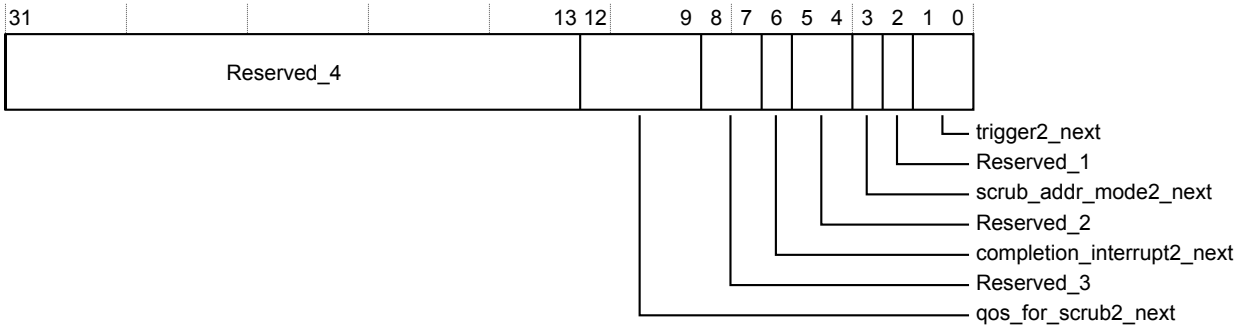

Figure 3-85 scrub_control2_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub2_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt2_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode2_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger2_next
Controls the trigger event associated with the channel operation.

3.3.86 scrub_address_min2_next

Configures the address space control for the scrub engine channel.

The scrub_address_min2_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x194`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

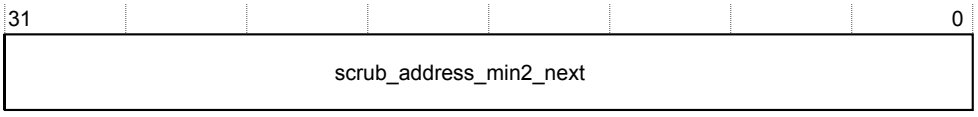

Figure 3-86 scrub_address_min2_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min2_next
Program to set the starting address for the scrub engine. When scrub_addr_mode2 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode2 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.87 scrub_address_max2_next

Configures the address space control for the scrub engine channel.

The scrub_address_max2_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x198`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

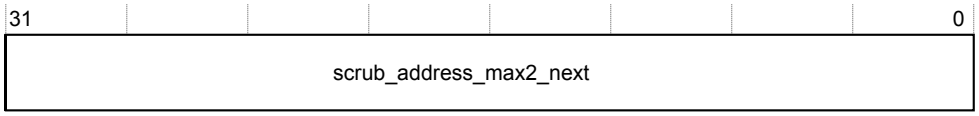

Figure 3-87 scrub_address_max2_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max2_next
Program to set the ending address for the scrub engine. When scrub_addr_mode2 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode2 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.88 scrub_control3_next

Scrub engine channel control register.

The scrub_control3_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1A0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

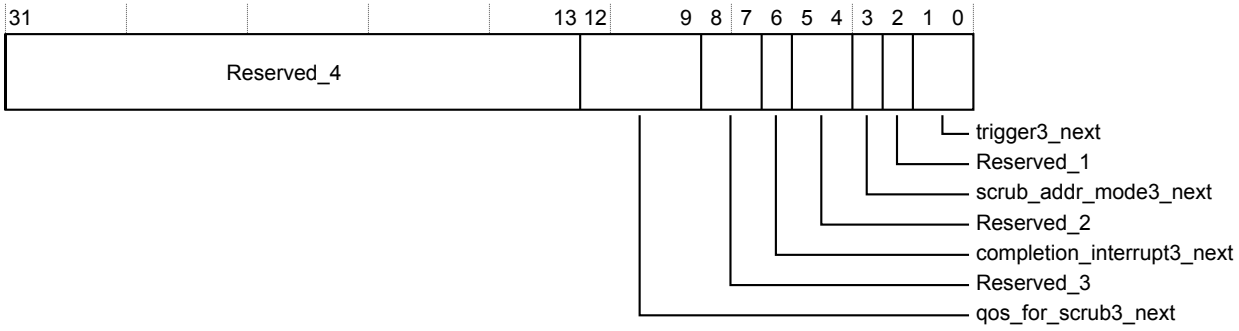

Figure 3-88 scrub_control3_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub3_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt3_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode3_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger3_next
Controls the trigger event associated with the channel operation.

3.3.89 scrub_address_min3_next

Configures the address space control for the scrub engine channel.

The scrub_address_min3_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1A4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

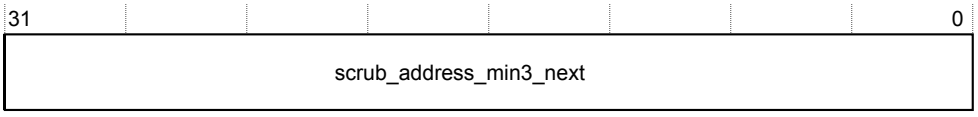

Figure 3-89 scrub_address_min3_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min3_next
Program to set the starting address for the scrub engine. When scrub_addr_mode3 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode3 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.90 scrub_address_max3_next

Configures the address space control for the scrub engine channel.

The scrub_address_max3_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1A8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

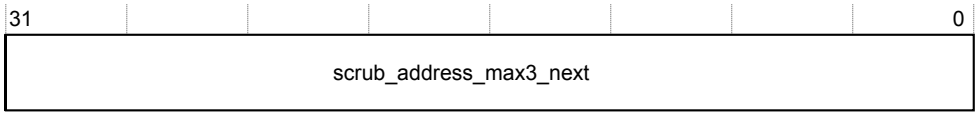

Figure 3-90 scrub_address_max3_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max3_next
Program to set the ending address for the scrub engine. When scrub_addr_mode3 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode3 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.91 scrub_control4_next

Scrub engine channel control register.

The scrub_control4_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1B0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

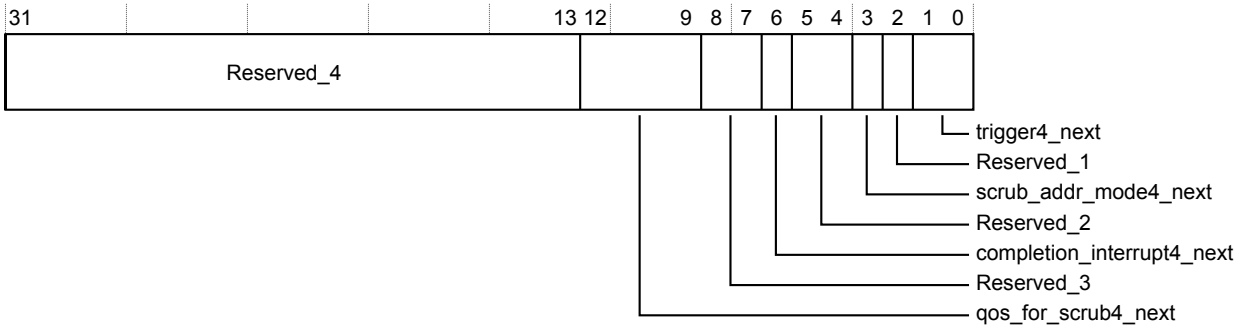

Figure 3-91 scrub_control4_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub4_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt4_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode4_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger4_next
Controls the trigger event associated with the channel operation.

3.3.92 scrub_address_min4_next

Configures the address space control for the scrub engine channel.

The scrub_address_min4_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1B4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

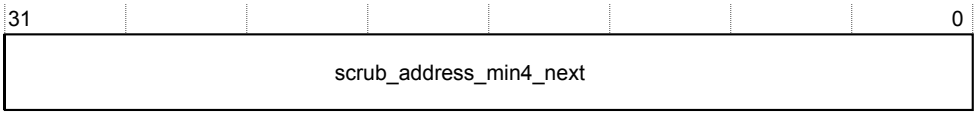

Figure 3-92 scrub_address_min4_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min4_next
Program to set the starting address for the scrub engine. When scrub_addr_mode4 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode4 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.93 scrub_address_max4_next

Configures the address space control for the scrub engine channel.

The scrub_address_max4_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1B8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

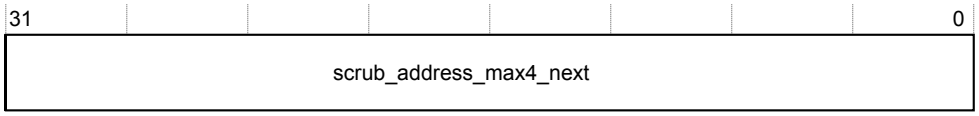

Figure 3-93 scrub_address_max4_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max4_next
Program to set the ending address for the scrub engine. When scrub_addr_mode4 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode4 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.94 scrub_control5_next

Scrub engine channel control register.

The scrub_control5_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1C0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

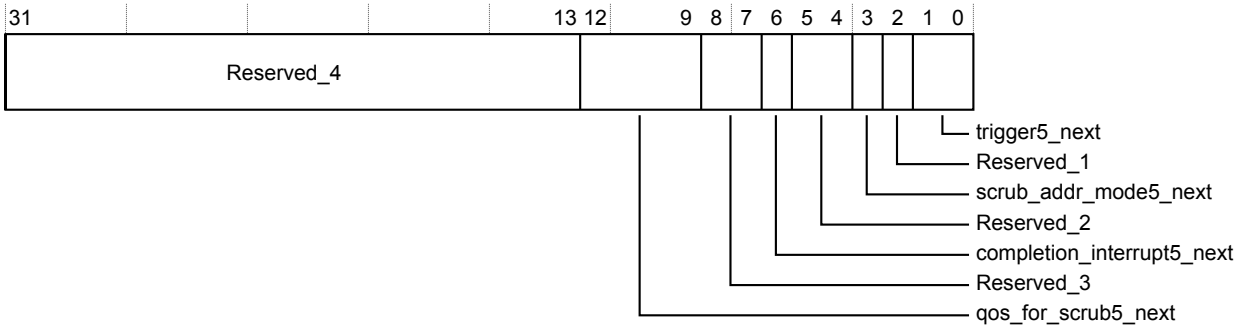

Figure 3-94 scrub_control5_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub5_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt5_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode5_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger5_next
Controls the trigger event associated with the channel operation.

3.3.95 scrub_address_min5_next

Configures the address space control for the scrub engine channel.

The scrub_address_min5_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1C4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

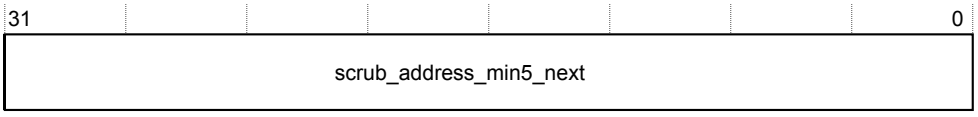

Figure 3-95 scrub_address_min5_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min5_next
Program to set the starting address for the scrub engine. When scrub_addr_mode5 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode5 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.96 scrub_address_max5_next

Configures the address space control for the scrub engine channel.

The scrub_address_max5_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1C8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

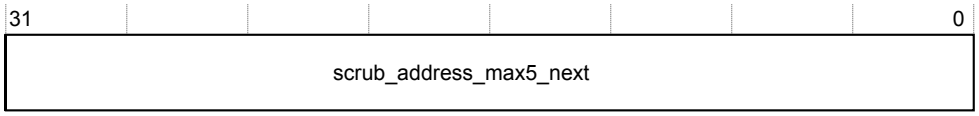

Figure 3-96 scrub_address_max5_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max5_next
Program to set the ending address for the scrub engine. When scrub_addr_mode5 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode5 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.97 scrub_control6_next

Scrub engine channel control register.

The scrub_control6_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1D0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

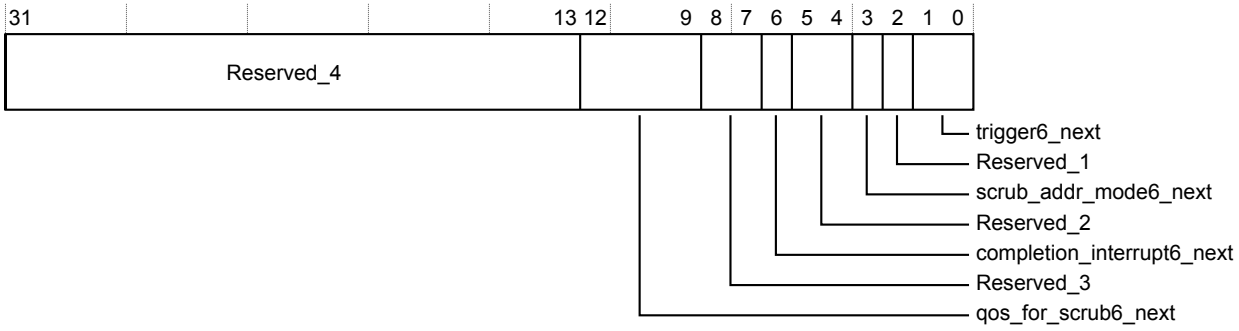

Figure 3-97 scrub_control6_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub6_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt6_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode6_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger6_next
Controls the trigger event associated with the channel operation.

3.3.98 scrub_address_min6_next

Configures the address space control for the scrub engine channel.

The scrub_address_min6_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1D4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

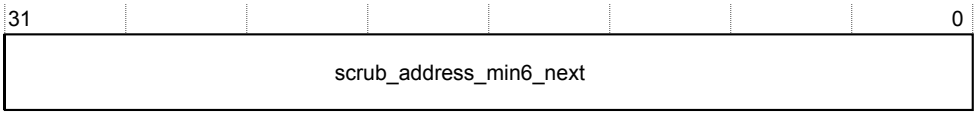

Figure 3-98 scrub_address_min6_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min6_next
Program to set the starting address for the scrub engine. When scrub_addr_mode6 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode6 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.99 scrub_address_max6_next

Configures the address space control for the scrub engine channel.

The scrub_address_max6_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1D8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

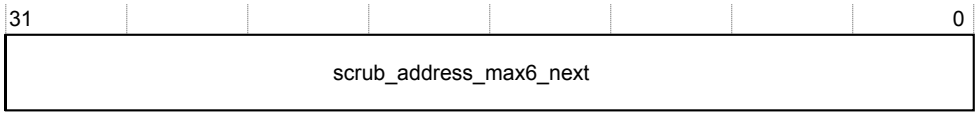

Figure 3-99 scrub_address_max6_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max6_next
Program to set the ending address for the scrub engine. When scrub_addr_mode6 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode6 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.100 scrub_control7_next

Scrub engine channel control register.

The scrub_control7_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1E0`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

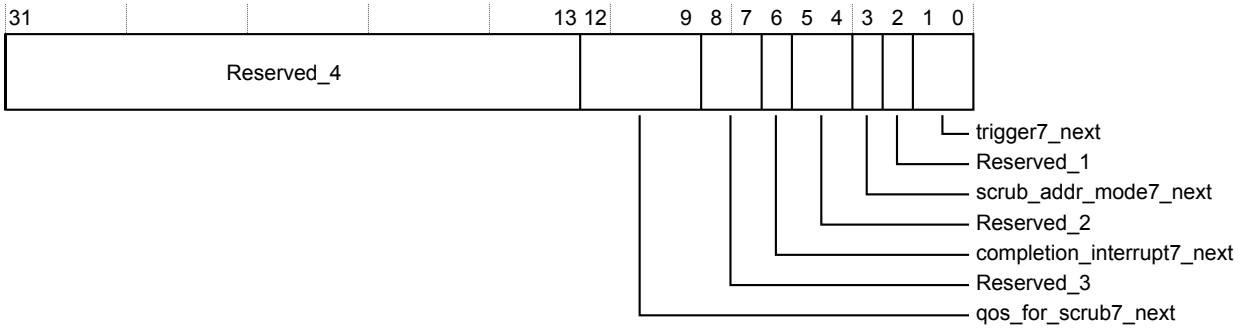

Figure 3-100 scrub_control7_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub7_next
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt7_next
Configures whether to emit an event when the sequence completes

[5:4] Reserved_2
Unused bits

[3] scrub_addr_mode7_next
Configures scrub address mode

[2] Reserved_1
Unused bits

[1:0] trigger7_next
Controls the trigger event associated with the channel operation.

3.3.101 scrub_address_min7_next

Configures the address space control for the scrub engine channel.

The scrub_address_min7_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1E4`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

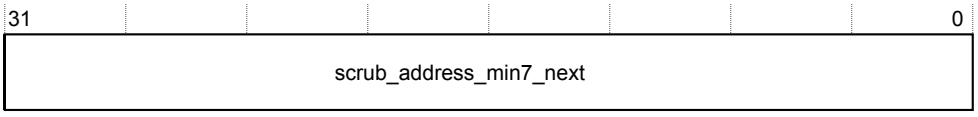

Figure 3-101 scrub_address_min7_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min7_next
Program to set the starting address for the scrub engine. When scrub_addr_mode7 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode7 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.102 scrub_address_max7_next

Configures the address space control for the scrub engine channel.

The scrub_address_max7_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1E8`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

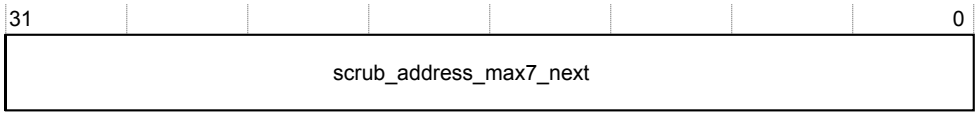

Figure 3-102 scrub_address_max7_next register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max7_next
Program to set the ending address for the scrub engine. When scrub_addr_mode7 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode7 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.103 feature_control_next

Control register for DMC features.

The feature_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1F0`
Type	Read-write
Reset	`0x0AA00000`
Width	32

The following figure shows the bit assignments.

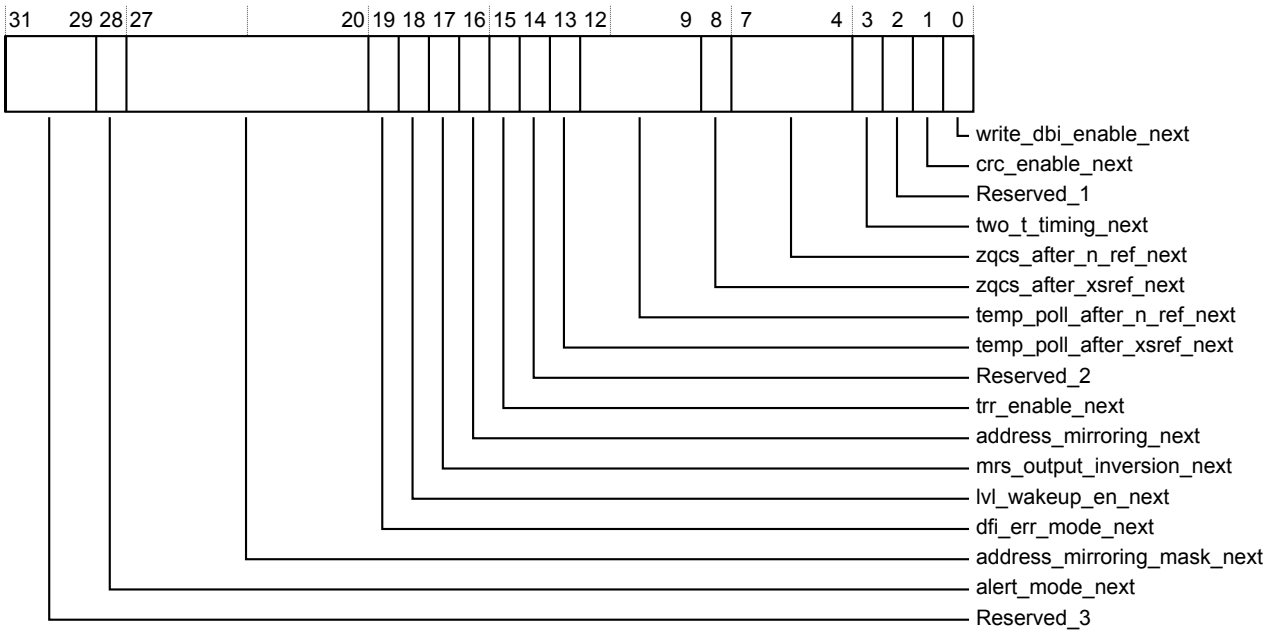

Figure 3-103 feature_control_next register bit assignments

The following shows the bit assignments.

[31:29] Reserved_3
Unused bits

[28] alert_mode_next
Configures the DMC behavior in response to dfi_alert_n being asserted. Note, when performing DIMM CA training using the ALERT pin this mode must be set to interrupt-only mode

[27:20] address_mirroring_mask_next
Each bit determines if address mirroring as per the DDR3/DDR4 RDIMM Design Specification must be applied to the corresponding rank. Set to 1 to enable mirroring, 0 to disable. Normally, this bit must be set high for odd physical ranks.

[19] dfi_err_mode_next
Configures the DMC behavior in response to dfi_err being asserted.

[18] lvl_wakeup_en_next
Program to enable the DMC to bring a rank out of self-refresh to perform PHY training. This must not be enabled when using geardown mode.

[17] mrs_output_inversion_next
Program to enable output inversion for MRS commands for DDR4 DIMMs.

[16] address_mirroring_next
Program to enable address mirroring for ranks identified by address_mirroring_mask.

[15] trr_enable_next
Program to enable issue of Target Row Refresh command on detection of potential maximum activate count (tMAC) violation. Must only be enabled for memories supporting this command.

[14] Reserved_2
Unused bits

[13] temp_poll_after_xsref_next
Program to insert an automatic temperature status poll command following exit from self-refresh.

[12:9] temp_poll_after_n_ref_next
Program to insert an automatic temperature status poll command following issue of n AUTOREFRESH commands. 0 disables the functionality. 1 is RESERVED

[8] zqcs_after_xsref_next
Program to insert an automatic ZQC short calibration command following exit from self-refresh.

[7:4] zqcs_after_n_ref_next
Program to insert an automatic ZQC short calibration command following n refreshes. 0 - disables the functionality. 1 is RESERVED

[3] two_t_timing_next
Program to enable or disable 2T command timing.

[2] Reserved_1
Unused bits

[1] crc_enable_next
Program to enable or disable Cyclic Redundancy Check (CRC) functionality on write data. Note: when enabling CRC t_wr, t_wtr and t_wtw must be extended by one cycle to accommodate the CRC functionality.

[0] write_dbi_enable_next
Program to enable or disable Data Bus Inversion (DBI) functionality for writes.

3.3.104 mux_control_next

Control multiplexing options for the DMC.

The mux_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1F4`
Type	Read-write
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

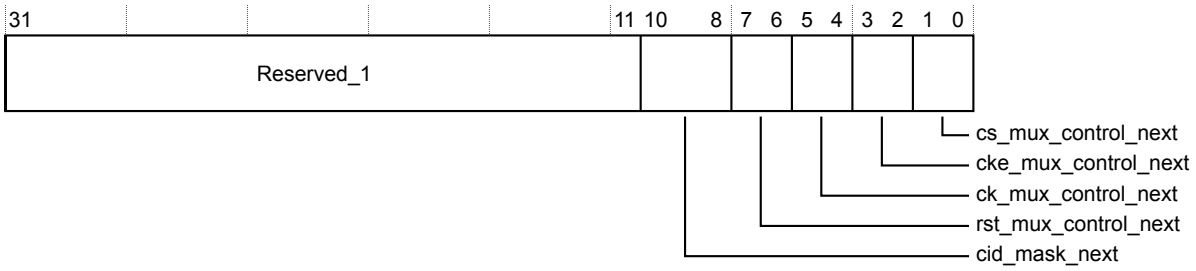

Figure 3-104 mux_control_next register bit assignments

The following shows the bit assignments.

[31:11] Reserved_1
Unused bits

[10:8] cid_mask_next
Program to mask inclusion of dfi_cid[2:0] output in parity calculation, where for each bit of cid_mask[2:0] a value of 1 means include the corresponding bit of dfi_cid[2:0].

[7:6] rst_mux_control_next
Program to control the multiplexing of the dfi_reset_n output for DIMM applications.

[5:4] ck_mux_control_next
Program to control the multiplexing of the dfi_ck output for DIMM applications.

[3:2] cke_mux_control_next
Program to control the multiplexing of the dfi_cke output for DIMM applications.

[1:0] cs_mux_control_next
Program to control the multiplexing of the dfi_cs_n output for DIMM applications.

3.3.105 rank_remap_control_next

Control register for rank remap.

The rank_remap_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1F8`

Type Read-write

Reset `0x76543210`

Width 32

The following figure shows the bit assignments.

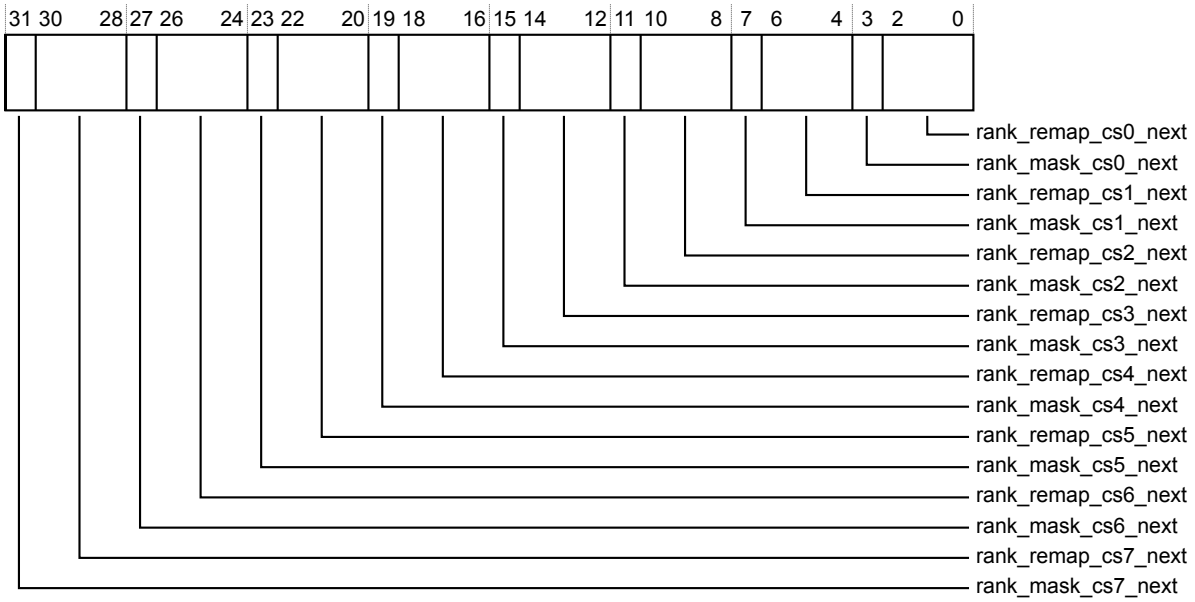

Figure 3-105 rank_remap_control_next register bit assignments

The following shows the bit assignments.

[31] rank_mask_cs7_next
Program to cause the DMC to abort all transactions to DRAM rank 7. Can be used to block transactions to a rank that is in maximum power down.

[30:28] rank_remap_cs7_next
Program to remap rank address 7 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[27] rank_mask_cs6_next
Program to cause the DMC to abort all transactions to DRAM rank 6. Can be used to block transactions to a rank that is in maximum power down.

[26:24] rank_remap_cs6_next
Program to remap rank address 6 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[23] rank_mask_cs5_next
Program to cause the DMC to abort all transactions to DRAM rank 5. Can be used to block transactions to a rank that is in maximum power down.

[22:20] rank_remap_cs5_next
Program to remap rank address 5 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[19] rank_mask_cs4_next
Program to cause the DMC to abort all transactions to DRAM rank 4. Can be used to block transactions to a rank that is in maximum power down.

[18:16] rank_remap_cs4_next
Program to remap rank address 4 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[15] rank_mask_cs3_next
Program to cause the DMC to abort all transactions to DRAM rank 3. Can be used to block transactions to a rank that is in maximum power down.

[14:12] rank_remap_cs3_next
Program to remap rank address 3 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[11] rank_mask_cs2_next
Program to cause the DMC to abort all transactions to DRAM rank 2. Can be used to block transactions to a rank that is in maximum power down.

[10:8] rank_remap_cs2_next
Program to remap rank address 2 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[7] rank_mask_cs1_next
Program to cause the DMC to abort all transactions to DRAM rank 1. Can be used to block transactions to a rank that is in maximum power down.

[6:4] rank_remap_cs1_next
Program to remap rank address 1 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[3] rank_mask_cs0_next
Program to cause the DMC to abort all transactions to DRAM rank 0. Can be used to block transactions to a rank that is in maximum power down.

[2:0] rank_remap_cs0_next
Program to remap rank address 0 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

3.3.106 t_refi_next

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8.

The t_refi_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x200`
Type	Read-write
Reset	`0x00090100`
Width	32

The following figure shows the bit assignments.

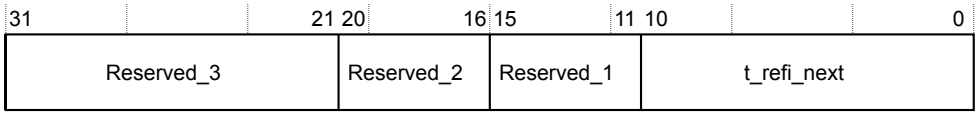

Figure 3-106 t_refi_next register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits

[20:16] Reserved_2
Unused bits

[15:11] Reserved_1
Unused bits

[10:0] t_refi_next
t_refi_next bitfield. The supported range for this bitfield is 63-2047.

3.3.107 t_rfc_next

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank.

The t_rfc_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x204
Type	Read-write
Reset	0x00008C23
Width	32

The following figure shows the bit assignments.

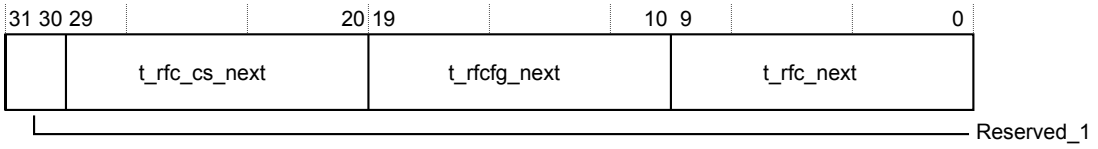

Figure 3-107 t_rfc_next register bit assignments

The following shows the bit assignments.

[31:30] Reserved_1
Unused bits

[29:20] t_rfc_cs_next
Configures the minimum delay between AUTOREFRESH operations to different ranks. The supported range for this bitfield is 0-700.

[19:10] t_rfcfg_next
Configures the tRFC timing parameter for fine-grained AUTOREFRESH operations. The supported range for this bitfield is 2-700.

[9:0] t_rfc_next
Configures the tRFC timing parameter for all-bank AUTOREFRESH operations. The supported range for this bitfield is 2-700.

3.3.108 t_mrr_next

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note: this value is used to determine the data cycles returned as a result of an MRR command.

The t_mrr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x208
Type	Read-write
Reset	0x00000002
Width	32

The following figure shows the bit assignments.

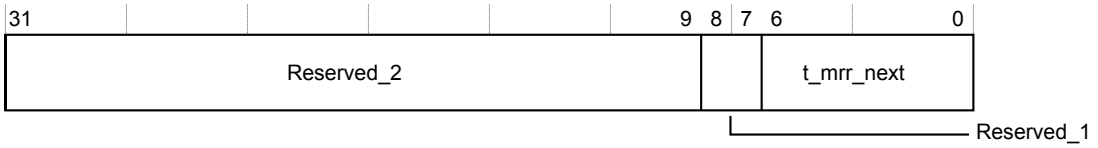

Figure 3-108 t_mrr_next register bit assignments

The following shows the bit assignments.

[31:9] Reserved_2
Unused bits
[8:7] Reserved_1
Unused bits
[6:0] t_mrr_next
t_mrr_next bitfield. The supported range for this bitfield is 1-127.

3.3.109 t_mrw_next

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed.

The t_mrw_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x20C`
Type	Read-write
Reset	`0x0000000C`
Width	32

The following figure shows the bit assignments.

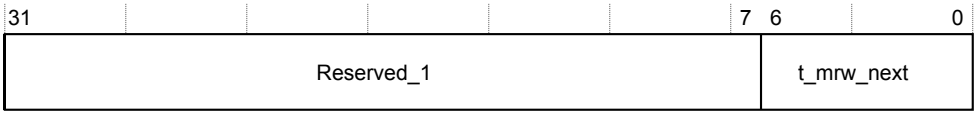

Figure 3-109 t_mrw_next register bit assignments

The following shows the bit assignments.

[31:7] Reserved_1
Unused bits
[6:0] t_mrw_next
t_mrw_next bitfield. The supported range for this bitfield is 12-127.

3.3.110 t_rdpden_next

Configures the tRDPDEN timing parameter. This determines the delay applied after a Read command before a power down command can be issued to the same rank.

The t_rdpden_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.
Attributes

Offset	`0x210`
Type	Read-write
Reset	`0x00000002`
Width	32

The following figure shows the bit assignments.

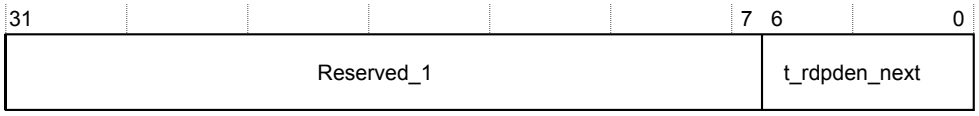

Figure 3-110 t_rdpden_next register bit assignments

The following shows the bit assignments.

[31:7] Reserved_1
Unused bits
[6:0] t_rdpden_next
t_rdpden_next bitfield. The supported range for this bitfield is 0-126.

3.3.111 t_rcd_next

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank.

The t_rcd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x218`
Type	Read-write
Reset	`0x00000005`
Width	32

The following figure shows the bit assignments.

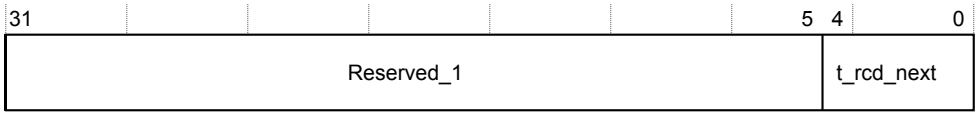

Figure 3-111 t_rcd_next register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits
[4:0] t_rcd_next
t_rcd_next bitfield. The supported range for this bitfield is 4-18.

3.3.112 t_ras_next

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank.

The t_ras_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x21C`
Type	Read-write
Reset	`0x0000000E`
Width	32

The following figure shows the bit assignments.

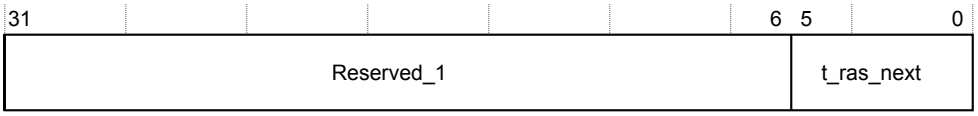

Figure 3-112 t_ras_next register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_ras_next
t_ras_next bitfield. The supported range for this bitfield is 8-39.

3.3.113 t_rp_next

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank.

The t_rp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x220`
Type	Read-write
Reset	`0x00000005`
Width	32

The following figure shows the bit assignments.

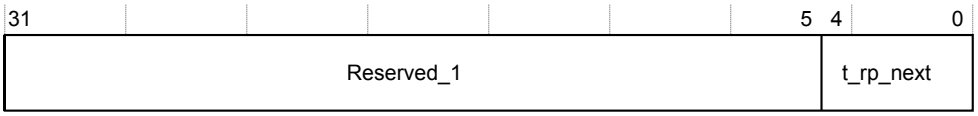

Figure 3-113 t_rp_next register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits
[4:0] t_rp_next
t_rp_next bitfield. The supported range for this bitfield is 4-18.

3.3.114 t_rpall_next

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank.

The t_rpall_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x224`
Type	Read-write
Reset	`0x00000005`
Width	32

The following figure shows the bit assignments.

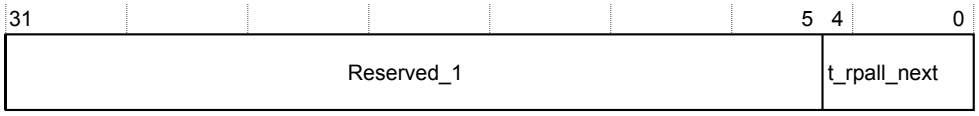

Figure 3-114 t_rpall_next register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits
[4:0] t_rpall_next
t_rpall_next bitfield. The supported range for this bitfield is 4-18.

3.3.115 t_rrd_next

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, and a different bank group, respectively, as described in the DDR4 specification.

The t_rrd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x228`
Type	Read-write
Reset	`0x00000404`
Width	32

The following figure shows the bit assignments.

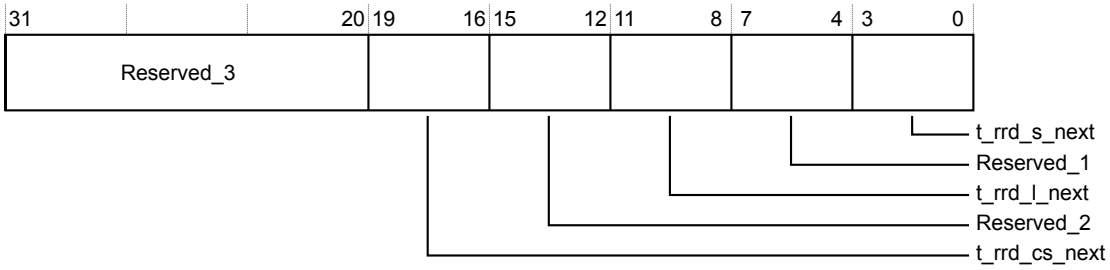

Figure 3-115 t_rrd_next register bit assignments

The following shows the bit assignments.

[31:20] Reserved_3
Unused bits
[19:16] t_rrd_cs_next
t_rrd_cs_next bitfield. The supported range for this bitfield is 0-15.
[15:12] Reserved_2
Unused bits
[11:8] t_rrd_l_next
t_rrd_l_next bitfield. The supported range for this bitfield is 1-15.
[7:4] Reserved_1
Unused bits
[3:0] t_rrd_s_next
t_rrd_s_next bitfield. The supported range for this bitfield is 1-15.

3.3.116 t_act_window_next

Configures the tFAW and tMAWi timing parameters.

The t_act_window_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x22C`
Type	Read-write
Reset	`0x03560014`
Width	32

The following figure shows the bit assignments.

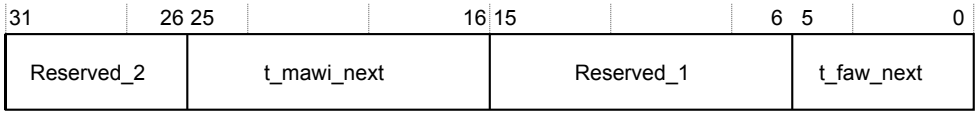

Figure 3-116 t_act_window_next register bit assignments

The following shows the bit assignments.

[31:26] Reserved_2
Unused bits
[25:16] t_mawi_next
Sets the value of the average delay required between ACTIVATE commands to the same row to not violate tMAC in tMAW. Must be programmed to (tMAW/(tMAC/2)).

[15:6] Reserved_1
Unused bits

[5:0] t_faw_next
The DMC does not issue more than 4 ACTIVATE commands within a rolling tFAW window. The supported range for this bitfield is 8-63.

3.3.117 t_rtr_next

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), and different chip-selects (t_rtr_cs).

The t_rtr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x234`
Type	Read-write
Reset	`0x00040404`
Width	32

The following figure shows the bit assignments.

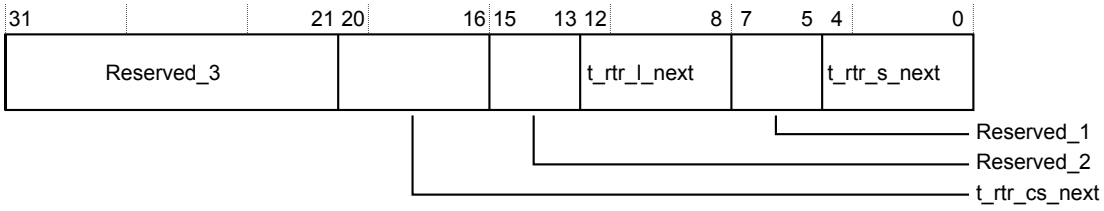

Figure 3-117 t_rtr_next register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits

[20:16] t_rtr_cs_next
t_rtr_cs_next bitfield. The supported range for this bitfield is 4-31.

[15:13] Reserved_2
Unused bits

[12:8] t_rtr_l_next
t_rtr_l_next bitfield. The supported range for this bitfield is 4-31.

[7:5] Reserved_1
Unused bits

[4:0] t_rtr_s_next
t_rtr_s_next bitfield. The supported range for this bitfield is 4-31.

3.3.118 t_rtw_next

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_trw_l), and other chip-selects (t_rtw_cs).

The t_rtw_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x238
Type	Read-write
Reset	0x00060606
Width	32

The following figure shows the bit assignments.

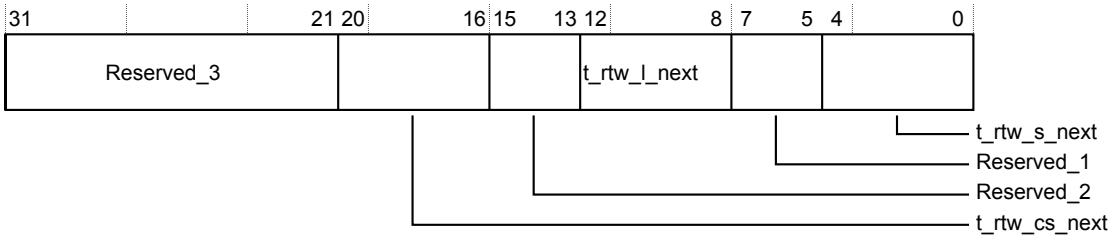

Figure 3-118 t_rtw_next register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits

[20:16] t_rtw_cs_next
t_rtw_cs_next bitfield. The supported range for this bitfield is 4-31.

[15:13] Reserved_2
Unused bits

[12:8] t_rtw_l_next
t_rtw_l_next bitfield. The supported range for this bitfield is 4-31.

[7:5] Reserved_1
Unused bits

[4:0] t_rtw_s_next
t_rtw_s_next bitfield. The supported range for this bitfield is 4-31.

3.3.119 t_rtp_next

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank.

The t_rtp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x23C
Type	Read-write
Reset	0x00000004
Width	32

The following figure shows the bit assignments.

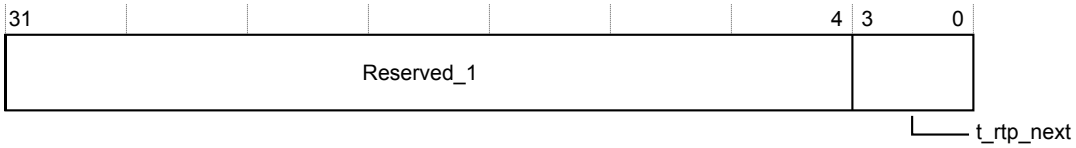

Figure 3-119 t_rtp_next register bit assignments

The following shows the bit assignments.

[31:4] Reserved_1
Unused bits

[3:0] t_rtp_next
t_rtp_next bitfield. The supported range for this bitfield is 4-15.

3.3.120 t_wr_next

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITEs, to the same bank. Note: this must take into account CRC timing requirements.

The t_wr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x244`
Type	Read-write
Reset	`0x00000005`
Width	32

The following figure shows the bit assignments.

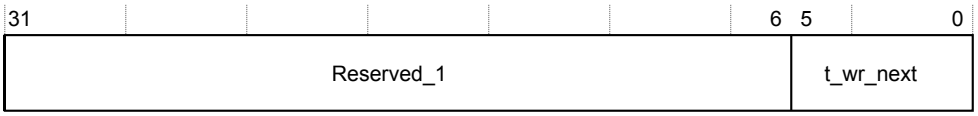

Figure 3-120 t_wr_next register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_wr_next
t_wr_next bitfield. The supported range for this bitfield is 4-63.

3.3.121 t_wtr_next

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs). Note: these must take into account CRC timing requirements.

The t_wtr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x248
Type Read-write
Reset 0x00040404
Width 32

The following figure shows the bit assignments.

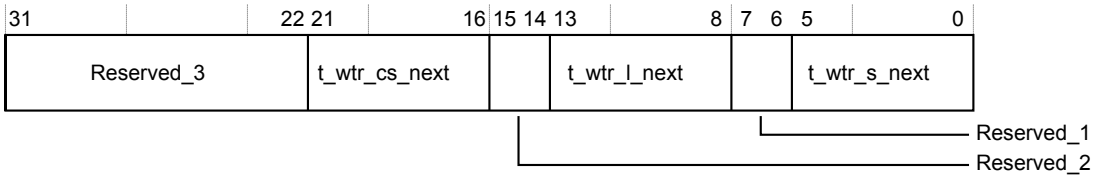

Figure 3-121 t_wtr_next register bit assignments

The following shows the bit assignments.

[31:22] Reserved_3
Unused bits
[21:16] t_wtr_cs_next
t_wtr_cs_next bitfield. The supported range for this bitfield is 2-63.
[15:14] Reserved_2
Unused bits
[13:8] t_wtr_l_next
t_wtr_l_next bitfield. The supported range for this bitfield is 4-63.
[7:6] Reserved_1
Unused bits
[5:0] t_wtr_s_next
t_wtr_s_next bitfield. The supported range for this bitfield is 4-63.

3.3.122 t_wtw_next

Configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes. Note: these must take into account CRC timing requirements.

The t_wtw_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x24C
Type Read-write
Reset 0x00040404
Width 32

The following figure shows the bit assignments.

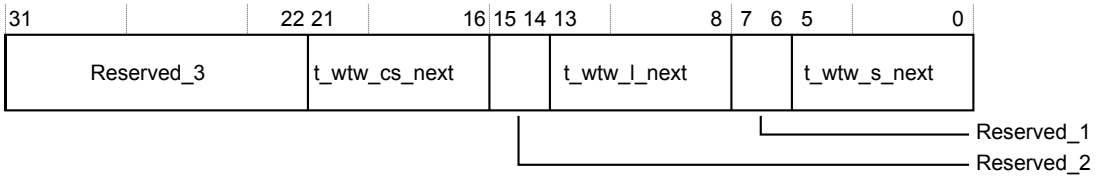

Figure 3-122 t_wtw_next register bit assignments

The following shows the bit assignments.

[31:22] Reserved_3
Unused bits
[21:16] t_wtw_cs_next
t_wtw_cs_next bitfield. The supported range for this bitfield is 4-35.
[15:14] Reserved_2
Unused bits
[13:8] t_wtw_l_next
t_wtw_l_next bitfield. The supported range for this bitfield is 4-35.
[7:6] Reserved_1
Unused bits
[5:0] t_wtw_s_next
t_wtw_s_next bitfield. The supported range for this bitfield is 4-35.

3.3.123 t_xmpd_next

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank.

The t_xmpd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x254`
Type	Read-write
Reset	`0x000003FF`
Width	32

The following figure shows the bit assignments.

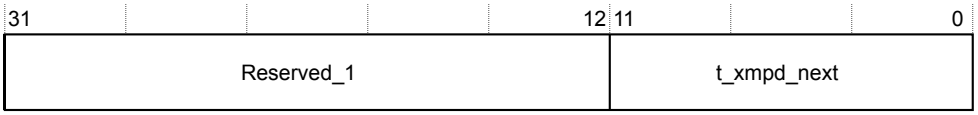

Figure 3-123 t_xmpd_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] t_xmpd_next
t_xmpd_next bitfield. The supported range for this bitfield is 1-4094.

3.3.124 t_ep_next

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank.

The t_ep_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x258

Type Read-write

Reset 0x00000002

Width 32

The following figure shows the bit assignments.

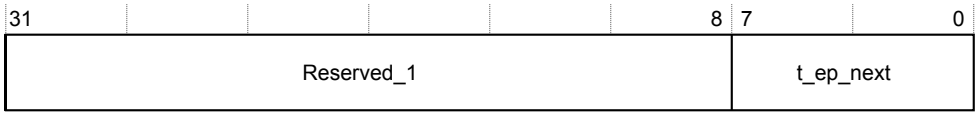

Figure 3-124 t_ep_next register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:0] t_ep_next
t_ep_next bitfield. The supported range for this bitfield is 1-255.

3.3.125 t_xp_next

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). Note: t_xpdll must be greater than or equal to tRCD and tCKE, and t_xp must be greater than or equal to tMPX_S.

The t_xp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x25C

Type Read-write

Reset 0x00060002

Width 32

The following figure shows the bit assignments.

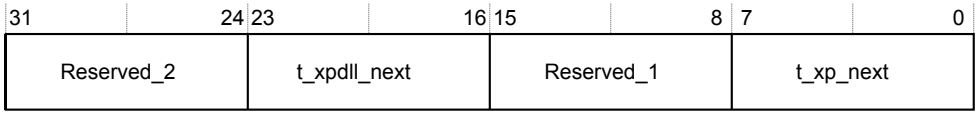

Figure 3-125 t_xp_next register bit assignments

The following shows the bit assignments.

[31:24] Reserved_2
Unused bits

[23:16] t_xpdll_next
This delay is applied for subsequent commands requiring a DLL The supported range for this bitfield is 5-255.

[15:8] Reserved_1
Unused bits

[7:0] t_xp_next
This delay is applied for subsequent commands not requiring a DLL The supported range for this bitfield is 1-255.

3.3.126 t_esr_next

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank.

The t_esr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x260`
Type	Read-write
Reset	`0x0000000E`
Width	32

The following figure shows the bit assignments.

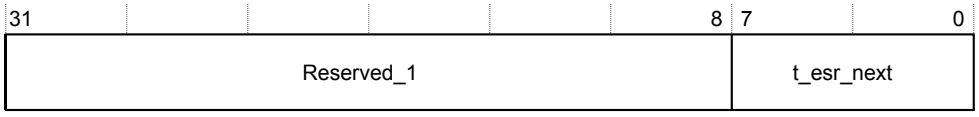

Figure 3-126 t_esr_next register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:0] t_esr_next
t_esr_next bitfield. The supported range for this bitfield is 1-255.

3.3.127 t_xsr_next

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank.

The t_xsr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x264`
Type	Read-write
Reset	`0x05120100`

Width 32

The following figure shows the bit assignments.

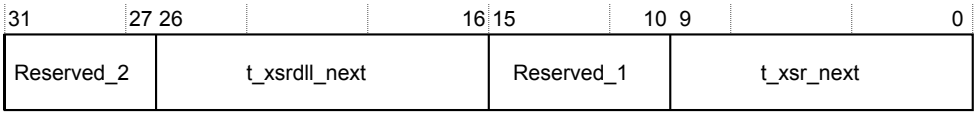

Figure 3-127 t_xsr_next register bit assignments

The following shows the bit assignments.

[31:27] Reserved_2
Unused bits

[26:16] t_xsrdll_next
This delay is applied for subsequent commands requiring a DLL. The supported range for this bitfield is 1-2047.

[15:10] Reserved_1
Unused bits

[9:0] t_xsr_next
This delay is applied for subsequent commands not requiring a DLL. The supported range for this bitfield is 1-1023.

3.3.128 t_esrck_next

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state.

The t_esrck_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x268`

Type Read-write

Reset `0x00000005`

Width 32

The following figure shows the bit assignments.

Figure 3-128 t_esrck_next register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits

[4:0] t_esrck_next
t_esrck_next bitfield. The supported range for this bitfield is 1-31.

3.3.129 t_ckxsr_next

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state.

The t_ckxsr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x26C`
Type	Read-write
Reset	`0x00000001`
Width	32

The following figure shows the bit assignments.

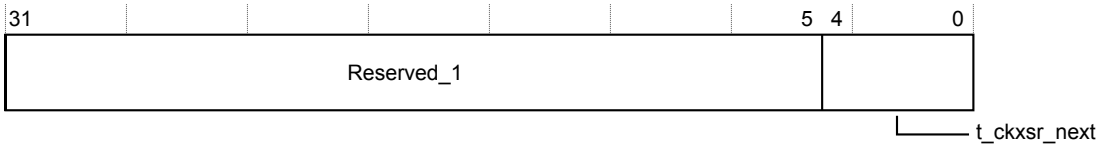

Figure 3-129 t_ckxsr_next register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits

[4:0] t_ckxsr_next
t_ckxsr_next bitfield. The supported range for this bitfield is 1-31.

3.3.130 t_cmd_next

Configures command signalling timing.

The t_cmd_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x270`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

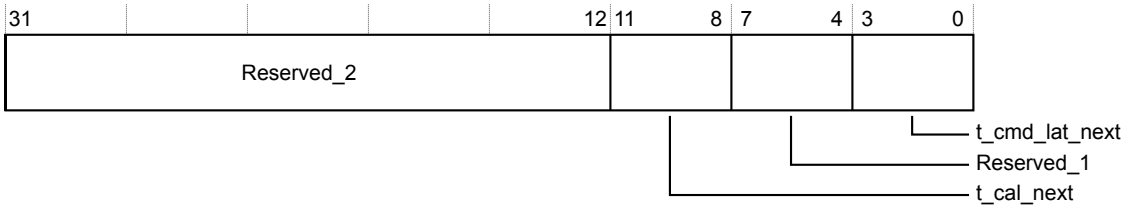

Figure 3-130 t_cmd_next register bit assignments

The following shows the bit assignments.

[31:12] Reserved_2
Unused bits

[11:8] t_cal_next
Specifies the Command Address latency at the DDR4 device. Note: t_cal must be zero when using RDIMMs. The supported range for this bitfield is 0-10.

[7:4] Reserved_1
Unused bits

[3:0] t_cmd_lat_next
Specifies the number of DFI clocks after the dfi_cs_n signal is asserted until the associated command and address bus is driven. The supported range for this bitfield is 0-10.

3.3.131 t_parity_next

Parity latencies t_parinlat and t_completion.

The t_parity_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x274`
Type	Read-write
Reset	`0x00000900`
Width	32

The following figure shows the bit assignments.

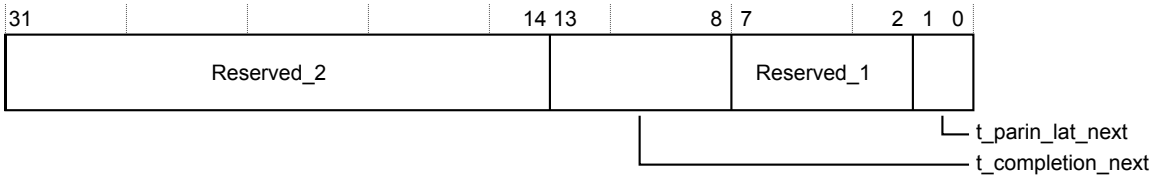

Figure 3-131 t_parity_next register bit assignments

The following shows the bit assignments.

[31:14] Reserved_2
Unused bits

[13:8] t_completion_next
Determines the DMC clock cycle delay between when the dfi_cs_n signal is asserted and the cycle in which that command can be considered complete. In programming this value, you must consider the DFI timing parameters t_wrdata_delay, t_error_resp, t_crcmax_lat, and t_phyrdlatmax to ensure all have expired, where applicable, within t_completion cycles. The supported range for this bitfield is 9-62.

[7:2] Reserved_1
Unused bits

[1:0] t_parin_lat_next
Specifies the number of DFI clocks between when the dfi_cs_n signal is asserted and when the associated dfi_parity_in signal is driven. The supported range for this bitfield is 0-3.

3.3.132 t_zqcs_next

Configures the delay to apply following a ZQC-Short calibration command.

The t_zqcs_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x278`
Type	Read-write
Reset	`0x00000040`
Width	32

The following figure shows the bit assignments.

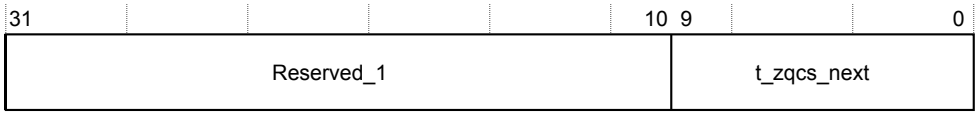

Figure 3-132 t_zqcs_next register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits

[9:0] t_zqcs_next
t_zqcs_next bitfield. The supported range for this bitfield is 2-1023.

3.3.133 t_rddata_en_next

Determines the time between a READ command commencing on the DFI interface, and the assertion of the **dfi_read_en signal**.

The t_rddata_en_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x300`
Type	Read-write
Reset	`0x00000001`
Width	32

The following figure shows the bit assignments.

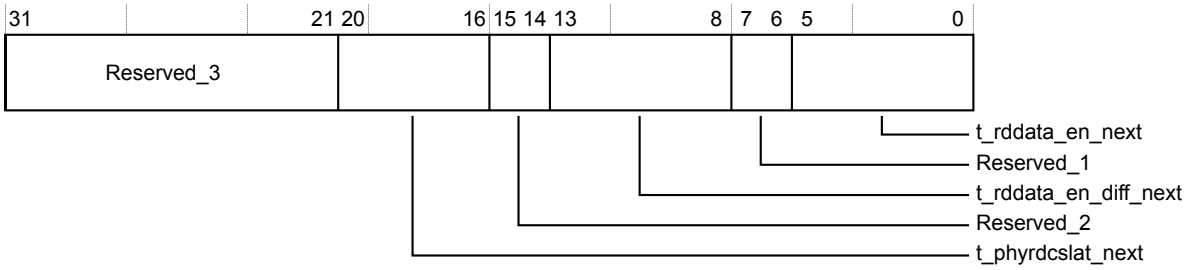

Figure 3-133 t_rddata_en_next register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits

[20:16] t_phyrdcslat_next
Specifies the number of DFI PHY clocks between a READ command commencing on the DFI interface (assertion of chip-select), and when the associated **dfi_rddata_cs_n** signal is asserted. The supported range for this bitfield is 0-31.

[15:14] Reserved_2
Unused bits

[13:8] t_rddata_en_diff_next
Describes a PHY specific value useful for aligning t_rddata_en for a specific PHY. This value has no effect on the controller. The supported range for this bitfield is 0-40.

[7:6] Reserved_1
Unused bits

[5:0] t_rddata_en_next
t_rddata_en_next bitfield. The supported range for this bitfield is 0-40.

3.3.134 t_phyrdlat_next

Determines the maximum possible time between the assertion of the dfi_read_en signal, and the assertion of the dfi_rddata_valid signal by the PHY.

The t_phyrdlat_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x304`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

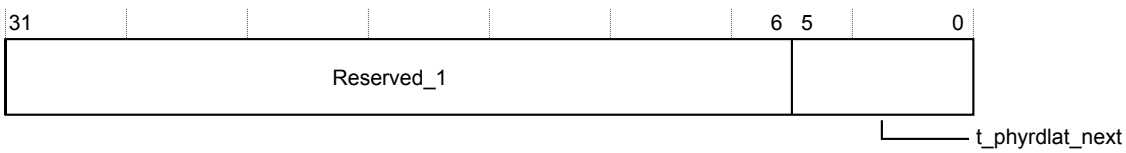

Figure 3-134 t_phyrdlat_next register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_phyrdlat_next
Determines the maximum time between the assertion of the dfi_read_en signal and the assertion of the dfi_rddata_valid signal by the PHY. The supported range for this bitfield is 1-62.

3.3.135 t_phywrlat_next

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrdata_en, dfi_wrdata_cs and dfi_wrdata signals.

The t_phywrlat_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x308`
Type	Read-write
Reset	`0x00000001`
Width	32

The following figure shows the bit assignments.

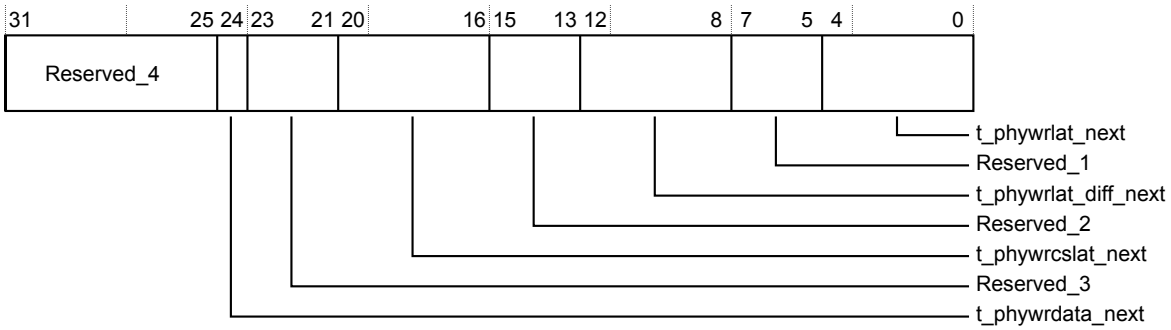

Figure 3-135 t_phywrlat_next register bit assignments

The following shows the bit assignments.

[31:25] Reserved_4
Unused bits

[24] t_phywrdata_next
Determines the time between the assertion of the **dfi_wrdata_en** and **dfi_wrdata** signals. The supported range for this bitfield is 0-1.

[23:21] Reserved_3
Unused bits

[20:16] t_phywrcslat_next
Specifies the number of DFI PHY clocks between when a write command is sent on the DFI control interface (dfi_cs_n assertion) and when the associated dfi_wrdata_cs_n signal is asserted. The supported range for this bitfield is 0-31.

[15:13] Reserved_2
Unused bits

[12:8] t_phywrlat_diff_next
Describes the PHY specific value useful for aligning t_phywrlat for a specific PHY. This value has no effect on the controller. The supported range for this bitfield is 0-31.

[7:5] Reserved_1
Unused bits

[4:0] t_phywrlat_next
Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrdata_en signal. The supported range for this bitfield is 0-31.

3.3.136 rdlvl_control_next

This register determines the DMC behavior during read training operations.

The rdlvl_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x310`
Type	Read-write
Reset	`0x00001080`
Width	32

The following figure shows the bit assignments.

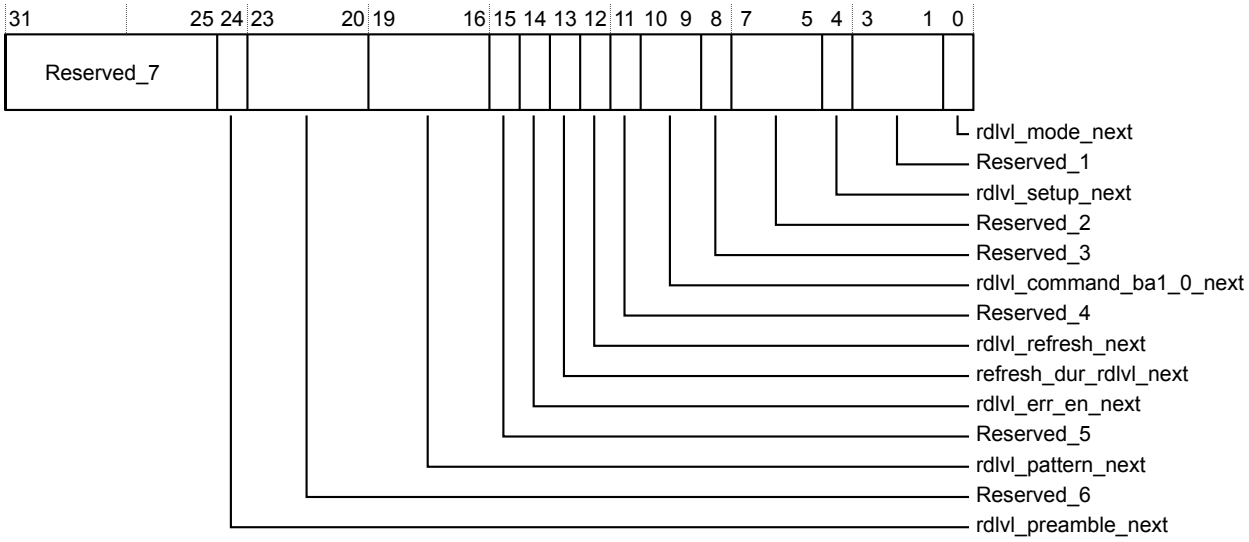

Figure 3-136 rdlvl_control_next register bit assignments

The following shows the bit assignments.

[31:25] Reserved_7
Unused bits

[24] rdlvl_preamble_next
For DDR4 program to enable or disable issue of preamble training mode MRS prior to performing read leveling training.

[23:20] Reserved_6
Unused bits

[19:16] rdlvl_pattern_next
Program the value to be driven onto dfi_lvl_pattern during training. The DMC ignores the value. For default DFI encodings see the DFI specification [5].

[15] Reserved_5
Unused bits

[14] rdlvl_err_en_next
If enabled replay commands because of dfi_err during training.

[13] refresh_dur_rdlvl_next
Program to enable AUTOREFRESH commands to be generated during training operations. When enabled (1'b1), the DMC exits a training sequence to perform refresh.

[12] rdlvl_refresh_next
Program to enable or disable issue of an AUTOREFRESH command prior to performing read leveling training.

[11] Reserved_4
Unused bits

[10:9] rdlvl_command_ba1_0_next
Program the BA address to use for training commands.

[8] Reserved_3
Unused bits

[7:5] Reserved_2
Unused bits

[4] rdlvl_setup_next
Program the command that sets up the DRAM for read leveling training.

[3:1] Reserved_1
Unused bits

[0] rdlvl_mode_next
Program the mode used for read leveling training.

3.3.137 rdlvl_mrs_next

This register determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl_control register.

The rdlvl_mrs_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x314`
Type	Read-write
Reset	`0x00000004`
Width	32

The following figure shows the bit assignments.

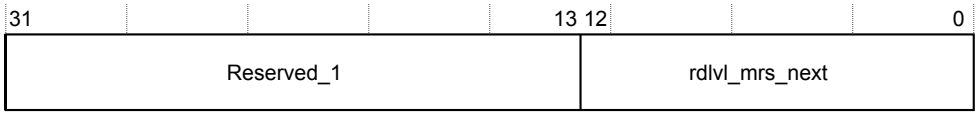

Figure 3-137 rdlvl_mrs_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_1
Unused bits

[12:0] rdlvl_mrs_next
Program the Mode Register command the DMC uses to place the DRAM into training mode. Set address bits [2:0] for the Mode Register write to MR3.

3.3.138 t_rdlvl_en_next

Configures the t_rdlvl_en timing parameter. This specifies the cycle delay between asserting dfi_rdlvl_en and the first training command, and also the cycle delay between deasserting dfi_rdlvl_en

and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training.

The t_rdlvl_en_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x318`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

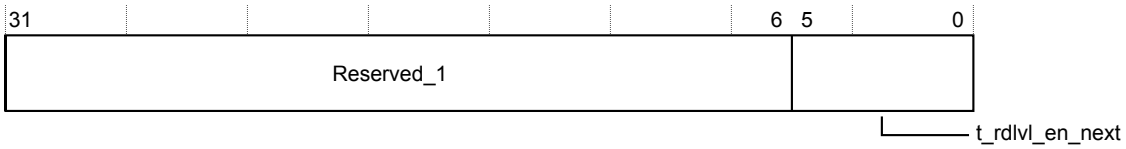

Figure 3-138 t_rdlvl_en_next register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_rdlvl_en_next
t_rdlvl_en_next bitfield. The supported range for this bitfield is 1-63.

3.3.139 t_rdlvl_rr_next

Configures the t_rdlvl_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi_rdlvl_en after observing dfi_rdlvl_resp.

The t_rdlvl_rr_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x31C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

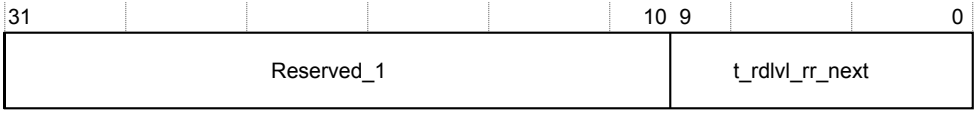

Figure 3-139 t_rdlvl_rr_next register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits

[9:0] t_rdlvl_rr_next
t_rdlvl_rr_next bitfield. The supported range for this bitfield is 4-1023.

3.3.140 wrlvl_control_next

This register determines the DMC behavior during write training operations.

The wrlvl_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x320`
Type	Read-write
Reset	`0x00001000`
Width	32

The following figure shows the bit assignments.

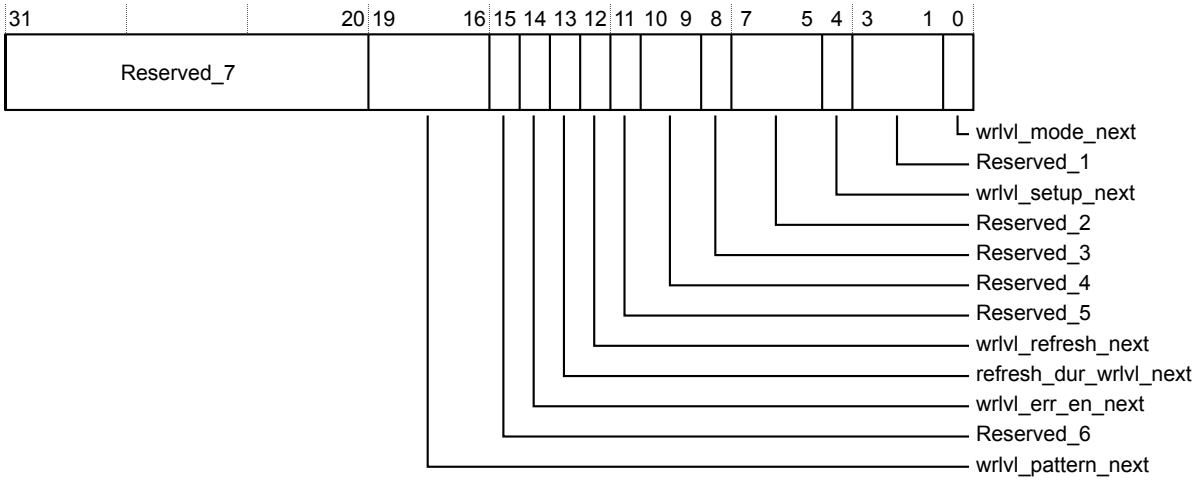

Figure 3-140 wrlvl_control_next register bit assignments

The following shows the bit assignments.

[31:20] Reserved_7
Unused bits

[19:16] wrlvl_pattern_next
Program the value to be driven onto dfi_lvl_pattern during training. The DMC ignores the value. For default DFI encodings see the DFI specification [5]. The supported range for this bitfield is 0-15.

[15] Reserved_6
Unused bits

[14] wrlvl_err_en_next
If enabled replay commands because of dfi_err during training.

[13] refresh_dur_wrlvl_next
Program to enable AUTOREFRESH commands to be generated during training operations. When enabled (1'b1), the DMC exits a training sequence to perform refresh.

[12] wrlvl_refresh_next
Program to enable or disable issue of an AUTOREFRESH command prior to performing write leveling training.

[11] Reserved_5
Unused bits

[10:9] Reserved_4
Unused bits

[8] Reserved_3
Unused bits

[7:5] Reserved_2
Unused bits

[4] wrlvl_setup_next
Program the command that sets up the DRAM for write leveling training.

[3:1] Reserved_1
Unused bits

[0] wrlvl_mode_next
Program the mode used for write leveling training.

3.3.141 wrlvl_mrs_next

This register determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write levelling. Enable this function with the wrlvl_control Register.

The wrlvl_mrs_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x324`
Type	Read-write
Reset	`0x00000086`
Width	32

The following figure shows the bit assignments.

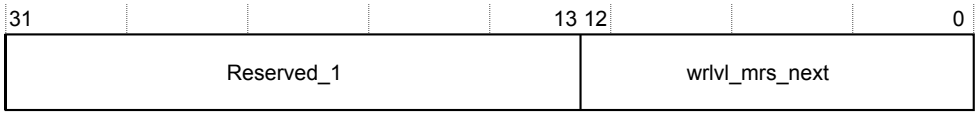

Figure 3-141 wrlvl_mrs_next register bit assignments

The following shows the bit assignments.

[31:13] Reserved_1
Unused bits

[12:0] wrlvl_mrs_next
Program the command the DMC uses to place the DRAM into training mode. Set address bits [12:0] for the Mode Register write to MR1.

3.3.142 t_wrlvl_en_next

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training.

The t_wrlvl_en_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x328
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

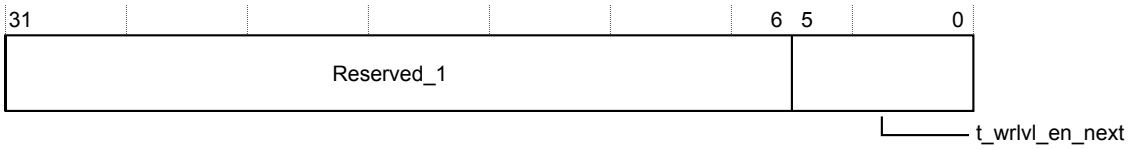

Figure 3-142 t_wrlvl_en_next register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_wrlvl_en_next
t_wrlvl_en_next bitfield. The supported range for this bitfield is 1-63.

3.3.143 t_wrlvl_ww_next

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvl_resp.

The t_wrlvl_ww_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x32C
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

Figure 3-143 t_wrlvl_ww_next register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits

[9:0] t_wrlvl_ww_next
t_wrlvl_ww_next bitfield. The supported range for this bitfield is 1-1023.

3.3.144 phy_power_control_next

Configures the low-power requests made to the PHY for the different channel states.

The phy_power_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x348`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

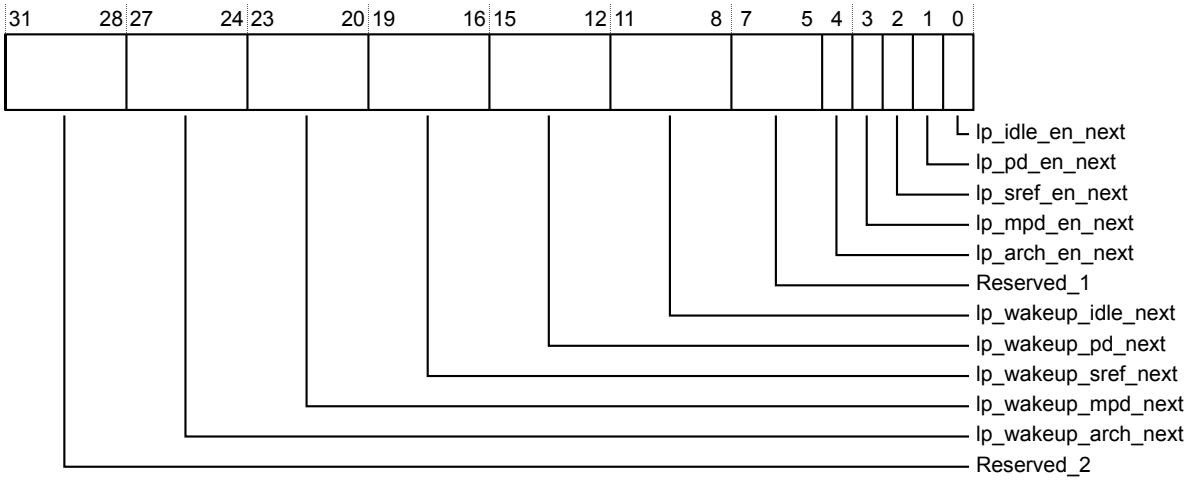

Figure 3-144 phy_power_control_next register bit assignments

The following shows the bit assignments.

[31:28] Reserved_2
Unused bits

[27:24] lp_wakeup_arch_next
Program the PHY wakeup encoding for PHY low-power requests when entering LOW-POWER architectural state. The supported range for this bitfield is 0-15.

[23:20] lp_wakeup_mpd_next
Program the PHY wakeup encoding for PHY low-power requests when in MPD. The supported range for this bitfield is 0-15.

[19:16] lp_wakeup_sref_next
Program the PHY wakeup encoding for PHY low-power requests when in self-refresh. The supported range for this bitfield is 0-15.

[15:12] lp_wakeup_pd_next
Program the PHY wakeup encoding for PHY low-power requests when powered down. The supported range for this bitfield is 0-15.

[11:8] lp_wakeup_idle_next
Program the PHY wakeup encoding for PHY low-power requests when idle. The supported range for this bitfield is 0-15.

[7:5] Reserved_1
Unused bits

[4] lp_arch_en_next
Program to enable or disable a PHY low-power request when entering LOW-POWER architectural state.

[3] lp_mpd_en_next
Program to enable or disable a PHY low-power request when in MPD.

[2] lp_sref_en_next
Program to enable or disable a PHY low-power request when in self-refresh.

[1] lp_pd_en_next
Program to enable or disable a PHY low-power request when in power down.

[0] lp_idle_en_next
Program to enable or disable a PHY low-power request when idle.

3.3.145 t_lpresp_next

Configures the minimum cycle delay to apply for PHY low-power handshakes.

The t_lpresp_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x34C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

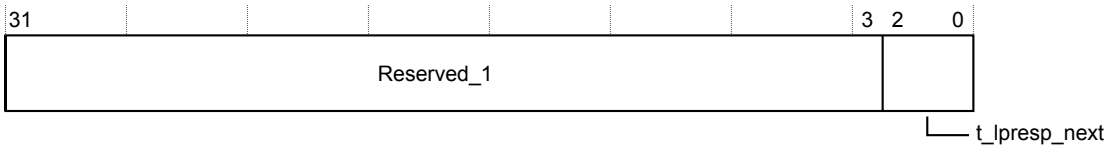

Figure 3-145 t_lpresp_next register bit assignments

The following shows the bit assignments.

[31:3] Reserved_1
Unused bits

[2:0] t_lpresp_next
The DMC waits a minimum t_lpresp cycles after asserting a PHY low power request before deasserting the request and resuming other commands. Zero means wait for dfi_lp_ack. The supported range for this bitfield is 0-7.

3.3.146 phy_update_control_next

Configures the update mechanism to use in response to PHY training requests.

The phy_update_control_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x350
Type Read-write
Reset 0x0FE00000
Width 32

The following figure shows the bit assignments.

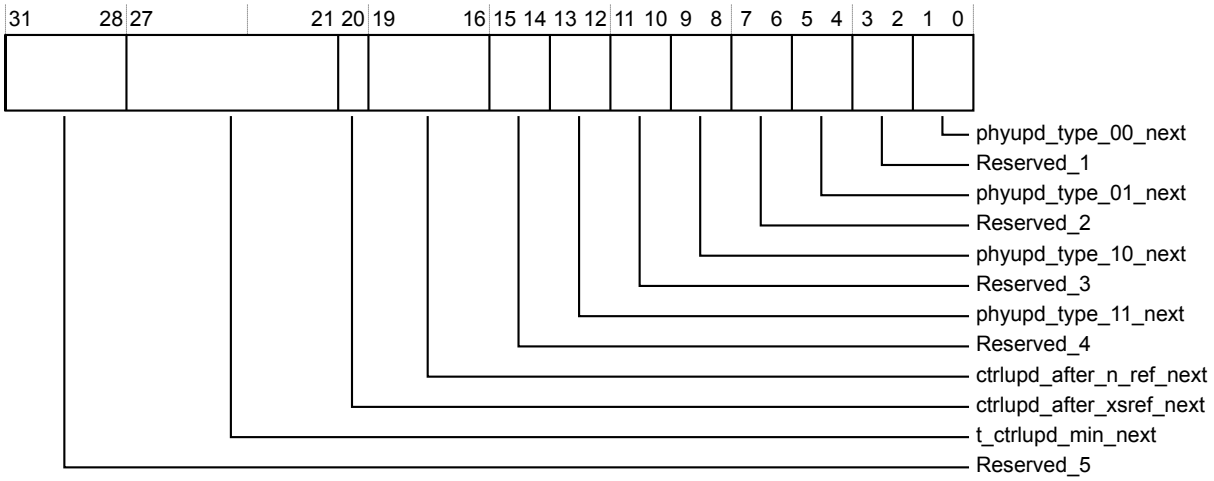

Figure 3-146 phy_update_control_next register bit assignments

The following shows the bit assignments.

[31:28] Reserved_5
Unused bits

[27:21] t_ctrlupd_min_next
Sets the number of cycles the DMC waits for acknowledgment of a cltrupd_req before deasserting the request and continuing normal operation. A value of 0x0 indicates the DMC must always wait for an acknowledgment before proceeding. The supported range for this bitfield is 0-127.

[20] ctrlupd_after_xsref_next
Program to enable an automatic DMC-initiated PHY update request after exiting self-refresh

[19:16] ctrlupd_after_n_ref_next
Program to enable an automatic DMC-initiated PHY update request after every n AUTOREFRESH commands. Zero disables the functionality. One is RESERVED

[15:14] Reserved_4
Unused bits

[13:12] phyupd_type_11_next
Program the required response to PHY update requests of type 11.

[11:10] Reserved_3
Unused bits

[9:8] phyupd_type_10_next
Program the required response to PHY update requsts of type 10.

[7:6] Reserved_2
Unused bits

[5:4] phyupd_type_01_next
Program the required response to PHY update requsts of type 01.

[3:2] Reserved_1
Unused bits

[1:0] phyupd_type_00_next
Program the required response to PHY update requsts of type 00.

3.3.147 odt_timing_next

Configures the ODT on and off timing.

The odt_timing_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0x358`
Type	Read-write
Reset	`0x06000600`
Width	32

The following figure shows the bit assignments.

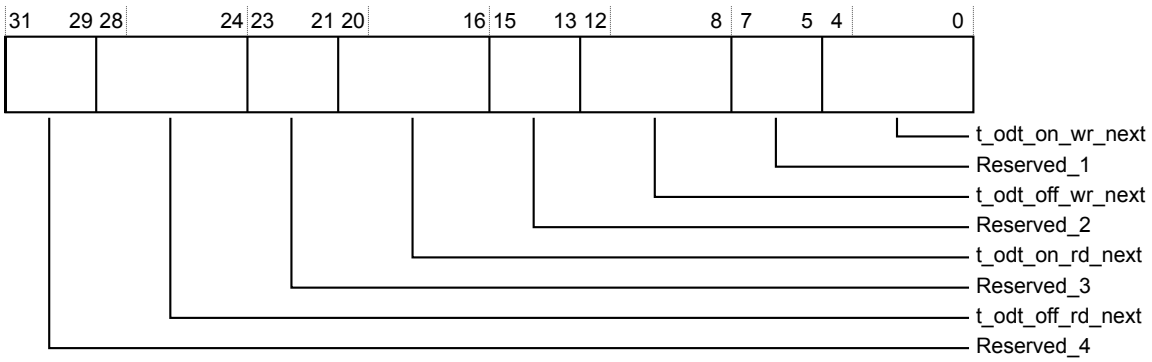

Figure 3-147 odt_timing_next register bit assignments

The following shows the bit assignments.

[31:29] Reserved_4

Unused bits

[28:24] t_odt_off_rd_next

Time from cs assertion to ODT being deasserted for read. The supported range for this bitfield is 2-31.

[23:21] Reserved_3

Unused bits

[20:16] t_odt_on_rd_next

Time from cs assertion to ODT being asserted for read. The supported range for this bitfield is 0-29.

[15:13] Reserved_2

Unused bits

[12:8] t_odt_off_wr_next

Time from cs assertion to ODT being deasserted for write. The supported range for this bitfield is 2-31.

[7:5] Reserved_1

Unused bits

[4:0] t_odt_on_wr_next

Time from cs assertion to ODT being asserted for write. The supported range for this bitfield is 0-29.

3.3.148 odt_wr_control_31_00_next

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_31_00_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x360`

Type Read-write

Reset `0x08040201`

Width 32

The following figure shows the bit assignments.

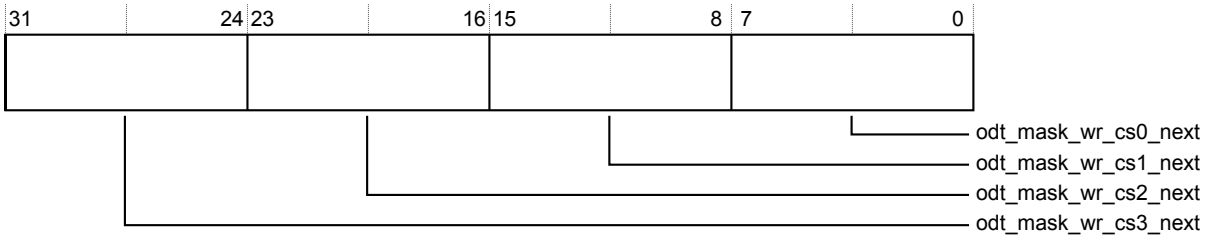

Figure 3-148 odt_wr_control_31_00_next register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_wr_cs3_next

Drives the dfi_odt[7:0] output signal during a write to DRAM rank 3. The supported range for this bitfield is 0-255.

[23:16] odt_mask_wr_cs2_next

Drives the dfi_odt[7:0] output signal during a write to DRAM rank 2. The supported range for this bitfield is 0-255.

[15:8] odt_mask_wr_cs1_next

Drives the dfi_odt[7:0] output signal during a write to DRAM rank 1. The supported range for this bitfield is 0-255.

[7:0] odt_mask_wr_cs0_next

Drives the dfi_odt[7:0] output signal during a write to DRAM rank 0. The supported range for this bitfield is 0-255.

3.3.149 odt_wr_control_63_32_next

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_63_32_next register characteristics are:

Usage constraints

Can be read from when in ALL states. Can be written to when in ALL states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x364`

Type Read-write

Reset `0x80402010`

Width 32

The following figure shows the bit assignments.

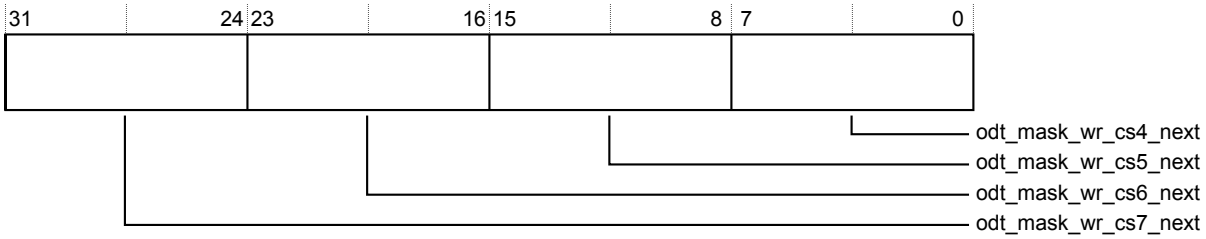

Figure 3-149 odt_wr_control_63_32_next register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_wr_cs7_next
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 7. The supported range for this bitfield is 0-255.

[23:16] odt_mask_wr_cs6_next
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 6. The supported range for this bitfield is 0-255.

[15:8] odt_mask_wr_cs5_next
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 5. The supported range for this bitfield is 0-255.

[7:0] odt_mask_wr_cs4_next
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 4. The supported range for this bitfield is 0-255.

3.3.150 odt_rd_control_31_00_next

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_31_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x368`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

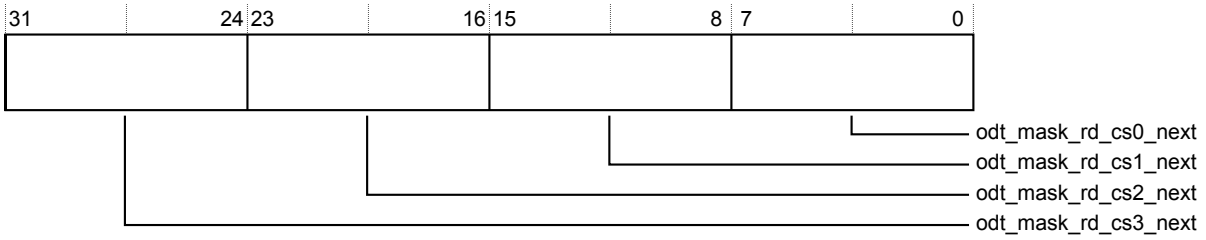

Figure 3-150 odt_rd_control_31_00_next register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_rd_cs3_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 3. The supported range for this bitfield is 0-255.

[23:16] odt_mask_rd_cs2_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 2. The supported range for this bitfield is 0-255.

[15:8] odt_mask_rd_cs1_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 1. The supported range for this bitfield is 0-255.

[7:0] odt_mask_rd_cs0_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 0. The supported range for this bitfield is 0-255.

3.3.151 odt_rd_control_63_32_next

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_63_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x36C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

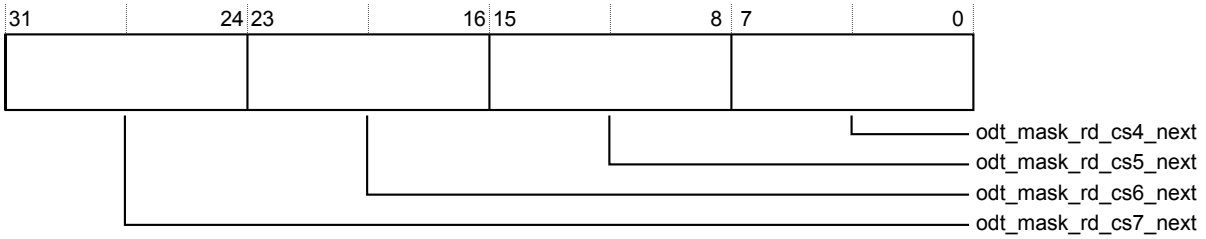

Figure 3-151 odt_rd_control_63_32_next register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_rd_cs7_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 7. The supported range for this bitfield is 0-255.

[23:16] odt_mask_rd_cs6_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 6. The supported range for this bitfield is 0-255.

[15:8] odt_mask_rd_cs5_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 5. The supported range for this bitfield is 0-255.

[7:0] odt_mask_rd_cs4_next
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 4. The supported range for this bitfield is 0-255.

3.3.152 temperature_readout

Holds the status of the temperature information. Reading the register returns the current temperature from the most recent automated temperature poll.

The temperature_readout register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be changed.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0x370`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

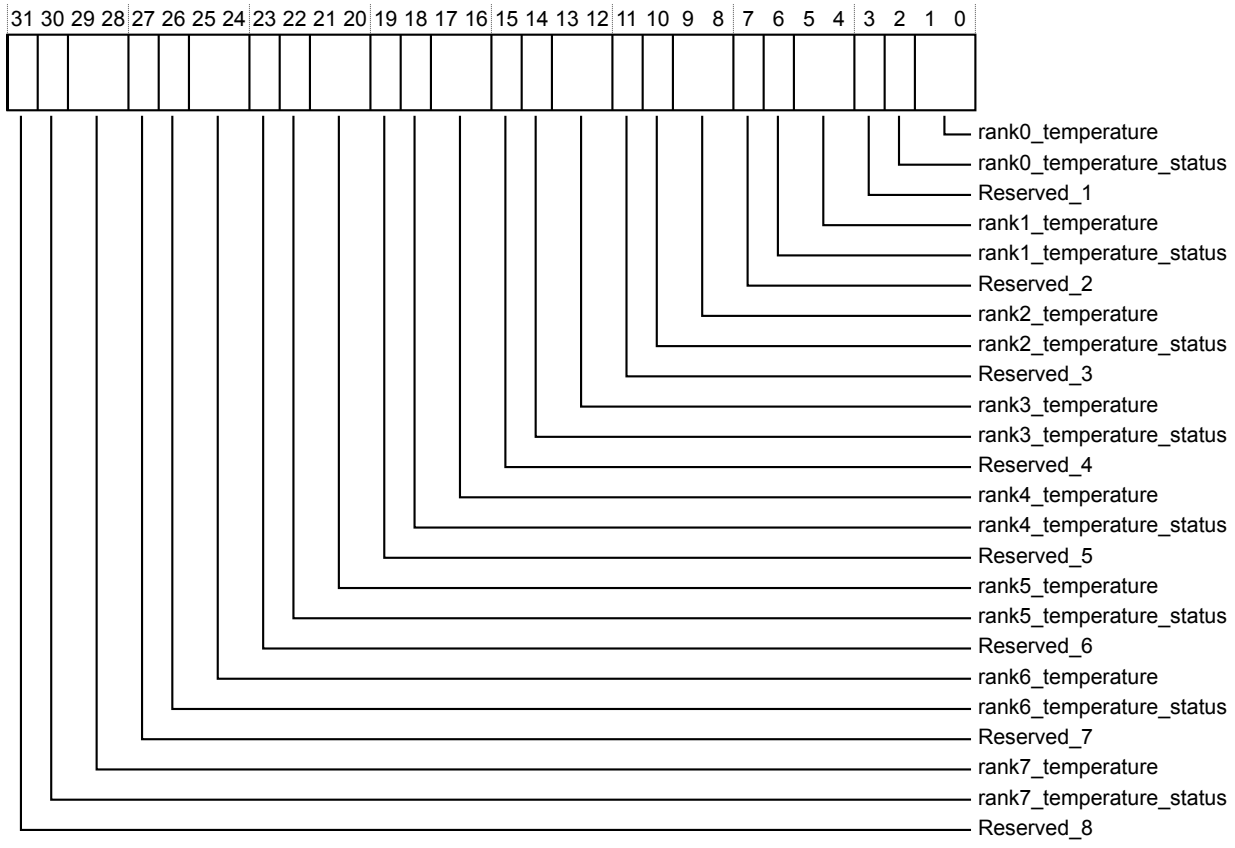

Figure 3-152 temperature_readout register bit assignments

The following shows the bit assignments.

[31] Reserved_8

Unused bits

[30] rank7_temperature_status

The current status of the returned value for this rank.

[29:28] rank7_temperature

The latest value of the multipurpose register for this rank.

[27] Reserved_7

Unused bits

[26] rank6_temperature_status
The current status of the returned value for this rank.
[25:24] rank6_temperature
The latest value of the multipurpose register for this rank.
[23] Reserved_6
Unused bits
[22] rank5_temperature_status
The current status of the returned value for this rank.
[21:20] rank5_temperature
The latest value of the multipurpose register for this rank.
[19] Reserved_5
Unused bits
[18] rank4_temperature_status
The current status of the returned value for this rank.
[17:16] rank4_temperature
The latest value of the multipurpose register for this rank.
[15] Reserved_4
Unused bits
[14] rank3_temperature_status
The current status of the returned value for this rank.
[13:12] rank3_temperature
The latest value of the multipurpose register for this rank.
[11] Reserved_3
Unused bits
[10] rank2_temperature_status
The current status of the returned value for this rank.
[9:8] rank2_temperature
The latest value of the multipurpose register for this rank.
[7] Reserved_2
Unused bits
[6] rank1_temperature_status
The current status of the returned value for this rank.
[5:4] rank1_temperature
The latest value of the multipurpose register for this rank.
[3] Reserved_1
Unused bits
[2] rank0_temperature_status
The current status of the returned value for this rank.
[1:0] rank0_temperature
The latest value of the multipurpose register for this rank.

3.3.153 training_status

Shows information relating to the training request status of the DMC.

The training_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x378`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

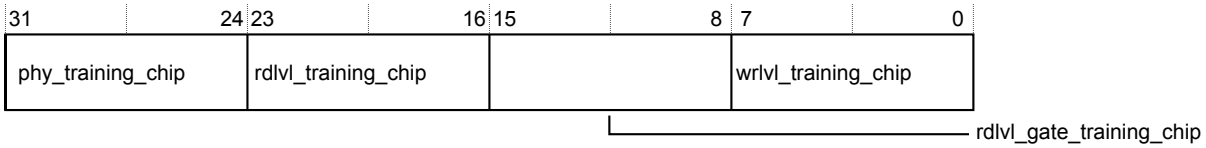

Figure 3-153 training_status register bit assignments

The following shows the bit assignments.

[31:24] phy_training_chip
One bit per rank indicating that the PHY has an outstanding request for PHY training on the indicated DRAM rank.

[23:16] rdlvl_training_chip
One bit per rank indicating that the PHY has an outstanding request for rdlvl gate training on the indicated DRAM rank.

[15:8] rdlvl_gate_training_chip
Waiting for rdlvl gate training on the indicated DRAM rank.

[7:0] wrlvl_training_chip
One bit per rank indicating that the PHY has an outstanding request for wrlvl training on the indicated DRAM rank.

3.3.154 dq_map_control_15_00_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_15_00_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x380`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

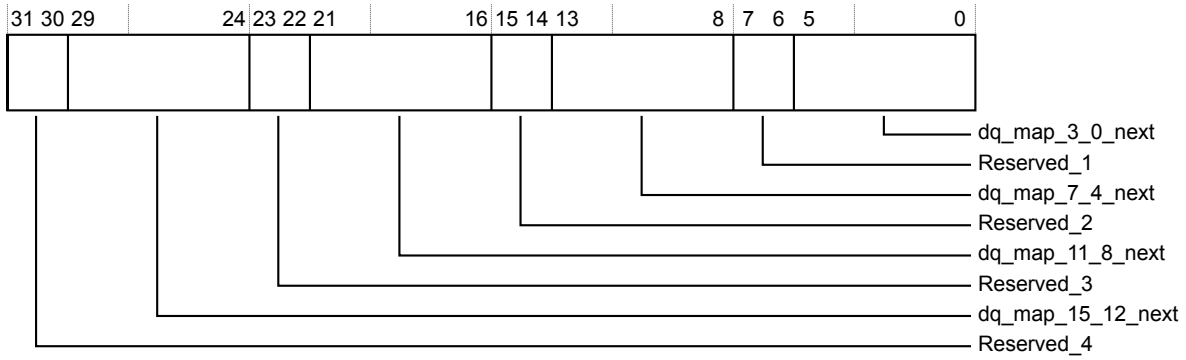

Figure 3-154 dq_map_control_15_00_next register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4
Unused bits

[29:24] dq_map_15_12_next
Controls DQ mapping for bits [15:12] of the DQ bus.

[23:22] Reserved_3
Unused bits

[21:16] dq_map_11_8_next
Controls DQ mapping for bits [11:8] of the DQ bus.

[15:14] Reserved_2
Unused bits

[13:8] dq_map_7_4_next
Controls DQ mapping for bits [7:4] of the DQ bus.

[7:6] Reserved_1
Unused bits

[5:0] dq_map_3_0_next
Controls DQ mapping for bits [3:0] of the DQ bus.

3.3.155 dq_map_control_31_16_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_31_16_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x384`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

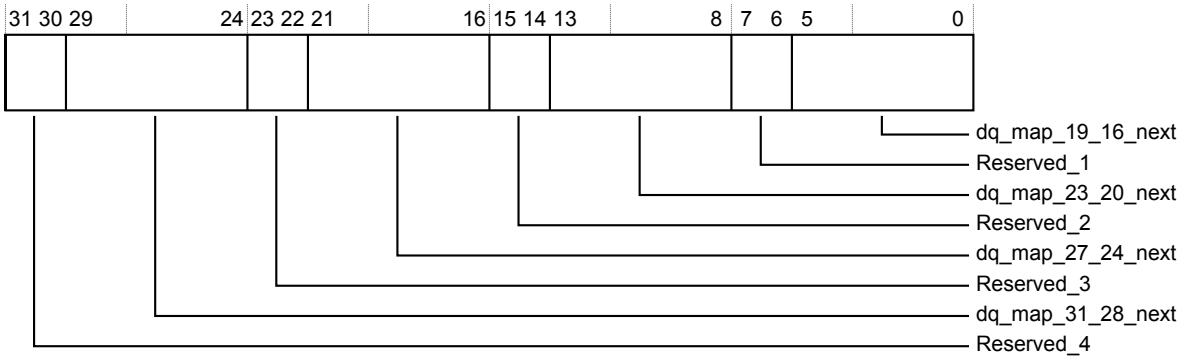

Figure 3-155 dq_map_control_31_16_next register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4
Unused bits

[29:24] dq_map_31_28_next
Controls DQ mapping for bits [31:28] of the DQ bus.

[23:22] Reserved_3
Unused bits

[21:16] dq_map_27_24_next
Controls DQ mapping for bits [27:24] of the DQ bus.

[15:14] Reserved_2
Unused bits

[13:8] dq_map_23_20_next
Controls DQ mapping for bits [23:20] of the DQ bus.

[7:6] Reserved_1
Unused bits

[5:0] dq_map_19_16_next
Controls DQ mapping for bits [19:16] of the DQ bus.

3.3.156 dq_map_control_47_32_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_47_32_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x388`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

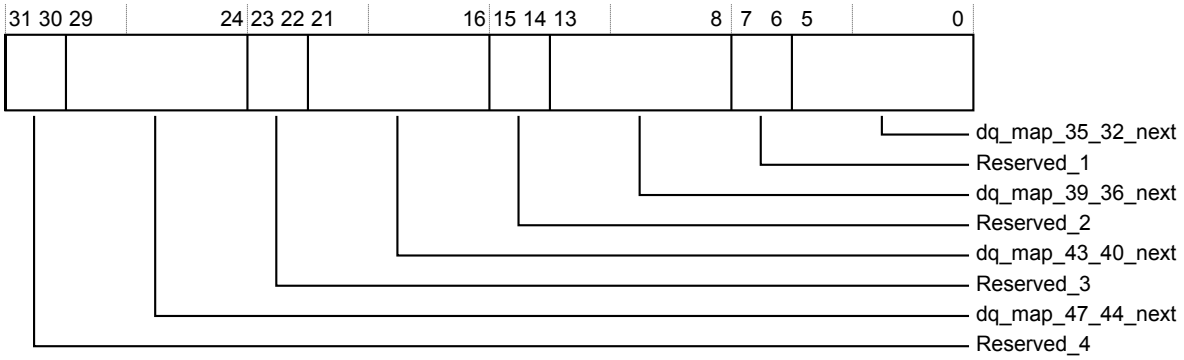

Figure 3-156 dq_map_control_47_32_next register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4
Unused bits

[29:24] dq_map_47_44_next
Controls DQ mapping for bits [47:44] of the DQ bus.

[23:22] Reserved_3
Unused bits

[21:16] dq_map_43_40_next
Controls DQ mapping for bits [43:40] of the DQ bus.

[15:14] Reserved_2
Unused bits

[13:8] dq_map_39_36_next
Controls DQ mapping for bits [39:36] of the DQ bus.

[7:6] Reserved_1
Unused bits

[5:0] dq_map_35_32_next
Controls DQ mapping for bits [35:32] of the DQ bus.

3.3.157 dq_map_control_63_48_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_63_48_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x38C`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

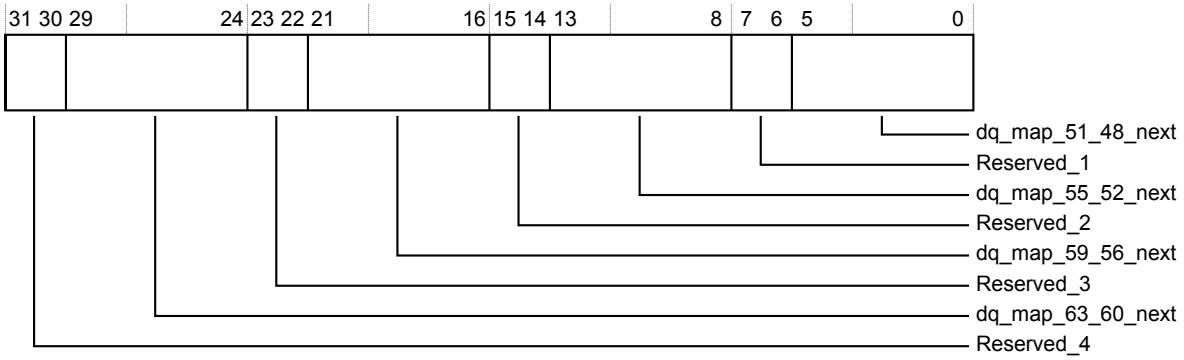

Figure 3-157 dq_map_control_63_48_next register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4
Unused bits

[29:24] dq_map_63_60_next
Controls DQ mapping for bits [63:60] of the DQ bus.

[23:22] Reserved_3
Unused bits

[21:16] dq_map_59_56_next
Controls DQ mapping for bits [59:56] of the DQ bus.

[15:14] Reserved_2
Unused bits

[13:8] dq_map_55_52_next
Controls DQ mapping for bits [55:52] of the DQ bus.

[7:6] Reserved_1
Unused bits

[5:0] dq_map_51_48_next
Controls DQ mapping for bits [51:48] of the DQ bus.

3.3.158 dq_map_control_71_64_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation.

The dq_map_control_71_64_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x390`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

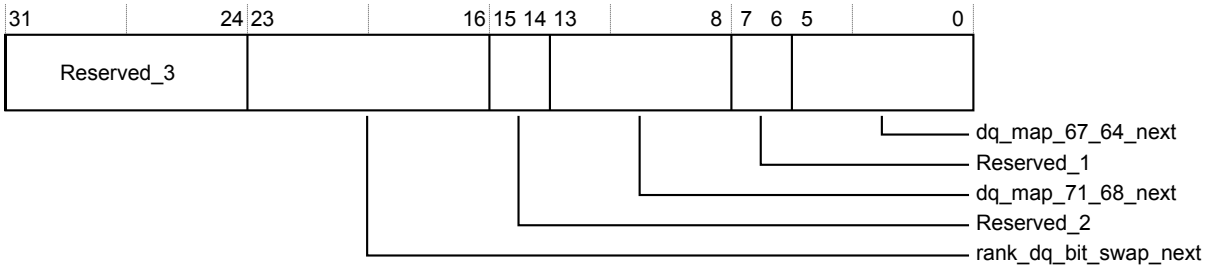

Figure 3-158 dq_map_control_71_64_next register bit assignments

The following shows the bit assignments.

[31:24] Reserved_3
Unused bits

[23:16] rank_dq_bit_swap_next
Each bit determines if the DQ bus has bit swapping as per the DDR4 RDIMM Design Specification applied to the corresponding rank. Normally, this bit must be set high for odd physical ranks.

[15:14] Reserved_2
Unused bits

[13:8] dq_map_71_68_next
Controls DQ mapping for bits [71:68] of the DQ bus. This corresponds to CB [7:4] on the DIMM.

[7:6] Reserved_1
Unused bits

[5:0] dq_map_67_64_next
Controls DQ mapping for bits [67:64] of the DQ bus. This corresponds to CB [3:0] on the DIMM.

3.3.159 rank_status

Shows the current status of geardown, MPD and CAL.

The rank_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x398`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

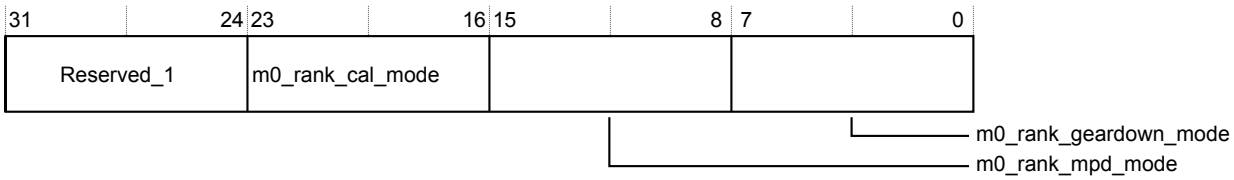

Figure 3-159 rank_status register bit assignments

The following shows the bit assignments.

[31:24] Reserved_1
Unused bits
[23:16] m0_rank_cal_mode
One-bit per rank indicating if the rank is in CAL mode
[15:8] m0_rank_mpd_mode
One-bit per rank indicating if the rank is in MPD mode
[7:0] m0_rank_geardown_mode
One-bit per rank indicating if the rank is in geardown mode

3.3.160 mode_change_status

Shows the current status of the sequence that is currently being processed.

The mode_change_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x39C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

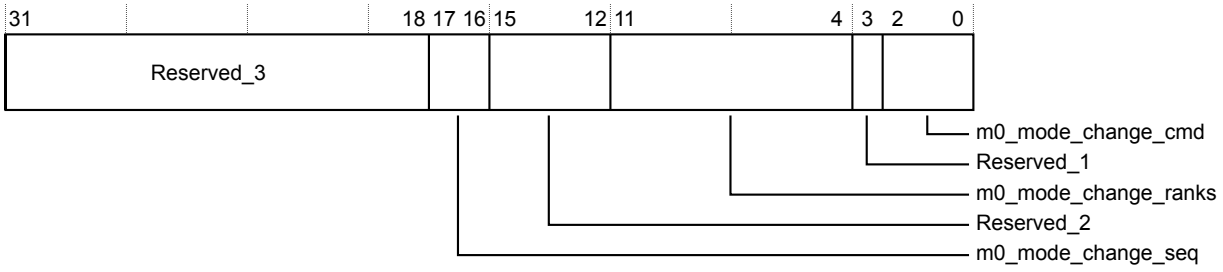

Figure 3-160 mode_change_status register bit assignments

The following shows the bit assignments.

[31:18] Reserved_3
Unused bits
[17:16] m0_mode_change_seq
The sequence position the mode change is performing.
[15:12] Reserved_2
Unused bits
[11:4] m0_mode_change_ranks
One-bit per rank indicating the ranks being targeted by the command.
[3] Reserved_1
Unused bits
[2:0] m0_mode_change_cmd
The command being performed.

3.3.161 user_status

Shows the value of the input user_status signals.

The user_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x400`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

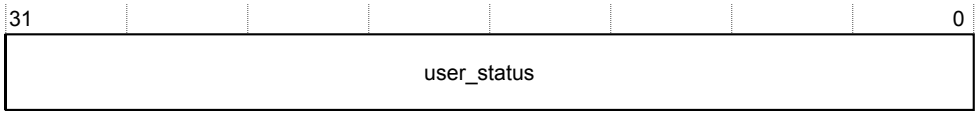

Figure 3-161 user_status register bit assignments

The following shows the bit assignments.

[31:0] user_status
user_status bitfield.

3.3.162 user_config0_next

Drives the output user_config0 signal.

The user_config0_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x408`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

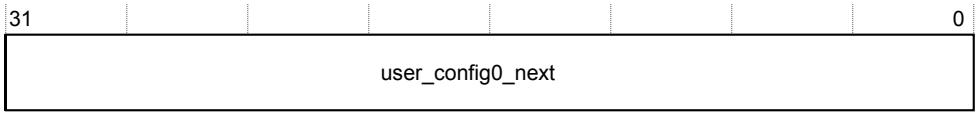

Figure 3-162 user_config0_next register bit assignments

The following shows the bit assignments.

[31:0] user_config0_next
user_config0_next bitfield.

3.3.163 user_config1_next

Drives the output user_config1 signal.

The user_config1_next register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x40C
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

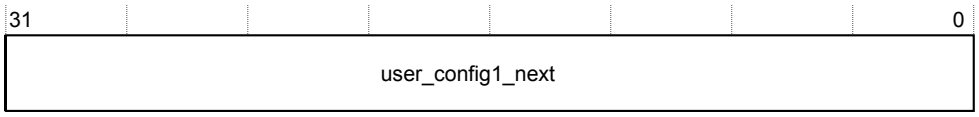

Figure 3-163 user_config1_next register bit assignments

The following shows the bit assignments.

[31:0] user_config1_next
user_config1_next bitfield.

3.3.164 user_config2

Drives the output user_config2 signal.

The user_config2 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x410
Type	Read-write
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

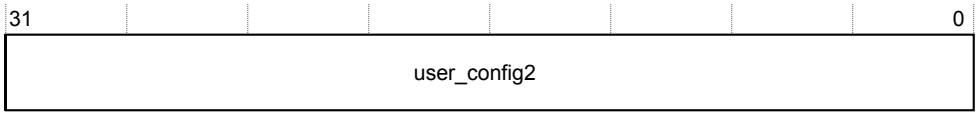

Figure 3-164 user_config2 register bit assignments

The following shows the bit assignments.

[31:0] user_config2
user_config2 bitfield.

3.3.165 user_config3

Drives the output user_config3 signal.

The user_config3 register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x414
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

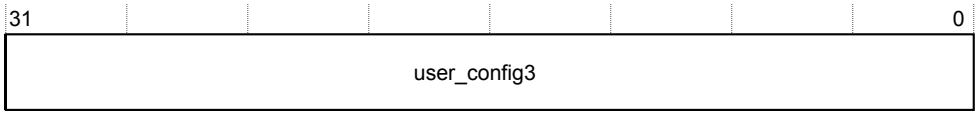

Figure 3-165 user_config3 register bit assignments

The following shows the bit assignments.

[31:0] user_config3
user_config3 bitfield.

3.3.166 interrupt_control

Configures interrupt behavior.

The interrupt_control register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x500
Type Read-write
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

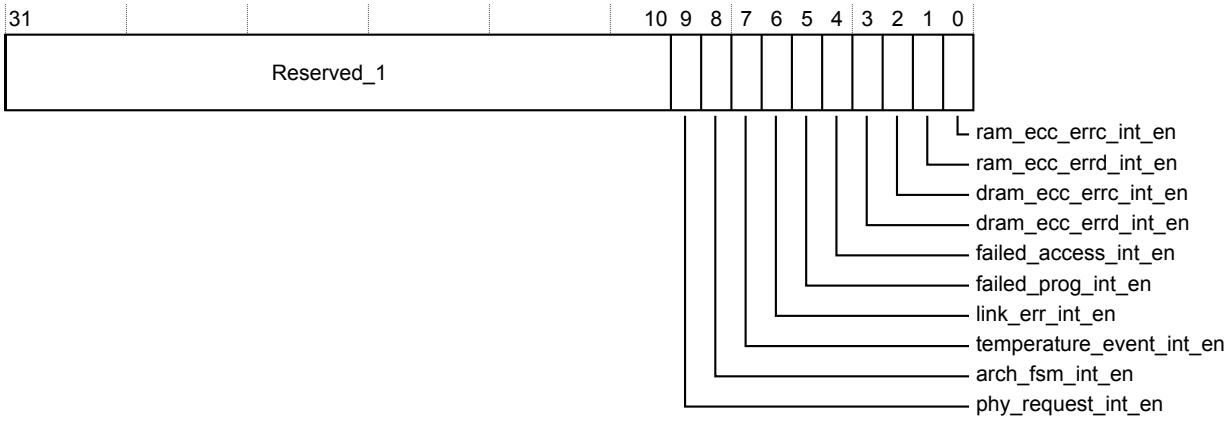

Figure 3-166 interrupt_control register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits

[9] phy_request_int_en
Program to enable or disable the PHY request interrupt.
[8] arch_fsm_int_en
Program to enable or disable the architectural fsm interrupt.
[7] temperature_event_int_en
Program to enable or disable the temperature event interrupt.
[6] link_err_int_en
Program to enable or disable the link error interrupt.
[5] failed_prog_int_en
Program to enable or disable the failed programmer's access interrupt.
[4] failed_access_int_en
Program to enable or disable the failed system access interrupt.
[3] dram_ecc_errd_int_en
Program to enable or disable the dram uncorrected error interrupt.
[2] dram_ecc_errc_int_en
Program to enable or disable the dram corrected error interrupt.
[1] ram_ecc_errd_int_en
Program to enable or disable the ram uncorrected error interrupt.
[0] ram_ecc_errc_int_en
Program to enable or disable the ram corrected error interrupt.

3.3.167 interrupt_clr

Clear register for interrupts.

The interrupt_clr register characteristics are:

Usage constraints
Cannot be read from. Can be written to when in ALL states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x508`
Type	Write-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

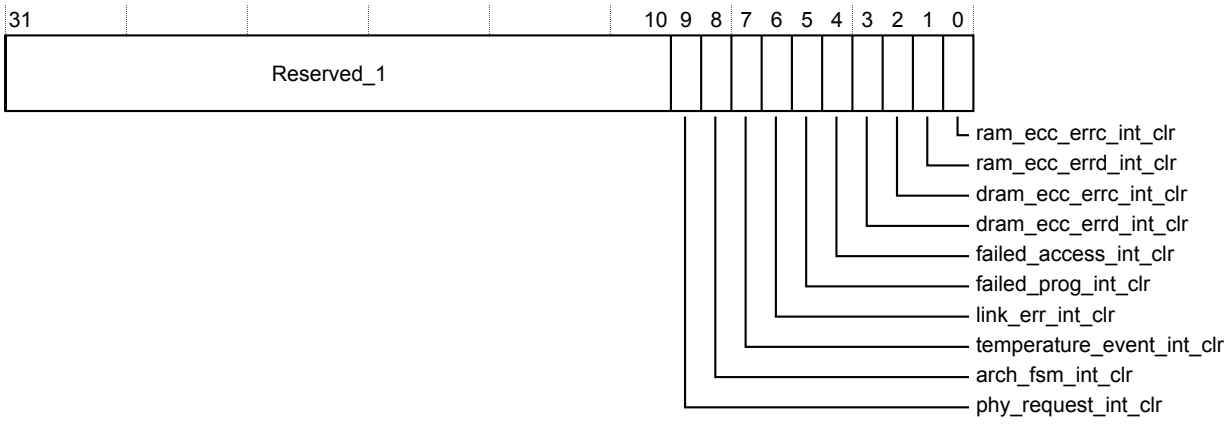

Figure 3-167 interrupt_clr register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits
[9] phy_request_int_clr
Program to clear the PHY request interrupt.
[8] arch_fsm_int_clr
Program to clear the architectural fsm interrupt.
[7] temperature_event_int_clr
Program to clear the temperature event interrupt.
[6] link_err_int_clr
Program to clear the link error interrupt.
[5] failed_prog_int_clr
Program to clear the failed programmer's access interrupt.
[4] failed_access_int_clr
Program to clear the failed system access interrupt.
[3] dram_ecc_errd_int_clr
Program to clear the dram uncorrected error interrupt.
[2] dram_ecc_errc_int_clr
Program to clear the dram corrected error interrupt.
[1] ram_ecc_errd_int_clr
Program to clear the ram uncorrected error interrupt.
[0] ram_ecc_errc_int_clr
Program to clear the ram corrected error interrupt.

3.3.168 interrupt_status

Status register for interrupts (pre-mask).

The interrupt_status register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x510`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

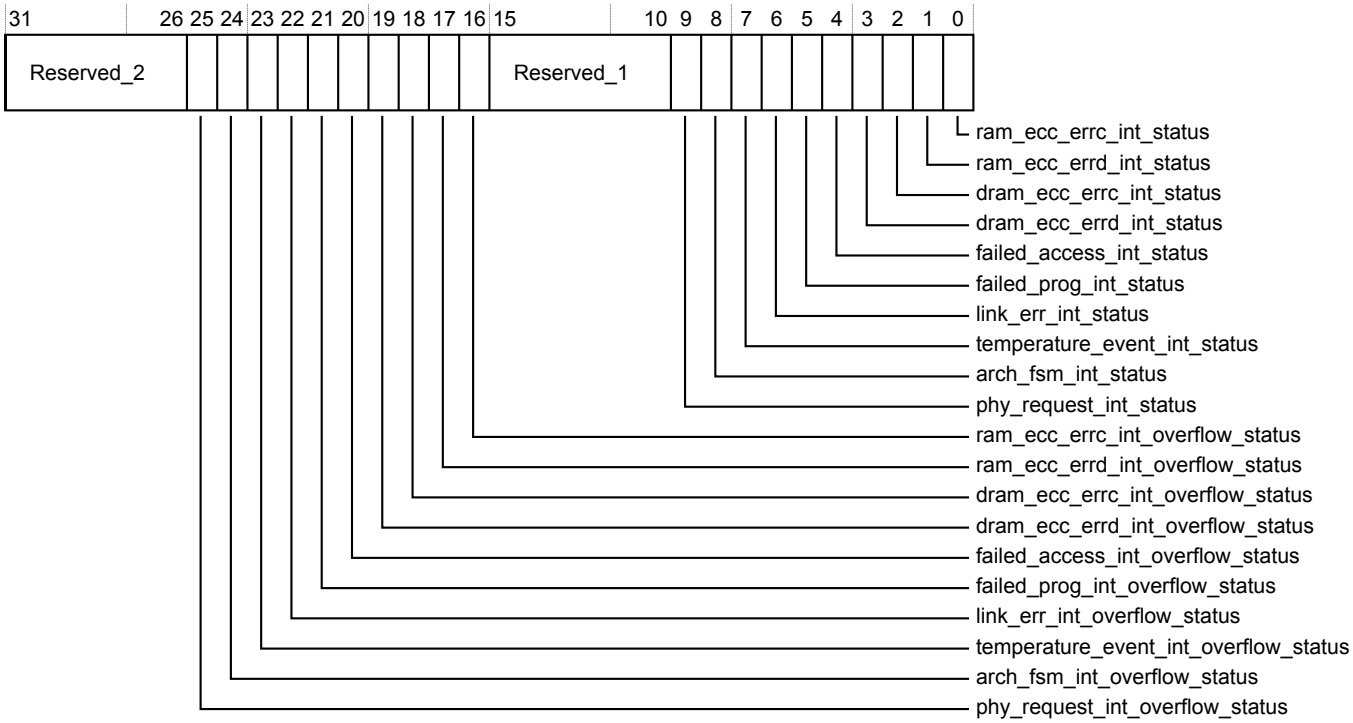

Figure 3-168 interrupt_status register bit assignments

The following shows the bit assignments.

[31:26] Reserved_2
Unused bits

[25] phy_request_int_overflow_status
Shows the status of the PHY request interrupt overflow.

[24] arch_fsm_int_overflow_status
Shows the status of the architectural fsm interrupt overflow.

[23] temperature_event_int_overflow_status
Shows the status of the link failure interrupt overflow.

[22] link_err_int_overflow_status
Shows the status of the link error interrupt overflow.

[21] failed_prog_int_overflow_status
Shows the status of the failed programmer's access interrupt overflow.

[20] failed_access_int_overflow_status
Shows the status of the failed system access interrupt overflow.

[19] dram_ecc_errd_int_overflow_status
Shows the status of the DRAM uncorrected error interrupt overflow.

[18] dram_ecc_errc_int_overflow_status
Shows the status of the DRAM corrected error interrupt overflow.

[17] ram_ecc_errd_int_overflow_status
Shows the status of the RAM uncorrected error interrupt overflow.

[16] ram_ecc_errc_int_overflow_status
Shows the status of the RAM corrected error interrupt overflow.

[15:10] Reserved_1
Unused bits

[9] phy_request_int_status
Shows the status of the PHY request interrupt.

[8] arch_fsm_int_status
Shows the status of the architectural fsm interrupt.

[7] temperature_event_int_status
Shows the status of the temperature event interrupt.
[6] link_err_int_status
Shows the status of the link error interrupt.
[5] failed_prog_int_status
Shows the status of the failed programmer's access interrupt.
[4] failed_access_int_status
Shows the status of the failed system access interrupt.
[3] dram_ecc_errd_int_status
Shows the status of the DRAM uncorrected error interrupt.
[2] dram_ecc_errc_int_status
Shows the status of the DRAM corrected error interrupt.
[1] ram_ecc_errd_int_status
Shows the status of the RAM uncorrected error interrupt.
[0] ram_ecc_errc_int_status
Shows the status of the RAM corrected error interrupt.

3.3.169 ram_ecc_errc_int_info_31_00

Shows information relating to the interrupt

The ram_ecc_errc_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x518`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

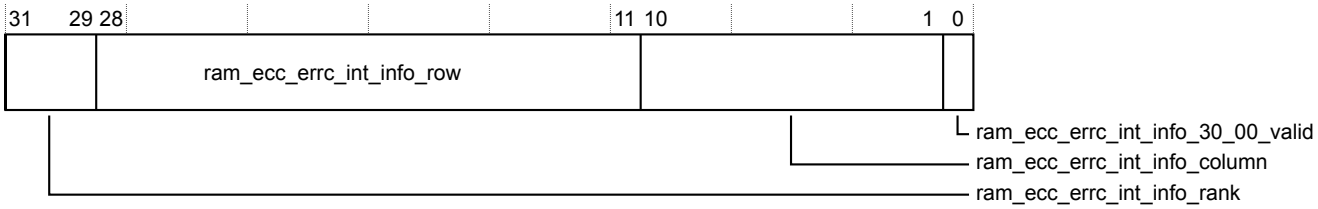

Figure 3-169 ram_ecc_errc_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:29] ram_ecc_errc_int_info_rank
Rank.
[28:11] ram_ecc_errc_int_info_row
Row.
[10:1] ram_ecc_errc_int_info_column
Column.
[0] ram_ecc_errc_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. 1 indicates it is valid and that no overflow has occurred.

3.3.170 ram_ecc_errc_int_info_63_32

Shows information relating to the interrupt

The ram_ecc_errc_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x51C

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

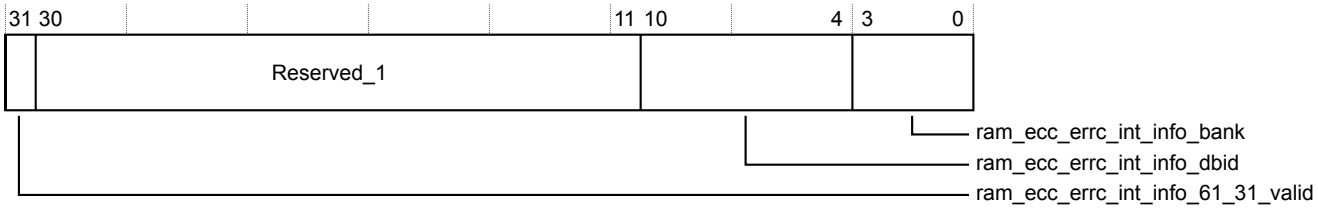

Figure 3-170 ram_ecc_errc_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] ram_ecc_errc_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. 1 indicates it is valid and that no overflow has occurred.

[30:11] Reserved_1
Unused bits

[10:4] ram_ecc_errc_int_info_dbid
Data Buffer ID.

[3:0] ram_ecc_errc_int_info_bank
Bank.

3.3.171 ram_ecc_errd_int_info_31_00

Shows information relating to the interrupt

The ram_ecc_errd_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x520

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

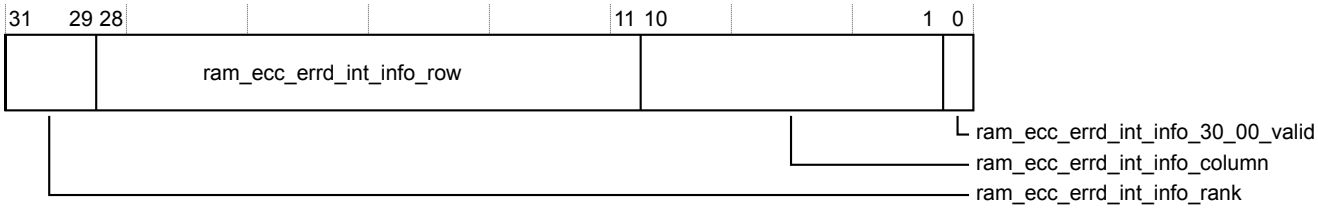

Figure 3-171 ram_ecc_errd_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:29] ram_ecc_errd_int_info_rank
Rank.

[28:11] ram_ecc_errd_int_info_row
Row.

[10:1] ram_ecc_errd_int_info_column
Column.

[0] ram_ecc_errd_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

3.3.172 ram_ecc_errd_int_info_63_32

Shows information relating to the interrupt

The ram_ecc_errd_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x524`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

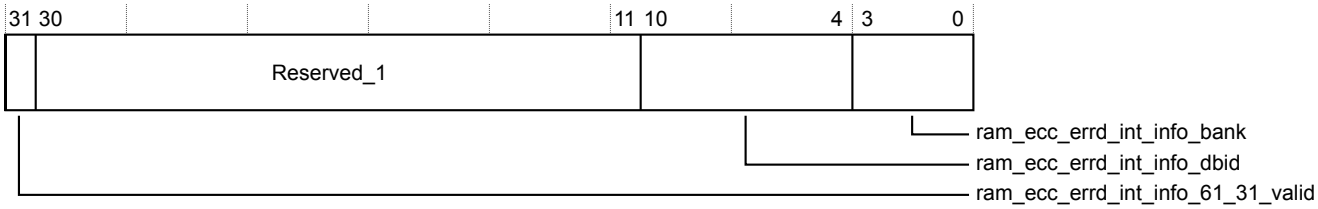

Figure 3-172 ram_ecc_errd_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] ram_ecc_errd_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

[30:11] Reserved_1
Unused bits

[10:4] ram_ecc_errd_int_info_dbid
Data Buffer ID.
[3:0] ram_ecc_errd_int_info_bank
Bank.

3.3.173 dram_ecc_errc_int_info_31_00

Shows information relating to the interrupt

The dram_ecc_errc_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x528`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

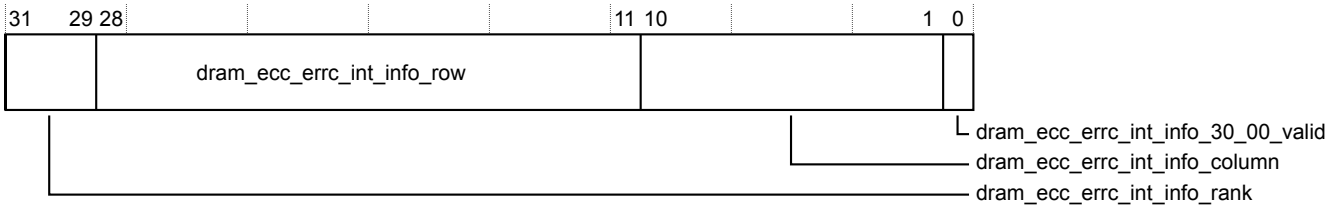

Figure 3-173 dram_ecc_errc_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:29] dram_ecc_errc_int_info_rank
Rank.
[28:11] dram_ecc_errc_int_info_row
Row.
[10:1] dram_ecc_errc_int_info_column
Column.
[0] dram_ecc_errc_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

3.3.174 dram_ecc_errc_int_info_63_32

Shows information relating to the interrupt

The dram_ecc_errc_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x52C`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

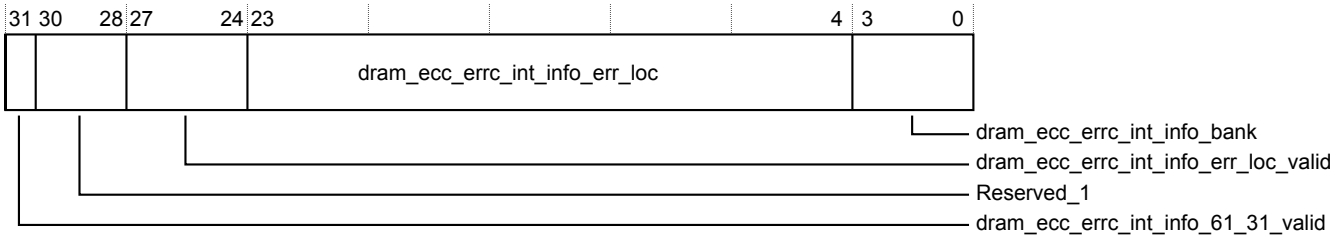

Figure 3-174 dram_ecc_errc_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] dram_ecc_errc_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. 1 indicates it is valid and that no overflow has occurred.

[30:28] Reserved_1
Unused bits

[27:24] dram_ecc_errc_int_info_err_loc_valid
Error location valid.

[23:4] dram_ecc_errc_int_info_err_loc
Error location containing 4 sets of 5-bit nibble locations indicating which of the 18 possible nibble locations (0..17) each error was found in.

[3:0] dram_ecc_errc_int_info_bank
Bank.

3.3.175 dram_ecc_errd_int_info_31_00

Shows information relating to the interrupt

The dram_ecc_errd_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x530`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

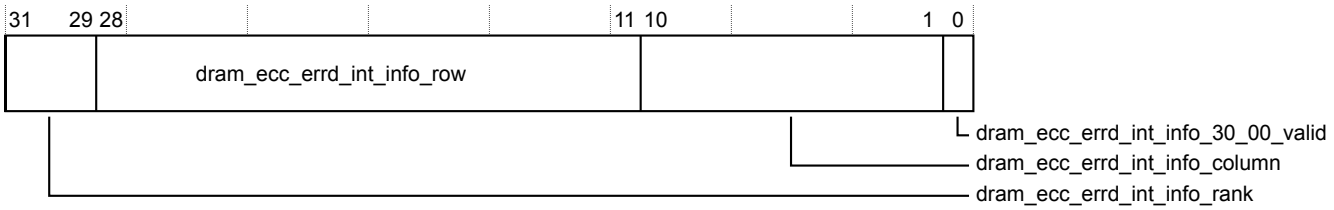

Figure 3-175 dram_ecc_errd_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:29] dram_ecc_errd_int_info_rank
Rank.
[28:11] dram_ecc_errd_int_info_row
Row.
[10:1] dram_ecc_errd_int_info_column
Column.
[0] dram_ecc_errd_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

3.3.176 dram_ecc_errd_int_info_63_32

Shows information relating to the interrupt

The dram_ecc_errd_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x534`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

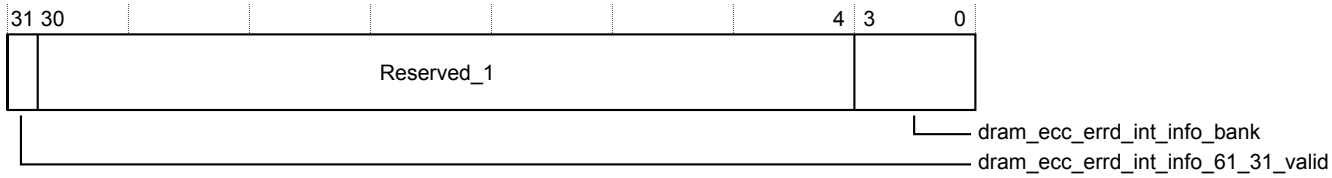

Figure 3-176 dram_ecc_errd_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] dram_ecc_errd_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.
[30:4] Reserved_1
Unused bits
[3:0] dram_ecc_errd_int_info_bank
Bank.

3.3.177 failed_access_int_info_31_00

Shows information relating to the interrupt

The failed_access_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x538
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

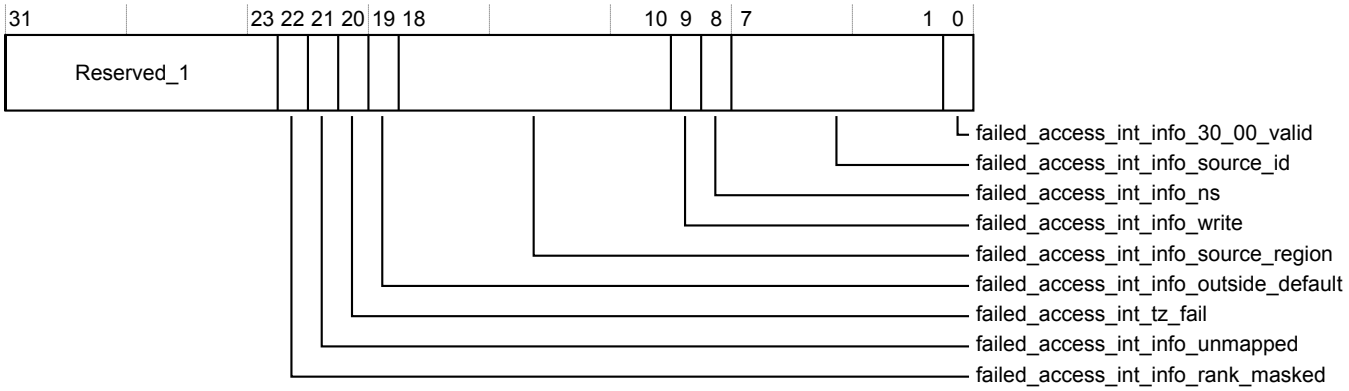

Figure 3-177 failed_access_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:23] Reserved_1
Unused bits
[22] failed_access_int_info_rank_masked
Access to a masked rank.
[21] failed_access_int_info_unmapped
Access to an unmapped (reserved) system address location.
[20] failed_access_int_tz_fail
Access failed the security checks of the matching regions
[19] failed_access_int_info_outside_default
Access to a memory address location greater than the maximum address of the default region
[18:10] failed_access_int_info_source_region
Address region of the failed access. The lower 8 bits map to address regions 0 to 7. The upper bit maps to the default region.
[9] failed_access_int_info_write
Direction of the failed access. When HIGH the access is a write.
[8] failed_access_int_info_ns
Security setting of the failed access. When HIGH the access is Non-secure.
[7:1] failed_access_int_info_source_id
Source ID of the failed access
[0] failed_access_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

3.3.178 failed_access_int_info_63_32

Shows information relating to the interrupt

The failed_access_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x53C
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

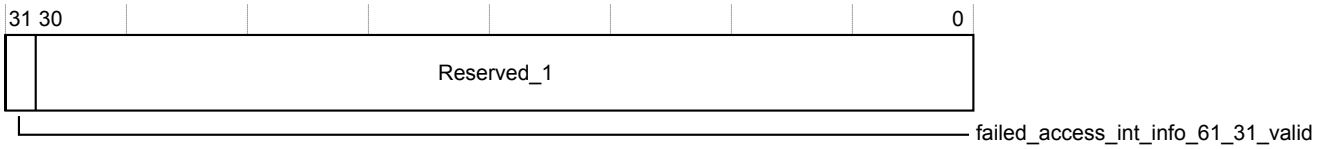

Figure 3-178 failed_access_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] failed_access_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

[30:0] Reserved_1
Unused bits

3.3.179 failed_prog_int_info_31_00

Shows information relating to the interrupt

The failed_prog_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x540
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

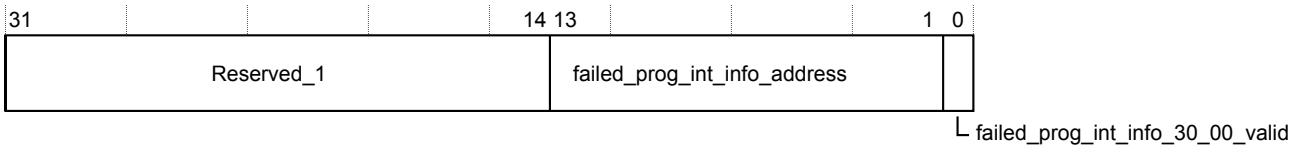

Figure 3-179 failed_prog_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:14] Reserved_1
Unused bits

[13:1] failed_prog_int_info_address
Register address (paddr[12:0]).

[0] failed_prog_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

3.3.180 failed_prog_int_info_63_32

Shows information relating to the interrupt

The failed_prog_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x544`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

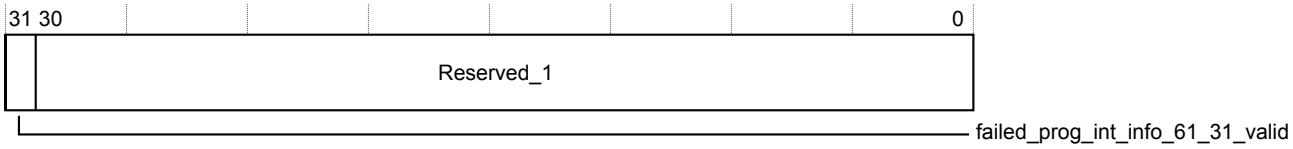

Figure 3-180 failed_prog_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] failed_prog_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

[30:0] Reserved_1
Unused bits

3.3.181 link_err_int_info_31_00

Shows information relating to the interrupt

The link_err_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x548`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

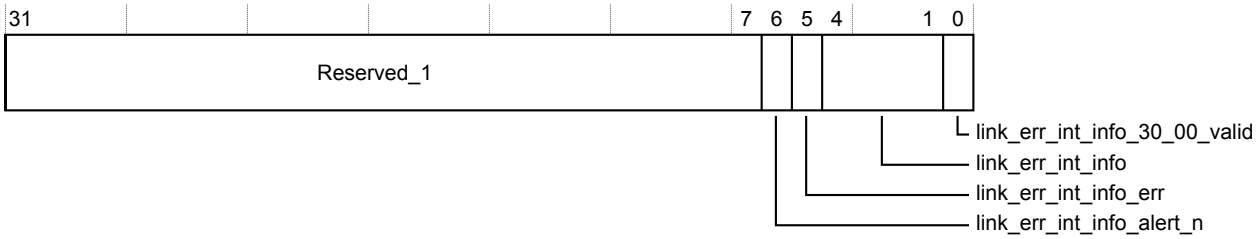

Figure 3-181 link_err_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:7] Reserved_1
Unused bits

[6] link_err_int_info_alert_n
Returns the value sent on the dfi_alert_n signal.

[5] link_err_int_info_err
Returns the value sent on the dfi_err signal.

[4:1] link_err_int_info
For a dfi_err error, returns the corresponding value sent on dfi_err_info. For all other errors it is not used.

[0] link_err_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

3.3.182 link_err_int_info_63_32

Shows information relating to the interrupt

The link_err_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x54C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

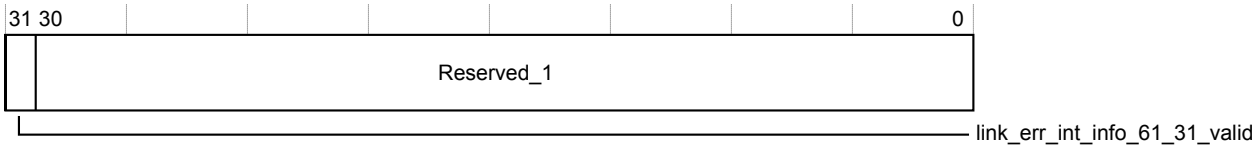

Figure 3-182 link_err_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] link_err_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

[30:0] Reserved_1
Unused bits

3.3.183 arch_fsm_int_info_31_00

Shows information relating to the interrupt

The arch_fsm_int_info_31_00 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x550`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

Figure 3-183 arch_fsm_int_info_31_00 register bit assignments

The following shows the bit assignments.

[31:3] Reserved_1
Unused bits

[2] arch_fsm_int_info_mgr_dci_failed
A direct command in a previous sequence has failed.

[1] arch_fsm_int_info_aborted
Signals that the transition completed cleanly or was aborted.

[0] arch_fsm_int_info_30_00_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

3.3.184 arch_fsm_int_info_63_32

Shows information relating to the interrupt

The arch_fsm_int_info_63_32 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x554`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

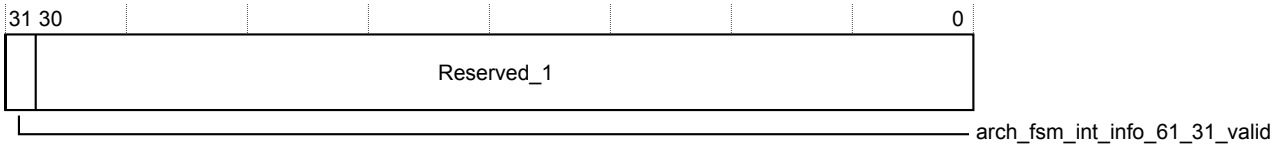

Figure 3-184 arch_fsm_int_info_63_32 register bit assignments

The following shows the bit assignments.

[31] arch_fsm_int_info_61_31_valid
Indicates if an overflow (single interrupt overflow, or multiple interrupt overflow) has occurred and whether the interrupt information is valid. One indicates it is valid and that no overflow has occurred.

[30:0] Reserved_1
Unused bits

3.3.185 integ_cfg

Integration test register to enable integration test mode.

The integ_cfg register characteristics are:

Usage constraints
Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0xE00`
Type	Read-write
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

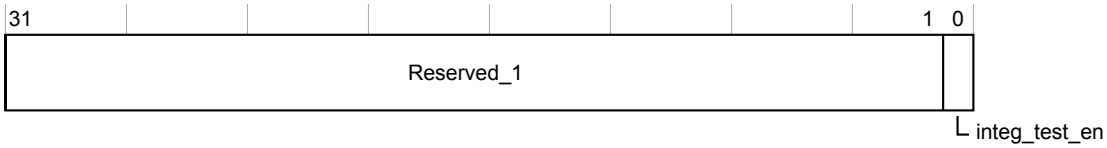

Figure 3-185 integ_cfg register bit assignments

The following shows the bit assignments.

[31:1] Reserved_1
Unused bits

[0] integ_test_en
integ_test_en bitfield. The supported range for this bitfield is 0-1.

3.3.186 integ_outputs

Drives the value of outputs when in integration test mode.

The integ_outputs register characteristics are:

Usage constraints
Cannot be read from. Can be written to when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0xE08`
Type	Write-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

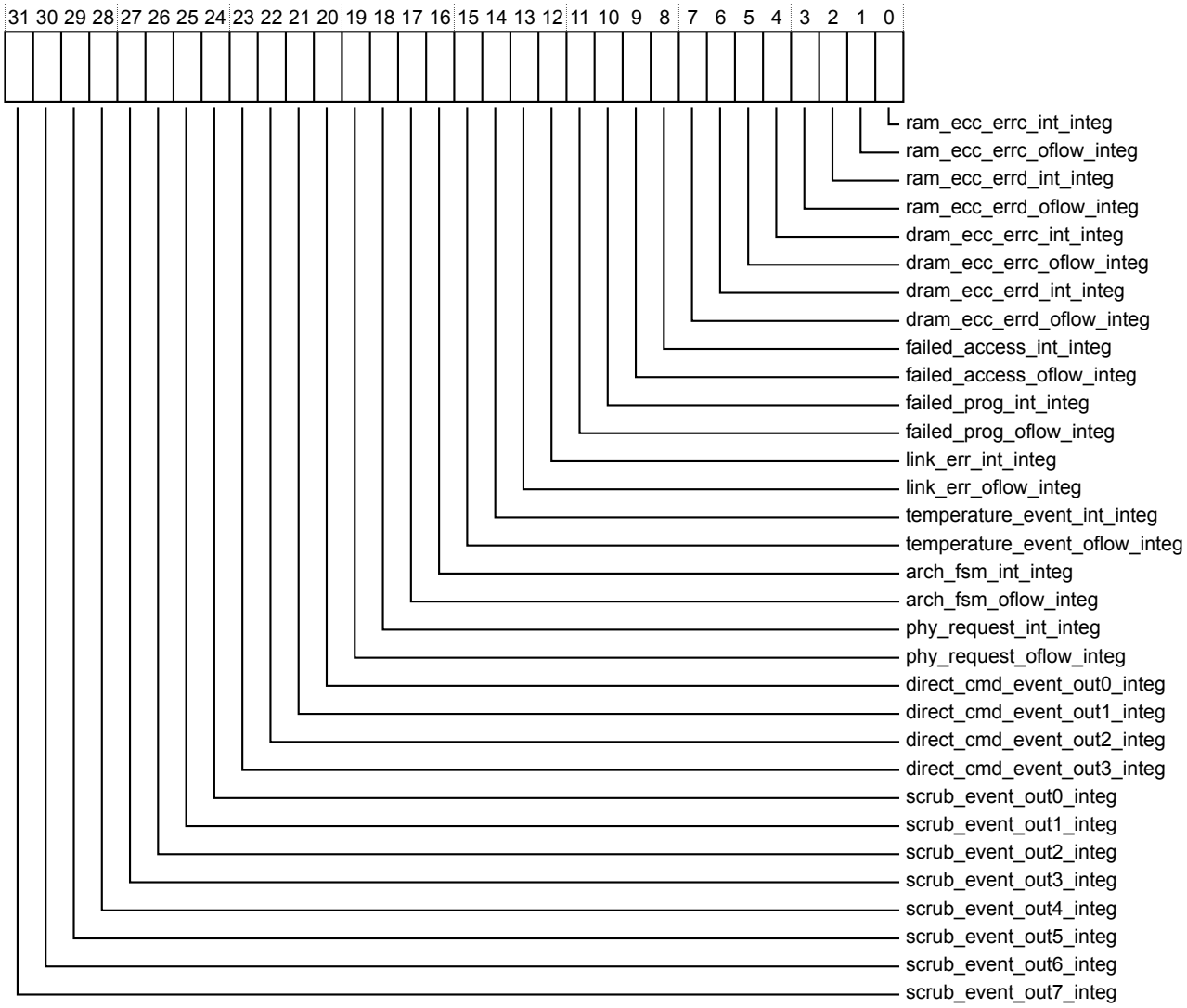

Figure 3-186 integ_outputs register bit assignments

The following shows the bit assignments.

[31] scrub_event_out7_integ

scrub_event_out7_integ bitfield.

[30] scrub_event_out6_integ

scrub_event_out6_integ bitfield.

[29] scrub_event_out5_integ

scrub_event_out5_integ bitfield.

[28] scrub_event_out4_integ
scrub_event_out4_integ bitfield.
[27] scrub_event_out3_integ
scrub_event_out3_integ bitfield.
[26] scrub_event_out2_integ
scrub_event_out2_integ bitfield.
[25] scrub_event_out1_integ
scrub_event_out1_integ bitfield.
[24] scrub_event_out0_integ
scrub_event_out0_integ bitfield.
[23] direct_cmd_event_out3_integ
direct_cmd_event_out3_integ bitfield.
[22] direct_cmd_event_out2_integ
direct_cmd_event_out2_integ bitfield.
[21] direct_cmd_event_out1_integ
direct_cmd_event_out1_integ bitfield.
[20] direct_cmd_event_out0_integ
direct_cmd_event_out0_integ bitfield.
[19] phy_request_oflow_integ
phy_request_oflow_integ bitfield.
[18] phy_request_int_integ
phy_request_int_integ bitfield.
[17] arch_fsm_oflow_integ
arch_fsm_oflow_integ bitfield.
[16] arch_fsm_int_integ
arch_fsm_int_integ bitfield.
[15] temperature_event_oflow_integ
temperature_event_oflow_integ bitfield.
[14] temperature_event_int_integ
temperature_event_int_integ bitfield.
[13] link_err_oflow_integ
link_err_oflow_integ bitfield.
[12] link_err_int_integ
link_err_int_integ bitfield.
[11] failed_prog_oflow_integ
failed_prog_oflow_integ bitfield.
[10] failed_prog_int_integ
failed_prog_int_integ bitfield.
[9] failed_access_oflow_integ
failed_access_oflow_integ bitfield.
[8] failed_access_int_integ
failed_access_int_integ bitfield.
[7] dram_ecc_errd_oflow_integ
dram_ecc_errd_oflow_integ bitfield.
[6] dram_ecc_errd_int_integ
dram_ecc_errd_int_integ bitfield.
[5] dram_ecc_errc_oflow_integ
dram_ecc_errc_oflow_integ bitfield.
[4] dram_ecc_errc_int_integ
dram_ecc_errc_int_integ bitfield.
[3] ram_ecc_errd_oflow_integ
ram_ecc_errd_oflow_integ bitfield.
[2] ram_ecc_errd_int_integ
ram_ecc_errd_int_integ bitfield.
[1] ram_ecc_errc_oflow_integ
ram_ecc_errc_oflow_integ bitfield.

[0] ram_ecc_errc_int_integ
ram_ecc_errc_int_integ bitfield.

3.3.187 address_control_now

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values.

The address_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1010`
Type	Read-only
Reset	`0x00030202`
Width	32

The following figure shows the bit assignments.

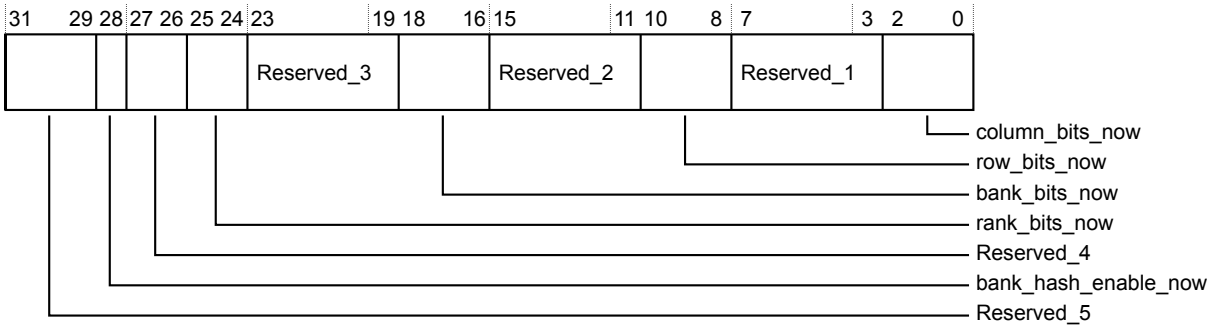

Figure 3-187 address_control_now register bit assignments

The following shows the bit assignments.

[31:29] Reserved_5
Unused bits

[28] bank_hash_enable_now
Configures the bank hash function used in system address decode. Used to alter traffic distribution across banks.

[27:26] Reserved_4
Unused bits

[25:24] rank_bits_now
Program to match the number of active ranks to be addressed.

[23:19] Reserved_3
Unused bits

[18:16] bank_bits_now
Program to match the number of banks per chip-select (rank) on the attached DRAM device.

——— **Note** ———

This number corresponds to the sum total of all banks in all bank groups (where applicable) on a device.

———————————

[15:11] Reserved_2
Unused bits

[10:8] row_bits_now
Program to match the number of row bits on the attached DRAM device.

[7:3] Reserved_1
Unused bits

[2:0] column_bits_now
Program to match the number of column address bits present on the DRAM device.

3.3.188 decode_control_now

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, bank, row address, and the column address.

The decode_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1014`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

Figure 3-188 decode_control_now register bit assignments

The following shows the bit assignments.

[31:7] Reserved_2
Unused bits

[6:4] stripe_decode_now
Determines the address boundary on which to stripe system requests across DRAM pages. The DMC decodes the bottom two page address bits from a programmable slice within the lowest 14 bits of the system address. To disable sub-page striping you must program this value to the DRAM page size (or use the default value 0). Note: you must not program the DMC to stripe at a higher boundary than the DRAM page size.

[3:2] Reserved_1
Unused bits

[1:0] address_decode_now
Determines in which pattern the DRAM address components are decoded from the system address.

3.3.189 address_map_now

Configures the system address mapping options.

The address_map_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x101C`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

Figure 3-189 address_map_now register bit assignments

The following shows the bit assignments.

[31:16] addr_map_mask_now

Configures the mask applied to system address bits [43:28]. The system address map uses upper address bits to select from multiple DMC instances in a system. The DMC must discard these address bits that fall outside physical memory to decode correctly.

[15:3] Reserved_1

Unused bits

[2:0] addr_map_mode_now

Selects the address translation mode. See the System Address Conversion section of the Design Manual for more information on address translation options.

3.3.190 low_power_control_now

Configures the low-power features of the DMC.

The low_power_control_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1020`

Type Read-only

Reset `0x00000020`

Width 32

The following figure shows the bit assignments.

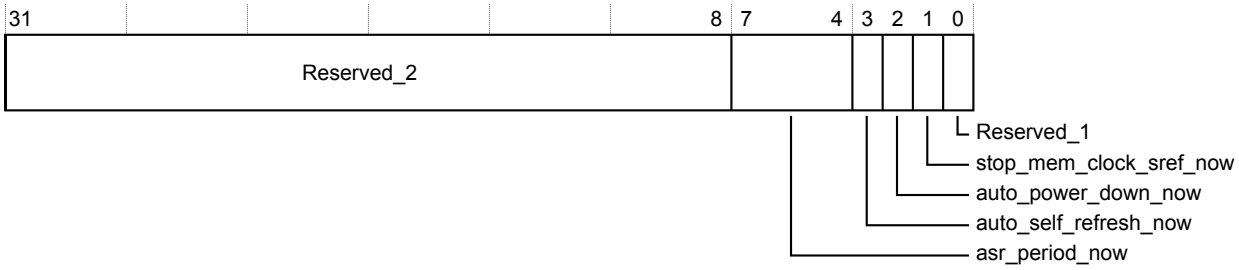

Figure 3-190 low_power_control_now register bit assignments

The following shows the bit assignments.

[31:8] Reserved_2
Unused bits

[7:4] asr_period_now
Program the number of tREFI intervals to wait without activity before placing the DRAM into a self-refresh state when auto_self_refresh is enabled. The supported range for this bitfield is 1-15.

[3] auto_self_refresh_now
Program to enable or disable placing a DRAM rank into a self-refresh state when the rank has been idle for the amount of time that asr_period defines.

[2] auto_power_down_now
Program to enable or disable placing the DRAM into a power-down state when idle.

[1] stop_mem_clock_sref_now
Program to enable or disable stopping the DRAM clock when the memory device is in self-refresh, reset, or maximum power down.

[0] Reserved_1
Unused bits

3.3.191 turnaround_control_now

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus.

The turnaround_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1028`
Type	Read-only
Reset	`0x0F0F0F0F`
Width	32

The following figure shows the bit assignments.

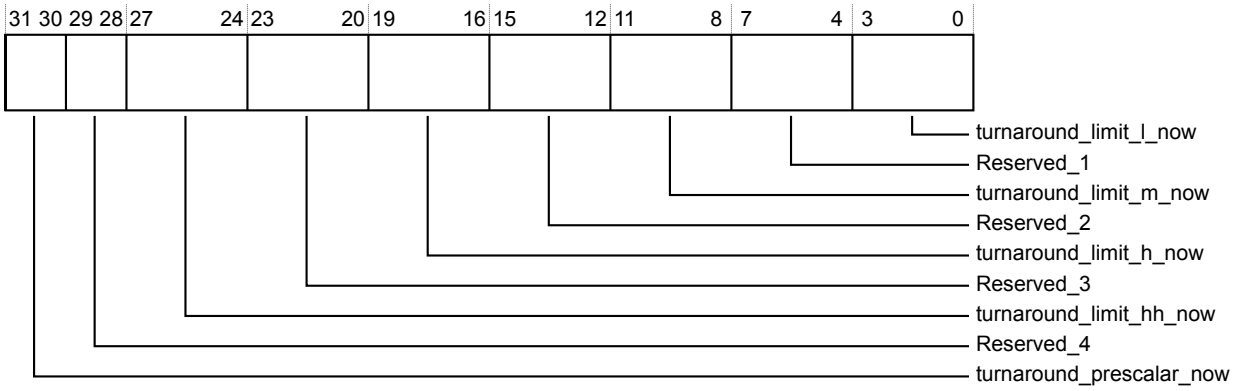

Figure 3-191 turnaround_control_now register bit assignments

The following shows the bit assignments.

[31:30] turnaround_prescalar_now
Turnaround counter prescaler.

[29:28] Reserved_4
Unused bits

[27:24] turnaround_limit_hh_now
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of HIGH-HIGH class requests. The supported range for this bitfield is 0-15.

[23:20] Reserved_3
Unused bits

[19:16] turnaround_limit_h_now
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of HIGH class requests. The supported range for this bitfield is 0-15.

[15:12] Reserved_2
Unused bits

[11:8] turnaround_limit_m_now
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of MEDIUM class requests. The supported range for this bitfield is 0-15.

[7:4] Reserved_1
Unused bits

[3:0] turnaround_limit_l_now
Program the number of turnaround prescaler periods to wait between arbitrating a turnaround in the presence of LOW class requests. The supported range for this bitfield is 0-15.

3.3.192 hit_turnaround_control_now

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams.

The hit_turnaround_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x102C`
Type	Read-only
Reset	`0x08101F1F`
Width	32

The following figure shows the bit assignments.

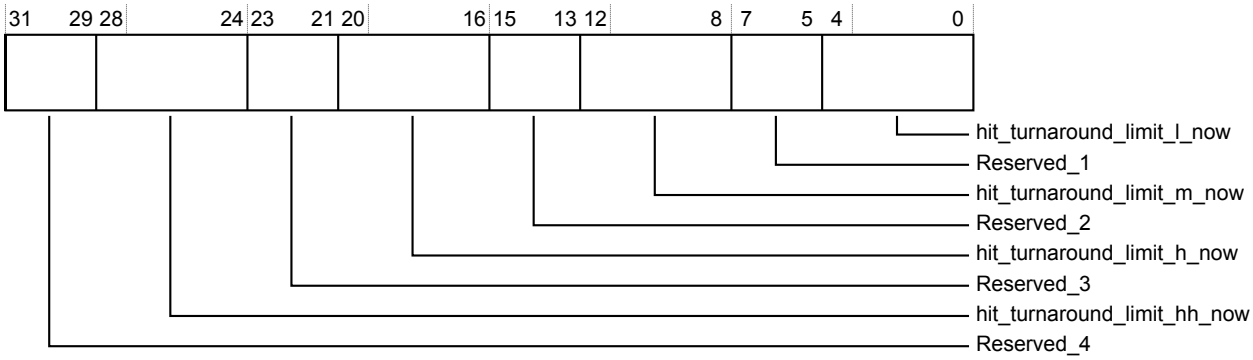

Figure 3-192 hit_turnaround_control_now register bit assignments

The following shows the bit assignments.

[31:29] Reserved_4
Unused bits

[28:24] hit_turnaround_limit_hh_now
Program the maximum number of consecutive in-row hits in the presence of HIGH-HIGH class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

[23:21] Reserved_3
Unused bits

[20:16] hit_turnaround_limit_h_now
Program the maximum number of consecutive in-row hits in the presence of HIGH class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

[15:13] Reserved_2
Unused bits

[12:8] hit_turnaround_limit_m_now
Program the maximum number of consecutive in-row hits in the presence of MEDIUM class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

[7:5] Reserved_1
Unused bits

[4:0] hit_turnaround_limit_l_now
Program the maximum number of consecutive in-row hits in the presence of LOW class requests. Zero disables increased priority of in-row hits. The supported range for this bitfield is 0-31.

3.3.193 qos_class_control_now

Configures the priority class for each QoS encoding.

The qos_class_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1030`
Type	Read-only
Reset	`0x00000FC8`
Width	32

The following figure shows the bit assignments.

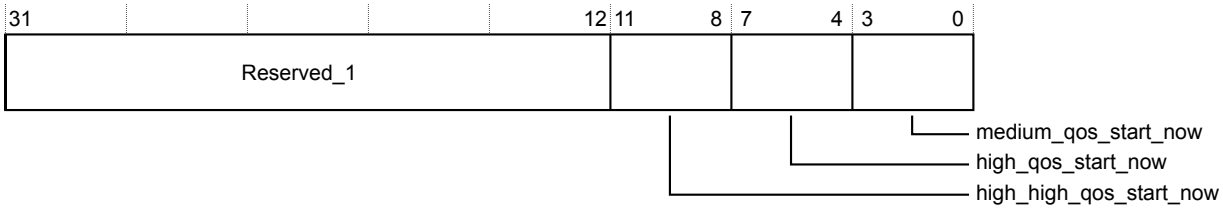

Figure 3-193 qos_class_control_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:8] high_high_qos_start_now
Determines the minimum Qv value mapped onto the HIGH-HIGH QoS class. The supported range for this bitfield is 0-15.

[7:4] high_qos_start_now
Determines the minimum Qv value mapped onto the HIGH QoS class. The supported range for this bitfield is 0-15.

[3:0] medium_qos_start_now
Determines the minimum Qv value mapped onto the MEDIUM QoS class. The supported range for this bitfield is 0-15.

3.3.194 escalation_control_now

Configures the settings for escalating the priority of entries in the queue.

The escalation_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1034`
Type	Read-only
Reset	`0x00080000`
Width	32

The following figure shows the bit assignments.

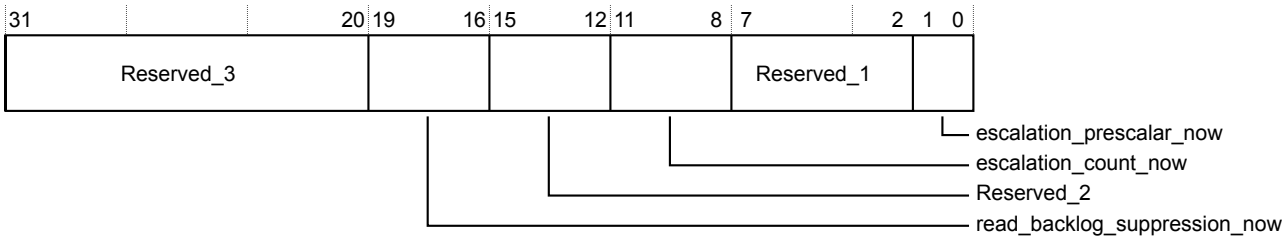

Figure 3-194 escalation_control_now register bit assignments

The following shows the bit assignments.

[31:20] Reserved_3
Unused bits

[19:16] read_backlog_suppression_now
Configures the number of completed reads (as a proportion in 16ths of the queue depth) at which to stop arbitrating more reads until the system drains the fetched read data. Zero disables this feature. The supported range for this bitfield is 0-15.

[15:12] Reserved_2
Unused bits

[11:8] escalation_count_now
Program the number of escalation prescaler periods between applying escalation. Zero disables priority escalation in the queue. The supported range for this bitfield is 0-15.

[7:2] Reserved_1
Unused bits

[1:0] escalation_prescalar_now
Escalation counter prescaler.

3.3.195 qv_control_31_00_now

Configures the priority settings for each QoS encoding.

The qv_control_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1038`
Type	Read-only
Reset	`0x76543210`
Width	32

The following figure shows the bit assignments.

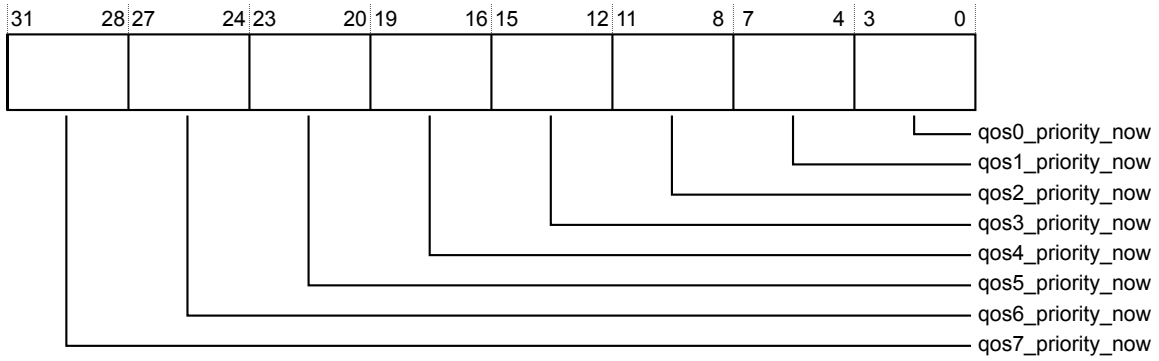

Figure 3-195 qv_control_31_00_now register bit assignments

The following shows the bit assignments.

[31:28] qos7_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos6_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos5_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos4_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos3_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos2_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos1_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos0_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

3.3.196 qv_control_63_32_now

Configures the priority settings for each QoS encoding.

The qv_control_63_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x103C`
Type	Read-only
Reset	`0xFEDCBA98`
Width	32

The following figure shows the bit assignments.

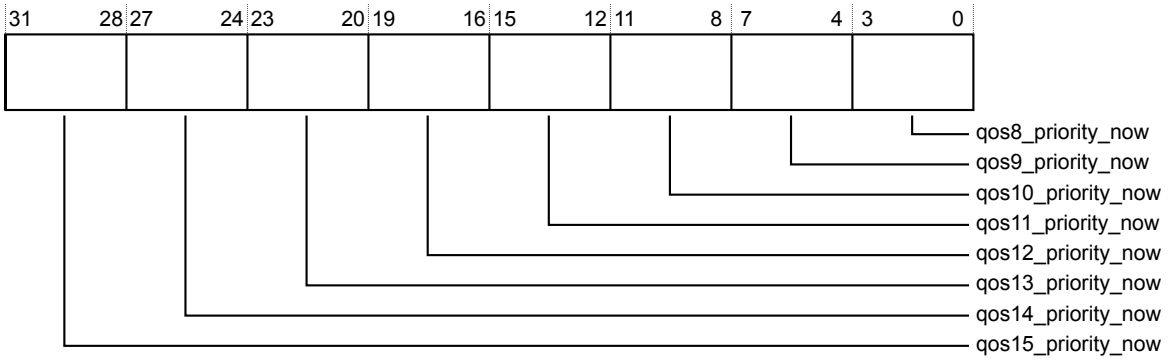

Figure 3-196 qv_control_63_32_now register bit assignments

The following shows the bit assignments.

[31:28] qos15_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos14_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos13_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos12_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos11_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos10_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos9_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos8_priority_now
Program the queueing priority for requests received with this QoS value. The supported range for this bitfield is 0-15.

3.3.197 rt_control_31_00_now

Configures the timeout settings for each QoS encoding.

The rt_control_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1040`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

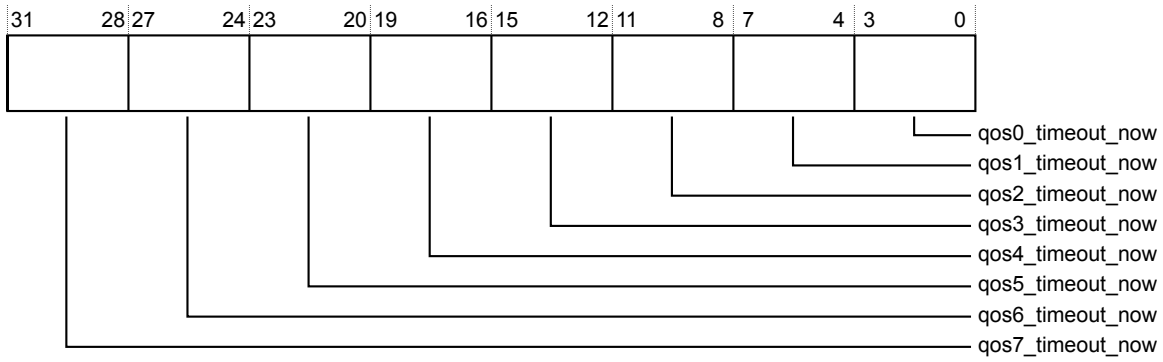

Figure 3-197 rt_control_31_00_now register bit assignments

The following shows the bit assignments.

[31:28] qos7_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos6_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos5_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos4_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos3_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos2_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos1_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos0_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

3.3.198 rt_control_63_32_now

Configures the timeout settings for each QoS encoding.

The rt_control_63_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1044`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

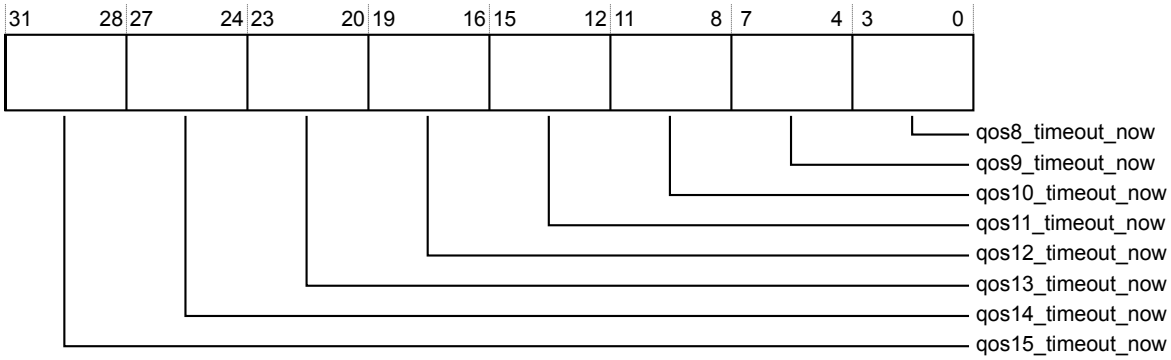

Figure 3-198 rt_control_63_32_now register bit assignments

The following shows the bit assignments.

[31:28] qos15_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[27:24] qos14_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[23:20] qos13_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[19:16] qos12_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[15:12] qos11_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[11:8] qos10_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[7:4] qos9_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

[3:0] qos8_timeout_now
Program the number of timeout prescaler periods to wait before elevating a received request to maximum priority. Zero disables this feature for request received with this QoS value. The supported range for this bitfield is 0-15.

3.3.199 timeout_control_now

Configures the prescaler applied to timeout values.

The timeout_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1048
Type	Read-only
Reset	0x00000001
Width	32

The following figure shows the bit assignments.

Figure 3-199 timeout_control_now register bit assignments

The following shows the bit assignments.

[31:2] Reserved_1
Unused bits

[1:0] timeout_prescalar_now
timeout_prescalar_now bitfield.

3.3.200 credit_control_now

Configures the settings for preventing starvation of CHI protocol retries.

The credit_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x104C
Type	Read-only
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

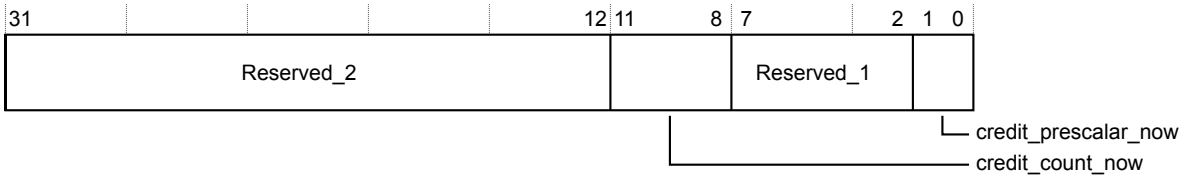

Figure 3-200 credit_control_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_2
Unused bits

[11:8] credit_count_now
Program the number of P-credit prescaler periods between applying escalation. 0 disables this feature. The supported range for this bitfield is 0-15.

[7:2] Reserved_1
Unused bits

[1:0] credit_prescalar_now
P-credit counter prescaler.

3.3.201 write_priority_control_31_00_now

Configures the priority settings for write requests within the DMC

The write_priority_control_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1050`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

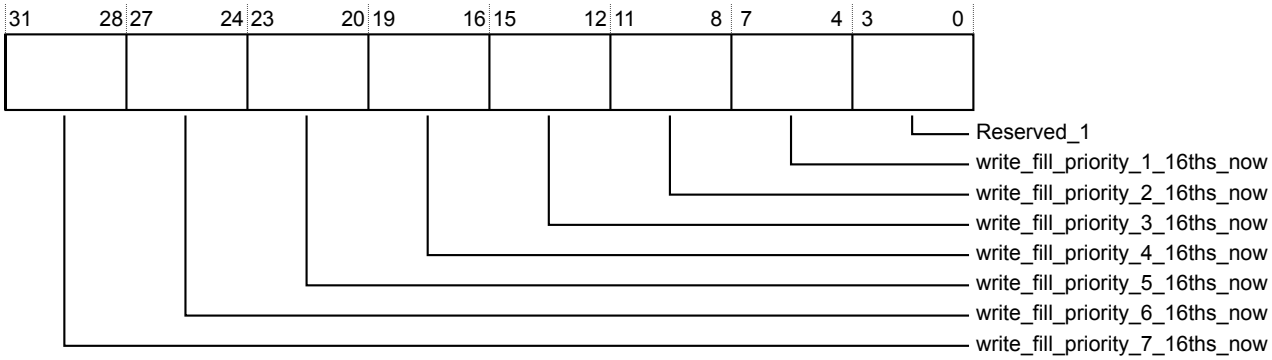

Figure 3-201 write_priority_control_31_00_now register bit assignments

The following shows the bit assignments.

[31:28] write_fill_priority_7_16ths_now
Program the priority of write requests when write requests occupy 7/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[27:24] write_fill_priority_6_16ths_now
Program the priority of write requests when write requests occupy 6/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[23:20] write_fill_priority_5_16ths_now
Program the priority of write requests when write requests occupy 5/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[19:16] write_fill_priority_4_16ths_now
Program the priority of write requests when write requests occupy 4/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[15:12] write_fill_priority_3_16ths_now
Program the priority of write requests when write requests occupy 3/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[11:8] write_fill_priority_2_16ths_now
Program the priority of write requests when write requests occupy 2/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[7:4] write_fill_priority_1_16ths_now
Program the priority of write requests when write requests occupy 1/16th of the DMC queue. The supported range for this bitfield is 0-15.

[3:0] Reserved_1
Unused bits

3.3.202 write_priority_control_63_32_now

Configures the priority settings for write requests within the DMC.

The write_priority_control_63_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1054`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

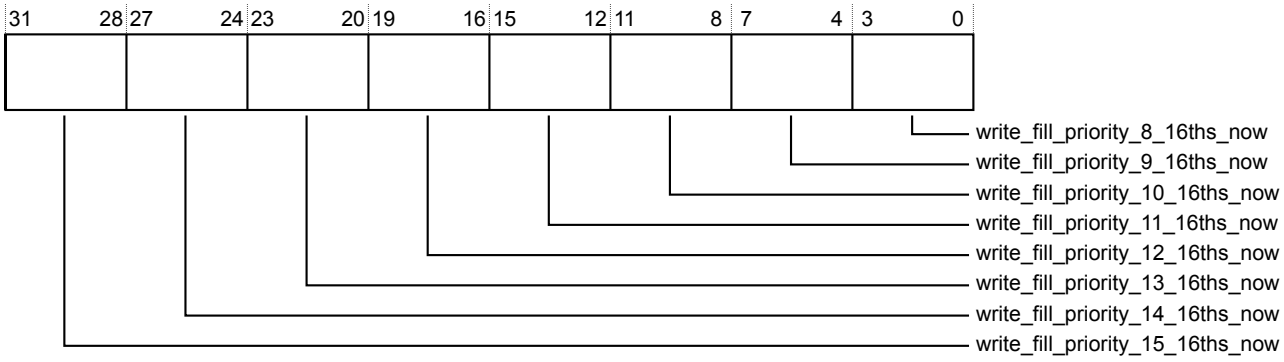

Figure 3-202 write_priority_control_63_32_now register bit assignments

The following shows the bit assignments.

[31:28] write_fill_priority_15_16ths_now
Program the priority of write requests when write requests occupy 15/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[27:24] write_fill_priority_14_16ths_now
Program the priority of write requests when write requests occupy 14/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[23:20] write_fill_priority_13_16ths_now
Program the priority of write requests when write requests occupy 13/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[19:16] write_fill_priority_12_16ths_now
Program the priority of write requests when write requests occupy 12/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[15:12] write_fill_priority_11_16ths_now
Program the priority of write requests when write requests occupy 11/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[11:8] write_fill_priority_10_16ths_now
Program the priority of write requests when write requests occupy 10/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[7:4] write_fill_priority_9_16ths_now
Program the priority of write requests when write requests occupy 9/16ths of the DMC queue. The supported range for this bitfield is 0-15.

[3:0] write_fill_priority_8_16ths_now
Program the priority of write requests when write requests occupy 8/16ths of the DMC queue. The supported range for this bitfield is 0-15.

3.3.203 queue_threshold_control_31_00_now

Configures the threshold settings for requests in the DMC

The queue_threshold_control_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1060`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

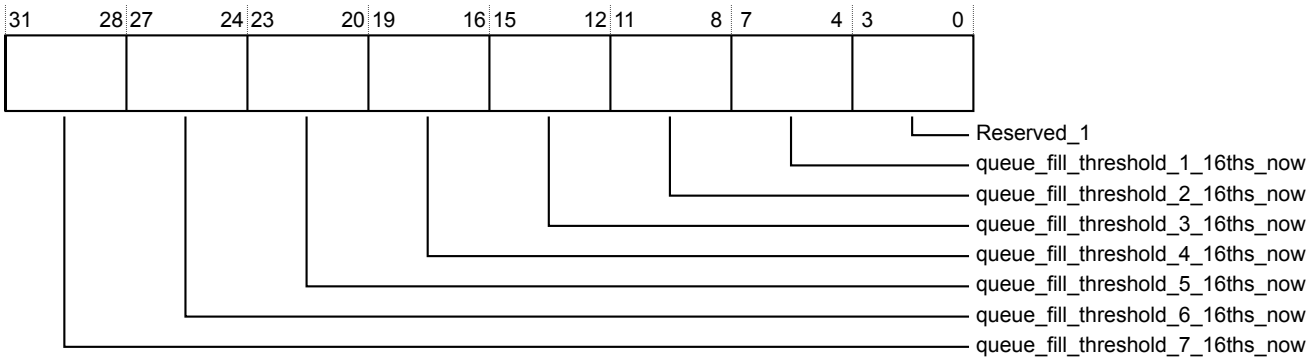

Figure 3-203 queue_threshold_control_31_00_now register bit assignments

The following shows the bit assignments.

[31:28] queue_fill_threshold_7_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 7/16ths full. The supported range for this bitfield is 0-15.

[27:24] queue_fill_threshold_6_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 6/16ths full. The supported range for this bitfield is 0-15.

[23:20] queue_fill_threshold_5_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 5/16ths full. The supported range for this bitfield is 0-15.

[19:16] queue_fill_threshold_4_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 4/16ths full. The supported range for this bitfield is 0-15.

[15:12] queue_fill_threshold_3_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 3/16ths full. The supported range for this bitfield is 0-15.

[11:8] queue_fill_threshold_2_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 2/16ths full. The supported range for this bitfield is 0-15.

[7:4] queue_fill_threshold_1_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 1/16ths full. The supported range for this bitfield is 0-15.

[3:0] Reserved_1
Unused bits

3.3.204 queue_threshold_control_63_32_now

Configures the threshold settings for requests in the DMC

The queue_threshold_control_63_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1064`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

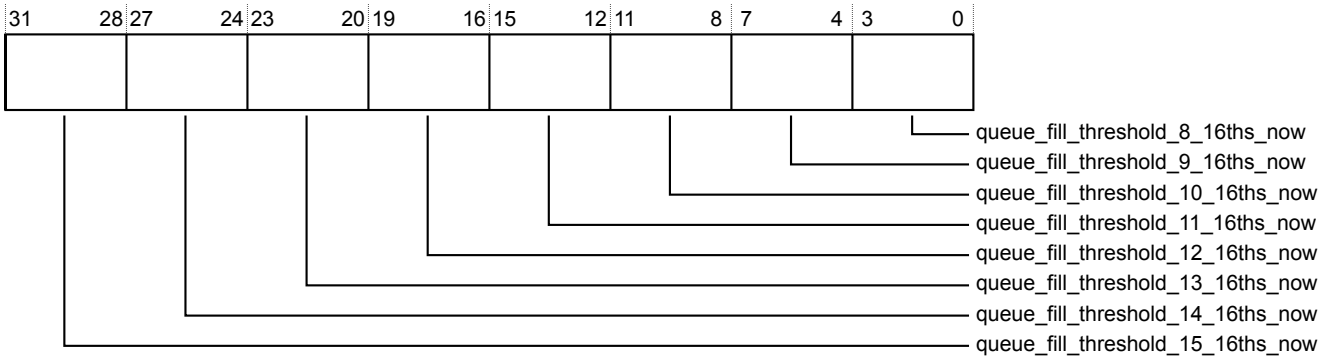

Figure 3-204 queue_threshold_control_63_32_now register bit assignments

The following shows the bit assignments.

[31:28] queue_fill_threshold_15_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 15/16ths full. The supported range for this bitfield is 0-15.

[27:24] queue_fill_threshold_14_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 14/16ths full. The supported range for this bitfield is 0-15.

[23:20] queue_fill_threshold_13_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 13/16ths full. The supported range for this bitfield is 0-15.

[19:16] queue_fill_threshold_12_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 12/16ths full. The supported range for this bitfield is 0-15.

[15:12] queue_fill_threshold_11_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 11/16ths full. The supported range for this bitfield is 0-15.

[11:8] queue_fill_threshold_10_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 10/16ths full. The supported range for this bitfield is 0-15.

[7:4] queue_fill_threshold_9_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 9/16ths full. The supported range for this bitfield is 0-15.

[3:0] queue_fill_threshold_8_16ths_now
Program to set the priority that requests must be equal to or above, to be accepted when the queue is 8/16ths full. The supported range for this bitfield is 0-15.

3.3.205 memory_address_max_31_00_now

Configures the address space control for the DMC default region.

The memory_address_max_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1078`
Type	Read-only
Reset	`0x00000010`
Width	32

The following figure shows the bit assignments.

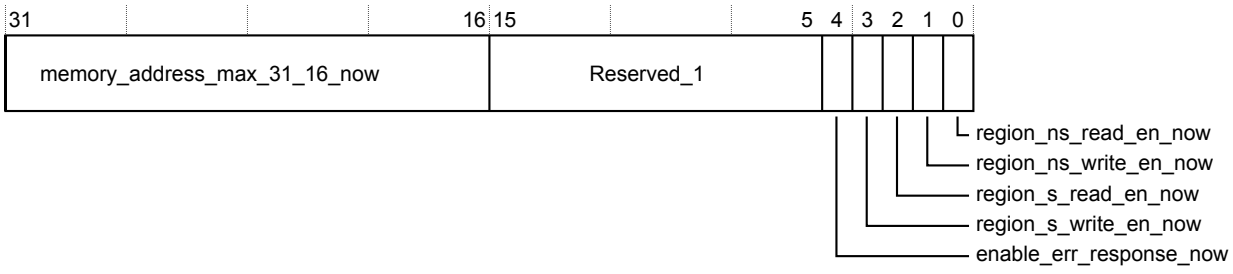

Figure 3-205 memory_address_max_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] memory_address_max_31_16_now
Program to set bits[31:16] of the maximum memory address. Note that this is the address value after address translation has been applied (if applicable).

[15:5] Reserved_1
Unused bits

[4] enable_err_response_now
Configures the response used for a request that fails address access checks.

[3] region_s_write_en_now
Enables Secure writes to the default region

[2] region_s_read_en_now
Enables Secure reads to the default region

[1] region_ns_write_en_now
Enables Non-secure writes to the default region

[0] region_ns_read_en_now
Enables Non-secure reads to the default region

3.3.206 memory_address_max_43_32_now

Configures the address space control for the DMC default region.

The memory_address_max_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x107C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

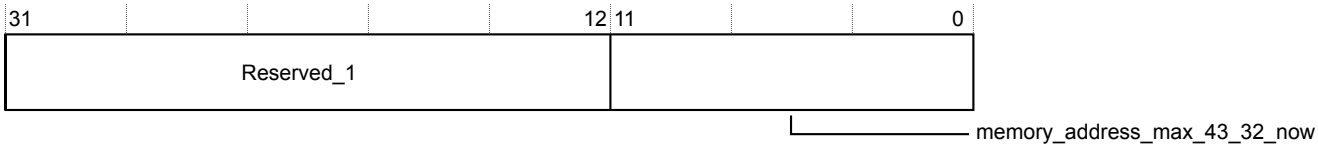

Figure 3-206 memory_address_max_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] memory_address_max_43_32_now
Program to set bits[43:32] of the maximum memory address. Note that this is the address value after address translation has been applied (if applicable).

3.3.207 access_address_min0_31_00_now

Configures the address space control for address region 0.

The access_address_min0_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1080`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

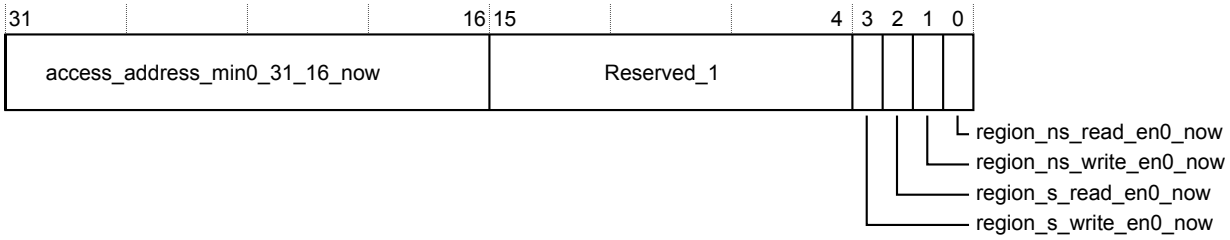

Figure 3-207 access_address_min0_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min0_31_16_now
Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1
Unused bits

[3] region_s_write_en0_now
Enables Secure writes to the region

[2] region_s_read_en0_now
Enables Secure reads to the region

[1] region_ns_write_en0_now
Enables Non-secure writes to the region

[0] region_ns_read_en0_now
Enables Non-secure reads to the region

3.3.208 access_address_min0_43_32_now

Configures the address space control for address region 0.

The access_address_min0_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1084`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

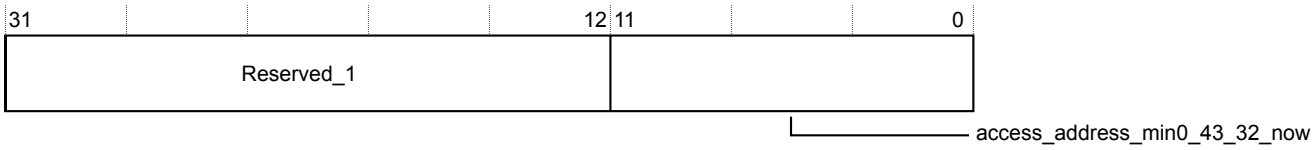

Figure 3-208 access_address_min0_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_min0_43_32_now
Program to set bits[43:32] of the minimum address in the region

3.3.209 access_address_max0_31_00_now

Configures the address space control for address region 0.

The access_address_max0_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1088`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

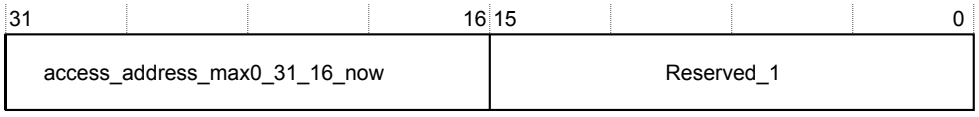

Figure 3-209 access_address_max0_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max0_31_16_now
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.210 access_address_max0_43_32_now

Configures the address space control for address region 0.

The access_address_max0_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x108C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

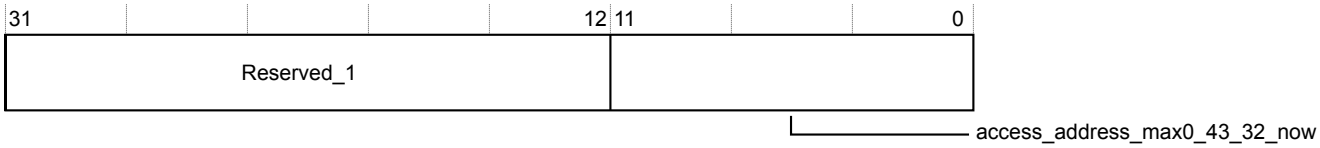

Figure 3-210 access_address_max0_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max0_43_32_now
Program to set bits[43:32] of the maximum address in the region

3.3.211 access_address_min1_31_00_now

Configures the address space control for address region 1.

The access_address_min1_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1090`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

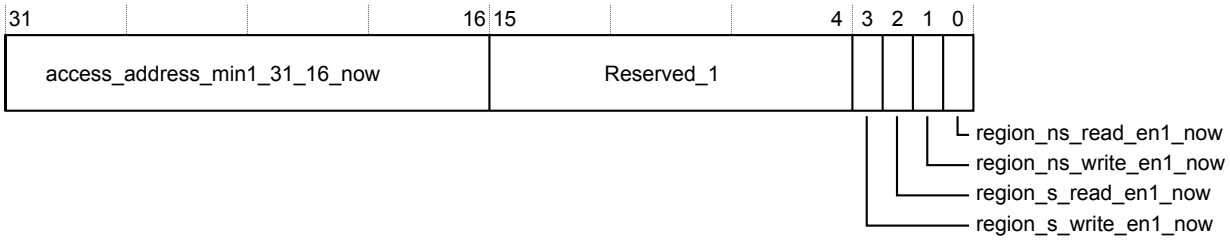

Figure 3-211 access_address_min1_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min1_31_16_now
Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1
Unused bits

[3] region_s_write_en1_now
Enables Secure writes to the region

[2] region_s_read_en1_now
Enables Secure reads to the region

[1] region_ns_write_en1_now
Enables Non-secure writes to the region

[0] region_ns_read_en1_now
Enables Non-secure reads to the region

3.3.212 access_address_min1_43_32_now

Configures the address space control for address region 1.

The access_address_min1_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1094`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

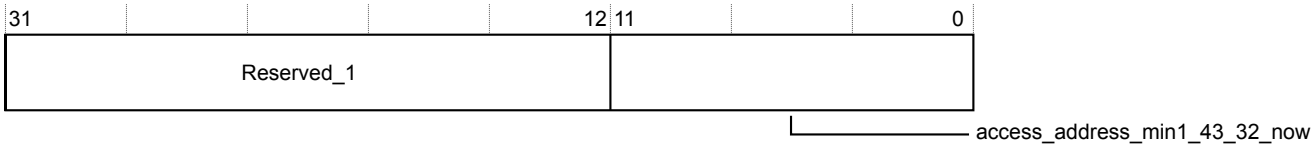

Figure 3-212 access_address_min1_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1

Unused bits

[11:0] access_address_min1_43_32_now

Program to set bits[43:32] of the minimum address in the region

3.3.213 access_address_max1_31_00_now

Configures the address space control for address region 1.

The access_address_max1_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1098`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

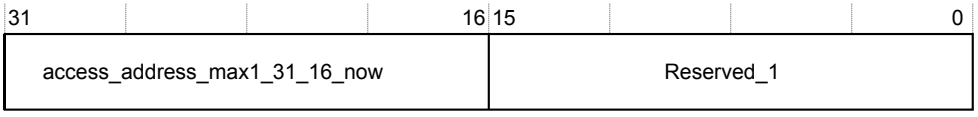

Figure 3-213 access_address_max1_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max1_31_16_now
Program to set bits[31:16] of the maximum address in the region
[15:0] Reserved_1
Unused bits

3.3.214 access_address_max1_43_32_now

Configures the address space control for address region 1.

The access_address_max1_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x109C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

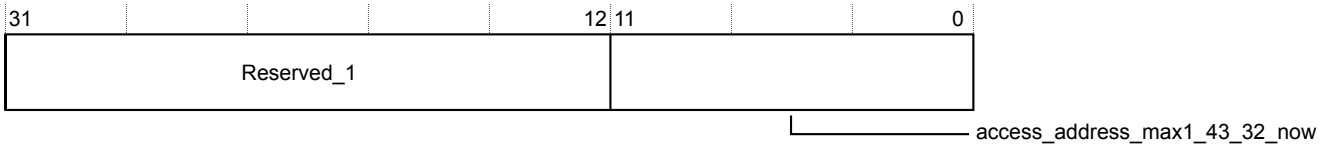

Figure 3-214 access_address_max1_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_max1_43_32_now
Program to set bits[43:32] of the maximum address in the region

3.3.215 access_address_min2_31_00_now

Configures the address space control for address region 2.

The access_address_min2_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x10A0`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

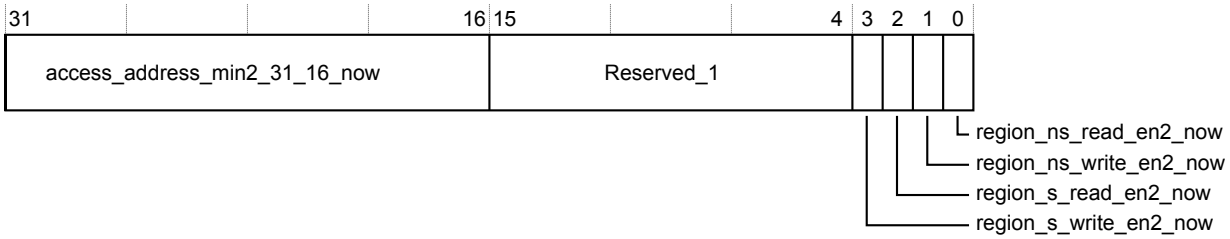

Figure 3-215 access_address_min2_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min2_31_16_now
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en2_now
Enables Secure writes to the region
[2] region_s_read_en2_now
Enables Secure reads to the region
[1] region_ns_write_en2_now
Enables Non-secure writes to the region
[0] region_ns_read_en2_now
Enables Non-secure reads to the region

3.3.216 access_address_min2_43_32_now

Configures the address space control for address region 2.

The access_address_min2_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x10A4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

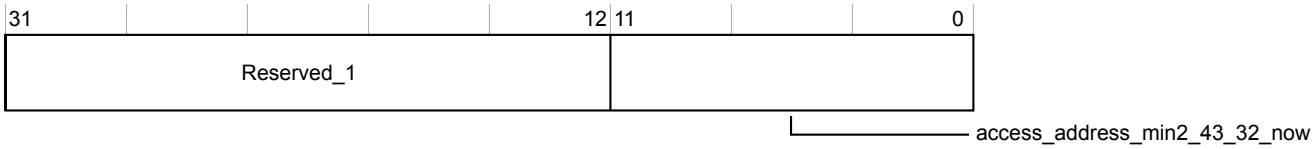

Figure 3-216 access_address_min2_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min2_43_32_now
Program to set bits[43:32] of the minimum address in the region

3.3.217 access_address_max2_31_00_now

Configures the address space control for address region 2.

The access_address_max2_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10A8`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

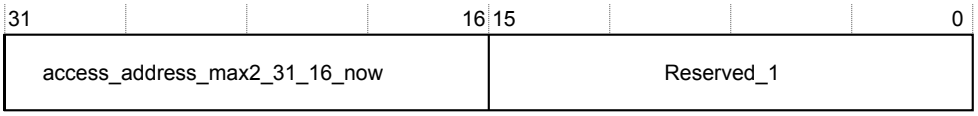

Figure 3-217 access_address_max2_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max2_31_16_now

Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1

Unused bits

3.3.218 access_address_max2_43_32_now

Configures the address space control for address region 2.

The access_address_max2_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x10AC`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

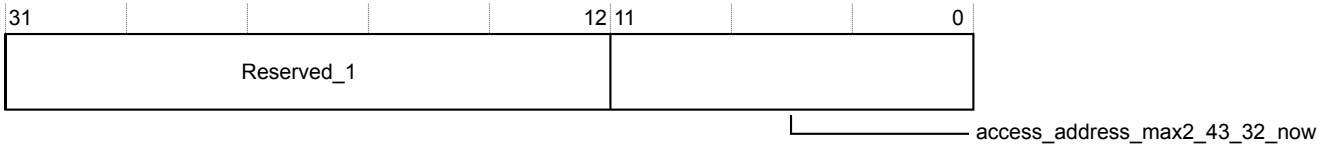

Figure 3-218 access_address_max2_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max2_43_32_now
Program to set bits[43:32] of the maximum address in the region

3.3.219 access_address_min3_31_00_now

Configures the address space control for address region 3.

The access_address_min3_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x10B0`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

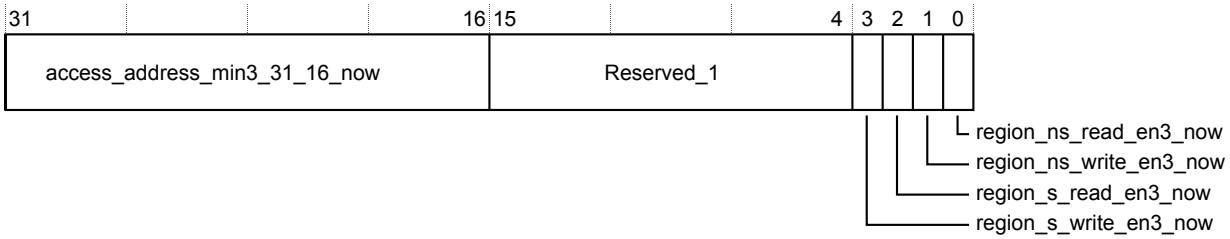

Figure 3-219 access_address_min3_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min3_31_16_now
Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1
Unused bits

[3] region_s_write_en3_now
Enables Secure writes to the region

[2] region_s_read_en3_now
Enables Secure reads to the region

[1] region_ns_write_en3_now
Enables Non-secure writes to the region

[0] region_ns_read_en3_now
Enables Non-secure reads to the region

3.3.220 access_address_min3_43_32_now

Configures the address space control for address region 3.

The access_address_min3_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10B4

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

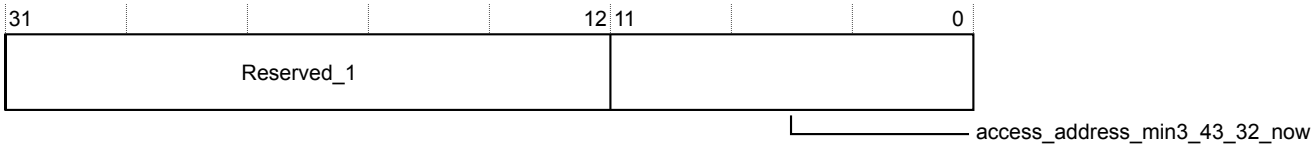

Figure 3-220 access_address_min3_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_min3_43_32_now
Program to set bits[43:32] of the minimum address in the region

3.3.221 access_address_max3_31_00_now

Configures the address space control for address region 3.

The access_address_max3_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x10B8

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

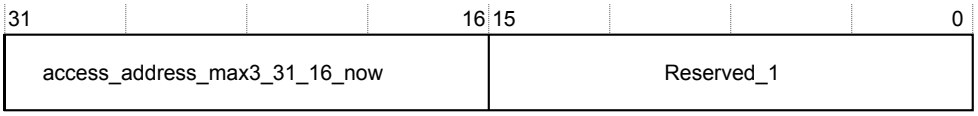

Figure 3-221 access_address_max3_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max3_31_16_now
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.222 access_address_max3_43_32_now

Configures the address space control for address region 3.

The access_address_max3_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x10BC

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

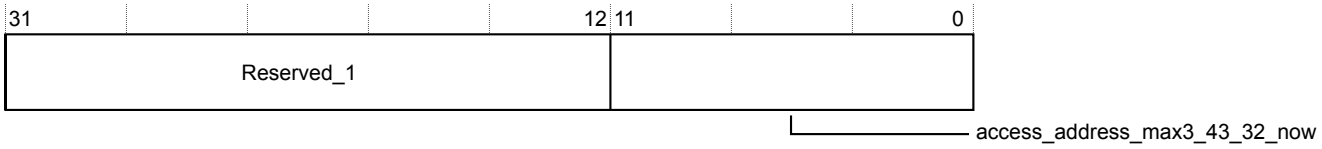

Figure 3-222 access_address_max3_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1

Unused bits

[11:0] access_address_max3_43_32_now

Program to set bits[43:32] of the maximum address in the region

3.3.223 access_address_min4_31_00_now

Configures the address space control for address region 4.

The access_address_min4_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x10C0

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

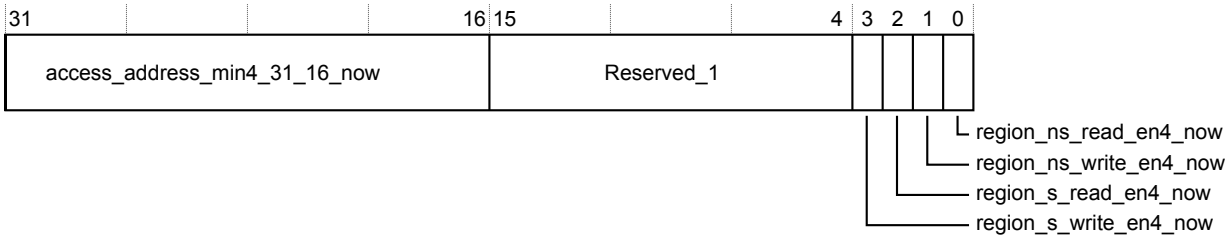

Figure 3-223 access_address_min4_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min4_31_16_now
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en4_now
Enables Secure writes to the region
[2] region_s_read_en4_now
Enables Secure reads to the region
[1] region_ns_write_en4_now
Enables Non-secure writes to the region
[0] region_ns_read_en4_now
Enables Non-secure reads to the region

3.3.224 access_address_min4_43_32_now

Configures the address space control for address region 4.

The access_address_min4_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x10C4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

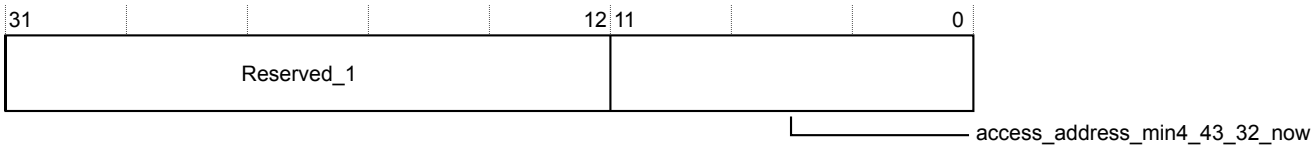

Figure 3-224 access_address_min4_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min4_43_32_now
Program to set bits[43:32] of the minimum address in the region

3.3.225 access_address_max4_31_00_now

Configures the address space control for address region 4.

The access_address_max4_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x10C8`

Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

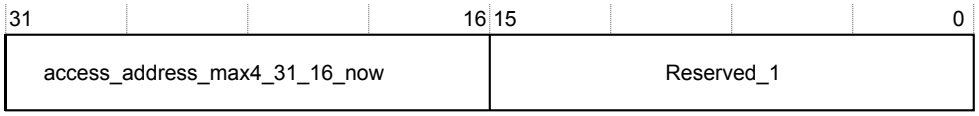

Figure 3-225 access_address_max4_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max4_31_16_now
Program to set bits[31:16] of the maximum address in the region
[15:0] Reserved_1
Unused bits

3.3.226 access_address_max4_43_32_now

Configures the address space control for address region 4.

The access_address_max4_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x10CC
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

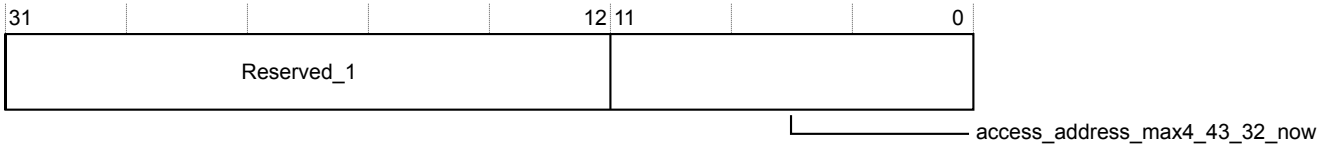

Figure 3-226 access_address_max4_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_max4_43_32_now
Program to set bits[43:32] of the maximum address in the region

3.3.227 access_address_min5_31_00_now

Configures the address space control for address region 5.

The access_address_min5_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x10D0

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

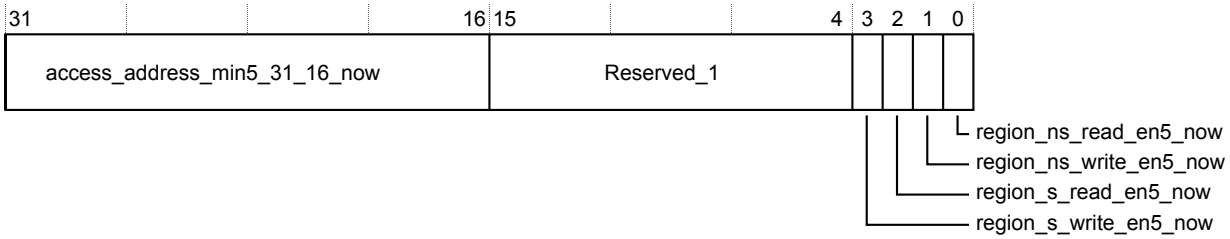

Figure 3-227 access_address_min5_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min5_31_16_now

Program to set bits[31:16] of the minimum address in the region

[15:4] Reserved_1

Unused bits

[3] region_s_write_en5_now

Enables Secure writes to the region

[2] region_s_read_en5_now

Enables Secure reads to the region

[1] region_ns_write_en5_now

Enables Non-secure writes to the region

[0] region_ns_read_en5_now

Enables Non-secure reads to the region

3.3.228 access_address_min5_43_32_now

Configures the address space control for address region 5.

The access_address_min5_43_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x10D4

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

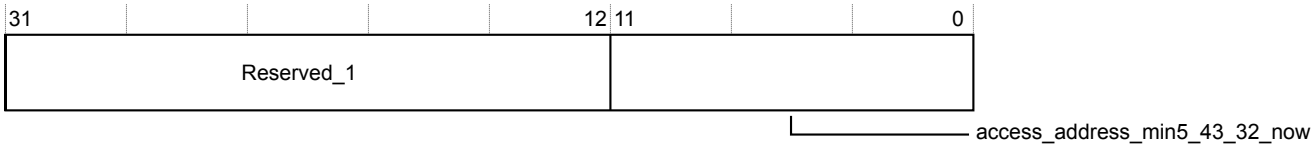

Figure 3-228 access_address_min5_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_min5_43_32_now
Program to set bits[43:32] of the minimum address in the region

3.3.229 access_address_max5_31_00_now

Configures the address space control for address region 5.

The access_address_max5_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x10D8`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

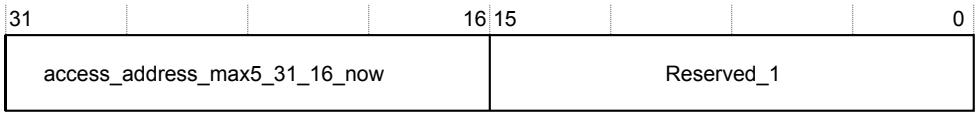

Figure 3-229 access_address_max5_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max5_31_16_now
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.230 access_address_max5_43_32_now

Configures the address space control for address region 5.

The access_address_max5_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x10DC`

Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

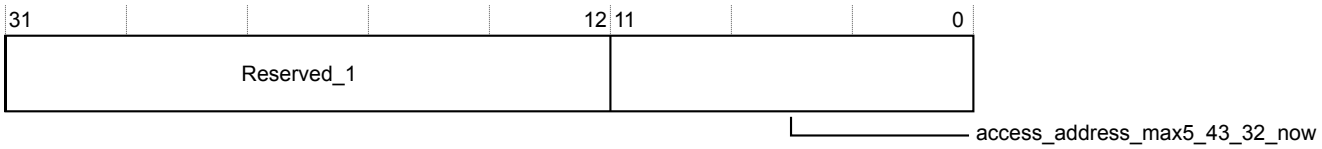

Figure 3-230 access_address_max5_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_max5_43_32_now
Program to set bits[43:32] of the maximum address in the region

3.3.231 access_address_min6_31_00_now

Configures the address space control for address region 6.

The access_address_min6_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x10E0
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

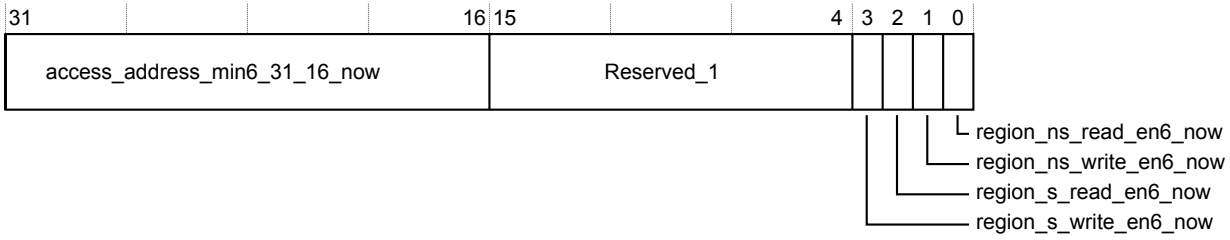

Figure 3-231 access_address_min6_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min6_31_16_now
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en6_now
Enables Secure writes to the region

[2] region_s_read_en6_now
Enables Secure reads to the region
[1] region_ns_write_en6_now
Enables Non-secure writes to the region
[0] region_ns_read_en6_now
Enables Non-secure reads to the region

3.3.232 access_address_min6_43_32_now

Configures the address space control for address region 6.

The access_address_min6_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x10E4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

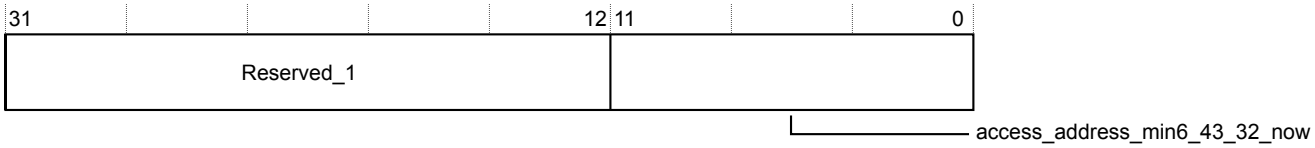

Figure 3-232 access_address_min6_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min6_43_32_now
Program to set bits[43:32] of the minimum address in the region

3.3.233 access_address_max6_31_00_now

Configures the address space control for address region 6.

The access_address_max6_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x10E8`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

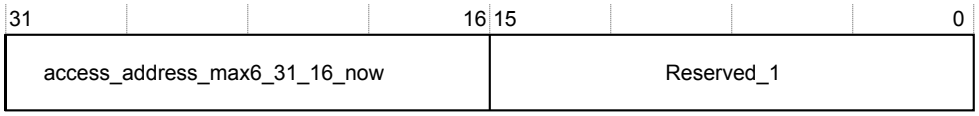

Figure 3-233 access_address_max6_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max6_31_16_now
Program to set bits[31:16] of the maximum address in the region

[15:0] Reserved_1
Unused bits

3.3.234 access_address_max6_43_32_now

Configures the address space control for address region 6.

The access_address_max6_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x10EC`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

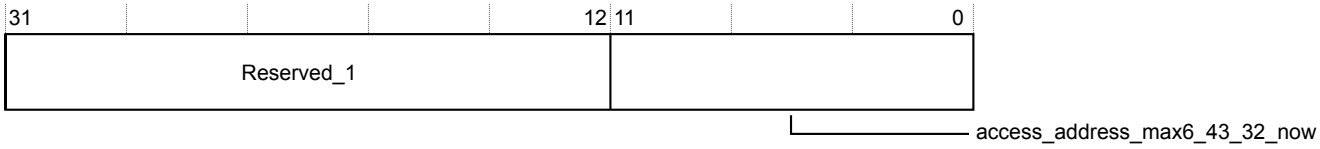

Figure 3-234 access_address_max6_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max6_43_32_now
Program to set bits[43:32] of the maximum address in the region

3.3.235 access_address_min7_31_00_now

Configures the address space control for address region 7.

The access_address_min7_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x10F0`

Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

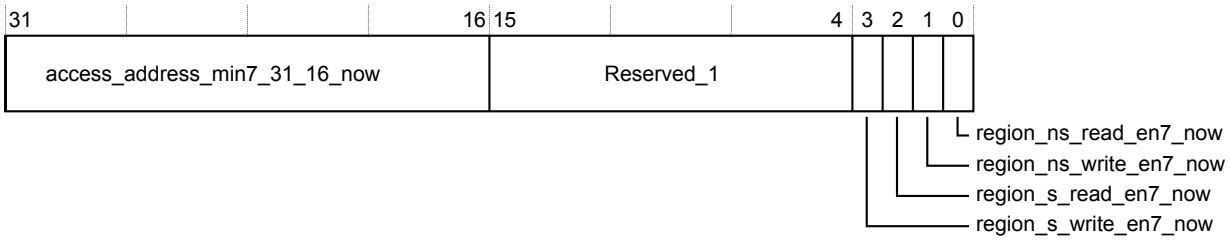

Figure 3-235 access_address_min7_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_min7_31_16_now
Program to set bits[31:16] of the minimum address in the region
[15:4] Reserved_1
Unused bits
[3] region_s_write_en7_now
Enables Secure writes to the region
[2] region_s_read_en7_now
Enables Secure reads to the region
[1] region_ns_write_en7_now
Enables Non-secure writes to the region
[0] region_ns_read_en7_now
Enables Non-secure reads to the region

3.3.236 access_address_min7_43_32_now

Configures the address space control for address region 7.

The access_address_min7_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x10F4
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

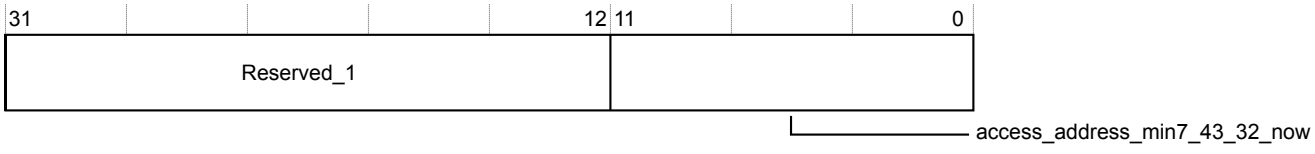

Figure 3-236 access_address_min7_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits
[11:0] access_address_min7_43_32_now
Program to set bits[43:32] of the minimum address in the region

3.3.237 access_address_max7_31_00_now

Configures the address space control for address region 7.

The access_address_max7_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset `0x10F8`
Type Read-only
Reset `0x00000000`
Width 32

The following figure shows the bit assignments.

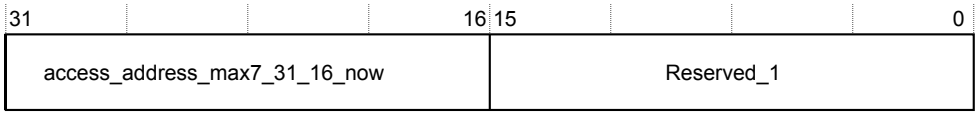

Figure 3-237 access_address_max7_31_00_now register bit assignments

The following shows the bit assignments.

[31:16] access_address_max7_31_16_now
Program to set bits[31:16] of the maximum address in the region
[15:0] Reserved_1
Unused bits

3.3.238 access_address_max7_43_32_now

Configures the address space control for the address region 7.

The access_address_max7_43_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset `0x10FC`
Type Read-only
Reset `0x00000000`
Width 32

The following figure shows the bit assignments.

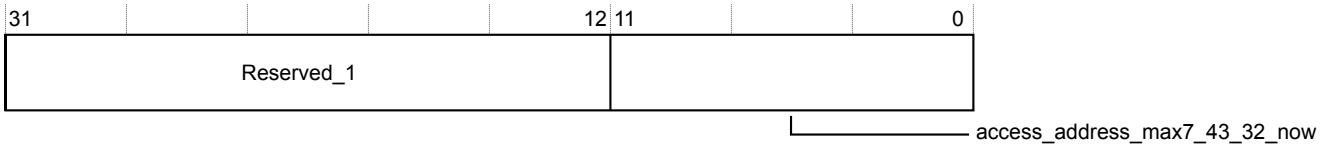

Figure 3-238 access_address_max7_43_32_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] access_address_max7_43_32_now
Program to set bits[43:32] of the maximum address in the region

3.3.239 dci_replay_type_now

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command.

The dci_replay_type_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1110`
Type	Read-only
Reset	`0x00000002`
Width	32

The following figure shows the bit assignments.

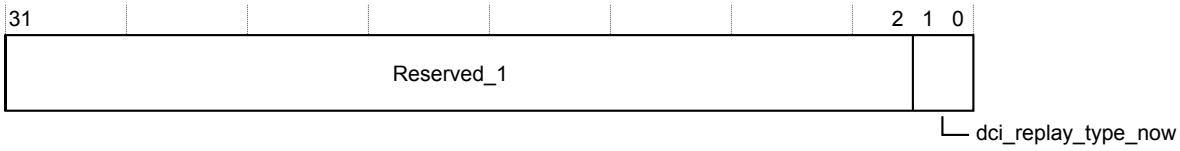

Figure 3-239 dci_replay_type_now register bit assignments

The following shows the bit assignments.

[31:2] Reserved_1
Unused bits

[1:0] dci_replay_type_now
dci_replay_type_now bitfield.

3.3.240 refresh_control_now

Configures the type of refresh commands issued by the DMC.

The refresh_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1120
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

Figure 3-240 refresh_control_now register bit assignments

The following shows the bit assignments.

[31:6] Reserved_2
Unused bits
[5:4] refresh_granularity_now
Configures the refresh rate mode of the DMC. You must program this to match the mode of the DRAM. All DRAMs requiring refresh must use the same refresh rate.
[3:0] Reserved_1
Unused bits

3.3.241 memory_type_now

Configures the DMC for the attached memory type.

The memory_type_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1128
Type Read-only
Reset 0x00000101
Width 32

The following figure shows the bit assignments.

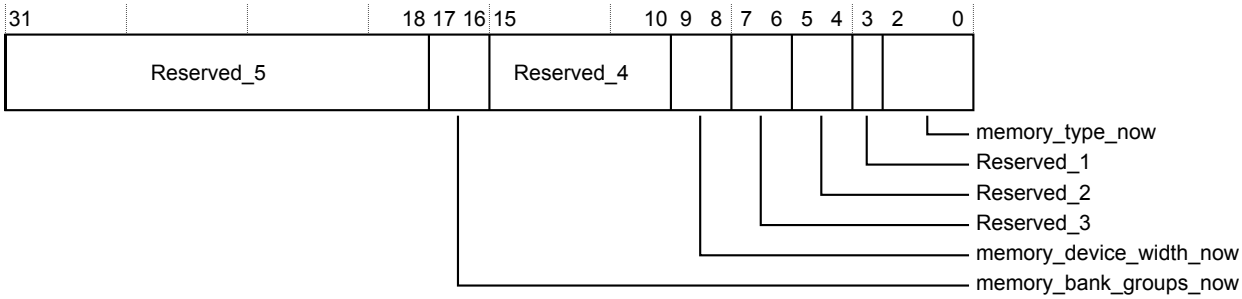

Figure 3-241 memory_type_now register bit assignments

The following shows the bit assignments.

[31:18] Reserved_5
Unused bits
[17:16] memory_bank_groups_now
Program to configure the number of bank groups in the attached memory device
[15:10] Reserved_4
Unused bits
[9:8] memory_device_width_now
Program to configure the device widths.
[7:6] Reserved_3
Unused bits
[5:4] Reserved_2
Unused bits
[3] Reserved_1
Unused bits
[2:0] memory_type_now
Program to configure the attached memory type

3.3.242 scrub_control0_now

Scrub engine channel control register.

The scrub_control0_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1170`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

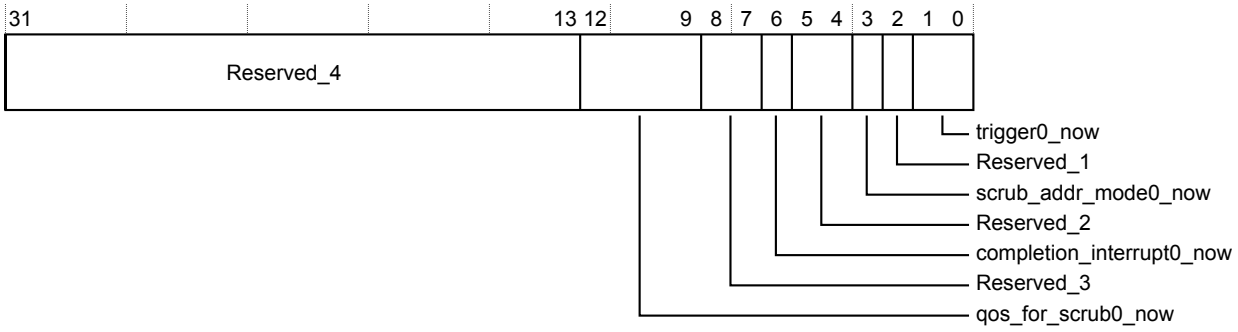

Figure 3-242 scrub_control0_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits
[12:9] qos_for_scrub0_now
Configures QoS value of scrub operations
[8:7] Reserved_3
Unused bits

[6] completion_interrupt0_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode0_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger0_now
Controls the trigger event associated with the channel operation.

3.3.243 scrub_address_min0_now

Configures the address space control for the scrub engine channel.

The scrub_address_min0_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1174`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

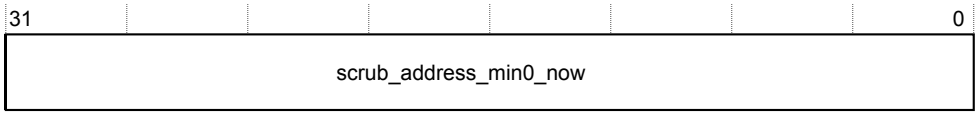

Figure 3-243 scrub_address_min0_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min0_now
Program to set the starting address for the scrub engine. When scrub_addr_mode0 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode0 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.244 scrub_address_max0_now

Configures the address space control for the scrub engine channel.

The scrub_address_max0_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1178`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

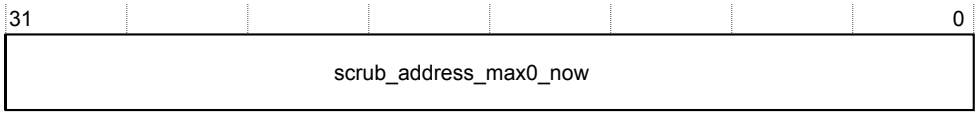

Figure 3-244 scrub_address_max0_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max0_now
Program to set the ending address for the scrub engine. When scrub_addr_mode0 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode0 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.245 scrub_control1_now

Scrub engine channel control register.

The scrub_control1_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1180`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

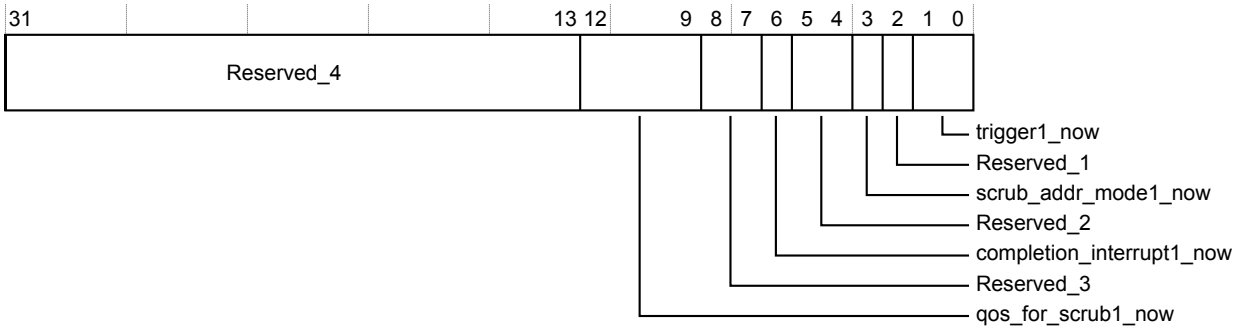

Figure 3-245 scrub_control1_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub1_now
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt1_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode1_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger1_now
Controls the trigger event associated with the channel operation.

3.3.246 scrub_address_min1_now

Configures the address space control for the scrub engine channel.

The scrub_address_min1_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1184`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

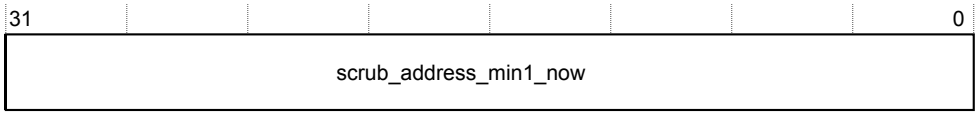

Figure 3-246 scrub_address_min1_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min1_now
Program to set the starting address for the scrub engine. When scrub_addr_mode1 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode1 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.247 scrub_address_max1_now

Configures the address space control for the scrub engine channel.

The scrub_address_max1_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1188`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

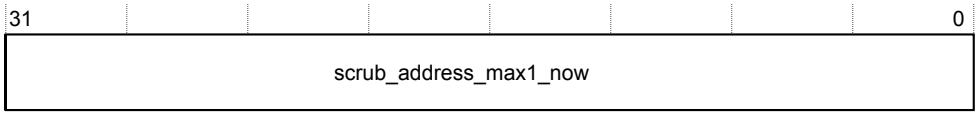

Figure 3-247 scrub_address_max1_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max1_now
Program to set the ending address for the scrub engine. When scrub_addr_mode1 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode1 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.248 scrub_control2_now

Scrub engine channel control register.

The scrub_control2_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1190`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

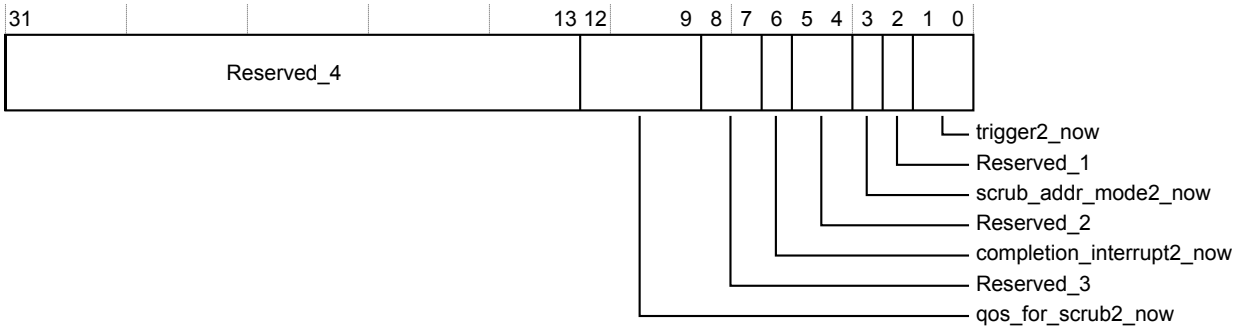

Figure 3-248 scrub_control2_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub2_now
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt2_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode2_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger2_now
Controls the trigger event associated with the channel operation.

3.3.249 scrub_address_min2_now

Configures the address space control for the scrub engine channel.

The scrub_address_min2_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1194`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

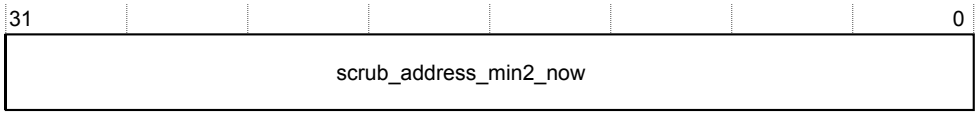

Figure 3-249 scrub_address_min2_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min2_now
Program to set the starting address for the scrub engine. When scrub_addr_mode2 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode2 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.250 scrub_address_max2_now

Configures the address space control for the scrub engine channel.

The scrub_address_max2_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1198`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

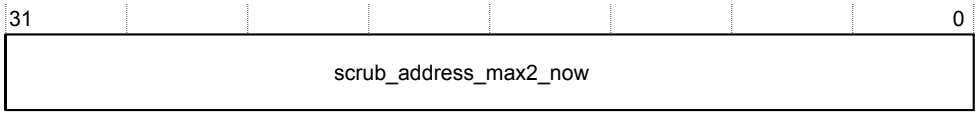

Figure 3-250 scrub_address_max2_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max2_now
Program to set the ending address for the scrub engine. When scrub_addr_mode2 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode2 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.251 scrub_control3_now

Scrub engine channel control register.

The scrub_control3_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x11A0`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

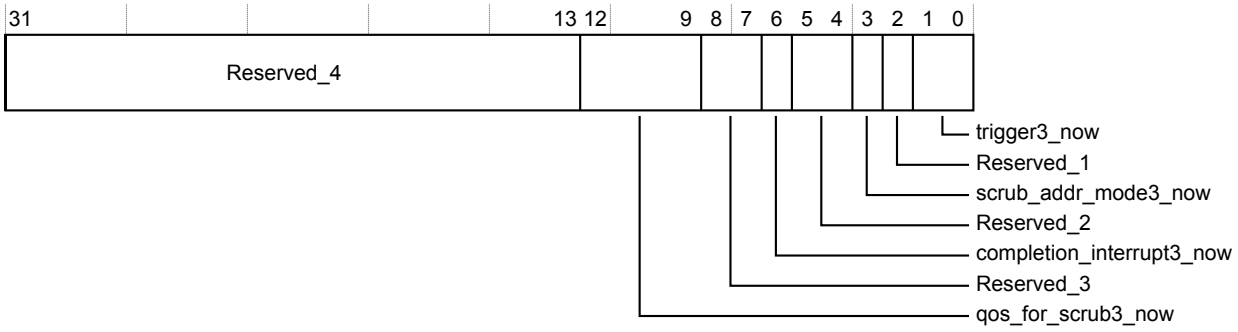

Figure 3-251 scrub_control3_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub3_now
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt3_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode3_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger3_now
Controls the trigger event associated with the channel operation.

3.3.252 scrub_address_min3_now

Configures the address space control for the scrub engine channel.

The scrub_address_min3_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11A4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

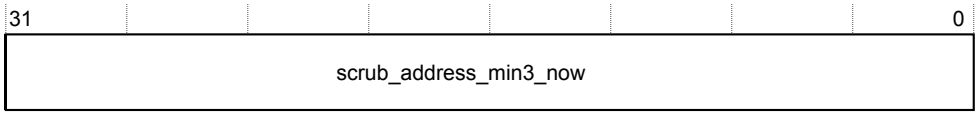

Figure 3-252 scrub_address_min3_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min3_now
Program to set the starting address for the scrub engine. When scrub_addr_mode3 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode3 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.253 scrub_address_max3_now

Configures the address space control for the scrub engine channel.

The scrub_address_max3_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11A8`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

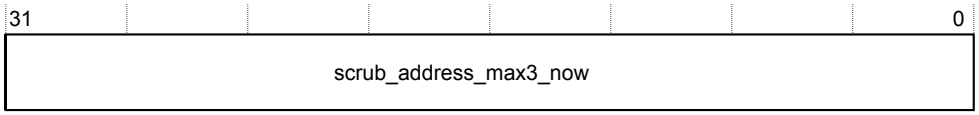

Figure 3-253 scrub_address_max3_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max3_now
Program to set the ending address for the scrub engine. When scrub_addr_mode3 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode3 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.254 scrub_control4_now

Scrub engine channel control register.

The scrub_control4_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x11B0`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

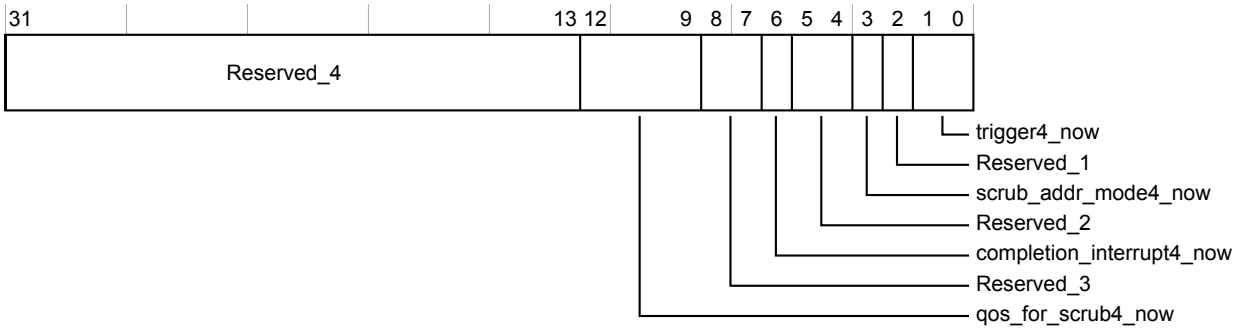

Figure 3-254 scrub_control4_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub4_now
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt4_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode4_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger4_now
Controls the trigger event associated with the channel operation.

3.3.255 scrub_address_min4_now

Configures the address space control for the scrub engine channel.

The scrub_address_min4_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11B4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

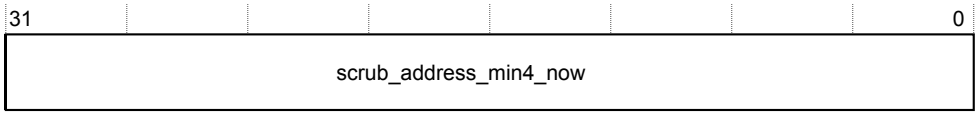

Figure 3-255 scrub_address_min4_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min4_now
Program to set the starting address for the scrub engine. When scrub_addr_mode4 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode4 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.256 scrub_address_max4_now

Configures the address space control for the scrub engine channel.

The scrub_address_max4_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11B8`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

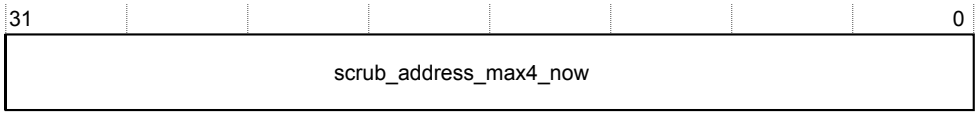

Figure 3-256 scrub_address_max4_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max4_now
Program to set the ending address for the scrub engine. When scrub_addr_mode4 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode4 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.257 scrub_control5_now

Scrub engine channel control register.

The scrub_control5_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x11C0`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

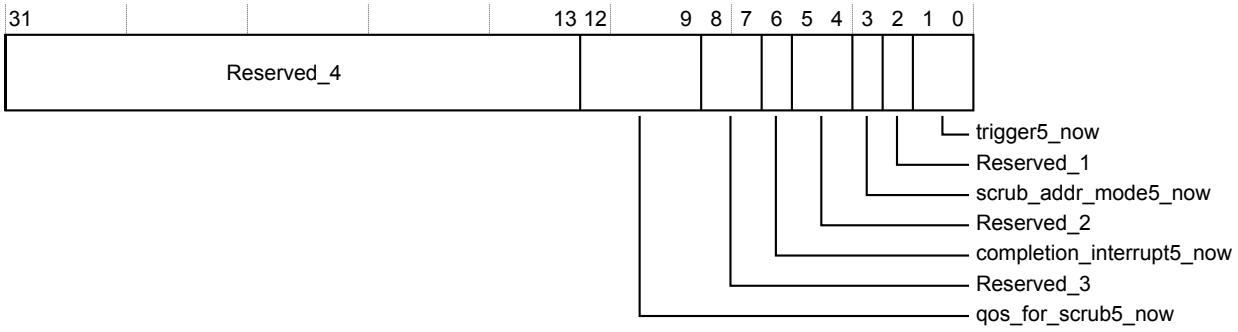

Figure 3-257 scrub_control5_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub5_now
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt5_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode5_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger5_now
Controls the trigger event associated with the channel operation.

3.3.258 scrub_address_min5_now

Configures the address space control for the scrub engine channel.

The scrub_address_min5_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11C4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

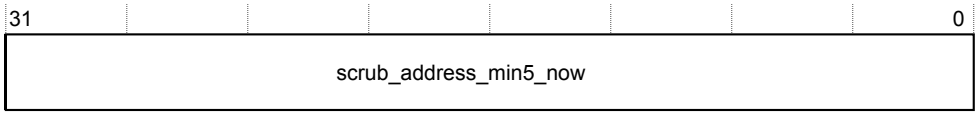

Figure 3-258 scrub_address_min5_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min5_now
Program to set the starting address for the scrub engine. When scrub_addr_mode5 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode5 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.259 scrub_address_max5_now

Configures the address space control for the scrub engine channel.

The scrub_address_max5_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11C8`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

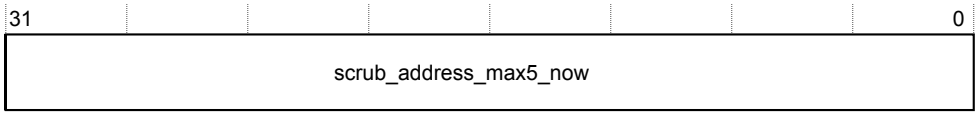

Figure 3-259 scrub_address_max5_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max5_now
Program to set the ending address for the scrub engine. When scrub_addr_mode5 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode5 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.260 scrub_control6_now

Scrub engine channel control register.

The scrub_control6_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x11D0`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

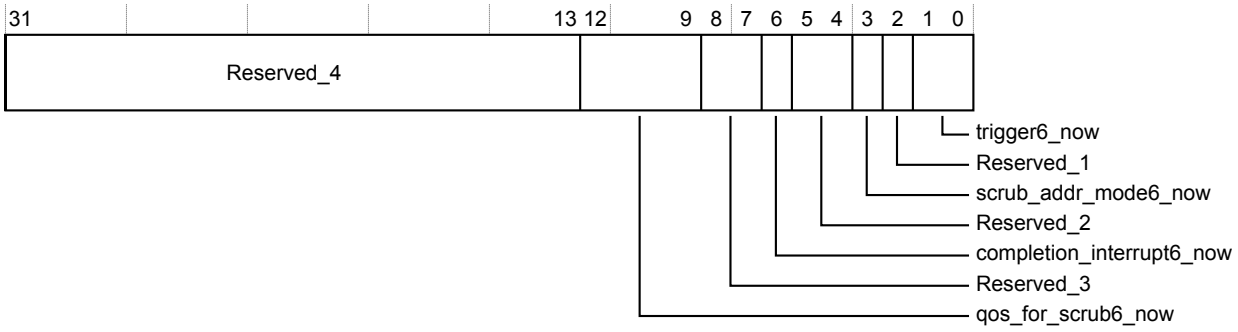

Figure 3-260 scrub_control6_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub6_now
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt6_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode6_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger6_now
Controls the trigger event associated with the channel operation.

3.3.261 scrub_address_min6_now

Configures the address space control for the scrub engine channel.

The scrub_address_min6_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11D4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

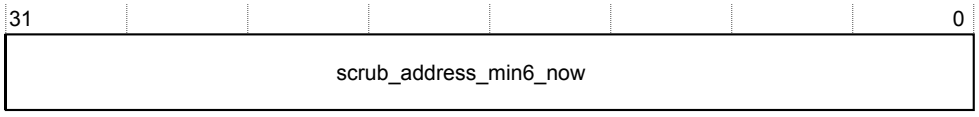

Figure 3-261 scrub_address_min6_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min6_now
Program to set the starting address for the scrub engine. When scrub_addr_mode6 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode6 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.262 scrub_address_max6_now

Configures the address space control for the scrub engine channel.

The scrub_address_max6_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11D8`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

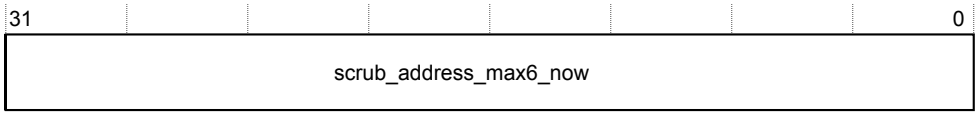

Figure 3-262 scrub_address_max6_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max6_now
Program to set the ending address for the scrub engine. When scrub_addr_mode6 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode6 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.263 scrub_control7_now

Scrub engine channel control register.

The scrub_control7_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x11E0`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

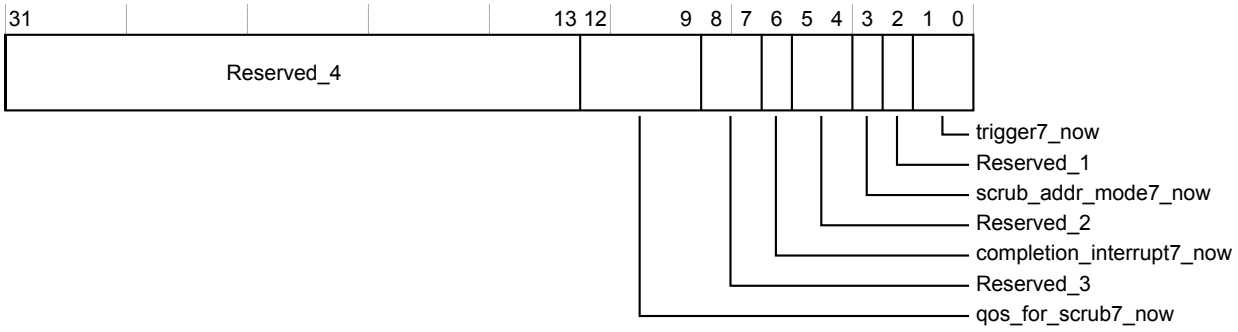

Figure 3-263 scrub_control7_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_4
Unused bits

[12:9] qos_for_scrub7_now
Configures QoS value of scrub operations

[8:7] Reserved_3
Unused bits

[6] completion_interrupt7_now
Configures whether to emit an event when the sequence completes
[5:4] Reserved_2
Unused bits
[3] scrub_addr_mode7_now
Configures scrub address mode
[2] Reserved_1
Unused bits
[1:0] trigger7_now
Controls the trigger event associated with the channel operation.

3.3.264 scrub_address_min7_now

Configures the address space control for the scrub engine channel.

The scrub_address_min7_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11E4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

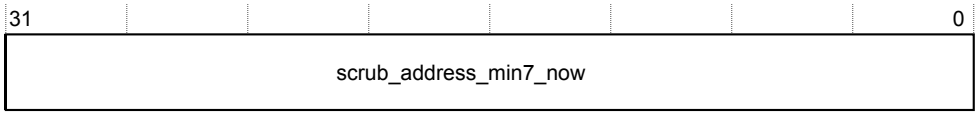

Figure 3-264 scrub_address_min7_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_min7_now
Program to set the starting address for the scrub engine. When scrub_addr_mode7 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode7 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.265 scrub_address_max7_now

Configures the address space control for the scrub engine channel.

The scrub_address_max7_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x11E8`
Type	Read-only
Reset	`0x00000000`

Width 32

The following figure shows the bit assignments.

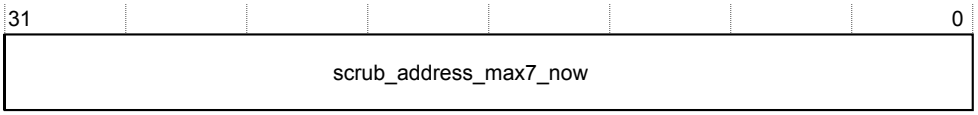

Figure 3-265 scrub_address_max7_now register bit assignments

The following shows the bit assignments.

[31:0] scrub_address_max7_now
Program to set the ending address for the scrub engine. When scrub_addr_mode7 is set to physical_address this register specifies logical rank [24:22], physical bank [21:18] and physical row address [17:0] directly. When scrub_addr_mode7 is set to system_address this register specifies the address in the same address format used by incoming system transactions.

3.3.266 feature_control_now

Control register for DMC features.

The feature_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x11F0`

Type Read-only

Reset `0x0AA00000`

Width 32

The following figure shows the bit assignments.

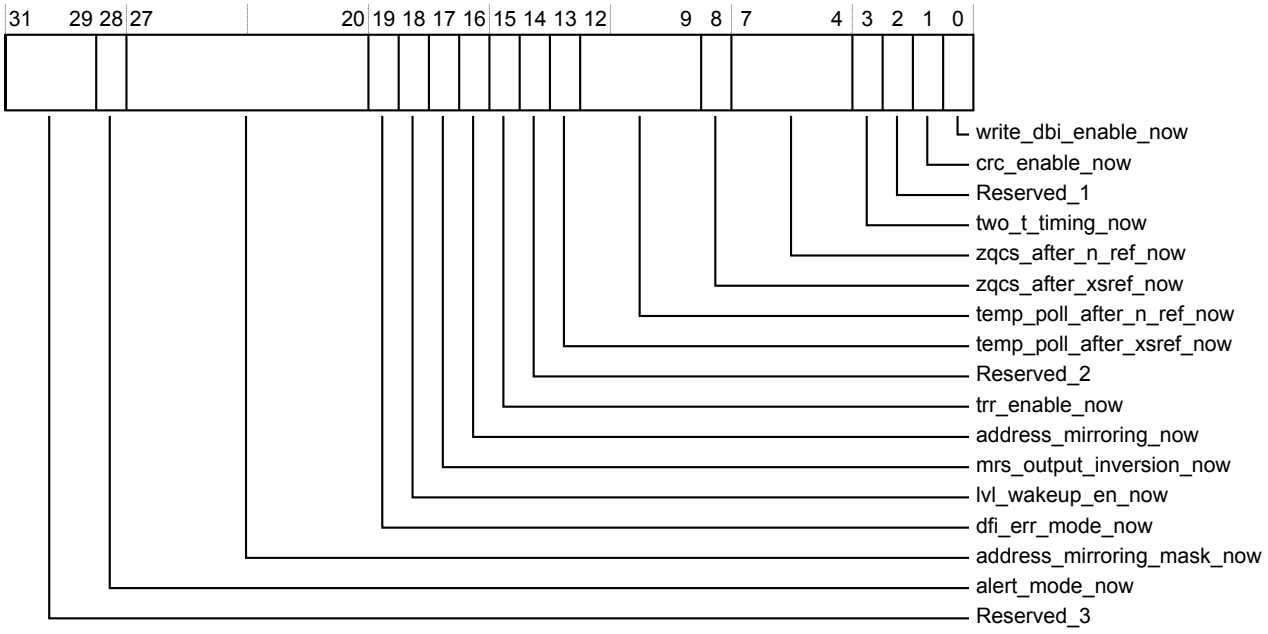

Figure 3-266 feature_control_now register bit assignments

The following shows the bit assignments.

[31:29] Reserved_3
Unused bits

[28] alert_mode_now
Configures the DMC behavior in response to dfi_alert_n being asserted. Note, when performing DIMM CA training using the ALERT pin this mode must be set to interrupt-only mode

[27:20] address_mirroring_mask_now
Each bit determines if address mirroring as per the DDR3/DDR4 RDIMM Design Specification must be applied to the corresponding rank. Set to 1 to enable mirroring, 0 to disable. Normally, this bit must be set high for odd physical ranks.

[19] dfi_err_mode_now
Configures the DMC behavior in response to dfi_err being asserted.

[18] lvl_wakeup_en_now
Program to enable the DMC to bring a rank out of self-refresh to perform PHY training. This must not be enabled when using geardown mode.

[17] mrs_output_inversion_now
Program to enable output inversion for MRS commands for DDR4 DIMMs.

[16] address_mirroring_now
Program to enable address mirroring for ranks identified by address_mirroring_mask.

[15] trr_enable_now
Program to enable issue of Target Row Refresh command on detection of potential maximum activate count (tMAC) violation. Must only be enabled for memories supporting this command.

[14] Reserved_2
Unused bits

[13] temp_poll_after_xsref_now
Program to insert an automatic temperature status poll command following exit from self-refresh.

[12:9] temp_poll_after_n_ref_now
Program to insert an automatic temperature status poll command following issue of n AUTOREFRESH commands. 0 disables the functionality. 1 is RESERVED

[8] zqcs_after_xsref_now
Program to insert an automatic ZQC short calibration command following exit from self-refresh.

[7:4] zqcs_after_n_ref_now
Program to insert an automatic ZQC short calibration command following n refreshes. 0 - disables the functionality. 1 is RESERVED

[3] two_t_timing_now
Program to enable or disable 2T command timing.

[2] Reserved_1
Unused bits

[1] crc_enable_now
Program to enable or disable Cyclic Redundancy Check (CRC) functionality on write data. Note: when enabling CRC t_wr, t_wtr and t_wtw must be extended by one cycle to accommodate the CRC functionality.

[0] write_dbi_enable_now
Program to enable or disable Data Bus Inversion (DBI) functionality for writes.

3.3.267 mux_control_now

Control the multiplexing options for the DMC.

The mux_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11F4`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

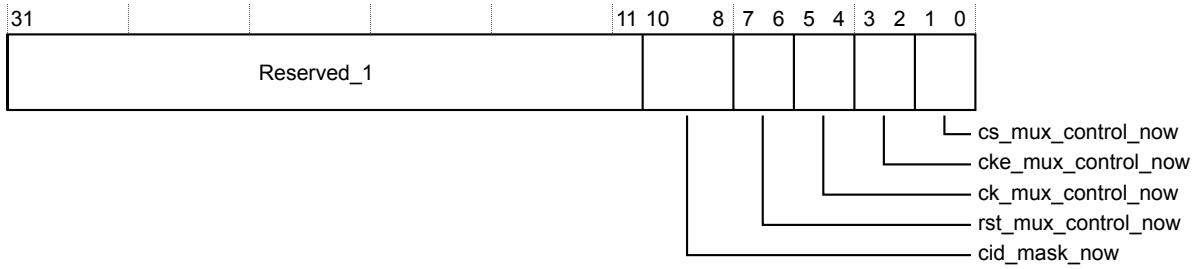

Figure 3-267 mux_control_now register bit assignments

The following shows the bit assignments.

[31:11] Reserved_1
Unused bits

[10:8] cid_mask_now
Program to mask inclusion of dfi_cid[2:0] output in parity calculation, where for each bit of cid_mask[2:0] a value of 1 means include the corresponding bit of dfi_cid[2:0].

[7:6] rst_mux_control_now
Program to control the multiplexing of the dfi_reset_n output for DIMM applications.

[5:4] ck_mux_control_now
Program to control the multiplexing of the dfi_ck output for DIMM applications.

[3:2] cke_mux_control_now
Program to control the multiplexing of the dfi_cke output for DIMM applications.

[1:0] cs_mux_control_now
Program to control the multiplexing of the dfi_cs_n output for DIMM applications.

3.3.268 rank_remap_control_now

Control register for rank remap.

The rank_remap_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x11F8`
Type	Read-only
Reset	`0x76543210`
Width	32

The following figure shows the bit assignments.

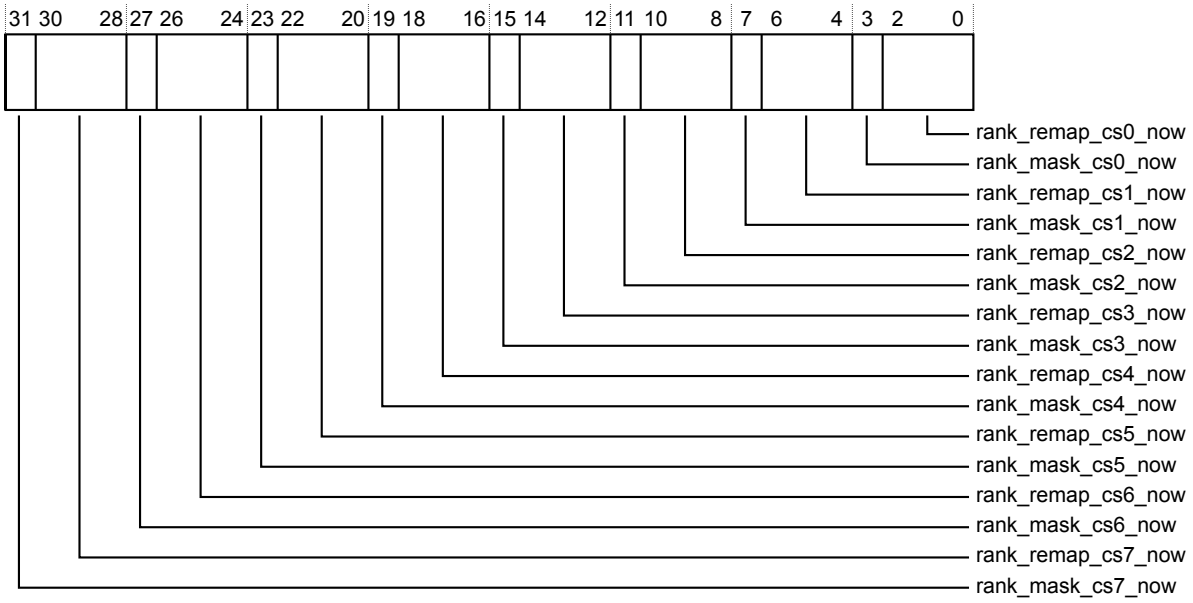

Figure 3-268 rank_remap_control_now register bit assignments

The following shows the bit assignments.

[31] rank_mask_cs7_now
Program to cause the DMC to abort all transactions to DRAM rank 7. Can be used to block transactions to a rank that is in maximum power down.

[30:28] rank_remap_cs7_now
Program to remap rank address 7 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[27] rank_mask_cs6_now
Program to cause the DMC to abort all transactions to DRAM rank 6. Can be used to block transactions to a rank that is in maximum power down.

[26:24] rank_remap_cs6_now
Program to remap rank address 6 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[23] rank_mask_cs5_now
Program to cause the DMC to abort all transactions to DRAM rank 5. Can be used to block transactions to a rank that is in maximum power down.

[22:20] rank_remap_cs5_now
Program to remap rank address 5 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[19] rank_mask_cs4_now
Program to cause the DMC to abort all transactions to DRAM rank 4. Can be used to block transactions to a rank that is in maximum power down.

[18:16] rank_remap_cs4_now
Program to remap rank address 4 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[15] rank_mask_cs3_now
Program to cause the DMC to abort all transactions to DRAM rank 3. Can be used to block transactions to a rank that is in maximum power down.

[14:12] rank_remap_cs3_now
Program to remap rank address 3 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[11] rank_mask_cs2_now
Program to cause the DMC to abort all transactions to DRAM rank 2. Can be used to block transactions to a rank that is in maximum power down.

[10:8] rank_remap_cs2_now
Program to remap rank address 2 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[7] rank_mask_cs1_now
Program to cause the DMC to abort all transactions to DRAM rank 1. Can be used to block transactions to a rank that is in maximum power down.

[6:4] rank_remap_cs1_now
Program to remap rank address 1 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

[3] rank_mask_cs0_now
Program to cause the DMC to abort all transactions to DRAM rank 0. Can be used to block transactions to a rank that is in maximum power down.

[2:0] rank_remap_cs0_now
Program to remap rank address 0 to DRAM rank 0..7. Used to remap ranks when replacing DIMMs.

3.3.269 t_refi_now

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8.

The t_refi_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1200`
Type	Read-only
Reset	`0x00090100`
Width	32

The following figure shows the bit assignments.

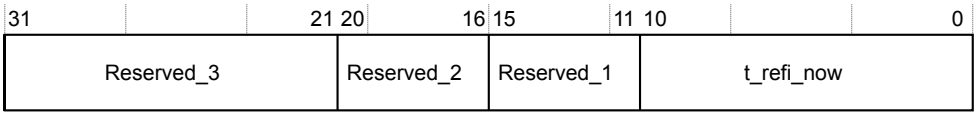

Figure 3-269 t_refi_now register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits
[20:16] Reserved_2
Unused bits
[15:11] Reserved_1
Unused bits
[10:0] t_refi_now
t_refi_now bitfield. The supported range for this bitfield is 63-2047.

3.3.270 t_rfc_now

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank.

The t_rfc_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1204`
Type	Read-only
Reset	`0x00008C23`
Width	32

The following figure shows the bit assignments.

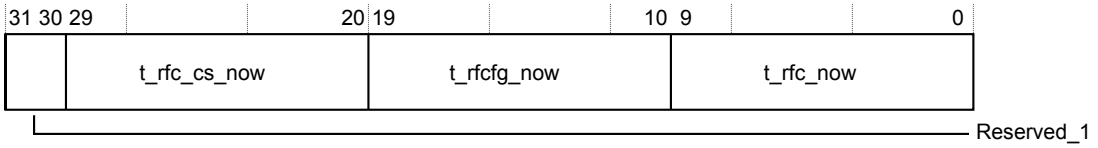

Figure 3-270 t_rfc_now register bit assignments

The following shows the bit assignments.

[31:30] Reserved_1
Unused bits
[29:20] t_rfc_cs_now
Configures the minimum delay between AUTOREFRESH operations to different ranks. The supported range for this bitfield is 0-700.
[19:10] t_rfcfg_now
Configures the tRFC timing parameter for fine-grained AUTOREFRESH operations. The supported range for this bitfield is 2-700.
[9:0] t_rfc_now
Configures the tRFC timing parameter for all-bank AUTOREFRESH operations. The supported range for this bitfield is 2-700.

3.3.271 t_mrr_now

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note: this value is used to determine the data cycles returned as a result of an MRR command.

The t_mrr_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1208`

Type Read-only

Reset `0x00000002`

Width 32

The following figure shows the bit assignments.

Figure 3-271 t_mrr_now register bit assignments

The following shows the bit assignments.

[31:9] Reserved_2

Unused bits

[8:7] Reserved_1

Unused bits

[6:0] t_mrr_now

t_mrr_now bitfield. The supported range for this bitfield is 1-127.

3.3.272 t_mrw_now

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed.

The t_mrw_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x120C`

Type Read-only

Reset `0x0000000C`

Width 32

The following figure shows the bit assignments.

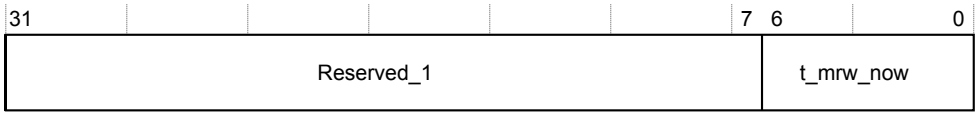

Figure 3-272 t_mrw_now register bit assignments

The following shows the bit assignments.

[31:7] Reserved_1
Unused bits

[6:0] t_mrw_now
t_mrw_now bitfield. The supported range for this bitfield is 12-127.

3.3.273 t_rdpden_now

Configures the tRDPDEN timing parameter. This determines the delay applied after a Read command before a power down command can be issued to the same rank.

The t_rdpden_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1210`
Type	Read-only
Reset	`0x00000002`
Width	32

The following figure shows the bit assignments.

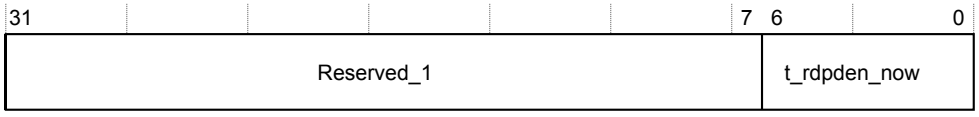

Figure 3-273 t_rdpden_now register bit assignments

The following shows the bit assignments.

[31:7] Reserved_1
Unused bits

[6:0] t_rdpden_now
t_rdpden_now bitfield. The supported range for this bitfield is 0-126.

3.3.274 t_rcd_now

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank.

The t_rcd_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1218`

Type Read-only
Reset 0x00000005
Width 32

The following figure shows the bit assignments.

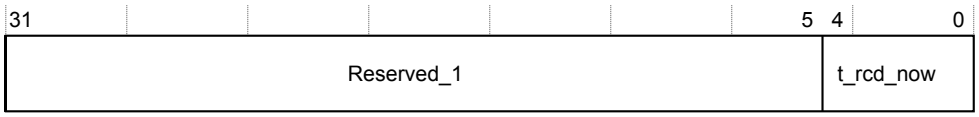

Figure 3-274 t_rcd_now register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits
[4:0] t_rcd_now
t_rcd_now bitfield. The supported range for this bitfield is 4-18.

3.3.275 t_ras_now

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank.

The t_ras_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x121C
Type Read-only
Reset 0x0000000E
Width 32

The following figure shows the bit assignments.

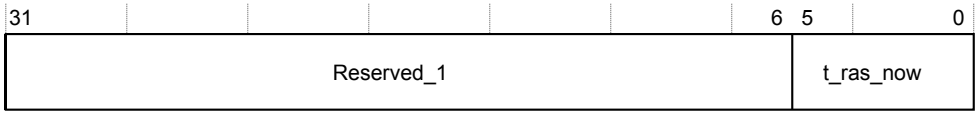

Figure 3-275 t_ras_now register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits
[5:0] t_ras_now
t_ras_now bitfield. The supported range for this bitfield is 8-39.

3.3.276 t_rp_now

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank.

The t_rp_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1220`
Type	Read-only
Reset	`0x00000005`
Width	32

The following figure shows the bit assignments.

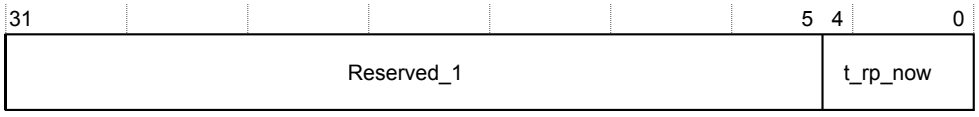

Figure 3-276 t_rp_now register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits

[4:0] t_rp_now
t_rp_now bitfield. The supported range for this bitfield is 4-18.

3.3.277 t_rpall_now

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank.

The t_rpall_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1224`
Type	Read-only
Reset	`0x00000005`
Width	32

The following figure shows the bit assignments.

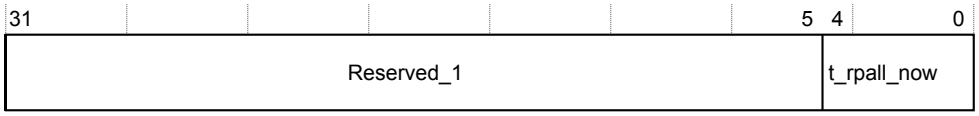

Figure 3-277 t_rpall_now register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits

[4:0] t_rpall_now
t_rpall_now bitfield. The supported range for this bitfield is 4-18.

3.3.278 t_rrd_now

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, and a different bank group, respectively, as described in the DDR4 specification.

The t_rrd_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0x1228`
Type	Read-only
Reset	`0x00000404`
Width	32

The following figure shows the bit assignments.

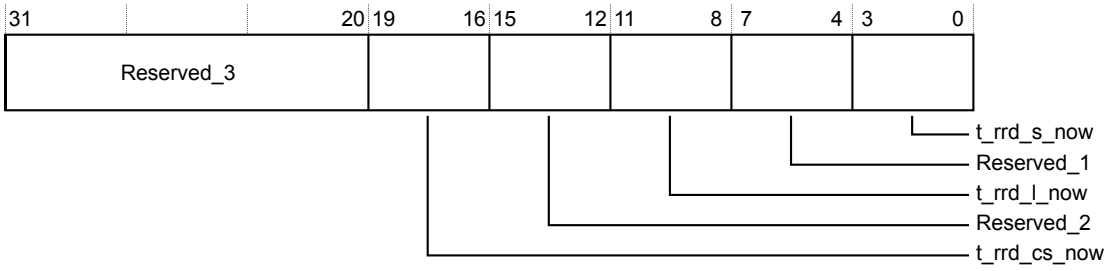

Figure 3-278 t_rrd_now register bit assignments

The following shows the bit assignments.

[31:20] Reserved_3

Unused bits

[19:16] t_rrd_cs_now

t_rrd_cs_now bitfield. The supported range for this bitfield is 0-15.

[15:12] Reserved_2

Unused bits

[11:8] t_rrd_l_now

t_rrd_l_now bitfield. The supported range for this bitfield is 1-15.

[7:4] Reserved_1

Unused bits

[3:0] t_rrd_s_now

t_rrd_s_now bitfield. The supported range for this bitfield is 1-15.

3.3.279 t_act_window_now

Configures the tFAW and tMAWi timing parameters.

The t_act_window_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x122C
Type Read-only
Reset 0x03560014
Width 32

The following figure shows the bit assignments.

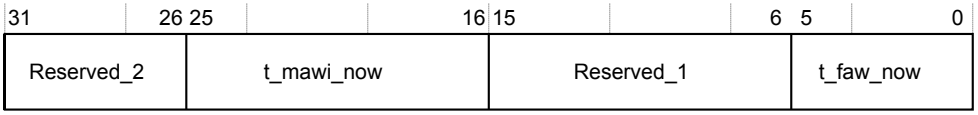

Figure 3-279 t_act_window_now register bit assignments

The following shows the bit assignments.

[31:26] Reserved_2
Unused bits
[25:16] t_mawi_now
Sets the value of the average delay required between ACTIVATE commands to the same row to not violate tMAC in tMAW. Must be programmed to (tMAW/(tMAC/2)).
[15:6] Reserved_1
Unused bits
[5:0] t_faw_now
The DMC does not issue more than 4 ACTIVATE commands within a rolling tFAW window. The supported range for this bitfield is 8-63.

3.3.280 t_rtr_now

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), and different chip-selects (t_rtr_cs).

The t_rtr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset 0x1234
Type Read-only
Reset 0x00040404
Width 32

The following figure shows the bit assignments.

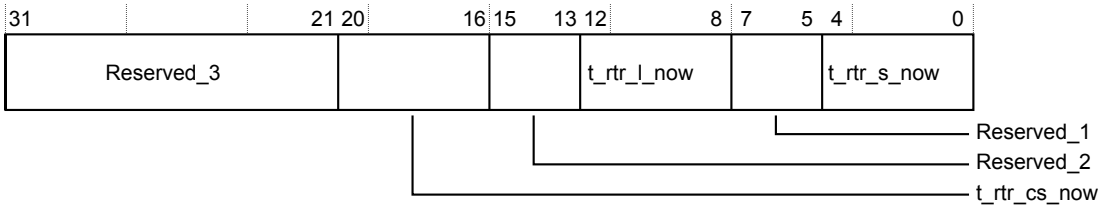

Figure 3-280 t_rtr_now register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits
[20:16] t_rtr_cs_now
t_rtr_cs_now bitfield. The supported range for this bitfield is 4-31.
[15:13] Reserved_2
Unused bits
[12:8] t_rtr_l_now
t_rtr_l_now bitfield. The supported range for this bitfield is 4-31.
[7:5] Reserved_1
Unused bits
[4:0] t_rtr_s_now
t_rtr_s_now bitfield. The supported range for this bitfield is 4-31.

3.3.281 t_rtw_now

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_trw_l), and other chip-selects (t_rtw_cs).

The t_rtw_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1238`
Type	Read-only
Reset	`0x00060606`
Width	32

The following figure shows the bit assignments.

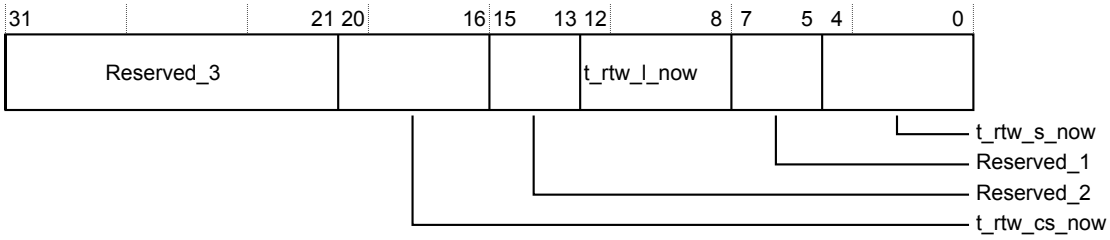

Figure 3-281 t_rtw_now register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits
[20:16] t_rtw_cs_now
t_rtw_cs_now bitfield. The supported range for this bitfield is 4-31.
[15:13] Reserved_2
Unused bits
[12:8] t_rtw_l_now
t_rtw_l_now bitfield. The supported range for this bitfield is 4-31.
[7:5] Reserved_1
Unused bits
[4:0] t_rtw_s_now
t_rtw_s_now bitfield. The supported range for this bitfield is 4-31.

3.3.282 t_rtp_now

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank.

The t_rtp_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x123C`

Type Read-only

Reset `0x00000004`

Width 32

The following figure shows the bit assignments.

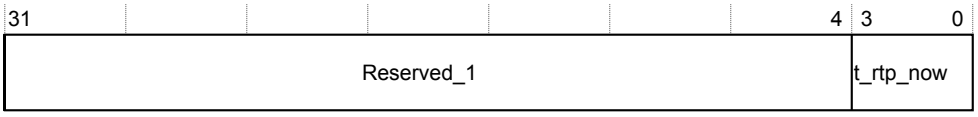

Figure 3-282 t_rtp_now register bit assignments

The following shows the bit assignments.

[31:4] Reserved_1

Unused bits

[3:0] t_rtp_now

t_rtp_now bitfield. The supported range for this bitfield is 4-15.

3.3.283 t_wr_now

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITEs, to the same bank. Note: this must take into account CRC timing requirements.

The t_wr_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1244`

Type Read-only

Reset `0x00000005`

Width 32

The following figure shows the bit assignments.

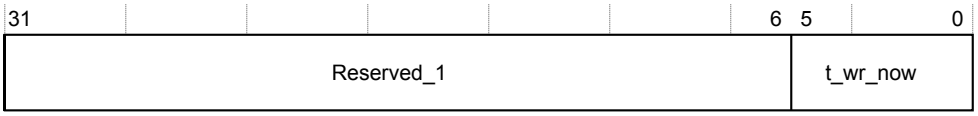

Figure 3-283 t_wr_now register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_wr_now
t_wr_now bitfield. The supported range for this bitfield is 4-63.

3.3.284 t_wtr_now

This register configures the write-to-read timing parameter, for same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs) transactions. These parameters must take into account CRC timing requirements.

The t_wtr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1248`
Type	Read-only
Reset	`0x00040404`
Width	32

The following figure shows the bit assignments.

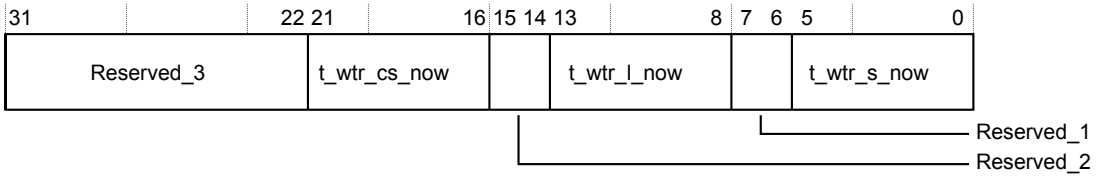

Figure 3-284 t_wtr_now register bit assignments

The following shows the bit assignments.

[31:22] Reserved_3
Unused bits

[21:16] t_wtr_cs_now
t_wtr_cs_now bitfield. The supported range for this bitfield is 2-63.

[15:14] Reserved_2
Unused bits

[13:8] t_wtr_l_now
t_wtr_l_now bitfield. The supported range for this bitfield is 4-63.

[7:6] Reserved_1
Unused bits

[5:0] t_wtr_s_now
t_wtr_s_now bitfield. The supported range for this bitfield is 4-63.

3.3.285 t_wtw_now

This register configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes. These parameters must take into account CRC timing requirements.

The t_wtw_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x124C

Type Read-only

Reset 0x00040404

Width 32

The following figure shows the bit assignments.

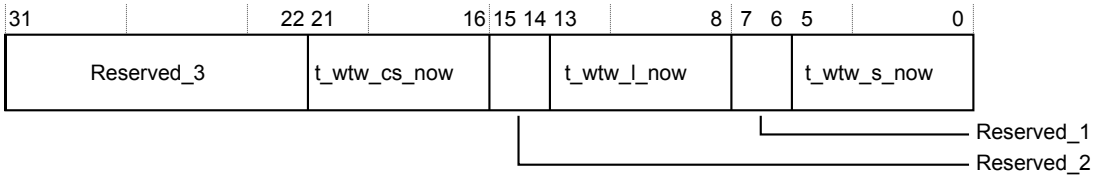

Figure 3-285 t_wtw_now register bit assignments

The following shows the bit assignments.

[31:22] Reserved_3

Unused bits

[21:16] t_wtw_cs_now

t_wtw_cs_now bitfield. The supported range for this bitfield is 4-35.

[15:14] Reserved_2

Unused bits

[13:8] t_wtw_l_now

t_wtw_l_now bitfield. The supported range for this bitfield is 4-35.

[7:6] Reserved_1

Unused bits

[5:0] t_wtw_s_now

t_wtw_s_now bitfield. The supported range for this bitfield is 4-35.

3.3.286 t_xmpd_now

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank.

The t_xmpd_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1254

Type Read-only

Reset 0x000003FF

Width 32

The following figure shows the bit assignments.

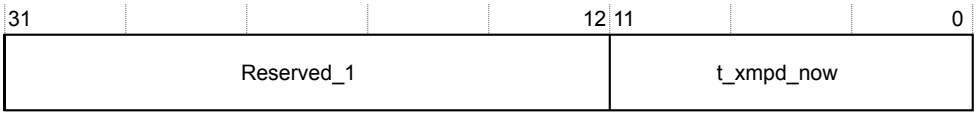

Figure 3-286 t_xmpd_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_1
Unused bits

[11:0] t_xmpd_now
t_xmpd_now bitfield. The supported range for this bitfield is 1-4094.

3.3.287 t_ep_now

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank.

The t_ep_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1258

Type Read-only

Reset 0x00000002

Width 32

The following figure shows the bit assignments.

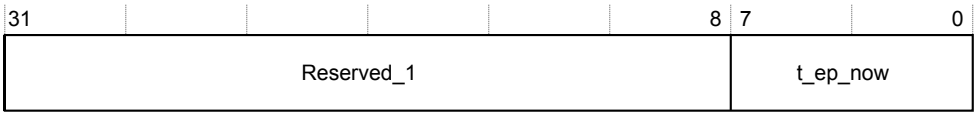

Figure 3-287 t_ep_now register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:0] t_ep_now
t_ep_now bitfield. The supported range for this bitfield is 1-255.

3.3.288 t_xp_now

This register configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). The t_xpdll parameter must be greater than or equal to tRCD and tCKE, and the t_xp parameter must be greater than or equal to tMPX_S.

The t_xp_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x125C

Type Read-only

Reset 0x00060002

Width 32

The following figure shows the bit assignments.

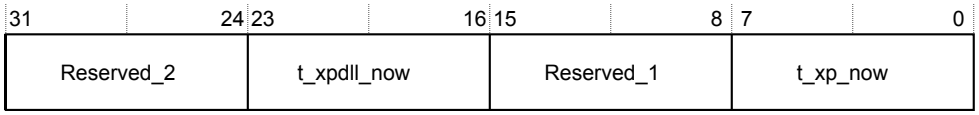

Figure 3-288 t_xp_now register bit assignments

The following shows the bit assignments.

[31:24] Reserved_2

Unused bits

[23:16] t_xpdll_now

This delay is applied for subsequent commands requiring a DLL The supported range for this bitfield is 5-255.

[15:8] Reserved_1

Unused bits

[7:0] t_xp_now

This delay is applied for subsequent commands not requiring a DLL The supported range for this bitfield is 1-255.

3.3.289 t_esr_now

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank.

The t_esr_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1260

Type Read-only

Reset 0x0000000E

Width 32

The following figure shows the bit assignments.

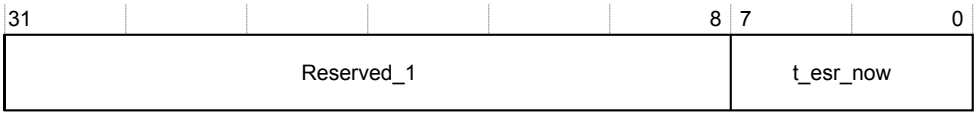

Figure 3-289 t_esr_now register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:0] t_esr_now
t_esr_now bitfield. The supported range for this bitfield is 1-255.

3.3.290 t_xsr_now

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank.

The t_xsr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1264`
Type	Read-only
Reset	`0x05120100`
Width	32

The following figure shows the bit assignments.

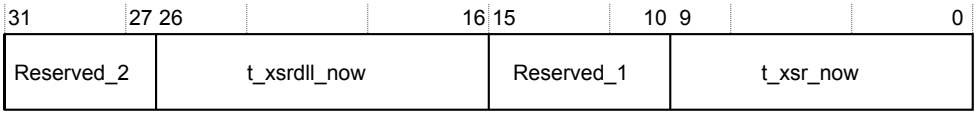

Figure 3-290 t_xsr_now register bit assignments

The following shows the bit assignments.

[31:27] Reserved_2
Unused bits

[26:16] t_xsrdll_now
This delay is applied for subsequent commands requiring a DLL. The supported range for this bitfield is 1-2047.

[15:10] Reserved_1
Unused bits

[9:0] t_xsr_now
This delay is applied for subsequent commands not requiring a DLL. The supported range for this bitfield is 1-1023.

3.3.291 t_esrck_now

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state.

The t_esrck_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1268
Type	Read-only
Reset	0x00000005
Width	32

The following figure shows the bit assignments.

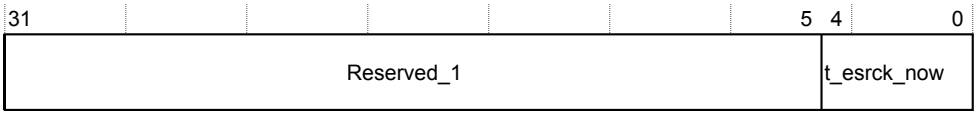

Figure 3-291 t_esrck_now register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits

[4:0] t_esrck_now
t_esrck_now bitfield. The supported range for this bitfield is 1-31.

3.3.292 t_ckxsr_now

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state.

The t_ckxsr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x126C
Type	Read-only
Reset	0x00000001
Width	32

The following figure shows the bit assignments.

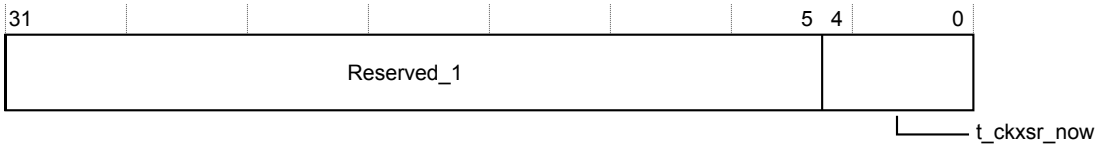

Figure 3-292 t_ckxsr_now register bit assignments

The following shows the bit assignments.

[31:5] Reserved_1
Unused bits

[4:0] t_ckxsr_now
t_ckxsr_now bitfield. The supported range for this bitfield is 1-31.

3.3.293 t_cmd_now

This register configures command signalling timing.

The t_cmd_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1270`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

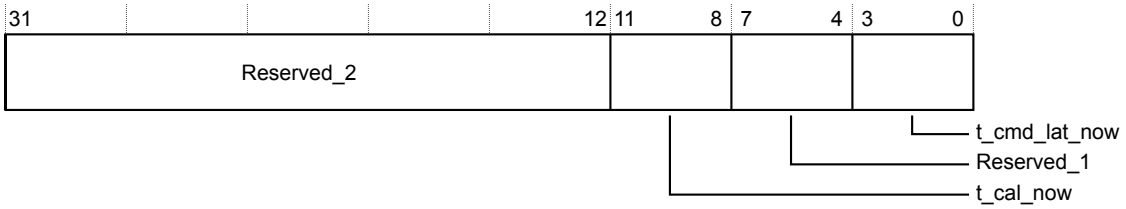

Figure 3-293 t_cmd_now register bit assignments

The following shows the bit assignments.

[31:12] Reserved_2
Unused bits

[11:8] t_cal_now
Specifies the Command Address latency at the DDR4 device. The supported range for this bitfield is 0-10.

——— **Note** ———
t_cal must be zero when using RDIMMs.
———————————

[7:4] Reserved_1
Unused bits

[3:0] t_cmd_lat_now
Specifies the number of DFI clocks after the **dfi_cs_n** signal is asserted until the associated command and address bus is driven. The supported range for this bitfield is 0-10.

3.3.294 t_parity_now

Parity latencies t_parinlat and t_completion.

The t_parity_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1274

Type Read-only

Reset 0x00000900

Width 32

The following figure shows the bit assignments.

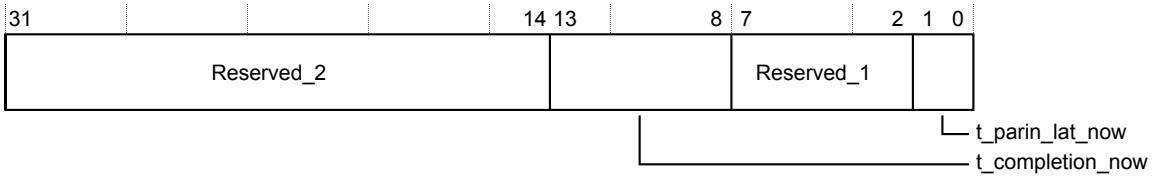

Figure 3-294 t_parity_now register bit assignments

The following shows the bit assignments.

[31:14] Reserved_2
Unused bits

[13:8] t_completion_now
Determines the DMC clock cycle delay between when the dfi_cs_n signal is asserted and the cycle in which that command can be considered complete. In programming this value, you must consider the DFI timing parameters t_wrdata_delay, t_error_resp, t_crcmax_lat, and t_phyrdlatmax to ensure all have expired, where applicable, within t_completion cycles. The supported range for this bitfield is 9-62.

[7:2] Reserved_1
Unused bits

[1:0] t_parin_lat_now
Specifies the number of DFI clocks between when the dfi_cs_n signal is asserted and when the associated dfi_parity_in signal is driven. The supported range for this bitfield is 0-3.

3.3.295 t_zqcs_now

Configures the delay to apply following a ZQC-Short calibration command.

The t_zqcs_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1278

Type Read-only

Reset 0x00000040

Width 32

The following figure shows the bit assignments.

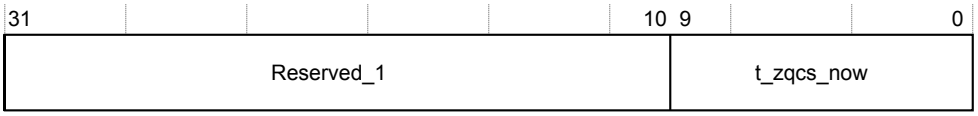

Figure 3-295 t_zqcs_now register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits

[9:0] t_zqcs_now
t_zqcs_now bitfield. The supported range for this bitfield is 2-1023.

3.3.296 t_rddata_en_now

Determines the time between a READ command commencing on the DFI interface, and the assertion of the dfi_read_en signal.

The t_rddata_en_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1300`
Type	Read-only
Reset	`0x00000001`
Width	32

The following figure shows the bit assignments.

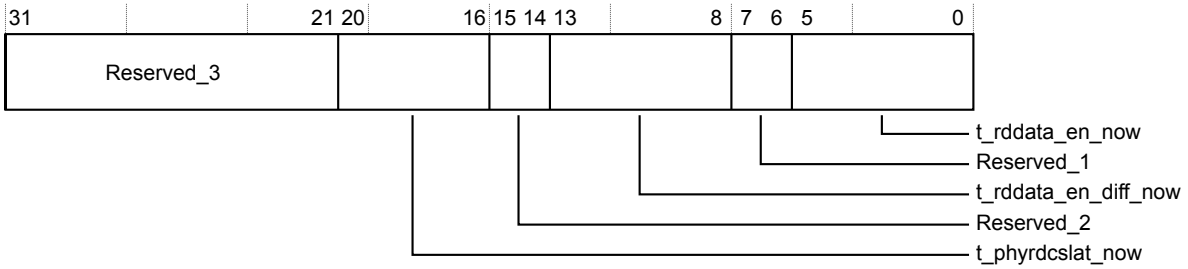

Figure 3-296 t_rddata_en_now register bit assignments

The following shows the bit assignments.

[31:21] Reserved_3
Unused bits

[20:16] t_phyrdcslat_now
Specifies the number of DFI PHY clocks between a READ command commencing on the DFI interface (assertion of chip-select), and when the associated **dfi_rddata_cs_n** signal is asserted. The supported range for this bitfield is 0-31.

[15:14] Reserved_2
Unused bits

[13:8] t_rddata_en_diff_now
Describes a PHY specific value useful for aligning t_rddata_en for a specific PHY. This value has no effect on the controller. The supported range for this bitfield is 0-40.

[7:6] Reserved_1
Unused bits

[5:0] t_rddata_en_now
t_rddata_en_now bitfield. The supported range for this bitfield is 0-40.

3.3.297 t_phyrdlat_now

Determines the maximum possible time between the assertion of the dfi_read_en signal, and the assertion of the dfi_rddata_valid signal by the PHY.

The t_phyrdlat_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1304`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

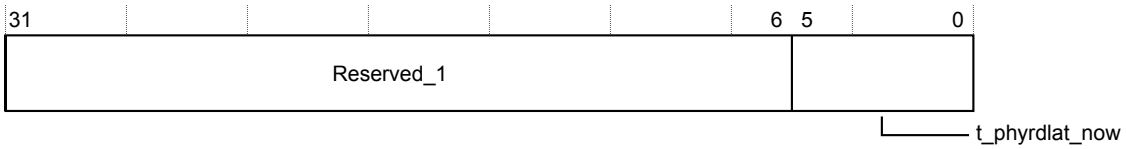

Figure 3-297 t_phyrdlat_now register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_phyrdlat_now
Determines the maximum time between the assertion of the dfi_read_en signal and the assertion of the dfi_rddata_valid signal by the PHY. The supported range for this bitfield is 1-62.

3.3.298 t_phywrlat_now

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrdata_en, dfi_wrdata_cs and dfi_wrdata signals.

The t_phywrlat_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset `0x1308`

Type Read-only

Reset `0x00000001`

Width 32

The following figure shows the bit assignments.

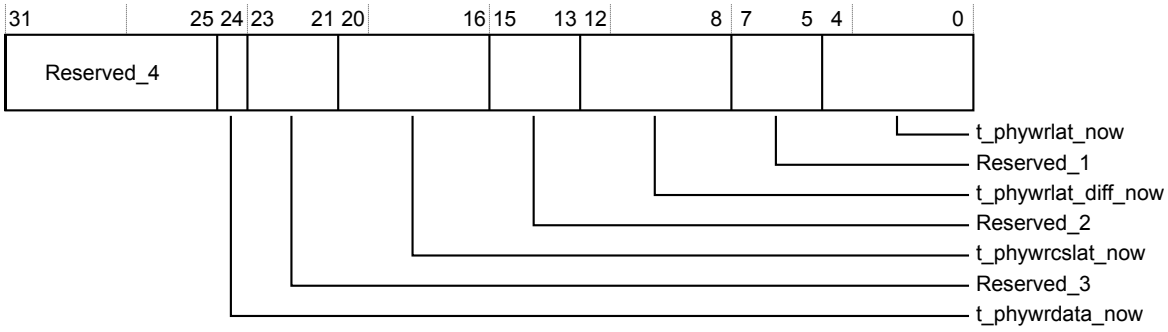

Figure 3-298 t_phywrlat_now register bit assignments

The following shows the bit assignments.

[31:25] Reserved_4
Unused bits

[24] t_phywrdata_now
Determines the time between the assertion of the dfi_wrdata_en and dfi_wrdata signals. The supported range for this bitfield is 0-1.

[23:21] Reserved_3
Unused bits

[20:16] t_phywrcslat_now
Specifies the number of DFI PHY clocks between when a write command is sent on the DFI control interface (dfi_cs_n assertion) and when the associated dfi_wrdata_cs_n signal is asserted. The supported range for this bitfield is 0-31.

[15:13] Reserved_2
Unused bits

[12:8] t_phywrlat_diff_now
Describes the PHY specific value useful for aligning t_phywrlat for a specific PHY. This value has no effect on the controller. The supported range for this bitfield is 0-31.

[7:5] Reserved_1
Unused bits

[4:0] t_phywrlat_now
Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the dfi_wrdata_en signal. The supported range for this bitfield is 0-31.

3.3.299 rdlvl_control_now

This register determines the DMC behavior during read training operations.

The rdlvl_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1310`
Type	Read-only
Reset	`0x00001080`
Width	32

The following figure shows the bit assignments.

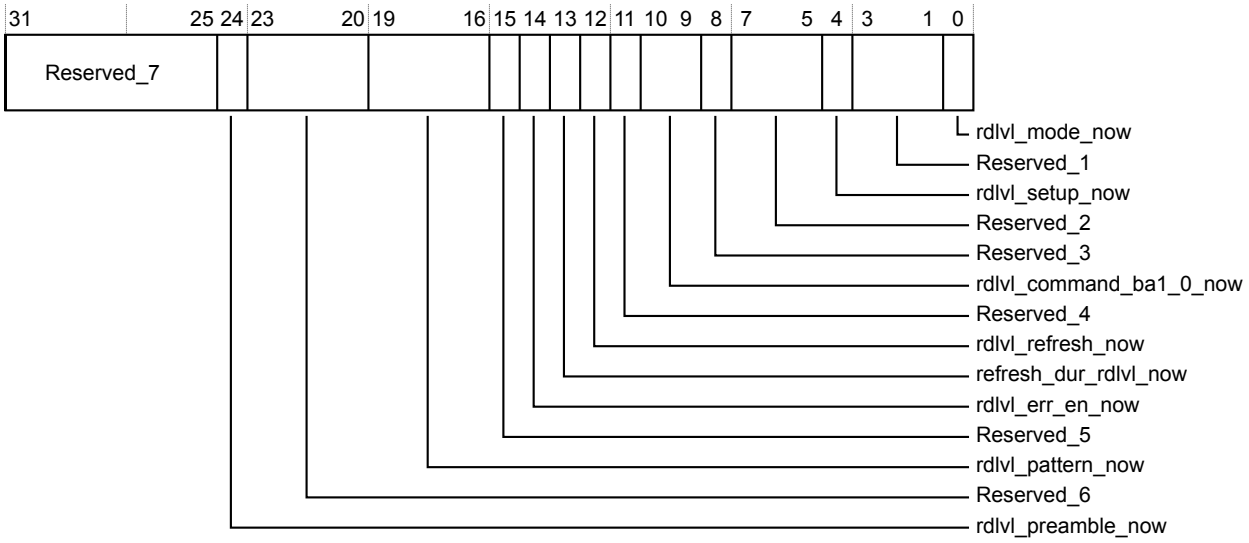

Figure 3-299 rdlvl_control_now register bit assignments

The following shows the bit assignments.

[31:25] Reserved_7
Unused bits

[24] rdlvl_preamble_now
For DDR4 program to enable or disable issue of preamble training mode MRS prior to performing read leveling training.

[23:20] Reserved_6
Unused bits

[19:16] rdlvl_pattern_now
Program the value to be driven onto dfi_lvl_pattern during training. The DMC ignores the value. For default DFI encodings see the DFI specification [5].

[15] Reserved_5
Unused bits

[14] rdlvl_err_en_now
If enabled replay commands because of dfi_err during training.

[13] refresh_dur_rdlvl_now
Program to enable AUTOREFRESH commands to be generated during training operations. When enabled (1'b1), the DMC exits a training sequence to perform refresh.

[12] rdlvl_refresh_now
Program to enable or disable issue of an AUTOREFRESH command prior to performing read leveling training.

[11] Reserved_4
Unused bits

[10:9] rdlvl_command_ba1_0_now
Program the BA address to use for training commands.

[8] Reserved_3
Unused bits

[7:5] Reserved_2
Unused bits

[4] rdlvl_setup_now
Program the command that sets up the DRAM for read leveling training.

[3:1] Reserved_1
Unused bits

[0] rdlvl_mode_now
Program the mode used for read leveling training.

3.3.300 rdlvl_mrs_now

This register determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl_control register.

The rdlvl_mrs_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1314`

Type Read-only

Reset `0x00000004`

Width 32

The following figure shows the bit assignments.

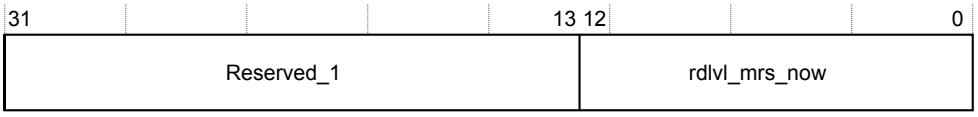

Figure 3-300 rdlvl_mrs_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_1

Unused bits

[12:0] rdlvl_mrs_now

Program the Mode Register command the DMC uses to place the DRAM into training mode. Set address bits [2:0] for the Mode Register write to MR3.

3.3.301 t_rdlvl_en_now

Configures the t_rdlvl_en timing parameter. This specifies the cycle delay between asserting dfi_rdlvl_en and the first training command, and also the cycle delay between deasserting dfi_rdlvl_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training.

The t_rdlvl_en_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1318`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

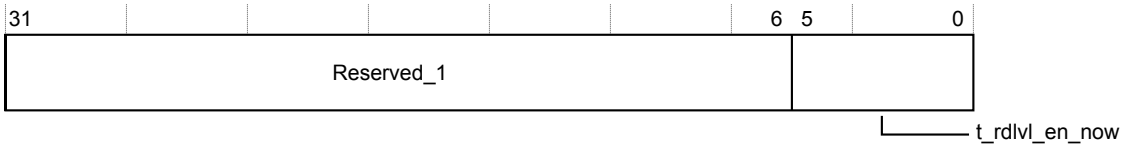

Figure 3-301 t_rdlvl_en_now register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_rdlvl_en_now
t_rdlvl_en_now bitfield. The supported range for this bitfield is 1-63.

3.3.302 t_rdlvl_rr_now

Configures the t_rdlvl_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi_rdlvl_en after observing dfi_rdlvl_resp.

The t_rdlvl_rr_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x131C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

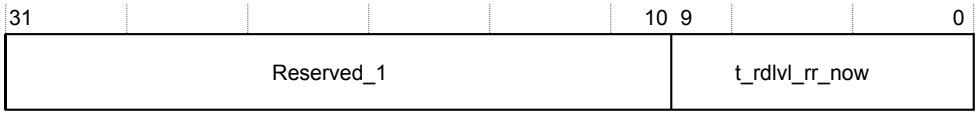

Figure 3-302 t_rdlvl_rr_now register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits

[9:0] t_rdlvl_rr_now
t_rdlvl_rr_now bitfield. The supported range for this bitfield is 4-1023.

3.3.303 wrlvl_control_now

This register determines the DMC behavior during write training operations.

The wrlvl_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1320
Type Read-only
Reset 0x00001000
Width 32

The following figure shows the bit assignments.

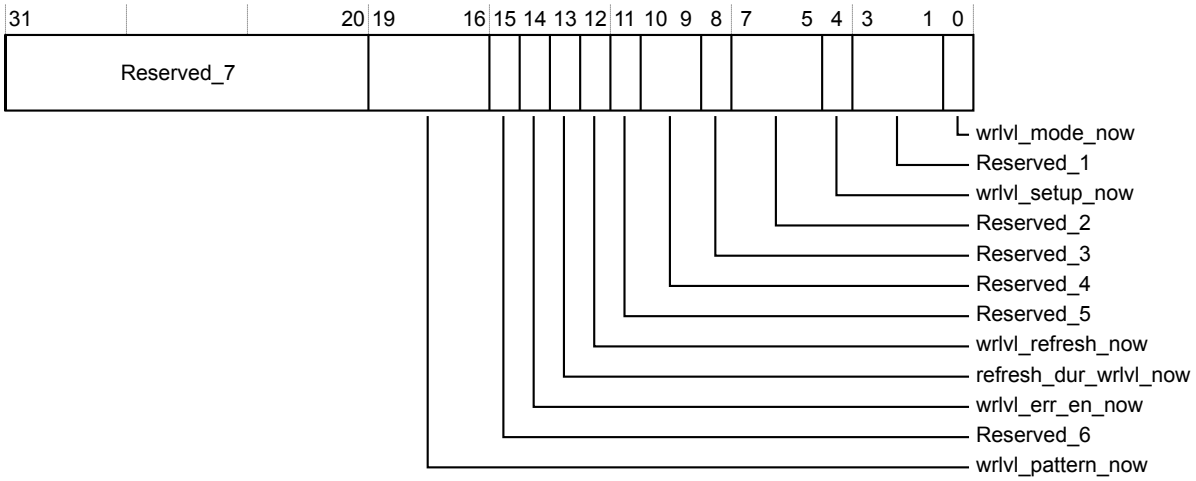

Figure 3-303 wrlvl_control_now register bit assignments

The following shows the bit assignments.

[31:20] Reserved_7
Unused bits

[19:16] wrlvl_pattern_now
Program the value to be driven onto dfi_lvl_pattern during training. The DMC ignores the value. For default DFI encodings see the DFI specification [5]. The supported range for this bitfield is 0-15.

[15] Reserved_6
Unused bits

[14] wrlvl_err_en_now
If enabled replay commands because of dfi_err during training.

[13] refresh_dur_wrlvl_now
Program to enable AUTOREFRESH commands to be generated during training operations. When enabled (1'b1), the DMC exits a training sequence to perform refresh.

[12] wrlvl_refresh_now
Program to enable or disable issue of an AUTOREFRESH command prior to performing write leveling training.

[11] Reserved_5
Unused bits

[10:9] Reserved_4
Unused bits

[8] Reserved_3
Unused bits

[7:5] Reserved_2
Unused bits

[4] wrlvl_setup_now
Program the command that sets up the DRAM for write leveling training.

[3:1] Reserved_1
Unused bits

[0] wrlvl_mode_now
Program the mode used for write leveling training.

3.3.304 wrlvl_mrs_now

This register determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write levelling. You enable this function with the wrlvl_control Register.

The wrlvl_mrs_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1324

Type Read-only

Reset 0x00000086

Width 32

The following figure shows the bit assignments.

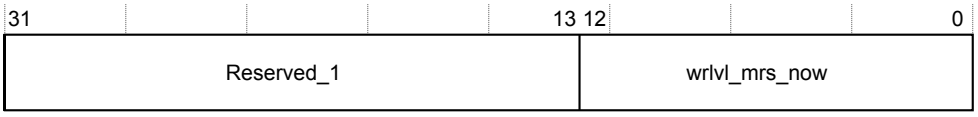

Figure 3-304 wrlvl_mrs_now register bit assignments

The following shows the bit assignments.

[31:13] Reserved_1

Unused bits

[12:0] wrlvl_mrs_now

Program the command the DMC uses to place the DRAM into training mode. Set address bits [12:0] for the Mode Register write to MR1.

3.3.305 t_wrlvl_en_now

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training.

The t_wrlvl_en_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1328

Type Read-only

Reset 0x00000000

Width 32

The following figure shows the bit assignments.

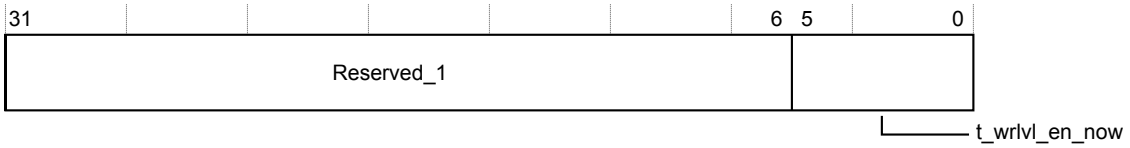

Figure 3-305 t_wrlvl_en_now register bit assignments

The following shows the bit assignments.

[31:6] Reserved_1
Unused bits

[5:0] t_wrlvl_en_now
t_wrlvl_en_now bitfield. The supported range for this bitfield is 1-63.

3.3.306 t_wrlvl_ww_now

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvl_resp.

The t_wrlvl_ww_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x132C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

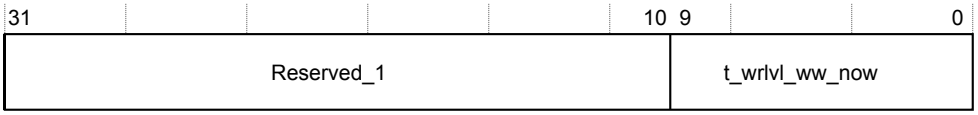

Figure 3-306 t_wrlvl_ww_now register bit assignments

The following shows the bit assignments.

[31:10] Reserved_1
Unused bits

[9:0] t_wrlvl_ww_now
t_wrlvl_ww_now bitfield. The supported range for this bitfield is 1-1023.

3.3.307 phy_power_control_now

Configures the low-power requests made to the PHY for the different channel states.

The phy_power_control_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1348
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

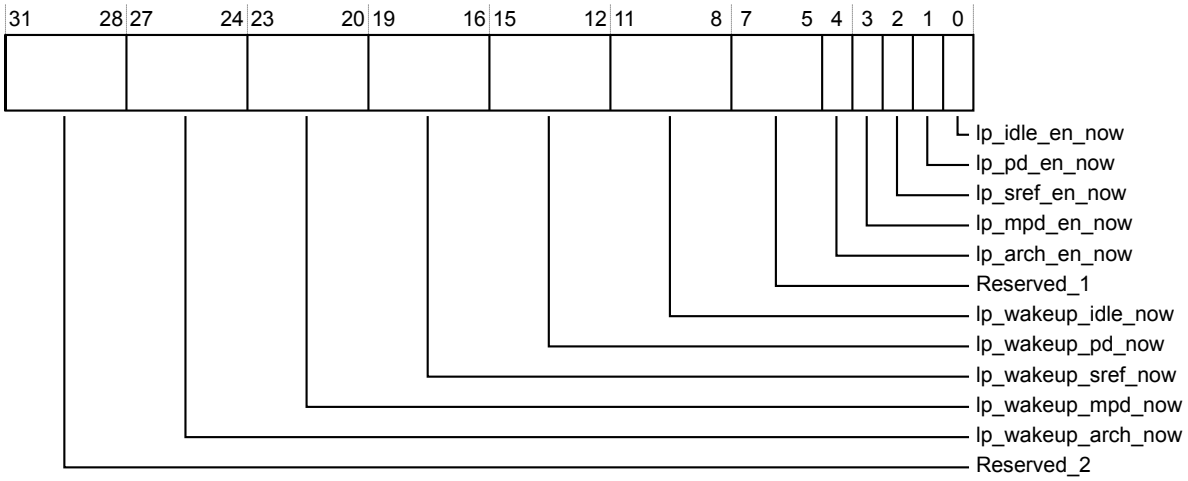

Figure 3-307 phy_power_control_now register bit assignments

The following shows the bit assignments.

[31:28] Reserved_2
Unused bits

[27:24] lp_wakeup_arch_now
Program the PHY wakeup encoding for PHY low-power requests when entering LOW-POWER architectural state. The supported range for this bitfield is 0-15.

[23:20] lp_wakeup_mpd_now
Program the PHY wakeup encoding for PHY low-power requests when in MPD. The supported range for this bitfield is 0-15.

[19:16] lp_wakeup_sref_now
Program the PHY wakeup encoding for PHY low-power requests when in self-refresh. The supported range for this bitfield is 0-15.

[15:12] lp_wakeup_pd_now
Program the PHY wakeup encoding for PHY low-power requests when powered down. The supported range for this bitfield is 0-15.

[11:8] lp_wakeup_idle_now
Program the PHY wakeup encoding for PHY low-power requests when idle. The supported range for this bitfield is 0-15.

[7:5] Reserved_1
Unused bits

[4] lp_arch_en_now
Program to enable or disable a PHY low-power request when entering LOW-POWER architectural state.

[3] lp_mpd_en_now
Program to enable or disable a PHY low-power request when in MPD.

[2] lp_sref_en_now
Program to enable or disable a PHY low-power request when in self-refresh.

[1] lp_pd_en_now
Program to enable or disable a PHY low-power request when in power down.

[0] lp_idle_en_now
Program to enable or disable a PHY low-power request when idle.

3.3.308 t_lpresp_now

Configures the minimum cycle delay to apply for PHY low-power handshakes.

The t_lpresp_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x134C`

Type Read-only

Reset `0x00000000`

Width 32

The following figure shows the bit assignments.

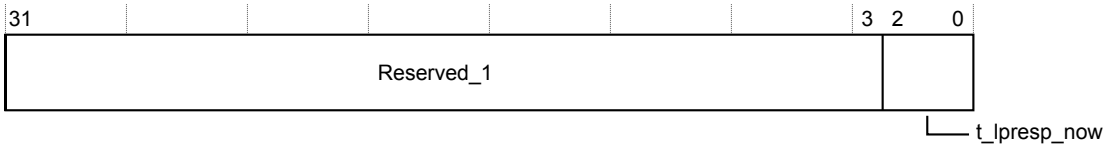

Figure 3-308 t_lpresp_now register bit assignments

The following shows the bit assignments.

[31:3] Reserved_1

Unused bits

[2:0] t_lpresp_now

The DMC waits a minimum t_lpresp cycles after asserting a PHY low power request before deasserting the request and resuming other commands. Zero means wait for dfi_lp_ack. The supported range for this bitfield is 0-7.

3.3.309 phy_update_control_now

Configures the update mechanism to use in response to PHY training requests.

The phy_update_control_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset `0x1350`

Type Read-only

Reset `0x0FE00000`

Width 32

The following figure shows the bit assignments.

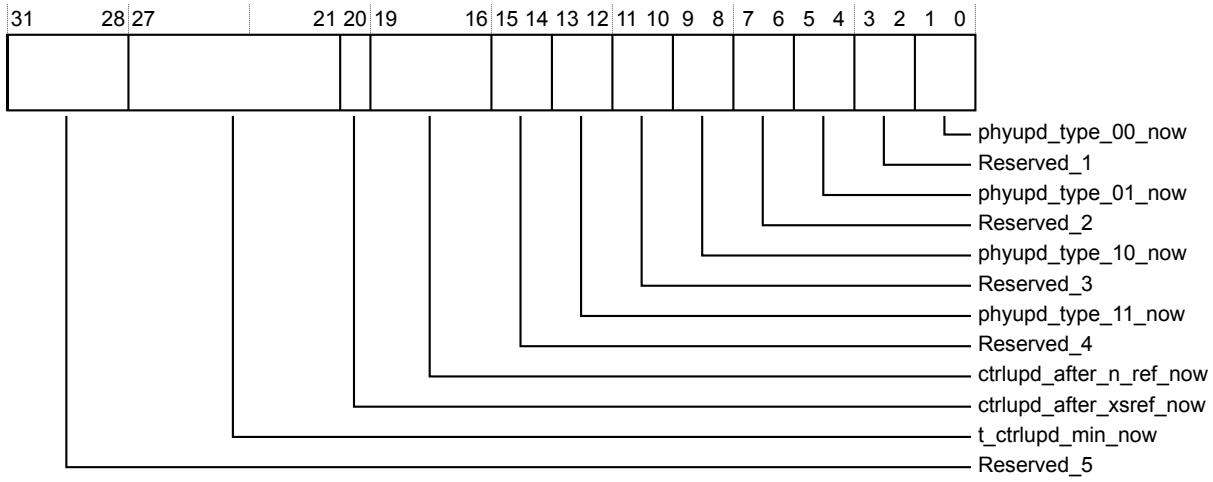

Figure 3-309 phy_update_control_now register bit assignments

The following shows the bit assignments.

[31:28] Reserved_5
Unused bits

[27:21] t_ctrlupd_min_now
Sets the number of cycles the DMC waits for acknowledgment of a cltrupd_req before deasserting the request and continuing normal operation. A value of 0x0 indicates the DMC must always wait for an acknowledgment before proceeding. The supported range for this bitfield is 0-127.

[20] ctrlupd_after_xsref_now
Program to enable an automatic DMC-initiated PHY update request after exiting self-refresh

[19:16] ctrlupd_after_n_ref_now
Program to enable an automatic DMC-initiated PHY update request after every n AUTOREFRESH commands. Zero disables the functionality. One is RESERVED

[15:14] Reserved_4
Unused bits

[13:12] phyupd_type_11_now
Program the required response to PHY update requsts of type 11.

[11:10] Reserved_3
Unused bits

[9:8] phyupd_type_10_now
Program the required response to PHY update requsts of type 10.

[7:6] Reserved_2
Unused bits

[5:4] phyupd_type_01_now
Program the required response to PHY update requsts of type 01.

[3:2] Reserved_1
Unused bits

[1:0] phyupd_type_00_now
Program the required response to PHY update requsts of type 00.

3.3.310 odt_timing_now

Configures the ODT on and off timing.

The odt_timing_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset	0x1358
Type	Read-only
Reset	0x06000600
Width	32

The following figure shows the bit assignments.

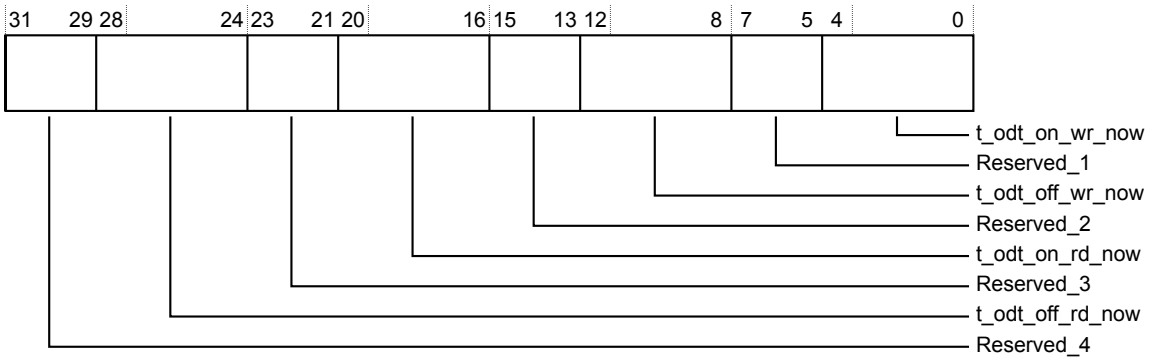

Figure 3-310 odt_timing_now register bit assignments

The following shows the bit assignments.

[31:29] Reserved_4

Unused bits

[28:24] t_odt_off_rd_now

Time from cs assertion to ODT being deasserted for read. The supported range for this bitfield is 2-31.

[23:21] Reserved_3

Unused bits

[20:16] t_odt_on_rd_now

Time from cs assertion to ODT being asserted for read. The supported range for this bitfield is 0-29.

[15:13] Reserved_2

Unused bits

[12:8] t_odt_off_wr_now

Time from cs assertion to ODT being deasserted for write. The supported range for this bitfield is 2-31.

[7:5] Reserved_1

Unused bits

[4:0] t_odt_on_wr_now

Time from cs assertion to ODT being asserted for write. The supported range for this bitfield is 0-29.

3.3.311 odt_wr_control_31_00_now

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_31_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1360

Type Read-only

Reset 0x08040201

Width 32

The following figure shows the bit assignments.

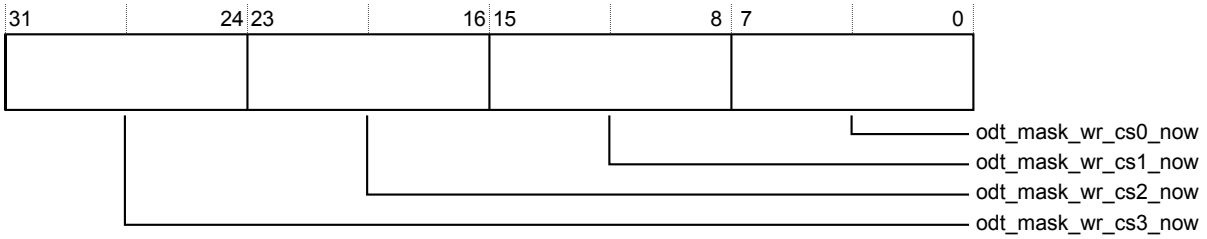

Figure 3-311 odt_wr_control_31_00_now register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_wr_cs3_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 3. The supported range for this bitfield is 0-255.

[23:16] odt_mask_wr_cs2_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 2. The supported range for this bitfield is 0-255.

[15:8] odt_mask_wr_cs1_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 1. The supported range for this bitfield is 0-255.

[7:0] odt_mask_wr_cs0_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 0. The supported range for this bitfield is 0-255.

3.3.312 odt_wr_control_63_32_now

Configures the ODT on and off settings for active and inactive ranks during writes.

The odt_wr_control_63_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1364

Type Read-only

Reset 0x80402010

Width 32

The following figure shows the bit assignments.

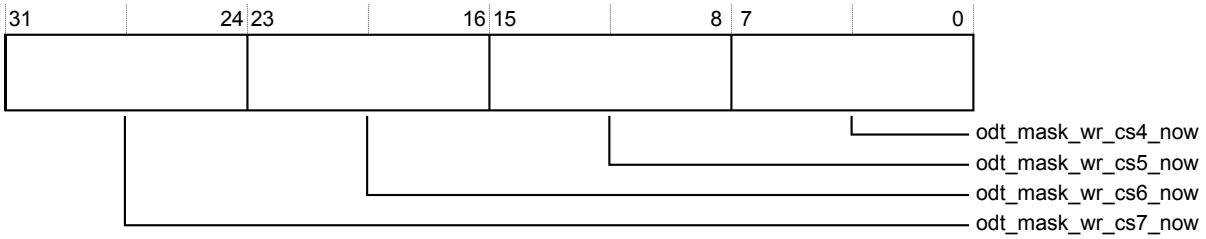

Figure 3-312 odt_wr_control_63_32_now register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_wr_cs7_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 7. The supported range for this bitfield is 0-255.

[23:16] odt_mask_wr_cs6_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 6. The supported range for this bitfield is 0-255.

[15:8] odt_mask_wr_cs5_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 5. The supported range for this bitfield is 0-255.

[7:0] odt_mask_wr_cs4_now
Drives the dfi_odt[7:0] output signal during a write to DRAM rank 4. The supported range for this bitfield is 0-255.

3.3.313 odt_rd_control_31_00_now

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_31_00_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1368`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

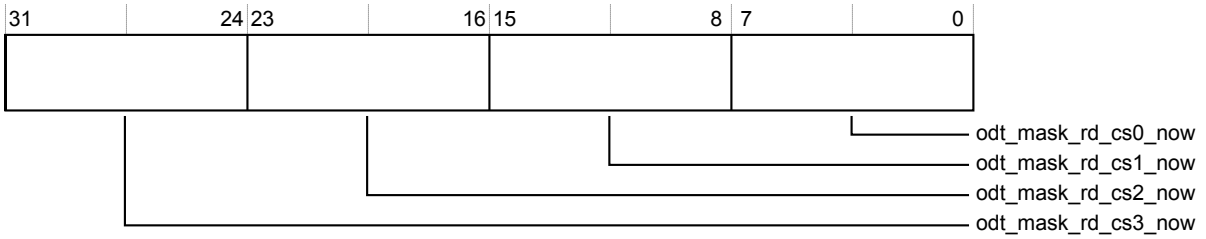

Figure 3-313 odt_rd_control_31_00_now register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_rd_cs3_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 3. The supported range for this bitfield is 0-255.

[23:16] odt_mask_rd_cs2_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 2. The supported range for this bitfield is 0-255.

[15:8] odt_mask_rd_cs1_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 1. The supported range for this bitfield is 0-255.

[7:0] odt_mask_rd_cs0_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 0. The supported range for this bitfield is 0-255.

3.3.314 odt_rd_control_63_32_now

Configures the ODT on and off settings for active and inactive ranks during reads.

The odt_rd_control_63_32_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x136C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

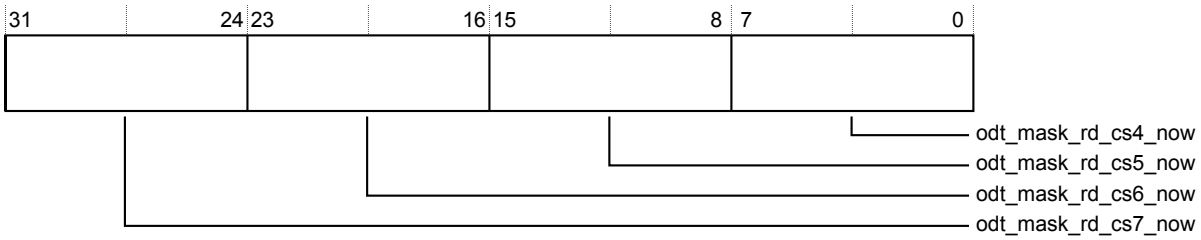

Figure 3-314 odt_rd_control_63_32_now register bit assignments

The following shows the bit assignments.

[31:24] odt_mask_rd_cs7_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 7. The supported range for this bitfield is 0-255.

[23:16] odt_mask_rd_cs6_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 6. The supported range for this bitfield is 0-255.

[15:8] odt_mask_rd_cs5_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 5. The supported range for this bitfield is 0-255.

[7:0] odt_mask_rd_cs4_now
Drives the dfi_odt[7:0] output signal during a read to DRAM rank 4. The supported range for this bitfield is 0-255.

3.3.315 dq_map_control_15_00_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_15_00_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0x1380`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

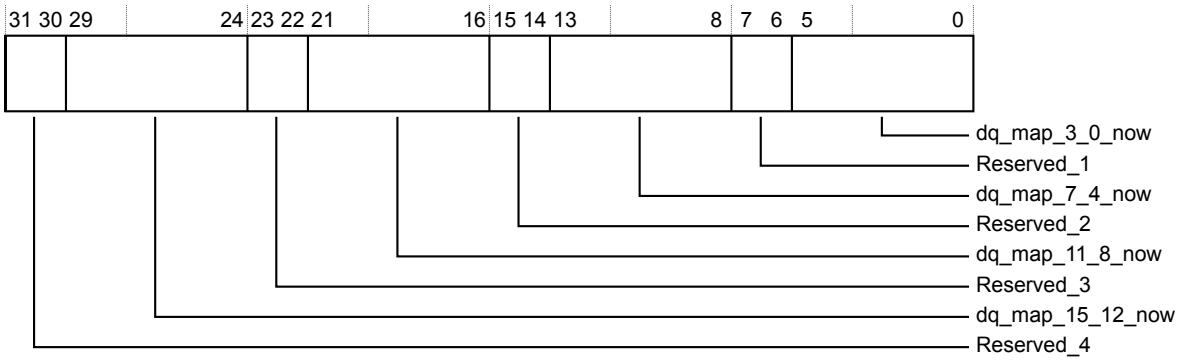

Figure 3-315 dq_map_control_15_00_now register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4

Unused bits

[29:24] dq_map_15_12_now

Controls DQ mapping for bits [15:12] of the DQ bus.

[23:22] Reserved_3

Unused bits

[21:16] dq_map_11_8_now

Controls DQ mapping for bits [11:8] of the DQ bus.

[15:14] Reserved_2

Unused bits

[13:8] dq_map_7_4_now

Controls DQ mapping for bits [7:4] of the DQ bus.

[7:6] Reserved_1

Unused bits

[5:0] dq_map_3_0_now

Controls DQ mapping for bits [3:0] of the DQ bus.

3.3.316 dq_map_control_31_16_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map

Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_31_16_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0x1384`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

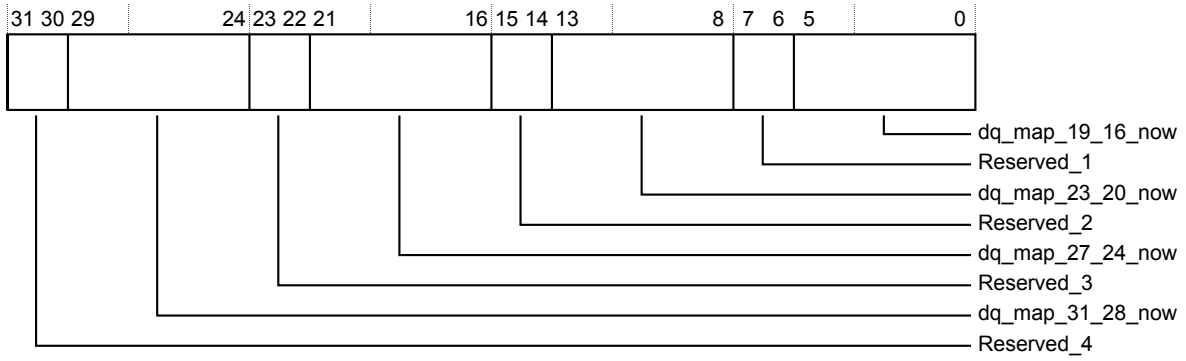

Figure 3-316 dq_map_control_31_16_now register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4

Unused bits

[29:24] dq_map_31_28_now

Controls DQ mapping for bits [31:28] of the DQ bus.

[23:22] Reserved_3

Unused bits

[21:16] dq_map_27_24_now

Controls DQ mapping for bits [27:24] of the DQ bus.

[15:14] Reserved_2

Unused bits

[13:8] dq_map_23_20_now

Controls DQ mapping for bits [23:20] of the DQ bus.

[7:6] Reserved_1

Unused bits

[5:0] dq_map_19_16_now

Controls DQ mapping for bits [19:16] of the DQ bus.

3.3.317 dq_map_control_47_32_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_47_32_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations

There is only one DMC configuration.

Attributes

Offset	`0x1388`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

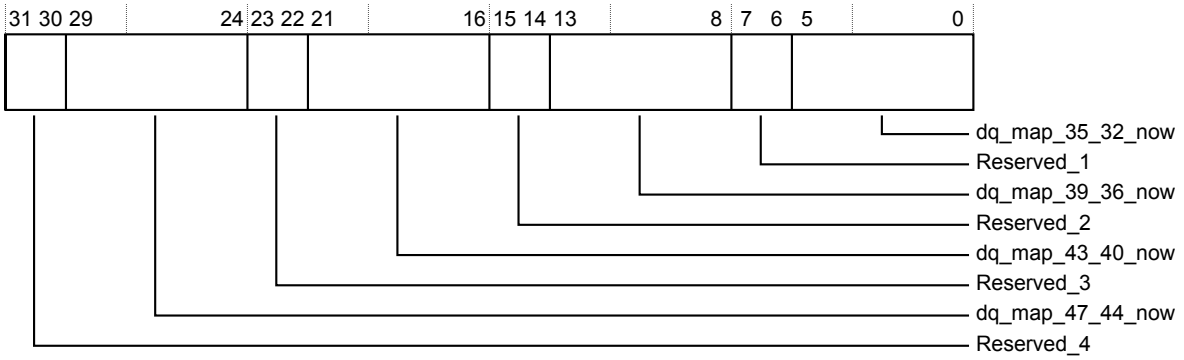

Figure 3-317 dq_map_control_47_32_now register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4

Unused bits

[29:24] dq_map_47_44_now

Controls DQ mapping for bits [47:44] of the DQ bus.

[23:22] Reserved_3

Unused bits

[21:16] dq_map_43_40_now

Controls DQ mapping for bits [43:40] of the DQ bus.

[15:14] Reserved_2

Unused bits

[13:8] dq_map_39_36_now

Controls DQ mapping for bits [39:36] of the DQ bus.

[7:6] Reserved_1

Unused bits

[5:0] dq_map_35_32_now

Controls DQ mapping for bits [35:32] of the DQ bus.

3.3.318 dq_map_control_63_48_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation.

The dq_map_control_63_48_now register characteristics are:

Usage constraints

Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x138C
Type	Read-only
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

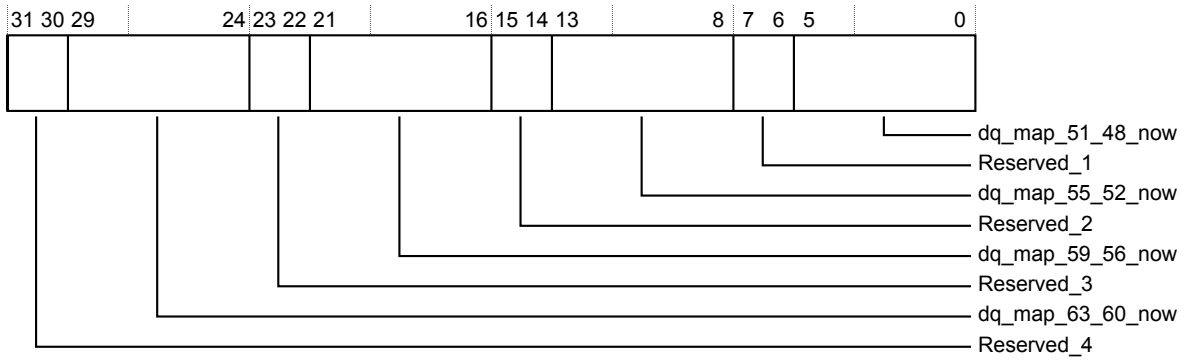

Figure 3-318 dq_map_control_63_48_now register bit assignments

The following shows the bit assignments.

[31:30] Reserved_4
Unused bits
[29:24] dq_map_63_60_now
Controls DQ mapping for bits [63:60] of the DQ bus.
[23:22] Reserved_3
Unused bits
[21:16] dq_map_59_56_now
Controls DQ mapping for bits [59:56] of the DQ bus.
[15:14] Reserved_2
Unused bits
[13:8] dq_map_55_52_now
Controls DQ mapping for bits [55:52] of the DQ bus.
[7:6] Reserved_1
Unused bits
[5:0] dq_map_51_48_now
Controls DQ mapping for bits [51:48] of the DQ bus.

3.3.319 dq_map_control_71_64_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation.

The dq_map_control_71_64_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1390
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

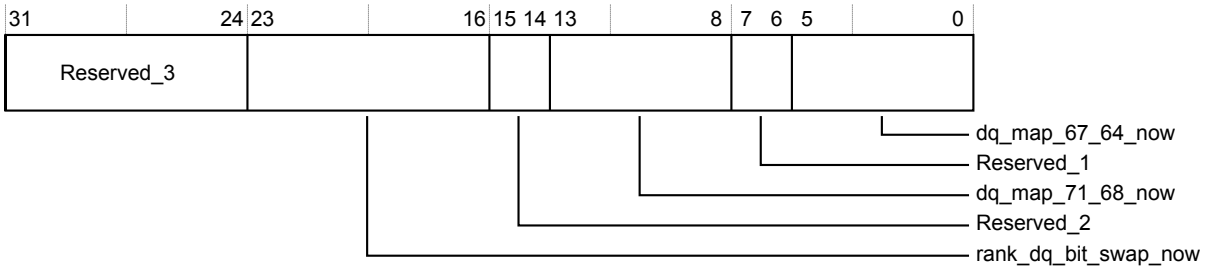

Figure 3-319 dq_map_control_71_64_now register bit assignments

The following shows the bit assignments.

[31:24] Reserved_3
Unused bits

[23:16] rank_dq_bit_swap_now
Each bit determines if the DQ bus has bit swapping as per the DDR4 RDIMM Design Specification applied to the corresponding rank. Normally, this bit must be set high for odd physical ranks.

[15:14] Reserved_2
Unused bits

[13:8] dq_map_71_68_now
Controls DQ mapping for bits [71:68] of the DQ bus. This corresponds to CB [7:4] on the DIMM.

[7:6] Reserved_1
Unused bits

[5:0] dq_map_67_64_now
Controls DQ mapping for bits [67:64] of the DQ bus. This corresponds to CB [3:0] on the DIMM.

3.3.320 user_config0_now

Drives the output user_config0 signal.

The user_config0_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1408
Type Read-only
Reset 0x00000000
Width 32

The following figure shows the bit assignments.

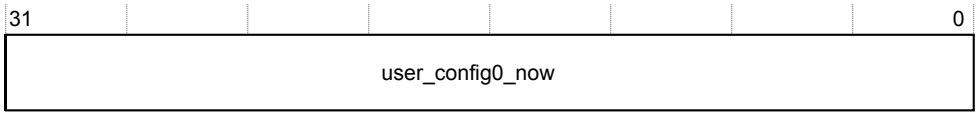

Figure 3-320 user_config0_now register bit assignments

The following shows the bit assignments.

[31:0] user_config0_now
user_config0_now bitfield.

3.3.321 user_config1_now

Drives the output user_config1 signal.

The user_config1_now register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x140C`
Type	Read-only
Reset	`0x00000000`
Width	32

The following figure shows the bit assignments.

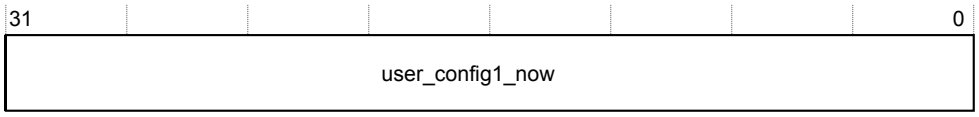

Figure 3-321 user_config1_now register bit assignments

The following shows the bit assignments.

[31:0] user_config1_now
user_config1_now bitfield.

3.3.322 periph_id_4

Peripheral ID register.

The periph_id_4 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FD0`
Type	Read-only
Reset	`0x00000014`
Width	32

The following figure shows the bit assignments.

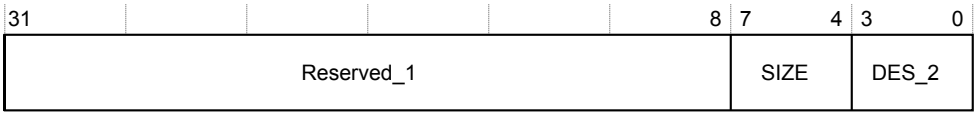

Figure 3-322 periph_id_4 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits
[7:4] SIZE
4KB Count
[3:0] DES_2
JEP continuation

3.3.323 periph_id_0

Peripheral ID register.

The periph_id_0 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1FE0`
Type	Read-only
Reset	`0x00000052`
Width	32

The following figure shows the bit assignments.

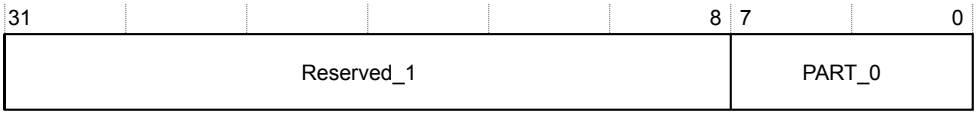

Figure 3-323 periph_id_0 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits
[7:0] PART_0
Part Number [7:0]

3.3.324 periph_id_1

Peripheral ID register.

The periph_id_1 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1FE4`
Type	Read-only

Reset 0x000000B4

Width 32

The following figure shows the bit assignments.

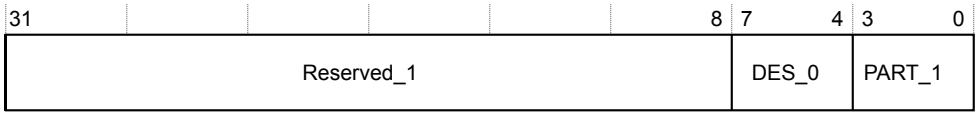

Figure 3-324 periph_id_1 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:4] DES_0
JEP106 Identity code [3:0]

[3:0] PART_1
Part Number [11:8]

3.3.325 periph_id_2

Peripheral ID register.

The periph_id_2 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1FE8

Type Read-only

Reset 0x0000000B

Width 32

The following figure shows the bit assignments.

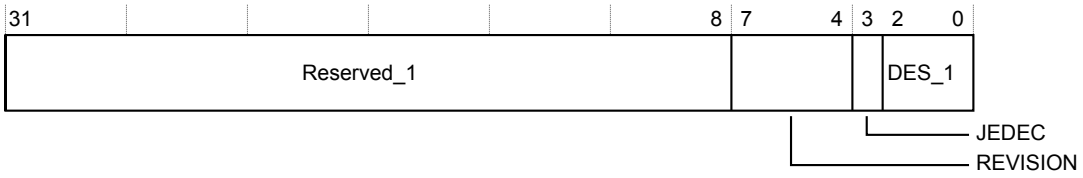

Figure 3-325 periph_id_2 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:4] REVISION
Revision

[3] JEDEC
JEDEC JEP106 Code Is Used

[2:0] DES_1
JEP106 Identity code [6:4]

3.3.326 periph_id_3

Peripheral ID register.

The periph_id_3 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1FEC
Type	Read-only
Reset	0x00000000
Width	32

The following figure shows the bit assignments.

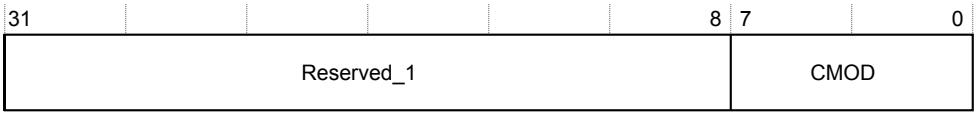

Figure 3-326 periph_id_3 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:0] CMOD
Customer modified number.

3.3.327 component_id_0

Component ID register.

The component_id_0 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	0x1FF0
Type	Read-only
Reset	0x0000000D
Width	32

The following figure shows the bit assignments.

Figure 3-327 component_id_0 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:0] PRMBL_0
Component ID

3.3.328 component_id_1

Component ID register.

The component_id_1 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FF4`
Type	Read-only
Reset	`0x000000F0`
Width	32

The following figure shows the bit assignments.

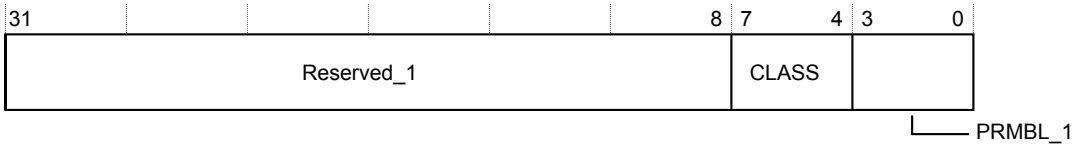

Figure 3-328 component_id_1 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits

[7:4] CLASS
Component ID

[3:0] PRMBL_1
Component ID

3.3.329 component_id_2

Component ID register.

The component_id_2 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.

Configurations
There is only one DMC configuration.

Attributes

Offset	`0x1FF8`
Type	Read-only
Reset	`0x00000005`
Width	32

The following figure shows the bit assignments.

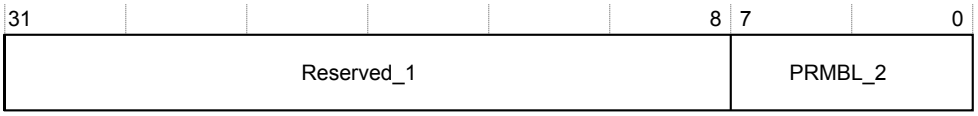

Figure 3-329 component_id_2 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits
[7:0] PRMBL_2
Component ID

3.3.330 component_id_3

Component ID register.

The component_id_3 register characteristics are:

Usage constraints
Can be read from when in ALL states. Cannot be changed.
Configurations
There is only one DMC configuration.
Attributes

Offset	`0x1FFC`
Type	Read-only
Reset	`0x000000B1`
Width	32

The following figure shows the bit assignments.

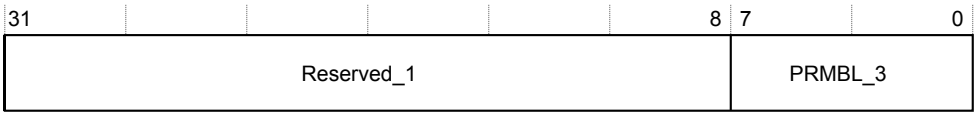

Figure 3-330 component_id_3 register bit assignments

The following shows the bit assignments.

[31:8] Reserved_1
Unused bits
[7:0] PRMBL_3
Component ID

Appendix A
Signal Descriptions

This appendix describes the DMC-520 signals.
It contains the following sections:

A.1 Signals list

DMC signals list that excludes bus interface signals. The bus interface signals are defined by their own bus protocol standard.

The following table shows the Primary clock and reset signals list of the DMC.

Table A-1 DMC Primary clock and reset signals list

Signal	Type	Width	Description
clk	Input	1	Primary DMC clock
resetn	Input	1	Primary DMC reset

The following table shows the APB clock and reset signals list of the DMC.

Table A-2 DMC APB clock and reset signals list

Signal	Type	Width	Description
pclk	Input	1	APB clock
presetn	Input	1	APB reset

The following table shows the User I/O with APB access list of the DMC.

Table A-3 DMC User I/O with APB access list

Signal	Type	Width	Description
user_status	Input	32	User defined inputs
user_config0	Output	32	User defined outputs
user_config1	Output	32	User defined outputs
user_config2	Output	32	User defined outputs
user_config3	Output	32	User defined outputs
user_periph_id_3	Input	8	Tie-off value to set the value of CMOD in the periph_id_3 bitfield. This input is exclusive ORed with the default register value.

The following table shows the Events list of the DMC.

Table A-4 DMC Events list

Signal	Type	Width	Description
scrub_event_in0	Input	1	Scrub event 0 trigger.
scrub_event_in1	Input	1	Scrub event 1 trigger.
scrub_event_in2	Input	1	Scrub event 2 trigger.
scrub_event_in3	Input	1	Scrub event 3 trigger.
scrub_event_in4	Input	1	Scrub event 4 trigger.
scrub_event_in5	Input	1	Scrub event 5 trigger.
scrub_event_in6	Input	1	Scrub event 6 trigger.

Table A-4 DMC Events list (continued)

Signal	Type	Width	Description
scrub_event_in7	Input	1	Scrub event 7 trigger.
scrub_event_out0	Output	1	Scrub event 0 triggered.
scrub_event_out1	Output	1	Scrub event 1 triggered.
scrub_event_out2	Output	1	Scrub event 2 triggered.
scrub_event_out3	Output	1	Scrub event 3 triggered.
scrub_event_out4	Output	1	Scrub event 4 triggered.
scrub_event_out5	Output	1	Scrub event 5 triggered.
scrub_event_out6	Output	1	Scrub event 6 triggered.
scrub_event_out7	Output	1	Scrub event 7 triggered.
direct_cmd_event_in0	Input	1	Direct cmd event 0 trigger.
direct_cmd_event_in1	Input	1	Direct cmd event 1 trigger.
direct_cmd_event_in2	Input	1	Direct cmd event 2 trigger.
direct_cmd_event_in3	Input	1	Direct cmd event 3 trigger.
direct_cmd_event_out0	Output	1	Direct cmd event 0 triggered.
direct_cmd_event_out1	Output	1	Direct cmd event 1 triggered.
direct_cmd_event_out2	Output	1	Direct cmd event 2 triggered.
direct_cmd_event_out3	Output	1	Direct cmd event 3 triggered.

The following table shows the Scan Signals list of the DMC.

Table A-5 DMC Scan Signals list

Signal	Type	Width	Description
dftse	Input	1	DFT scan enable
dftclkcgen	Input	1	DFT clk clock gate enable
dftclkdiv2cgen	Input	1	DFT clkdiv2 clock gate enable
dftpclkcgen	Input	1	DFT pclk clock gate enable
dftrstdisable	Input	1	DFT reset synchronizer disable
dftramhold	Input	1	DFT on-chip RAM hold
dftmcphold	Input	1	DFT multi-cycle path hold

The following table shows the PMU Signals list of the DMC.

Table A-6 DMC PMU Signals list

Signal	Type	Width	Description
ev_request_valid_valid	Output	1	Indicates that ev_request_valid_payload is valid
ev_request_tzfail_valid	Output	1	Indicates that ev_request_tzfail_payload is valid
ev_request_retry_valid	Output	1	Indicates that ev_request_retry_payload is valid
ev_retry_grant_valid	Output	1	Indicates that ev_retry_grant_payload is valid
ev_request_valid_payload	Output	27	A request enters the DMC
ev_request_tzfail_payload	Output	22	A request fails an address translation or TrustZone permissions check
ev_request_retry_payload	Output	25	A request is retried
ev_retry_grant_payload	Output	15	Indicates that a P-credit has been granted.
ev_queue_fill_status_payload	Output	8	Count of entries in the DMC
ev_queued_reads_payload	Output	8	Count of read entries in the DMC
ev_queued_writes_payload	Output	8	Count of write entries in the DMC
ev_enqueued_reads_payload	Output	8	Count of read entries in the queue
ev_enqueued_writes_payload	Output	8	Count of write entries in the queue
ev_arbitrated_reads_payload	Output	8	Count of read entries in the arbitrated, without data state
ev_arbitrated_writes_payload	Output	8	Count of write entries in the arbitrated, not clean state
ev_read_backlog_payload	Output	8	Count of read entries in the backlog queue
ev_enqueue_backlog_payload	Output	8	Count of entries that are waiting to get enqueued
ev_hazard_resolution_backlog_payload	Output	8	Count of entries that are ready to be merged
ev_queue_allocation_backlog_payload	Output	8	Count of entries that in allocation backlog
ev_enqueue_valid	Output	1	Indicates that ev_enqueue_payload is valid
ev_arbitrate_valid	Output	1	Indicates that ev_arbitrate_payload is valid
ev_rank_targetted_valid	Output	RANKS_PER_CHANNEL	A rank is targeted by an enqueued entry
ev_enqueue_payload	Output	34	A request is enqueued in the arbitration queue
ev_arbitrate_payload	Output	12	A request is arbitrated from the arbitration queue
ev_allocate_valid	Output	1	Indicates that ev_allocate_payload is valid
ev_allocate_payload	Output	22	Maps sysid to allocated tag ID on entry to the DCB
ev_request_hazard_valid	Output	1	Indicates that ev_request_hazard_payload is valid

Table A-6 DMC PMU Signals list (continued)

Signal	Type	Width	Description
ev_request_hazard_payload	Output	2	A request forms a data hazard on an existing entry
ev_request_partial_valid	Output	1	A request is partial (not a complete burst)
ev_request_rmw_valid	Output	1	A request requires a read-modify-write
ev_ram_err_detect_valid	Output	9	Indicates that ev_ram_err_detect_payload is valid
ev_ram_err_detect_payload	Output	42	See ram_ecc_errd_int description
ev_ram_err_correct_valid	Output	9	Indicates that ev_ram_err_correct_payload is valid
ev_ram_err_correct_payload	Output	42	See ram_ecc_errc_int description
ev_dram_err_detect_valid	Output	1	Indicates that ev_dram_err_detect_payload is valid
ev_dram_err_detect_payload	Output	35	See dram_ecc_errd_int description
ev_dram_err_correct_valid	Output	1	Indicates that ev_dram_err_correct_payload is valid
ev_dram_err_correct_payload	Output	59	See dram_ecc_errc_int description
ev_turnaround_valid	Output	1	Indicates that ev_rank_turnaround_payload is valid
ev_activate_valid	Output	1	Indicates that ev_activate_payload is valid
ev_rdwr_valid	Output	1	Indicates that ev_rdwr_payload is valid
ev_precharge_valid	Output	1	Indicates that ev_precharge_payload is valid
ev_refresh_valid	Output	1	Indicates that ev_refresh_payload is valid
ev_turnaround_payload	Output	9	A turnaround has occurred
ev_activate_payload	Output	29	An ACTIVATE command has been sent
ev_rdwr_payload	Output	15	A READ/WRITE command has been sent
ev_precharge_payload	Output	9	A PRECHARGE command has been sent
ev_refresh_payload	Output	3	A REFRESH command has been sent
ev_pwr_state_active_valid	Output	`MEMORY_CHIP_SELECTS`	The rank is active
ev_pwr_state_idle_valid	Output	`MEMORY_CHIP_SELECTS`	The rank is idle
ev_pwr_state_pd_valid	Output	`MEMORY_CHIP_SELECTS`	The rank is in a POWER DOWN state
ev_pwr_state_sref_valid	Output	`MEMORY_CHIP_SELECTS`	The rank is in a SELF_REFRESH state
ev_bank_active_valid	Output	`BANKS_PER_CHANNEL`	A bank is active (has a row open)
ev_bank_busy_valid	Output	`BANKS_PER_CHANNEL`	A bank is busy (one or more timing parameters is being measured following an access)
ev_phy_update_req_valid	Output	1	Indicates that ev_phy_update_req_payload is valid

Table A-6 DMC PMU Signals list (continued)

Signal	Type	Width	Description
ev_phy_update_valid	Output	1	Indicates that ev_phy_update_payload is valid
ev_phy_update_req_payload	Output	4	A PHY update request has been received (update or training)
ev_phy_update_payload	Output	4	A PHY update request is in progress (update or training)
ev_phy_update_complete_valid	Output	1	A PHY update request has been completed (update or training)
ev_link_err_valid	Output	1	A link error has been detected
ev_tmac_limit_reached_valid	Output	1	Indicates that a bank row has reached the tMAC threshold for triggering a Target Row Refresh
ev_tmaw_tracker_full_valid	Output	1	Indicates that tMAC/tMAW tracking resource is full

The following table shows the Misc. signals list of the DMC.

Table A-7 DMC Misc. signals list

Signal	Type	Width	Description
memory_type	Output	3	An external output of the value of the memory_type register bitfield.
abort_req	Input	1	An input to abort retries in the face of DFI link errors.
abort_ack	Output	1	An output to acknowledge that the DMC has completed outstanding transactions as a result of an abort.

The following table shows the Tie-off signals list of the DMC.

Table A-8 DMC Tie-off signals list

Signal	Type	Width	Description
t_rddata_en_diff_tie_off	Input	6	Tie-off value for reset of register bitfield t_rddata_en_diff
t_phyrdcslat_tie_off	Input	5	Tie-off value for reset of register bitfield t_phyrdcslat
t_phyrdlat_tie_off	Input	6	Tie-off value for reset of register bitfield t_phyrdlat
t_phywrlat_diff_tie_off	Input	5	Tie-off value for reset of register bitfield t_phywrlat_diff
t_phywrcslat_tie_off	Input	5	Tie-off value for reset of register bitfield t_phywrcslat
t_phywrdata_tie_off	Input	1	Tie-off value for reset of register bitfield t_phywrdata
refresh_dur_rdlvl_tie_off	Input	1	Tie-off value for reset of register bitfield refresh_dur_rdlvl
t_rdlvl_en_tie_off	Input	6	Tie-off value for reset of register bitfield t_rdlvl_en
t_rdlvl_rr_tie_off	Input	10	Tie-off value for reset of register bitfield t_rdlvl_rr
refresh_dur_wrlvl_tie_off	Input	1	Tie-off value for reset of register bitfield refresh_dur_wrlvl
t_wrlvl_en_tie_off	Input	6	Tie-off value for reset of register bitfield t_wrlvl_en

Table A-8 DMC Tie-off signals list (continued)

Signal	Type	Width	Description
t_wrlvl_ww_tie_off	Input	10	Tie-off value for reset of register bitfield t_wrlvl_ww
t_lpresp_tie_off	Input	3	Tie-off value for reset of register bitfield t_lpresp
user_config0_tie_off	Input	32	Tie-off value for reset of register bitfield user_config0
user_config1_tie_off	Input	32	Tie-off value for reset of register bitfield user_config1
user_config2_tie_off	Input	32	Tie-off value for reset of register bitfield user_config2
user_config3_tie_off	Input	32	Tie-off value for reset of register bitfield user_config3

The following table shows the Tie-off values for AMBA5 CHI list of the DMC.

Table A-9 DMC Tie-off values for AMBA5 CHI list

Signal	Type	Width	Description
system_id	Input	SKY_RSP_FLIT_SRCID_WIDTHparmname>	Tie-off value to set the physical node ID of the DMC
home_node_id	Input	(SKY_REQ_FLIT_SRCID_WIDTH*SYSTEM_REQUESTORS)parmname>	Tie off value to specify the concatenated physical node IDs of up to 8 Home Nodes that are permitted to access the DMC

The following table shows the DFI Interface bus list of the DMC.

Table A-10 DMC DFI Interface list

Name	Width	Description
dfi_address	18	Address to DDR3 PHY
dfi_bank	3	Bank Address to PHY
dfi_ras_n	1	Row address strobe to PHY
dfi_cas_n	1	Column address strobe to PHY
dfi_we_n	1	Write enable to PHY
dfi_cs_n	MEMORY_CHIP_SELECTS	Chip-select to PHY
dfi_act_n	1	Activate to PHY
dfi_bg	2	Bank group address to PHY
dfi_cid	3	Chip ID to PHY
dfi_cke	MEMORY_CHIP_SELECTS	Clock enable to PHY
dfi_odt	MEMORY_CHIP_SELECTS	On Die Termination to PHY
dfi_reset_n	MEMORY_CHIP_SELECTS	Reset to PHY
dfi_parity_in	1	Command parity to PHY
dfi_wrdata_en	(DMC_DATA_BYTES + DMC_ECC_BYTES)	Write data enable PHY

Table A-10 DMC DFI Interface list (continued)

Name	Width	Description
dfi_wrdata	(DMC_DATA_BITS + DMC_ECC_BITS)	Write data to PHY
dfi_wrdata_cs_n	MEMORY_CHIP_SELECTS	Write Data Path Chip-select to PHY
dfi_wrdata_mask	(DMC_DATA_BYTES + DMC_ECC_BYTES)	Write data mask PHY
dfi_rddata_en	(DMC_DATA_BYTES + DMC_ECC_BYTES)	Enable for read data
dfi_rddata	(DMC_DATA_BITS + DMC_ECC_BITS)	Read data input from PHY
dfi_rddata_dbi_n	(DMC_DATA_BYTES + DMC_ECC_BYTES) * 2	Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal must be tied to 'b1.
dfi_rddata_valid	(DMC_DATA_BYTES + DMC_ECC_BYTES)	Indicates read data valid
dfi_rddata_cs_n	MEMORY_CHIP_SELECTS	Read Data Path Chip-select to PHY
dfi_ctrlupd_req	1	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_ctrlupd_ack	1	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_phyupd_req	1	DFI PHY-initiated update request
dfi_phyupd_ack	1	DFI PHY-initiated update acknowledge
dfi_phyupd_type	2	DFI PHY-initiated update type
dfi_phy_crc_mode	1	Sends CRC data as part of the data burst. 'b0 = CRC code generation and validation performed in the MC. 'b1 = CRC code generation and validation performed in the PHY.
dfi_data_byte_disable	(DMC_DATA_BYTES + DMC_ECC_BYTES)	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_dram_clk_disable	MEMORY_CHIP_SELECTS	DRAM clock disable to PHY
dfi_init_start	1	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_init_complete	1	Indicates PHY initialization complete
dfi_alert_n	1	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_err	1	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_err_info	4	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_phylvl_req_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.1, see JEDEC specification for more information.
dfi_phylvl_ack_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.1, see JEDEC specification for more information.

Table A-10 DMC DFI Interface list (continued)

Name	Width	Description
dfi_rdlvl_req	1	DFI read data eye training request
dfi_rdlvl_cs_n	MEMORY_CHIP_SELECTS	DFI read data eye training request target chip-select
dfi_rdlvl_periodic	1	DFI read data eye training request periodic
dfi_rdlvl_en	1	DFI read data eye training enable
dfi_rdlvl_resp	1	DFI read data eye training response
dfi_rdlvl_gate_req	1	DFI read gate training request
dfi_rdlvl_gate_cs_n	MEMORY_CHIP_SELECTS	DFI read gate training request target chip-select
dfi_rdlvl_gate_periodic	1	DFI read gate training request periodic
dfi_rdlvl_gate_en	1	DFI read gate training enable
dfi_rdlvl_gate_resp	1	DFI read gate training response
dfi_wrlvl_req	1	DFI write leveling training request
dfi_wrlvl_cs_n	MEMORY_CHIP_SELECTS	DFI write leveling training request target chip-select
dfi_wrlvl_periodic	1	DFI write leveling training request periodic
dfi_wrlvl_en	1	DFI write leveling training enable
dfi_wrlvl_strobe	1	DFI write leveling training strobe
dfi_wrlvl_resp	1	DFI write leveling training response
dfi_lvl_pattern	4	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_lvl_periodic	1	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_lvl_cs_n	MEMORY_CHIP_SELECTS	This signal is part of DFI 3.0, see JEDEC specification for more information.
dfi_ref_en	1	DFI refresh during training enable
dfi_lp_ctrl_req	1	DFI command low power request
dfi_lp_data_req	1	DFI data low power request
dfi_lp_wakeup	4	DFI command low power PHY wakeup allowance
dfi_lp_ack	1	DFI command low power acknowledge

The following table shows the Q-Channel Interface for DMC bus list of the DMC.

Table A-11 DMC Q-Channel Interface for DMC list

Name	Width	Description
qreqn	1	Request from the external clock controller to prepare to stop the clock
qacceptn	1	Positive acknowledgment after receiving QREQn assertion indicating that the DMC has completed preparation to stop the clocks and that the external clock controller can stop the clock

Table A-11 DMC Q-Channel Interface for DMC list (continued)

Name	Width	Description
qdeny	1	Negative acknowledgment after receiving QREQn assertion indicating that the DMC has refused the request from the external clock controller to prepare to stop the clock
qactive	1	Indication that the DMC is active

The following table shows the Q-Channel Interface for APB interface bus list of the DMC.

Table A-12 DMC Q-Channel Interface for APB interface list

Name	Width	Description
qreqn_apb	1	Request from the external clock controller to prepare to stop the clock
qacceptn_apb	1	Positive acknowledgment after receiving QREQn assertion indicating that the APB interface has completed preparation to stop the clocks and that the external clock controller can stop the clock
qdeny_apb	1	Negative acknowledgment after receiving QREQn assertion indicating that the APB interface has refused the request from the external clock controller to prepare to stop the clock
qactive_apb	1	Indication that the APB interface is active

The following table shows the Clock Frequency Change Interface bus list of the DMC.

Table A-13 DMC Clock Frequency Change Interface list

Name	Width	Description
cc_frequency	5	Used to indicate new frequency as part of frequency change protocol
cc_freq_change_req	1	Signals to an external clock control that the clock frequency can be updated
cc_freq_change_ack	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Clock Frequency Change Interface bus list of the DMC.

Table A-14 DMC Clock Frequency Change Interface list

Name	Width	Description
dfi_frequency	5	Used to indicate new frequency as part of frequency change protocol
dfi_freq_change_req	1	Signals to an external clock control that the clock frequency can be updated
dfi_freq_change_ack	1	Signals to the DMC from an external clock control that the clock frequency has been updated

The following table shows the Memory BIST interface bus list of the DMC.

Table A-15 DMC Memory BIST interface list

Name	Width	Description
mbistresetn	1	MBIST reset. Active low.
mbistreq	1	MBIST request
mbistack	1	MBIST acknowledge

Table A-15 DMC Memory BIST interface list (continued)

Name	Width	Description
mbistwriteen	1	MBIST write enable
mbistreaden	1	MBIST read enable
mbistaddr	7	MBIST address
mbistarray	5	MBIST array selection
mbistindata	154	MBIST write data
mbistoutdata	154	MBIST read data

The following table shows the interrupt signal list of the DMC. All the signals are outputs from the DMC.

Table A-16 DMC interrupt list

Name	Width	Description
ram_ecc_errc_int	1	The DMC has detected a correctable error in an internal RAM
ram_ecc_errd_int	1	The DMC has detected an un-correctable error in an internal RAM
dram_ecc_errc_int	1	The DMC has detected a correctable error in a DRAM burst
dram_ecc_errd_int	1	The DMC has detected a data failure that could not be corrected in a DRAM burst operation
failed_access_int	1	The DMC has detected a system request that has failed a permissions check
failed_prog_int	1	The DMC has detected a programming request that is not permitted
link_err_int	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun
temperature_event_int	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor
arch_fsm_int	1	The DMC has detected a change in the architectural state
phy_request_int	1	The DMC has detected a PHY request
combined_int	1	A combined interrupt that is the logical OR of the other interrupts
ram_ecc_errc_oflow	1	The DMC has detected a correctable error in an internal RAM and a previously detected assertion was not cleared
ram_ecc_errd_oflow	1	The DMC has detected a un-correctable error in an internal RAM and a previously detected assertion was not cleared
dram_ecc_errc_oflow	1	The DMC has detected a correctable error in a DRAM burst and a previously detected assertion was not cleared
dram_ecc_errd_oflow	1	The DMC has detected a data failure that could not be corrected in a DRAM burst operation and a previously detected assertion was not cleared
failed_access_oflow	1	The DMC has detected a system request that has failed a permissions check and a previously detected assertion was not cleared
failed_prog_oflow	1	The DMC has detected a programming request that is not permitted and a previously detected assertion was not cleared

Table A-16 DMC interrupt list (continued)

Name	Width	Description
link_err_oflow	1	The DRAM interface has suffered from a link failure and a recovery attempt has begun and a previously detected assertion was not cleared
temperature_event_oflow	1	The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor and a previously detected assertion was not cleared
arch_fsm_oflow	1	The DMC has detected a change in the architectural state and a previously detected assertion was not cleared
phy_request_oflow	1	The DMC has detected a PHY request and a previously detected assertion was not cleared
combined_oflow	1	A combined interrupt that is the logical OR of the other interrupt overflows

Appendix B
Revisions

This appendix describes the technical changes between released issues of this book. It contains the following sections:

B.1 Revisions

This appendix describes the technical changes between released issues of this book.

Table B-1 Issue 00

Change	Location	Affects
First release	-	-