ARM PrimeCell
Vectored Interrupt Controller (PL190)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r2p0 of PL190 VIC -Perpetual

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General suggestion for additions and improvements are also welcome.

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INTRODUCTION

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Change Control

31 Oct 2008: Changes in Document v3

Page	Status	ID	Cat	Summary
8	New	606317	Doc	Incorrect procedure and example code in TRM for servicing daisy chained interrupts

14 Dec 2004: Changes in Document v2

Page	Status	ID	Cat	Summary
12	New	120265	Cat 3	Sensitivity list issue in VicPriority.v
13	New	318670	Cat 3	Daisychain results in transient vectors for asynchronous interrupts

ERRATA SUMMARY TABLE

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r1p2-00rel0	r1p2-00rel0
120265	Cat 3	Sensitivity list issue in VicPriority.v	X	
318670	Cat 3	Daisychain results in transient vectors for asynchronous interrupts	X	
606317	Doc	Incorrect procedure and example code in TRM for servicing daisy chained interrupts		X

ERRATA - DOCUMENTATION

606317: Incorrect procedure and example code in TRM for servicing daisy chained interrupts

Status

Affects: product PL190 VIC -Perpetual.

Fault status: Doc, Present in: r1p2-00rel0, Open.

Description

There should be a new section 2.2.3 in the TRM (ARM-DDI-0181E) titled 'Daisy-chained interrupt flow sequence' to provide information about the operation of VICs that are daisy chained.

There are two daisy-chained VICs in the example case given below. VIC0 is directly connected to the CPU and VIC1 is connected to VIC0.

1. An interrupt occurs.

2. The ARM processor branches to either the IRQ or FIQ interrupt vector.

3. If the interrupt is an IRQ, read the VICVectAddr Register in VIC0 and branch to the interrupt service routine. You can do this using an LDR PC instruction. Reading the VICVectorAddr Register updates the interrupt controllers hardware priority register.

4. Stack the workspace

5. Read the VICVectAddr register in daisy chained interrupt controller VIC1. Reading the VICVectorAddr Register updates the interrupt controllers hardware priority register in the daisy chained interrupt controller. Branch to the interrupt service routine address given by VICVectorAddr for VIC1 plus offset to skip the interrupt stacking preamble. You can do this using an LDR PC instruction.

6. Enable the IRQ interrupts so that a higher priority can be serviced.

7. Execute the Interrupt Service Routine (ISR).

8. Clear the requesting interrupt in the peripheral, or write to the VICSoftIntClear Register if the request was generated by a software interrupt.

9. Disable the interrupts and restore the workspace.

10. Write to the daisy chained VICVectAddr Register VIC1. This clears the respective interrupt in the daisy chained interrupt controller.

11. Write to the VICVectAddr Register in VIC0. This clears the respective interrupt in the internal interrupt priority hardware.

12. Return from the interrupt. This re-enables the interrupts.

Moreover, the code in the TRM section "B.1.12. Daisy-chained vectored interrupt service routine" is incomplete and should include the code snippet specified in the workaround.

Implications

For daisy-chained interrupts, if only the VAR from one VIC is read, it does not update the hardware priority in the other VIC. This means the daisy chained interrupt controller doesn't realise the interrupt is being serviced and keeps the interrupt request active.

For daisy-chained interrupts the processor must read the VAR register from both interrupt controllers and branch to the addresses provided. However the address provided by reading the daisy-chained VAR register must be manipulated to skip the interrupt preamble. If two daisy chained interrupts occur soon after each other and the daisy chained VAR register address isn't branched to, the interrupt controller priority logic may be updated incorrectly. This may cause a low priority interrupt to be missed.

Hence, the erratum implication can be severe if the entire sequence for servicing daisy-chained interrupts is not followed.

Workaround

For already existing software that services daisy-chained nested interrupts, a possible software work around would be to branch to the address provided by the VIC1 VAR register. This ensures that the correct ISR is serviced.

```
0x18 LDR pc, [VIC0_VAR]          ; VIC0 VAR read


daisy_chained_vector_handler:
        STMFD r13!, {r12-r14}
        LDR r12, [VIC1_VAR]      ; Read VIC1 VAR and update PC,
                                 ; VIC1 priority hardware is updated
        LDR PC, [r12, #12]       ; Processor branches to the highest priority daisy
                                 ; chained ISR and skips the pre-amble (+12)
```

Please note that the value 12 used in instruction LDR PC, [r12, #12] is only specific to the example code given here. The offset #12 will be dependent on the system's interrupt stacking preamble code size.

ERRATA - CATEGORY 1

There are no Errata in this Category

ERRATA - CATEGORY 2

There are no Errata in this Category

ERRATA - CATEGORY 3

120265: Sensitivity list issue in VicPriority.v

Status

Affects: product PL190 VIC -Perpetual.

Fault status: Cat 3, Present in: 1, Fixed in r1p2-00rel0.

Description

VicPriority.v

Line 427 : PriorityMask

The signal name, which is not in the sensitivity list, is used.

Implications

Simulation results at RTL and gate level may differ.

Workaround

None

318670: Daisychain results in transient vectors for asynchronous interrupts

Status

Affects: product PL190 VIC -Perpetual.

Fault status: Cat 3, Present in: 1, Fixed in r1p2-00rel0.

Description

If there are two VICs daisychained together,VIC1 and VIC2, VIC2 feeding into VIC1;

- when there is a vectored interrupt pending on VIC2, and an asynchronous interrupt occurs on VIC1:

- the VECTADDROUT register in VIC1 may be updated with a temporary transition value for one clock cycle.

The result is that when servicing the VIC2 interrupt, an incorrect interrupt vector may be read by the system processor core.

Implications

If there are VICs daisychained together, when servicing the daisy chained VICs' interrupt, an incorrect interrupt vector may be read by the system processor core. Therefore it may not be possible to use the daisy-chaining feature of the PL190, particularly if vectored interrupts are being used.

Workaround

None

ERRATA – DRIVER SOFTWARE

There are no Errata in this Category