Arm® CoreLink™ SDK-200 System Design Kit

Revision: r1p0

Technical Overview

arm

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Arm® CoreLink™ SDK-200 System Design Kit

Technical Overview

Release Information

Document History

Issue	Date	Confidentiality	Change
0000-00	26 June 2017	Non-Confidential	First release for r0p0 Beta
0100-00	26 September 2017	Non-Confidential	First release for r1p0 EAC

Confidentiality Status

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Product Status

The information in this document is Final, that is for a developed product.

Web Address

http://www.arm.com

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Arm® CoreLink™ SDK-200 System Design Kit Technical Overview

Appendix A Revisions

Preface

This preface introduces the *Arm® CoreLink™ SDK-200 System Design Kit Technical Overview*.

It contains the following:

About this book

This book is for the Arm® CoreLink™ SDK-200 System Design Kit (SDK-200). It describes the hardware and software for the system.

Product revision status

The r*m*p*n* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*m* Identifies the major revision of the product, for example, r1.

p*n* Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for hardware or software engineers who want an overview of the functionality in the CoreLink™ SDK-200 System Design Kit.

Using this book

This book is organized into the following chapters:

Chapter 1 SDK-200 overview
This chapter introduces the Arm CoreLink SDK-200 System Design Kit (SDK-200).

Chapter 2 Functional overview
This chapter describes the IP products included in the SDK-200 license.

Appendix A Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space
Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
Denotes language keywords when used outside example code.

`<and>`
Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Additional reading

This section lists publications by Arm and by third parties.

See *Infocenter*, for access to Arm documentation.

Arm publications
: This book contains information that is specific to this product. See the following documents for other relevant information:

- *Arm® CoreLink™ SSE-050 Subsystem for Embedded Technical Reference Manual* (100918).
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Technical Reference Manual* (101104).
- *Arm® CoreLink™ SIE-200 System IP for Embedded Technical Reference Manual* (DDI 0571).
- *Arm® Cortex®-M3 Processor Technical Reference Manual* (100165).
- *Arm® Cortex®-M33 Processor Technical Reference Manual* (100230).
- *Arm® Cortex®-M System Design Kit Technical Reference Manual* (DDI 0479).
- *Arm® CoreLink™ CG092 AHB Flash Cache Technical Reference Manual* (DDI 0569).
- *Arm® CoreLink™ LPD-500 Low Power Distributor Technical Reference Manual* (100361).
- *Arm® PrimeCell Real Time Clock (PL031) Technical Reference Manual* (DDI 0224).
- *Arm® PrimeCell µDMA Controller (PL230) Technical Reference Manual* (DDI 0417).
- *Arm® TrustZone® True Random Number Generator Technical Reference Manual* (100976).
- *Arm® AMBA® APB Protocol Specification* (IHI 0024).
- *ARMv8-M Architecture Reference Manual* (DDI 0553).

The following confidential books are only available to licensees or require registration with Arm:

- *Arm® CoreLink™ SSE-050 Subsystem for Embedded Configuration and Integration Manual* (100919).
- *Arm® CoreLink™ SSE-200 Subsystem for Embedded Configuration and Integration Manual* (100224).
- *Arm® Cortex®-M0 and M0+ System Design Kit Example System Guide* (DUI 0559).
- *Arm® Cortex®-M System Design Kit Example System Guide* (DUI 0594).

Note

- See *www.arm.com/cmsis* for embedded software development resources including the *Cortex Microcontroller Software Interface Standard* (CMSIS).
- See Arm Mbed™ platform, *https://www.mbed.com* for information on the Mbed tools including Mbed OS and online tools.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *Arm CoreLink SDK-200 System Design Kit Technical Overview*.
- The number 101063_0100_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

Note

Arm tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Chapter 1
SDK-200 overview

This chapter introduces the Arm CoreLink SDK-200 System Design Kit (SDK-200).

It contains the following sections:

1.1 About the SDK-200

The SDK-200 provides a subsystem architecture, a reference platform, and a collection of IP products that can be used to create a secure IoT system. To provide this functionality, the SDK-200 product grants licenses to the following subsystem and component IP products:

CoreLink SSE-050 Subsystem for Embedded
: The SSE-050 provides a starting point for a product in the *Internet of Things* (IoT) and embedded market segments. The SSE-050 provides a process and technology agnostic reference, pre-integrated, validated, hardware and software subsystem for Arm Cortex-M3 processors that can be extended to provide an IoT endpoint system.

CoreLink SSE-200 Subsystem for Embedded
: The SSE-200 provides a high-performance and low-power computing subsystem for Arm Cortex-M33 processors. It can be the foundation of a secure system because of system-level support for TrustZone technologies.

Cortex-M System Design Kit
: The Cortex-M System Design Kit provides an example system for the Arm Cortex-M processors and reusable AMBA AHB-Lite and APB components for low-power designs.

Cortex-M0 and M0+ System Design Kit
: The Cortex-M0 and Cortex-M0+ System Design Kit provides an example system-level design for the Arm Cortex-M0 and Cortex-M0+ processors and reusable AMBA components for system-level development.

CoreLink SIE-200 System IP for Embedded
: The SIE-200 product is a collection of interconnect, peripheral, and TrustZone controller components for use with a processor that complies with the ARMv8-M processor architecture.

CoreLink LPD-500 Low Power Distributor
: The LPD-500 is a standalone configurable component to distribute Q-Channel interfaces to multiple devices and subsystems. Q-Channels are used to manage clock gating and power control.

CoreLink CG092 AHB Flash Cache
: The CG092 is an instruction cache that is designed to be instantiated between the bus interconnect and the *embedded Flash* (eFlash) controller.

PrimeCell Real Time Clock
: The *Real Time Clock* (RTC) is an AMBA slave module that connects to the *Advanced Peripheral Bus* (APB).

  The RTC can be used to provide a basic alarm function or long time base counter. This is achieved by generating an interrupt signal after counting for a programmed number of cycles of a real-time clock input. Counting in one second intervals is achieved by use of a 1Hz clock input to the RTC.

TrustZone True Random Number Generator
: The *True Random Number Generator* (TRNG) provides an assured level of entropy (as analyzed by Entropy Estimation logic). The output from the TRNG can be used to seed deterministic random bit generators.

1.1.1 Using the SDK IP products

The SDK-200 licensed IP can be used in the following ways:

- Use the CoreLink SSE-050 or SSE-200 subsystem as a verified foundation for your own IoT solution that is based around the Cortex-M3 or Cortex-M33 processors, respectively.

  Use the SIE-200 components to add bus and controller IP to create secure TrustZone systems.
- Use the *Cortex-M System Design Kit* (CMSDK) and the example system as a starting point for your own IoT solution that is based around the Cortex-M0, Cortex-M0+, Cortex-M3, or Cortex-M4 processors.

- Use the Cortex-M0 and Cortex-M0+ System Design Kit and the example system as a foundation for your own IoT solution that is based around the Cortex-M0 or Cortex-M0+ processors.
- Use the system IP provided with the SSE-050, SSE-200, CMSDK, LPD-500, CG092, or the SIE-200, and your own IP to create a custom solution. You can use the example systems and software libraries as a reference for your system solution.

Note

- The SSE-050 or SSE-200 and CMSDK build scripts include interconnections to a processor, but a processor must be separately licensed and installed.

  Using the SSE-200 also requires a license for the CoreSight™ SoC-400M product bundle (TM150).
- See the *Arm® CoreLink™ SDK-200 Release Note* for details about how to download and install the SDK-200 components that you require.

1.2 Product deliverables

The CoreLink SDK-200 product bundle (BP310) does not have hardware or software deliverables. Its subsystems and IP component products include these deliverables.

The hardware deliverables must be downloaded separately for the following IP products that are included in the SDK-200 license:

- CoreLink SSE-050 Subsystem for Embedded (CG063).
- CoreLink SSE-200 Subsystem for Embedded (CG062).
- CoreLink SIE-200 System IP for Embedded (BP300).
- Cortex-M System Design Kit (BP210).
- Cortex-M0 and M0+ System Design Kit (BP200).
- CoreLink LPD-500 Low Power Distributor (PL408).
- CoreLink CG092 AHB Flash Cache (CG092).
- PrimeCell Real Time Clock (PL031).
- TrustZone True Random Number Generator (CC003).

See the *Arm® CoreLink™ SDK-200 Release Note* for the component versions.

1.3 Compliance

See the *Technical Reference Manuals* for more details of the product's compliance to the following specifications:

- Arm architecture.
- CoreSight Debug.
- Advanced Microcontroller Bus Architecture.

1.4 Documentation

The following documents are supplied with the CoreLink SDK-200 product bundle (BP310):

Technical Overview
The *Technical Overview* (TO) describes the functionality of the SDK-200 System Design Kit.

Release Note
The *Release Note* describes download and installation instructions for the IP products included in the SDK-200.

Note

- The separately downloaded product bundles also contain documentation such as *Technical Reference Manual*s or *Configuration and Integration Manual*s.
- See the individual product bundles for details of what documentation is provided for that IP bundle.

Chapter 2
Functional overview

This chapter describes the IP products included in the SDK-200 license.

It contains the following sections:

2.1 Supported processors

The following table lists the processors supported by the products in the CoreLink SDK-200 bundle used to create a secure IoT system.

Table 2-1 Supported processors

CoreLink SDK-200 products								
Processor	**CM0SDK**	**CMSDK**	**LPD-500**	**SIE-200 System IP**	**SSE-050 Subsystem**	**SSE-200 Subsystem**	**RTC**	**TRNG**
Cortex-M0	Yes	Yes	-	-	-	-	Yes	Yes
Cortex-M0+	Yes	Yes	-	-	-	-	Yes	Yes
Cortex-M23	-	Limited[a]	Yes	Yes	-	Limited[b]	Yes	Yes
Cortex-M3	-	Yes	-	Yes[c]	Yes	-	Yes	Yes
Cortex-M4	-	Yes	-	Yes[c]	-	-	Yes	Yes
Cortex-M33	-	Limited[a]	Yes	Yes	-	Yes	Yes	Yes
Cortex-M7	-	Limited[d]	-	Limited[d]	-	-	Yes	Yes

a Does not propagate all AHB5 attributes and is not security aware.
b Enabled by subsystem modification rights.
c Enabled by Cortex-M3/Cortex-M4 AHB5 Adapter component, which is part of SIE-200.
d Enabled by using the Cortex-M7 AHB bus and/or an AXI2AHB converter.

2.2 CoreLink Subsystem for Embedded

The Arm CoreLink SSE-050 and SSE-200 Subsystem for Embedded are subsystems that provide a starting point for a product in the *Internet of Things* (IoT) and embedded market segments.

The SSE-050 subsystem delivers a process and technology agnostic reference, pre-integrated, validated, hardware and software subsystem that can be extended to provide an IoT endpoint system.

The SSE-200 subsystem drives system architecture and software standardization, and was developed to provide a high-performance computing subsystem that encompasses leading-edge Cortex-M and TrustZone technologies.

The SSE solution consists of hardware, software, and software tools to enable the rapid development of IoT *System on Chip* (SoC) solutions.

2.2.1 CoreLink SSE-050 Subsystem for Embedded

The SSE-050 subsystem contains the following components:

- A Cortex-M3 processor.
- Configurable Debug and Trace.
- Multilayer AMBA AHB-Lite interconnect.
- Memory system.
- Two APB timers.

The following figure shows the SSE-050 subsystem, with other IP, in an example design.

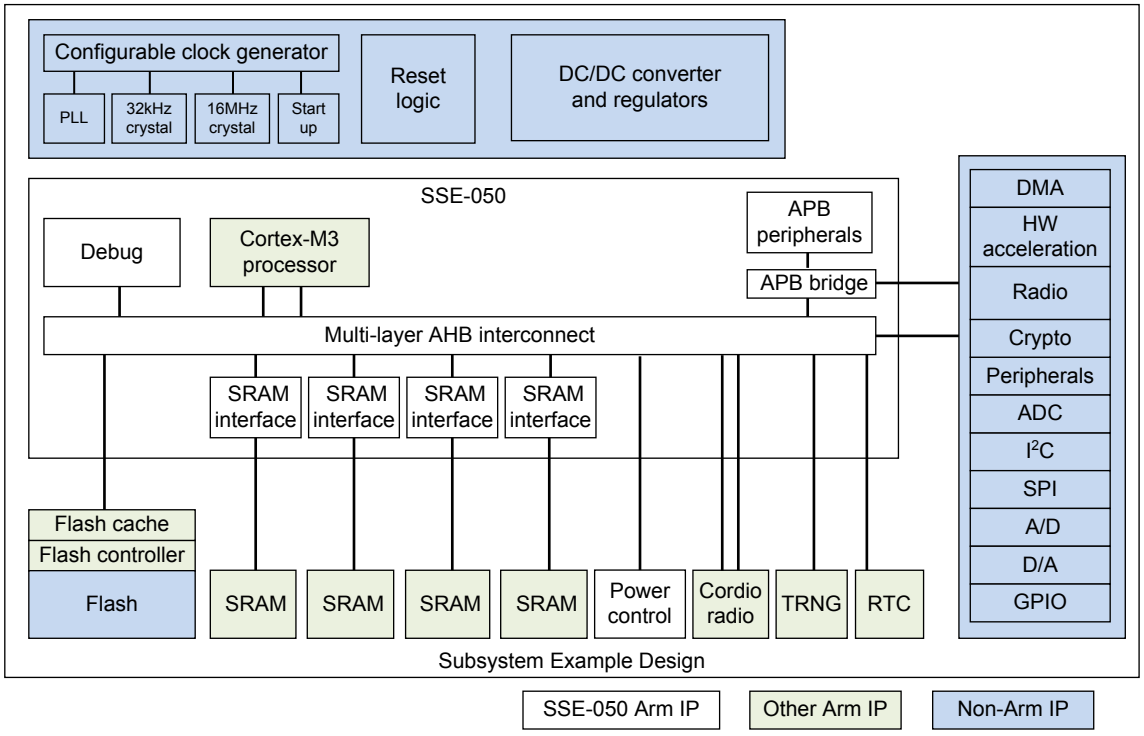

Figure 2-1 SSE-050 Subsystem for Embedded example design

2.2.2 CoreLink SSE-200 Subsystem for Embedded

The SSE-200 subsystem provides the following pre-assembled elements to use as the basis of an IoT SoC:

- Two Cortex-M33 processors that must be separately licensed.
- AMBA AHB5 bus matrix for internal and expansion buses.
- System controller.
- I-cache.
- CoreSight debug and trace that must be separately licensed.
- CoreLink SIE-200 and CMSDK components.
- SRAM memory.
- Power, clock, and reset control infrastructure.

Note

- For details of the separately licensed Cortex-M33 processor, see the *Arm® Cortex®-M33 Processor Technical Reference Manual*.
- For details of the SIE-200 components, see the *Arm® CoreLink™ SIE-200 Technical Reference Manual*.
- The SSE-200 is complemented by software libraries that are integrated with the Mbed operating system.
- The provided system components only form part of the finished SoC and Arm expects system designers to extend and customize the subsystem for their application requirements.

The following figure shows a block diagram of the SSE-200 elements:

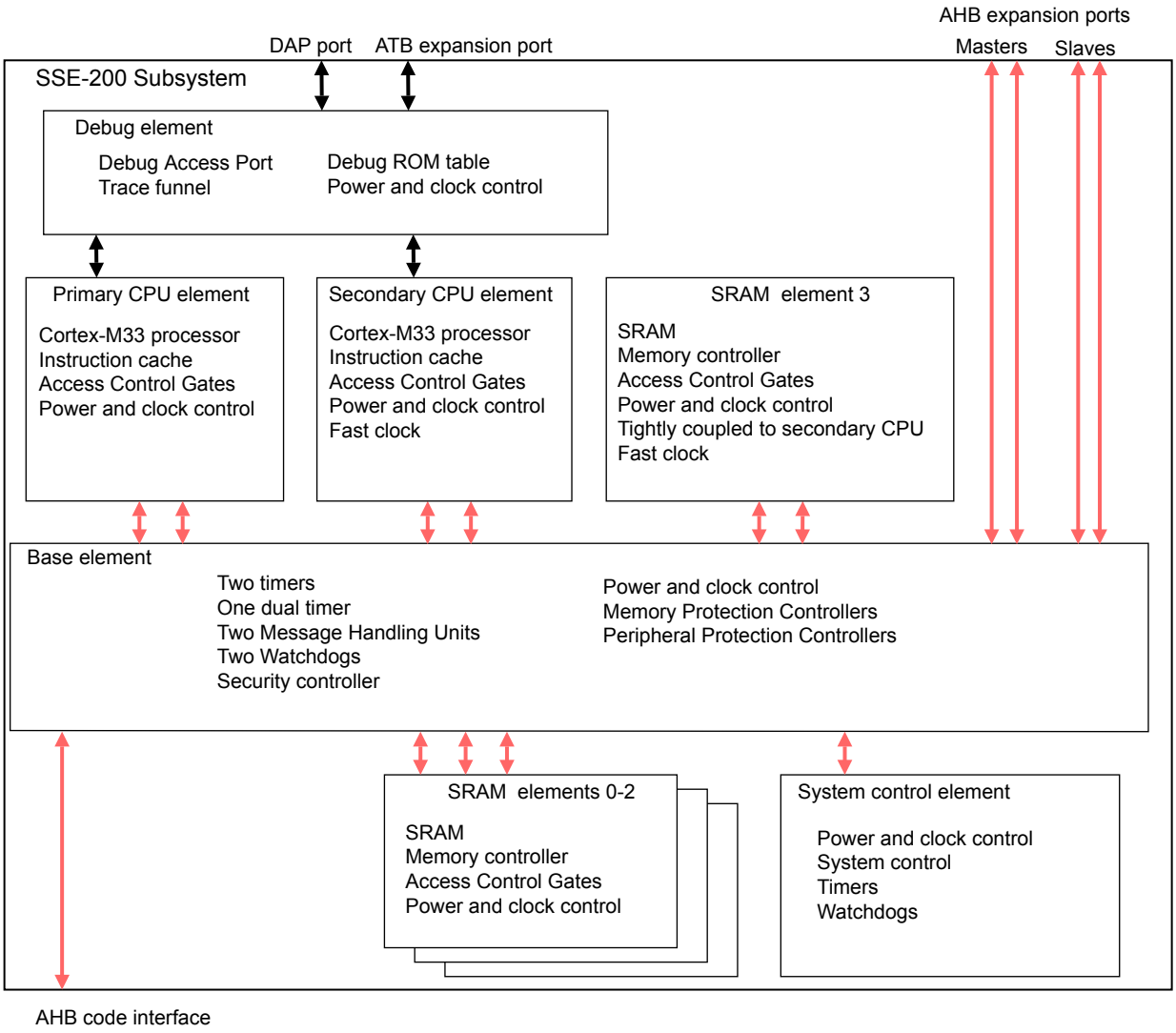

Figure 2-2 SSE-200 Subsystem for Embedded high-level example system block diagram

2.2.3 Subsystem for Embedded software

Application processor firmware, which is available separately, consists of the code that is required to boot the subsystem up to the point where the OS execution starts. Contact your Arm representative for details on the software and its location.

The firmware contains:

- *Cortex Microcontroller Software Interface Standard* (CMSIS) compliant drivers.
- Flash programming support code, which is separate from Mbed OS.
- Separately ported Mbed OS that includes uVisor ported onto the SSE-050 and SSE-200 systems.
- Execution support for the SSE-200 *Fixed Virtual Platform* (FVP) and RTL simulators.
- Support for SSE-200 on MPS2 FPGA Development Platform.
- Mbed OS driver support and code, for example I/O peripherals.
- Code that is required to load Mbed from boot media and set up the initial security environment.
- Support for system security components, including memory protection controllers.
- Support for runtime processor power state control.

2.3 Cortex-M System Design Kit

The Cortex-M System Design Kit helps you design products using Arm Cortex-M3 and Cortex-M4 processors.

The design kit contains the following:

- A selection of AHB-Lite and APB components, including several peripherals such as GPIO, timers, watchdog, and UART.

  These components are used in the CMSDK example system, but you can also use the components to create your own custom system.
- An example system for supported processor products.
- Example synthesis scripts for the example system.
- Example compilation and simulation scripts for the Verilog environment that supports ModelSim, VCS, and NC Verilog.
- Example code for software drivers.
- Example test code to demonstrate various operations of the systems.
- Example compilation scripts and example software project files that support:
  - Arm Development Studio 5 (DS-5).
  - Arm RealView Development Suite.
  - Keil® *Microcontroller Development Kit* (MDK).
  - GNU tools for Arm embedded processors (Arm GCC).
- Documentation including:
  - *Arm® Cortex®-M System Design Kit Technical Reference Manual*.
  - *Arm® Cortex®-M0 and M0+ System Design Kit Example System Guide*.
  - *Arm® Cortex®-M System Design Kit Example System Guide*.

For details of the CMSDK components, see the *Arm® Cortex®-M System Design Kit Technical Reference Manual*.

This section contains the following subsections:

- *2.3.1 Example system* on page 2-21.
- *2.3.2 Components* on page 2-22.
- *2.3.3 Cortex-M Software Design Kit software* on page 2-22.

2.3.1 Example system

The following figure shows the block diagram of the CMSDK example system:

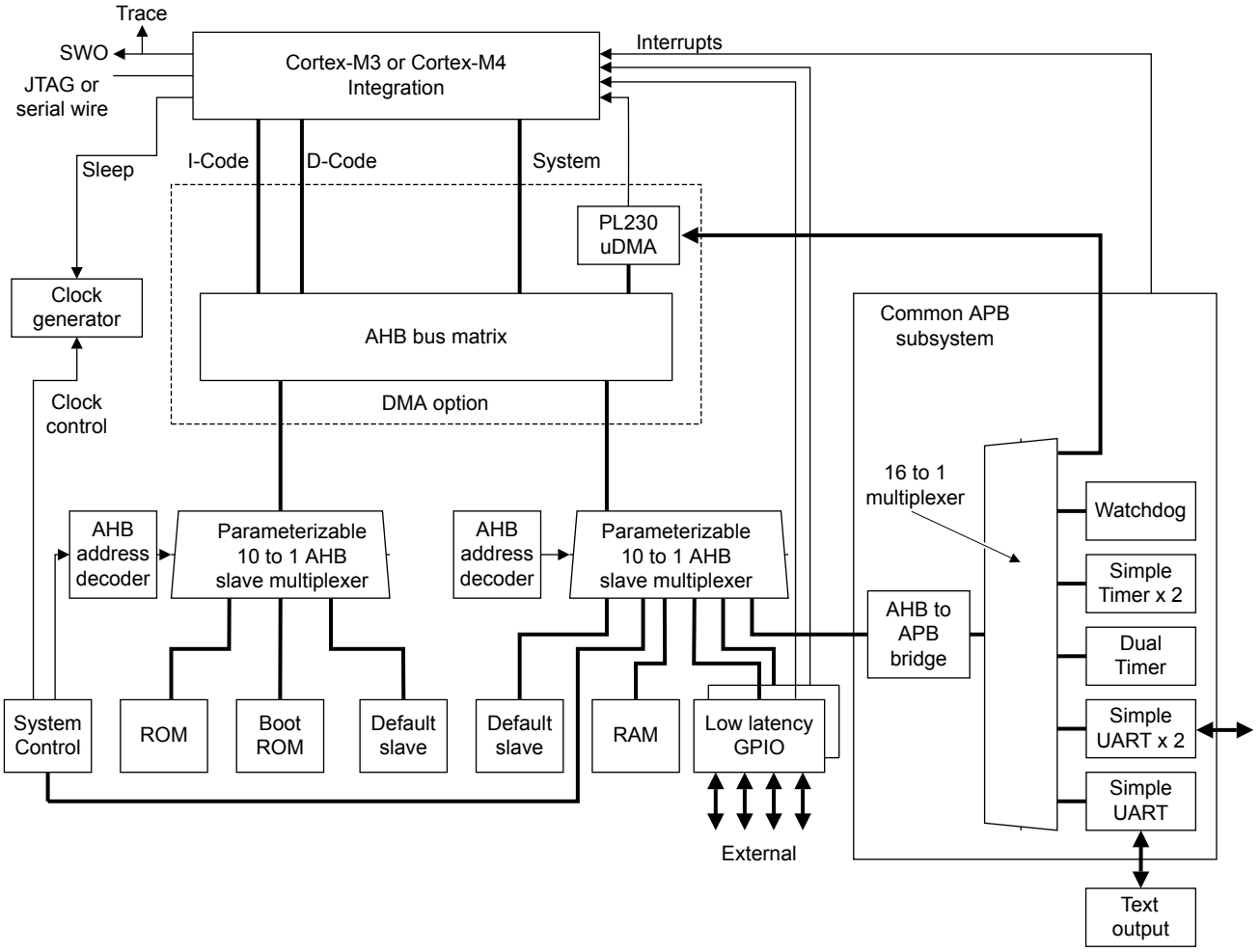

Figure 2-3 CMSDK example system

Note

The µDMA Controller (PL230) is not included in the SDK-200 license and, if instantiated, must be licensed separately. See the *Arm® PrimeCell µDMA Controller (PL230) Technical Reference Manual* for more information.

2.3.2 Components

The CMSDK example system consists of the following components and models:

- Basic AHB-Lite components.
- APB components.
- Advanced AHB-Lite components.
- Behavioral memory models.

2.3.3 Cortex-M Software Design Kit software

The Cortex-M System Design Kit includes the following software:

- CMSIS-compliant drivers.
- Device-specific header files, startup code, and example drivers including retargeting code for the `printf()` and `puts()` functions.
- Platform hardware adaptation layer code that is required in addition to the open-source code and generic Cortex-M processor header files.

- Mbed OS driver support.

  Further Cortex-M code is available on the Mbed website.
- Shell scripts to sync, build, and run the software.

2.4 Cortex-M0 and M0+ System Design Kit

The Cortex-M0 and Cortex-M0+ System Design Kit provides:

- An example system-level design for the Arm Cortex-M0 and Cortex-M0+ processors.
- Reusable AMBA components for system-level development from the CMSDK.

For information on the AMBA components that the design kit uses, see the *Arm® Cortex®-M System Design Kit Technical Reference Manual*.

This section contains the following subsections:

- *2.4.1 About the example system* on page 2-24.
- *2.4.2 Cortex-M0 and Cortex-M0+ software* on page 2-25.

2.4.1 About the example system

The *Arm Cortex-M0 and M0+ System Design Kit Example System Guide* describes an example system for the Cortex-M0 and Cortex-M0+ processors.

Figure 2-3 CMSDK example system on page 2-22 shows the example system block diagram. The following figure shows the testbench of the example system.

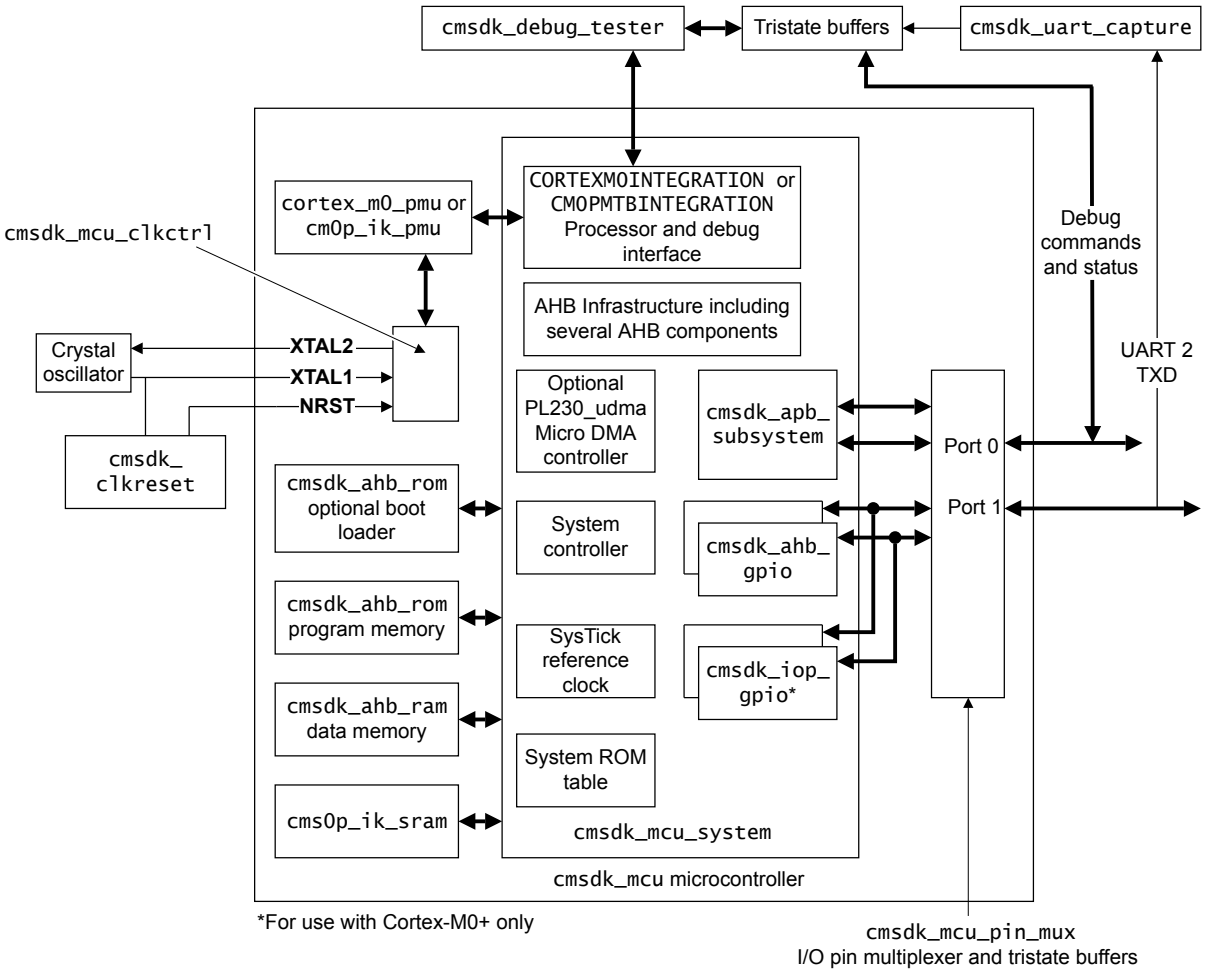

Figure 2-4 CMSDK example system

The example system is a simple microcontroller design that contains the following:

- A single Cortex-M0 or Cortex-M0+ processor.
- Internal program memory.
- SRAM data memory.
- Boot loader.
- The following peripherals:
  - Several timers.
  - *General-Purpose input/output* (GPIO).
  - *Universal Asynchronous Receiver Transmitter* (UART).
  - Watchdog timer.
- Debug connection.

Note

The optional µDMA Controller (PL230) is not included in the SDK-200 license and, if instantiated, must be licensed separately. See the *Arm® PrimeCell µDMA Controller (PL230) Technical Reference Manual* for more information.

2.4.2 Cortex-M0 and Cortex-M0+ software

The Cortex-M0 and M0+ System Design Kit products include the following software:

- CMSIS-compliant drivers.
- Device-specific header files, startup code, and example drivers including retargeting code for the `printf()` and `puts()` functions.
- Platform hardware adaptation layer code that is required in addition to the open-source code and generic Cortex-M processor header files.
- Mbed OS driver support.

  Further Cortex-M0 and Cortex-M0+ code is available on the Mbed website.
- Shell scripts to sync, build, and run the software.

2.5 SIE-200 System IP for Embedded

The CoreLink SIE-200 System IP for Embedded product is a collection of interconnect, peripheral, and TrustZone controller components for use with a processor that complies with the ARMv8-M processor architecture and the AMBA 5 AHB5 protocol.

The SIE-200 components are used in the SSE-200 product, but you can also use the SIE-200 components to create your own custom system.

The CoreLink SIE-200 System IP for Embedded consists of the following components and models that support the AHB5 standard:

- AHB5 system components.
- AHB5 bridge components.
- TrustZone protection controllers.
- Verification components.

2.6 CoreLink CG092 AHB Flash Cache

The CG092 AHB Flash Cache is an instruction cache that is instantiated between the bus interconnect and the eFlash controller.

The CG092 is a simple cache for on-chip *embedded Flash* (eFlash). The CG092 design is optimized for fetching Cortex-M3 or Cortex-M4 instructions directly from an eFlash. The main benefit of the CG092 is improved power efficiency, but there are also improvements in code fetching performance.

Note

The AHB Flash Cache can also be used with external eFlash if the Flash controller is modified accordingly.

The following figure shows the connections in a typical Flash subsystem.

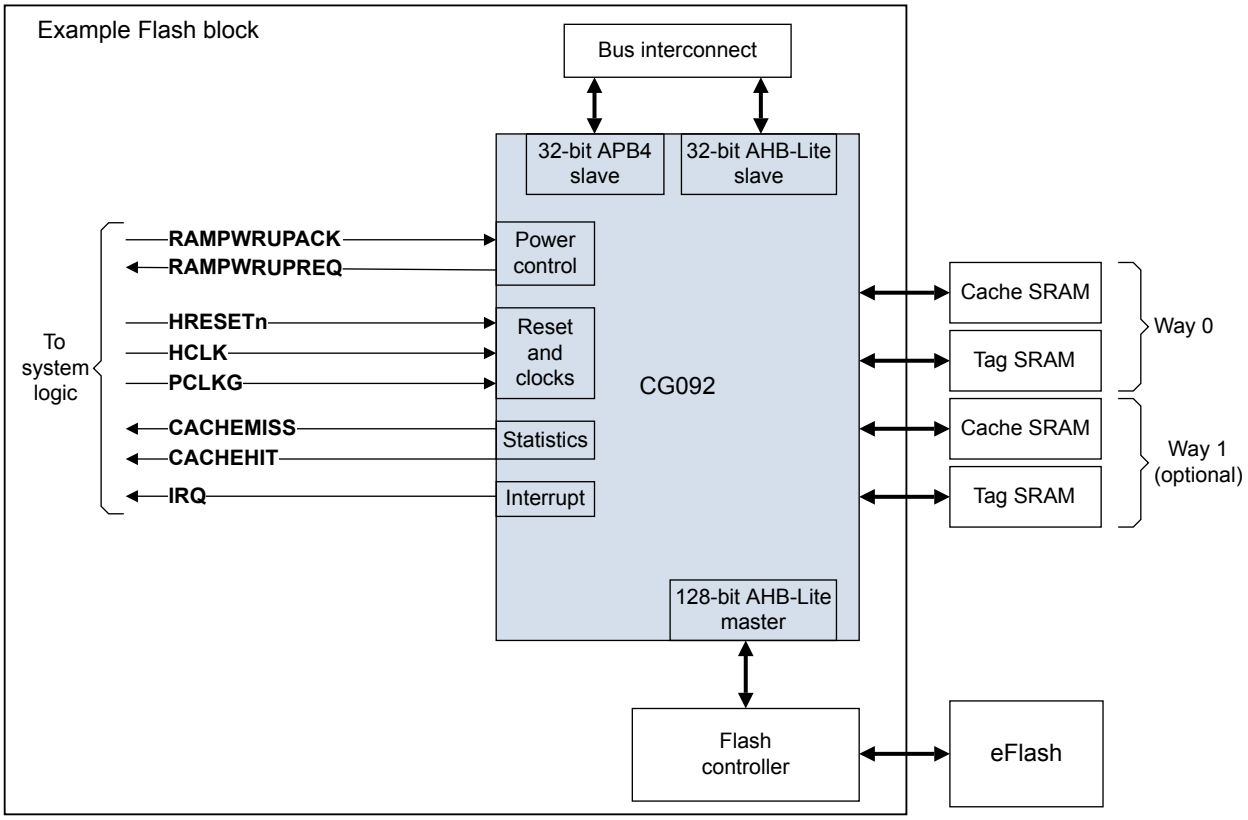

Figure 2-5 Example eFlash implementation

2.7 LPD-500 Low Power Distributor

The LPD-500 Low Power Distributor is a standalone configurable component to distribute Q-Channel interfaces to multiple devices and subsystems.

Q-Channels are used to manage quiescence, in components of the system that allow the clock to be gated off or power to be removed, to save power when not operational.

The LPD-500 can be used as an expander or sequencer. The following figure shows its use as an expander:

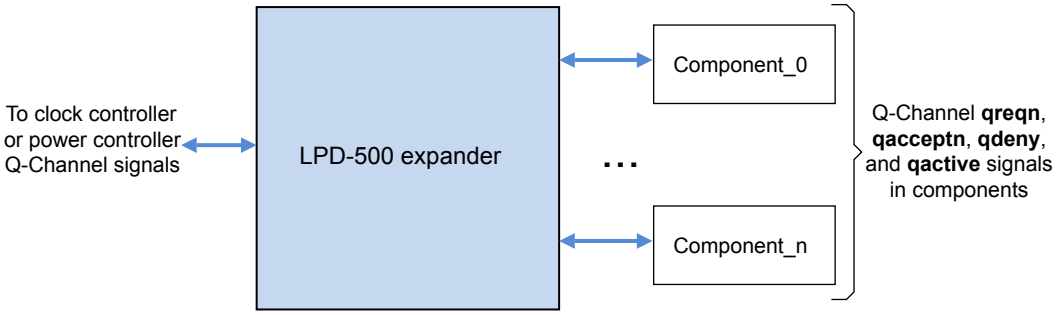

Figure 2-6 LPD-500 expander connections

2.8 Real Time Clock

The *Real Time Clock* (RTC) is an AMBA slave module that connects to the *Advanced Peripheral Bus* (APB).

The following figure shows the RTC block diagram.

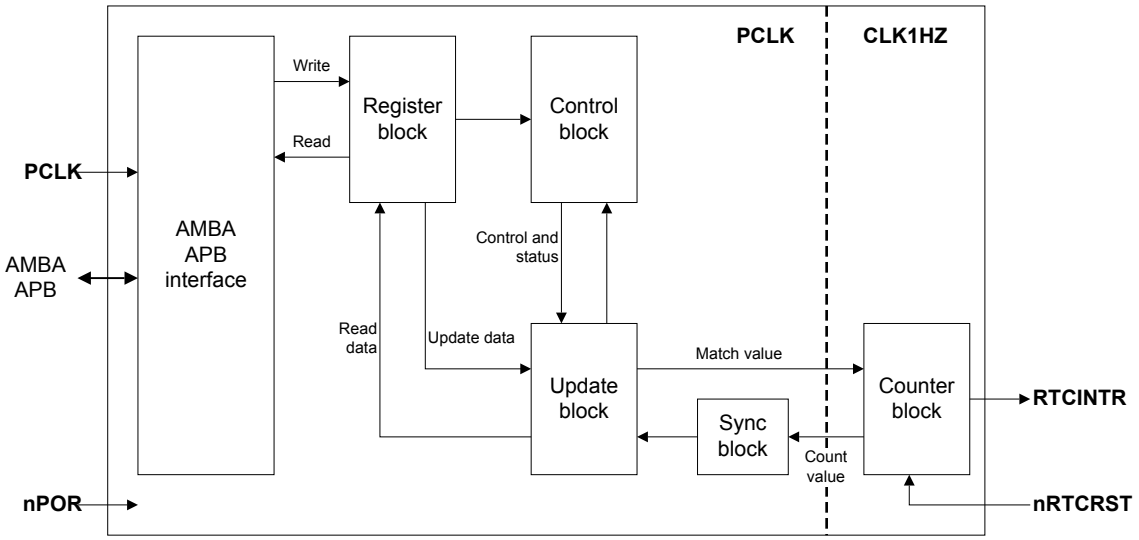

Figure 2-7 RTC block diagram

The RTC can be used to provide a basic alarm function or long time base counter. This is achieved by generating an interrupt signal after counting for a programmed number of cycles of a real-time clock input. Counting in one second intervals requires a 1Hz clock input to the RTC.

2.9 True Random Number Generator

The *True Random Number Generator* (TRNG) provides an assured level of entropy (as analyzed by Entropy Estimation logic). The output from the TRNG can be used to seed deterministic random bit generators.

The following figure shows the TRNG.

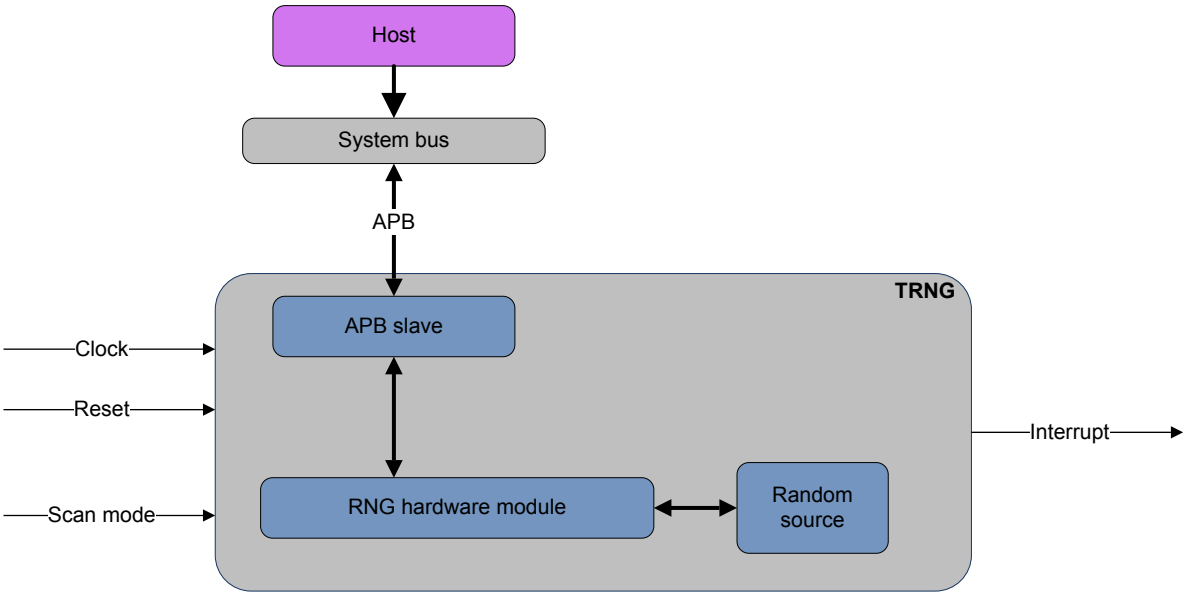

Figure 2-8 TRNG hardware overview

Appendix A
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- *A.1 Revisions* on page Appx-A-32.

A.1 Revisions

This appendix describes technical changes between released issues of this book.

Table A-1 Issue 0000-00

Change	Location	Affects
First release	-	-

Table A-2 Issue 0100-00

Change	Location	Affects
Subsystem for Embedded update (SSE-050 and SSE-200)	• *1.1 About the SDK-200* on page 1-11 • *1.2 Product deliverables* on page 1-13 • *2.2 CoreLink Subsystem for Embedded* on page 2-18 • *2.2.1 CoreLink SSE-050 Subsystem for Embedded* on page 2-18 • *2.2.2 CoreLink SSE-200 Subsystem for Embedded* on page 2-18 • *2.2.3 Subsystem for Embedded software* on page 2-20	r1p0 EAC release