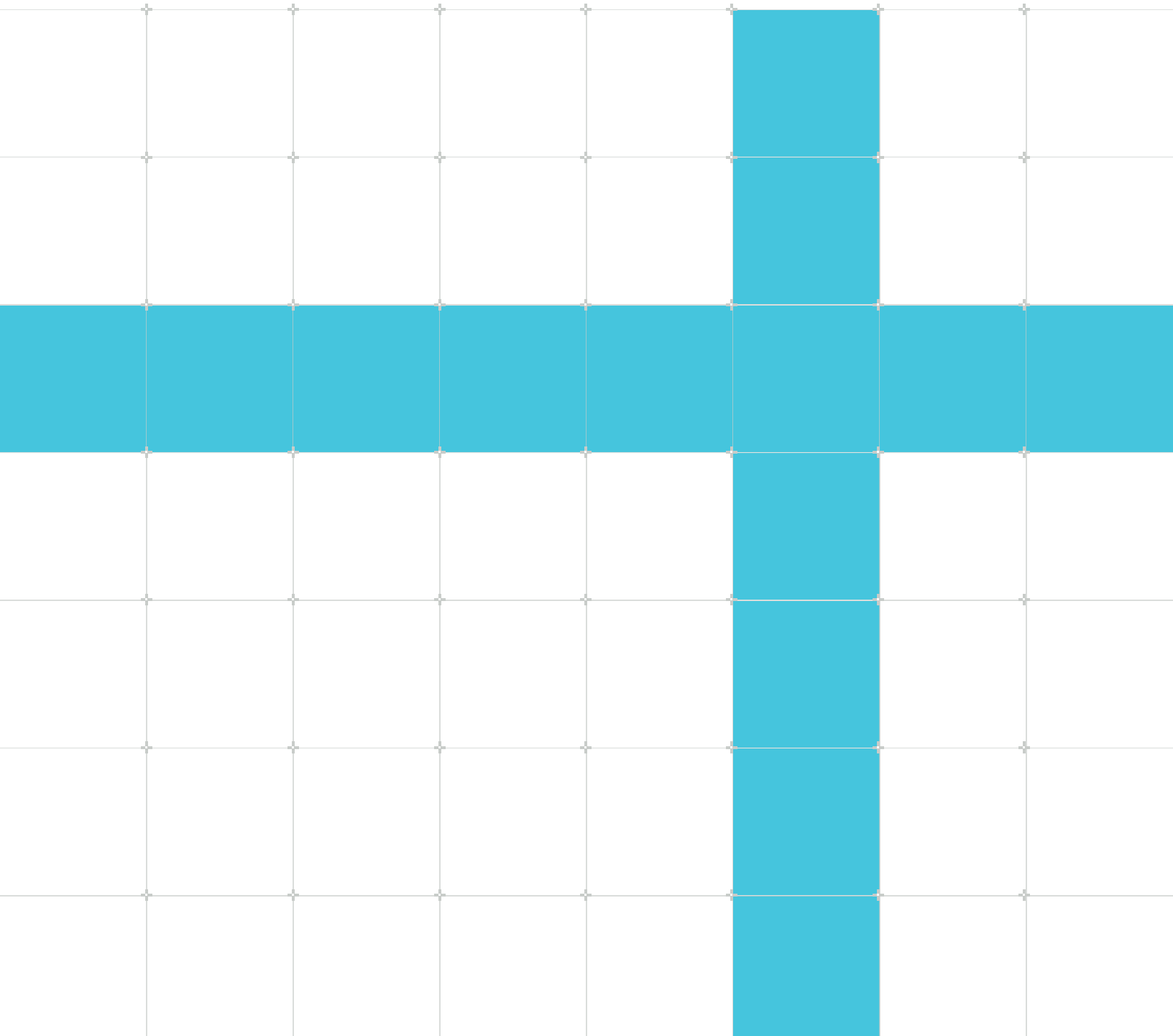
Arm® Cortex®-X1 Core Cryptographic Extension

Revision: r1p2

Technical Reference Manual

Issue 07
101435_0102_07_en



Arm® Cortex®-X1 Core Cryptographic Extension

Technical Reference Manual

Release Information

Document history

Issue	Date	Confidentiality	Change
0000-01	12 December 2018	Confidential	First beta release for r0p0
0000-02	25 March 2019	Confidential	First limited access release for r0p0
0100-03	27 September 2019	Confidential	First early access release for r1p0
0101-04	29 May 2020	Non-Confidential	First early access release for r1p1
0102-05	28 April 2021	Non-Confidential	First release for r1p2
0102-06	3 December 2021	Non-Confidential	Second release for r1p2
0102-07	29 June 2023	Non-Confidential	Third release for r1p2

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(LES-PRE-20349|version 21.0)

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Contents

1. Introduction

1.1 Product revision status

The r*x*p*y* identifier indicates the revision status of the product described in this manual, for example, r1p2, where:

r*x* Identifies the major revision of the product, for example, r1.
p*y* Identifies the minor revision or modification status of the product, for example, p2.

1.2 Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the Cortex®-X1 core with the optional Cryptographic Extension.

1.3 Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: developer.arm.com/glossary.

Convention	Use
italic	Citations.
bold	Terms in descriptive lists, where appropriate.
`monospace`	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace underline`	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

Convention	Use
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Terms that have specific technical meanings as defined in the *Arm® Glossary*. For example, **IMPLEMENTATION DEFINED**, **IMPLEMENTATION SPECIFIC**, **UNKNOWN**, and **UNPREDICTABLE**.

Recommendations. Not following these recommendations might lead to system failure or damage.

Requirements for the system. Not following these requirements might result in system failure or damage.

Requirements for the system. Not following these requirements will result in system failure or damage.

An important piece of information that needs your attention.

A useful tip that might make it easier, better or faster to perform a task.

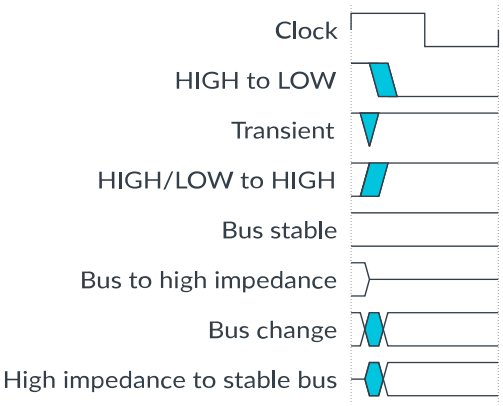
A reminder of something important that relates to the information you are reading.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

Figure 1-1: Key to timing diagram conventions



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

1.4 Useful resources

This document contains information that is specific to this product. See the following resources for other useful information.

Access to Arm documents depends on their confidentiality:

- Non-Confidential documents are available at developer.arm.com/documentation. Each document link in the following tables goes to the online version of the document.
- Confidential documents are available to licensees only through the product package.

Arm product resources	Document ID	Confidentiality
Arm® Cortex®-X1 Core Configuration and Integration Manual	101434	Confidential
Arm® Cortex®-X1 Core Technical Reference Manual	101433	Non-Confidential

Arm architecture and specifications	Document ID	Confidentiality
Arm® Architecture Reference Manual for A-profile architecture	DDI 0487	Non-Confidential

Non-Arm resources	Document ID	Organization
Advanced Encryption Standard. (FIPS 197, November 2001)	-	-
Secure Hash Standard (SHS) (FIPS 180-4, March 2012)	-	-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2. Functional description

This chapter describes the Cortex®-X1 core Cryptographic Extension.

2.1 About the Cryptographic Extension

The Cortex®-X1 core Cryptographic Extension supports the Arm®v8-A Cryptographic Extension. Some parts of the Arm®v8-A Cryptographic Extension are optional.

For more information on the optional parts of the Arm®v8-A Cryptographic Extension, see the *AArch64 Instruction Set Attribute Register 0, EL1* register (ID_AA64ISAR0_EL1) in the *Arm® Cortex®-X1 Core Technical Reference Manual*.

The Cryptographic Extension adds new A64, A32, and T32 instructions to Advanced SIMD that accelerate *Advanced Encryption Standard* (AES) encryption and decryption. It also adds instructions to implement the *Secure Hash Algorithm* (SHA) functions SHA-1, SHA-224, and SHA-256.

The optional Cryptographic Extension is not included in the base product. Arm supplies the Cryptographic Extension only under an additional license to the Cortex®-X1 core.

2.2 Revisions

This section describes the differences in functionality between product revisions.

r0p0 First release

r1p0 No functional changes

r1p1 No functional changes

r1p2 No functional changes

3. Register descriptions

This chapter describes the Cryptographic Extension registers.

3.1 Identifying the Cryptographic instructions implemented

Software can identify the Cryptographic instructions that are implemented by reading two registers.

About this task

The two registers are:

- ID_AA64ISAR0_EL1 in the AArch64 Execution state
- ID_ISAR5_EL1 in the AArch64 Execution state

3.2 Disabling the Cryptographic Extension

To disable the Cryptographic Extension, assert the CRYPTODISABLE input signal, which applies to all the Cortex®-X1 cores present in a cluster. This signal is sampled only during reset of the cores.

About this task

When CRYPTODISABLE is asserted:

- Executing a Cryptographic instruction results in an **UNDEFINED** exception.
- The ID registers described in Table 3-1: Cryptographic Extension register summary on page 11 indicate that the Cryptographic Extension is not implemented.

3.3 Register summary

The core has two instruction identification registers. Each register has a specific purpose, usage constraints, configurations, and attributes.

The following table lists the instruction identification registers for the Cortex®-X1 core Cryptographic Extension.

Table 3-1: Cryptographic Extension register summary

Name	Execution state	Description
ID_AA64ISAR0_EL1	AArch64	See 3.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0, EL1 on page 12.
ID_ISAR5_EL1	AArch64	See 3.5 ID_ISAR5_EL1, AArch32 Instruction Set Attribute Register 5, EL1 on page 14.

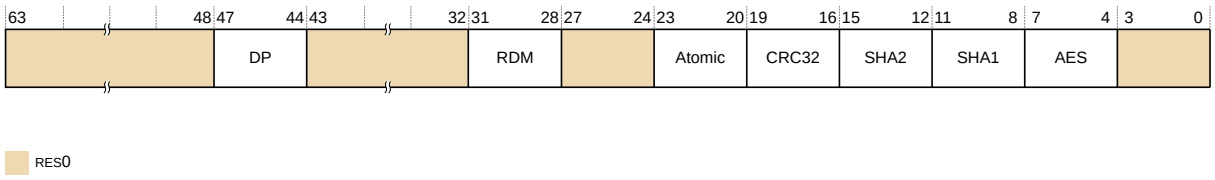
3.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0, EL1

The ID_AA64ISAR0_EL1 provides information about the instructions that are implemented in AArch64 state, including the instructions provided by the Cryptographic Extension.

Bit field descriptions

ID_AA64ISAR0_EL1 is a 64-bit register.

Figure 3-1: ID_AA64ISAR0_EL1 bit assignments



RES0, [63:48]

RES0	Reserved

DP, [47:44]

Indicates whether Dot Product support instructions are implemented.

0x1	`UDOT`, `SDOT` instructions are implemented.

RES0, [43:32]

RES0	Reserved

RDM, [31:28]

Indicates whether *Rounding Double Multiply* (`RDM`) instructions are implemented. The value is:

0x1	`SQRDMLAH` and `SQRDMLSH` instructions are implemented.

RES0, [27:24]

RES0	Reserved

Atomic, [23:20]

Indicates whether atomic instructions are implemented. The value is:

0x2	`LDADD`, `LDCLR`, `LDEOR`, `LDSET`, `LDSMAX`, `LDSMIN`, `LDUMAX`, `LDUMIN`, `CAS`, `CASP`, and `SWP` instructions are implemented.

CRC32, [19:16]

Indicates whether CRC32 instructions are implemented. The value is:

0x1 CRC32 instructions are implemented.

SHA2, [15:12]

Indicates whether SHA2 instructions are implemented. The possible values are:

0x0 No SHA2 instructions are implemented. This is the value if the core implementation does not include the Cryptographic Extension.

0x1 `SHA256H`, `SHA256H2`, `SHA256U0`, and `SHA256U1` are implemented. This is the value if the core implementation includes the Cryptographic Extension.

SHA1, [11:8]

Indicates whether SHA1 instructions are implemented. The possible values are:

0x0 No SHA1 instructions are implemented. This is the value if the core implementation does not include the Cryptographic Extension.

0x1 `SHA1C`, `SHA1P`, `SHA1M`, `SHA1SU0`, and `SHA1SU1` are implemented. This is the value if the core implementation includes the Cryptographic Extension.

AES, [7:4]

Indicates whether AES instructions are implemented. The possible values are:

0x0 No AES instructions implemented. This is the value if the core implementation does not include the Cryptographic Extension.

0x2 `AESE`, `AESD`, `AESMC`, and `AESIMC` are implemented, plus `PMULL` and `PMULL2` instructions operating on 64-bit data. This is the value if the core implementation includes the Cryptographic Extension.

RES0, [3:0]

RES0 Reserved

Configurations

ID_AA64ISAR0_EL1 is architecturally mapped to external register ID_AA64ISAR0.

Usage constraints

Accessing the ID_AA64ISAR0_EL1

To access the ID_AA64ISAR0_EL1:

```
MRS <Xt>, ID_AA64ISAR0_EL1 ; Read ID_AA64ISAR0_EL1 into Xt
```

Register access is encoded as follows:

Table 3-2: ID_AA64ISAR0_EL1 access encoding

op0	op1	CRn	CRm	op2
11	000	0000	0110	000

Accessibility

This register is accessible as follows:

EL0	EL1 (NS)	EL1 (S)	EL2	EL3 (SCR.NS = 1)	EL3 (SCR.NS = 0)
-	RO	RO	RO	RO	RO

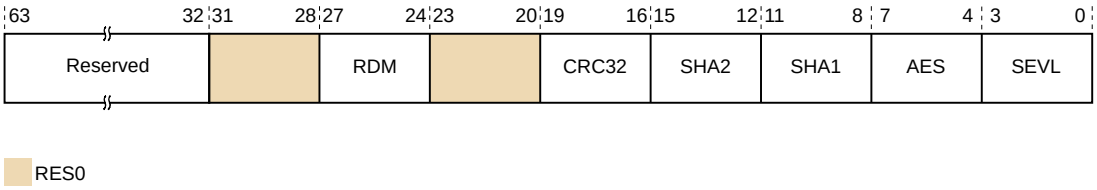
3.5 ID_ISAR5_EL1, AArch32 Instruction Set Attribute Register 5, EL1

The AArch64 register ID_ISAR5_EL1 provides information about the instructions that are implemented in AArch32 state, including the instructions provided by the optional Cryptographic Extension.

Bit-field descriptions

ID_ISAR5_EL1 is a 64-bit register.

Figure 3-2: ID_ISAR5_EL1 bit assignments



Reserved, [63:32]

Reserved.

RES0, [31:28]

RES0 Reserved

RDM, [27:24]

Indicates whether RDM instructions are implemented. The value is:

0x1 SQRDMLAH and SQRDMLSH instructions are implemented.

RES0, [23:20]

RES0 Reserved

CRC32, [19:16]

Indicates whether CRC32 instructions are implemented in AArch32 state. The value is:

0x1 CRC32 instructions are implemented.

SHA2, [15:12]

Indicates whether SHA2 instructions are implemented in AArch32 state. The possible values are:

0x0 Cryptographic Extension is not implemented or is disabled.
0x1 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions are implemented.

SHA1, [11:8]

Indicates whether SHA1 instructions are implemented in AArch32 state. The possible values are:

0x0 Cryptographic Extension is not implemented or is disabled.
0x1 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions are implemented.

AES, [7:4]

Indicates whether AES instructions are implemented in AArch32 state. The possible values are:

0x0 Cryptographic Extension is not implemented or is disabled.
0x2 AESE, AESD, AESMC, and AESIMC are implemented, plus PMULL and PMULL2 instructions operating on 64-bit data.

SEVL, [3:0]

Indicates whether the SEVL instruction is implemented. The value is:

0x1 SEVL implemented to send event local.

Configurations

This register has no configuration options.

Usage constraints

Accessing the ID_ISAR5_EL1

To access the ID_ISAR5_EL1:

```
MRS <Xt>, ID_ISAR5_EL1 ; Read ID_ISAR5_EL1 into Xt
```

Register access is encoded as follows:

Table 3-4: ID_ISAR5_EL1 access encoding

op0	op1	CRn	CRm	op2
11	000	0000	0010	101

Accessibility

This register is accessible as follows:

EL0	EL1 (NS)	EL1 (S)	EL2	EL3 (SCR.NS = 1)	EL3 (SCR.NS = 0)
-	RO	RO	RO	RO	RO

Appendix A Revisions

This appendix describes the technical changes between released issues of this document.

A.1 Revisions

This section describes the technical changes between released issues of this document.

Table A-1: Issue 0000-01

Change	Location
First beta release for r0p0	-

Table A-2: Differences between Issue 0000-01 and Issue 0000-02

Change	Location
First limited access release for r0p0	-
No technical changes	-

Table A-3: Differences between Issue 0000-02 and Issue 0100-03

Change	Location
First early access release for r1p0	-
No technical changes	-

Table A-4: Differences between Issue 0100-03 and Issue 0101-04

Change	Location
First early access release for r1p1	-
No technical changes	-

Table A-5: Differences between Issue 0101-04 and Issue 0102-05

Change	Location
First release for r1p2	-
No technical changes	-

Table A-6: Differences between Issue 0102-05 and Issue 0102-06

Change	Location
Second release for r1p2	-
No technical changes	-

Table A-7: Differences between Issue 0102-06 and Issue 0102-07

Change	Location
Third release for r1p2	-
No technical changes	-