Arm® Cortex®-X1C Core Cryptographic Extension

Revision: r0p2

Technical Reference Manual

arm

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Arm® Cortex®-X1C Core Cryptographic Extension

Technical Reference Manual

Release Information

Document History

Issue	Date	Confidentiality	Change
0000-01	31 January 2020	Confidential	First early access release for r0p0
0001-02	02 November 2020	Confidential	First early access release for r0p1
0002-03	28 April 2021	Confidential	First release for r0p2
0002-04	16 November 2021	Non-Confidential	Second release for r0p2

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Arm values inclusive communities. Arm recognizes that we and our industry have used language that can be offensive. Arm strives to lead the industry and create change.

This document includes language that can be offensive. We will replace this language in a future issue of this document.

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Contents

Arm® Cortex®-X1C Core Cryptographic Extension Technical Reference Manual

Preface

This preface introduces the *Arm® Cortex®-X1C Core Cryptographic Extension Technical Reference Manual*.

It contains the following:

About this book

This document describes the optional cryptographic features of the core. It includes descriptions of the registers used by the Cryptographic Extension.

Product revision status

The r*x*p*y* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*x* Identifies the major revision of the product, for example, r1.

p*y* Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the Cortex®-X1C core with the optional Cryptographic Extension.

Using this book

This book is organized into the following chapters:

Chapter 1 Functional description
This chapter describes the Cortex-X1C core Cryptographic Extension.

Chapter 2 Register descriptions
This chapter describes the Cryptographic Extension registers.

Appendix A Document revisions
Changes between released issues of this book are summarized in tables.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`monospace`
Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
Denotes language keywords when used outside example code.

`<and>`

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

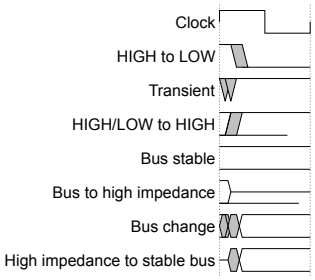

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information:

Arm publications

- *Arm® Cortex®-X1C Core Technical Reference Manual* (101968)
- *Arm® Cortex®-X1C Core Configuration and Integration Manual* (101969)
- *Arm® Architecture Reference Manual Armv8, for A-profile architecture* (DDI 0487)

Other publications

- *Advanced Encryption Standard.* (FIPS 197, November 2001)
- *Secure Hash Standard (SHS)* (FIPS 180-4, March 2012)

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *Arm Cortex-X1C Core Cryptographic Extension Technical Reference Manual*.
- The number 101970_0002_04_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

——— **Note** ———

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Chapter 1
Functional description

This chapter describes the Cortex-X1C core Cryptographic Extension.

It contains the following sections:

1.1 About the Cryptographic Extension

The Cortex-X1C core Cryptographic Extension supports the Armv8-A Cryptographic Extension. Some parts of the Armv8-A Cryptographic Extension are optional.

For more information on the optional parts of the Armv8-A Cryptographic Extension, see the *AArch64 Instruction Set Attribute Register 0, EL1* register (ID_AA64ISAR0_EL1) in the *Arm® Cortex®-X1C Core Technical Reference Manual*.

The Cryptographic Extension adds new A64, A32, and T32 instructions to Advanced SIMD that accelerate *Advanced Encryption Standard* (AES) encryption and decryption. It also adds instructions to implement the *Secure Hash Algorithm* (SHA) functions SHA-1, SHA-224, and SHA-256.

Note

The optional Cryptographic Extension is not included in the base product. Arm supplies the Cryptographic Extension only under an additional license to the Cortex-X1C core.

1.2 Revisions

This section describes the differences in functionality between product revisions.

r0p0	First release
r0p1	No functional changes
r0p2	No functional changes

Chapter 2
Register descriptions

This chapter describes the Cryptographic Extension registers.

It contains the following sections:

2.1 Identifying the Cryptographic instructions implemented

Software can identify the Cryptographic instructions that are implemented by reading two registers.

The two registers are:

- ID_AA64ISAR0_EL1 in the AArch64 Execution state
- ID_ISAR5_EL1 in the AArch64 Execution state

2.2 Disabling the Cryptographic Extension

To disable the Cryptographic Extension, assert the **CRYPTODISABLE** input signal, which applies to all the Cortex-X1C cores present in a cluster. This signal is sampled only during reset of the cores.

When **CRYPTODISABLE** is asserted:

- Executing a Cryptographic instruction results in an UNDEFINED exception.
- The ID registers described in *Table 2-1 Cryptographic Extension register summary* on page 2-15 indicate that the Cryptographic Extension is not implemented.

2.3 Register summary

The core has two instruction identification registers. Each register has a specific purpose, usage constraints, configurations, and attributes.

The following table lists the instruction identification registers for the Cortex-X1C core Cryptographic Extension.

Table 2-1 Cryptographic Extension register summary

Name	Execution state	Description
ID_AA64ISAR0_EL1	AArch64	See *2.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0, EL1* on page 2-16.
ID_ISAR5_EL1	AArch64	See *2.5 ID_ISAR5_EL1, AArch32 Instruction Set Attribute Register 5, EL1* on page 2-18.

2.4 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0, EL1

The ID_AA64ISAR0_EL1 provides information about the instructions that are implemented in AArch64 state, including the instructions provided by the Cryptographic Extension.

Bit field descriptions

ID_AA64ISAR0_EL1 is a 64-bit register.

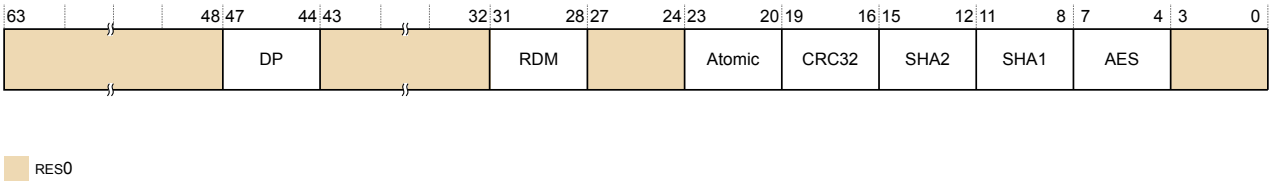

Figure 2-1 ID_AA64ISAR0_EL1 bit assignments

RES0, [63:48]

RES0 Reserved

DP, [47:44]

Indicates whether Dot Product support instructions are implemented.

0x1 UDOT, SDOT instructions are implemented.

RES0, [43:32]

RES0 Reserved

RDM, [31:28]

Indicates whether *Rounding Double Multiply* (RDM) instructions are implemented. The value is:

0x1 SQRDMLAH and SQRDMLSH instructions are implemented.

RES0, [27:24]

RES0 Reserved

Atomic, [23:20]

Indicates whether atomic instructions are implemented. The value is:

0x2 LDADD, LDCLR, LDEOR, LDSET, LDSMAX, LDSMIN, LDUMAX, LDUMIN, CAS, CASP, and SWP instructions are implemented.

CRC32, [19:16]

Indicates whether CRC32 instructions are implemented. The value is:

0x1 CRC32 instructions are implemented.

SHA2, [15:12]

Indicates whether SHA2 instructions are implemented. The possible values are:

0x0 No SHA2 instructions are implemented. This is the value if the core implementation does not include the Cryptographic Extension.

0x1 SHA256H, SHA256H2, SHA256U0, and SHA256U1 are implemented. This is the value if the core implementation includes the Cryptographic Extension.

SHA1, [11:8]

Indicates whether SHA1 instructions are implemented. The possible values are:

`0x0` No SHA1 instructions are implemented. This is the value if the core implementation does not include the Cryptographic Extension.

`0x1` `SHA1C`, `SHA1P`, `SHA1M`, `SHA1SU0`, and `SHA1SU1` are implemented. This is the value if the core implementation includes the Cryptographic Extension.

AES, [7:4]

Indicates whether AES instructions are implemented. The possible values are:

`0x0` No AES instructions implemented. This is the value if the core implementation does not include the Cryptographic Extension.

`0x2` `AESE`, `AESD`, `AESMC`, and `AESIMC` are implemented, plus `PMULL` and `PMULL2` instructions operating on 64-bit data. This is the value if the core implementation includes the Cryptographic Extension.

RES0, [3:0]

RES0 Reserved

Configurations

ID_AA64ISAR0_EL1 is architecturally mapped to external register ID_AA64ISAR0.

Usage constraints

Accessing the ID_AA64ISAR0_EL1

To access the ID_AA64ISAR0_EL1:

```
MRS <Xt>, ID_AA64ISAR0_EL1 ; Read ID_AA64ISAR0_EL1 into Xt
```

Register access is encoded as follows:

Table 2-2 ID_AA64ISAR0_EL1 access encoding

op0	op1	CRn	CRm	op2
11	000	0000	0110	000

Accessibility

This register is accessible as follows:

EL0	EL1 (NS)	EL1 (S)	EL2	EL3 (SCR.NS = 1)	EL3 (SCR.NS = 0)
-	RO	RO	RO	RO	RO

2.5 ID_ISAR5_EL1, AArch32 Instruction Set Attribute Register 5, EL1

The AArch64 register ID_ISAR5_EL1 provides information about the instructions that are implemented in AArch32 state, including the instructions provided by the optional Cryptographic Extension.

Bit-field descriptions

ID_ISAR5_EL1 is a 32-bit register.

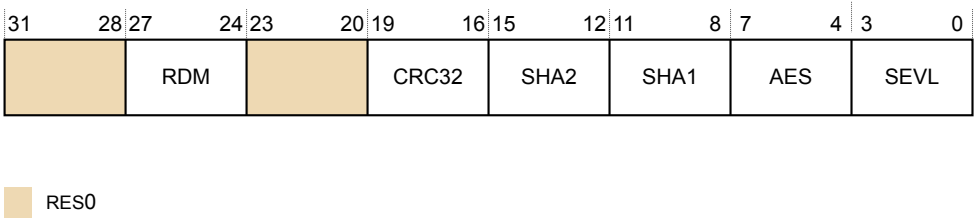

Figure 2-2 ID_ISAR5_EL1 bit assignments

RES0, [31:28]

RES0 Reserved

RDM, [27:24]

Indicates whether RDM instructions are implemented. The value is:

0x1 SQRDMLAH and SQRDMLSH instructions are implemented.

RES0, [23:20]

RES0 Reserved

CRC32, [19:16]

Indicates whether CRC32 instructions are implemented in AArch32 state. The value is:

0x1 CRC32 instructions are implemented.

SHA2, [15:12]

Indicates whether SHA2 instructions are implemented in AArch32 state. The possible values are:

0x0 Cryptographic Extension is not implemented or is disabled.

0x1 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions are implemented.

SHA1, [11:8]

Indicates whether SHA1 instructions are implemented in AArch32 state. The possible values are:

0x0 Cryptographic Extension is not implemented or is disabled.

0x1 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions are implemented.

AES, [7:4]

Indicates whether AES instructions are implemented in AArch32 state. The possible values are:

0x0 Cryptographic Extension is not implemented or is disabled.

0x2 AESE, AESD, AESMC, and AESIMC are implemented, plus PMULL and PMULL2 instructions operating on 64-bit data.

SEVL, [3:0]

Indicates whether the SEVL instruction is implemented. The value is:

0x1 SEVL implemented to send event local.

Configurations

This register has no configuration options.

Usage constraints

Accessing the ID_ISAR5_EL1

To access the ID_ISAR5_EL1:

```
MRS <Xt>, ID_ISAR5_EL1 ; Read ID_ISAR5_EL1 into Xt
```

Register access is encoded as follows:

Table 2-3 ID_ISAR5_EL1 access encoding

op0	op1	CRn	CRm	op2
11	000	0000	0010	101

Accessibility

This register is accessible as follows:

EL0	EL1 (NS)	EL1 (S)	EL2	EL3 (SCR.NS = 1)	EL3 (SCR.NS = 0)
-	RO	RO	RO	RO	RO

Appendix A
Document revisions

Changes between released issues of this book are summarized in tables.

It contains the following section:

A.1 Revisions

This section describes the technical changes between released issues of this document.

Table A-1 Issue 0000-01

Change	Location
First Confidential early access release for r0p0	-

Table A-2 Differences between Issue 0000-01 and Issue 0001-02

Change	Location
First Confidential early access release for r0p1	-
No technical changes	-

Table A-3 Differences between Issue 0001-02 and Issue 0002-03

Change	Location
First Confidential release for r0p2	-
No technical changes	-

Table A-4 Differences between Issue 0002-03 and Issue 0002-04

Change	Location
First Non-Confidential release for r0p2	-
No technical changes	-