Arm® Neoverse™ N1 System Development Platform

Technical Reference Manual

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Arm® Neoverse™ N1 System Development Platform

Technical Reference Manual

Release Information

Document History

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0000-00	01 March 2019	Confidential	Alpha1 release
0000-01	17 September 2019	Non-Confidential	Alpha2 release.
0000-02	06 April 2020	Non-Confidential	Beta release.

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Web Address

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This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Conformity

The *Waste Electrical and Electronic Equipment* (WEEE) marking, that is, the crossed out wheelie-bin figure, indicates that this product must not be disposed of with general waste within the European Union. To prevent possible harm to the environment from uncontrolled waste disposal, the user is required to recycle the product responsibly to promote reuse of material resources. To comply with EU law, you must dispose of the product in one of the following ways:

- Return it to the distributer where it was purchased. The distributer is required to arrange free collection when requested.
- Recycle it using local WEEE recycling facilities. These facilities are now very common and might provide free collection.
- If purchased directly from Arm, Arm provides free collection. Please e-mail *weee@arm.com* for instructions.

The CE Declaration of Conformity for this product is available on request.

The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling this product.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across any sensitive equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note

It is recommended that wherever possible shielded interface cables be used.

Contents
Arm® Neoverse™ N1 System Development Platform Technical Reference Manual

Preface

This preface introduces the *Arm® Neoverse™ N1 System Development Platform Technical Reference Manual*.

It contains the following:

About this book

This book describes the Arm® Neoverse™ N1 System Development Platform.

Intended audience

This book is written for experienced hardware and software developers. It enables demonstration of coherent traffic between the N1 SoC and an accelerator daughterboard, and PCI Express Gen 4 development.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter introduces the Arm Neoverse N1 System Development Platform (N1 SDP).

Chapter 2 Hardware description
This chapter describes the N1 SDP hardware.

Chapter 3 Configuration
This chapter describes the powerup and configuration process of the N1 SDP.

Chapter 4 Programmers model
This chapter describes the programmers model of the N1 SDP.

Appendix A Signal descriptions
This appendix describes the signals that are present at the N1 SDP ports.

Appendix B Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`monospace`
Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
Denotes language keywords when used outside example code.

<and>
: Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

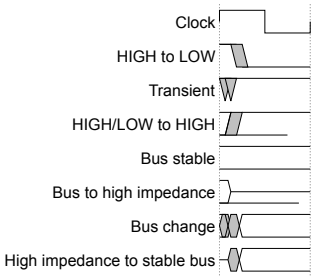

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
: The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n
: At the start or end of a signal name, n denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications

- *Arm® Neoverse™ N1 Core Technical Reference Manual* (100616).
- *Arm® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual* (100568).
- *Arm® CoreLink™ MMU-600 System Memory Management Unit Technical Reference Manual* (100310).
- *Arm® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (DDI 0475).
- *Arm® CoreLink™ CMN-600 Coherent Mesh Network Technical Reference Manual* (100180).
- *Arm® CoreLink™ TLX-400 Network Interconnect Thin Links Supplement to Arm® CoreLink™ NIC-400 Network Interconnect Technical Reference Manual* (DSU 0028).
- *Arm® CoreLink™ GIC-600 Generic Interrupt Controller Technical Reference Manual* (100336).
- *Arm® CoreLink™ GIC-400 Generic Interrupt Controller Technical Reference Manual* (DDI 0471).
- *Arm® Cortex®-M7 Processor Technical Reference Manual* (DDI 0489).
- *Arm® PrimeCell UART(PL011) Technical Reference Manual* (DDI 0183).
- *Arm® PrimeCell General Purpose Input/Output (PL061) Technical Reference Manual* (DDI 0190).
- *Arm® PrimeCell Real Time Clock (PL031) Technical Reference Manual* (DDI 0224).
- *Arm® Dual-Timer (SP804) Technical Reference Manual* (DDI 0271).
- *Arm® Watchdog Module (SP805) Technical Reference Manual* (DDI 0270).
- *Arm® PrimeCell System Controller SP810 Technical Reference Manual* (DDI 0254)
- *Arm® CoreSight™ Components Technical Reference Manual* (DDI 0314).
- *Arm® DS-5 Getting Started Guide* (100950).
- *Arm® DS-5 Arm DSTREAM User Guide* (100955).
- *Arm® DS-5 Debugger User Guide* (100953).

The following book is only available to licensees or requires registration with Arm.

- *Arm® DynamIQ™ Shared Unit Technical Reference Manual* (100453).

Feedback

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If you have any comments or suggestions about this product, contact your supplier and give:

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- The product revision or version.
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- The title *Arm Neoverse N1 System Development Platform Technical Reference Manual*.
- The number 101489_0000_02_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

Note

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Chapter 1
Introduction

This chapter introduces the Arm Neoverse N1 System Development Platform (N1 SDP).

It contains the following sections:

1.1 Precautions

This section describes precautions that ensure safety and prevent damage to your N1 SDP.

This section contains the following subsections:

1.1.1 Ensuring safety

The N1 SDP is supplied in a mains-powered standard PC tower. A standard 5V ATX supply powers the board.

——— Warning ———

- Do not use the N1 SDP near equipment that is sensitive to electromagnetic emissions, for example, medical equipment.
- To reduce the risk of injury, ensure that the N1 SDP is powered down and that the fans have stopped turning before opening the chassis.

———————————

1.1.2 Operating temperature

The N1 SDP has been tested in the temperature range 15°C-30°C.

1.1.3 Preventing damage

The N1 SDP is intended for use within a laboratory or engineering development environment.

——— Caution ———

If you remove the N1 SDP from the PC tower, observe the following precautions:

- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.

———————————

1.2 About the N1 SDP

The N1 SDP provides access to the Arm Neoverse N1 SoC.

N1 SoC and board

The N1 SDP enables software development for key enterprise technology and general Arm software development.

The N1 SDP consists of the N1 board containing the N1 SoC. The N1 board is a micro-ATX form factor board and is supplied in a standard PC tower unit. The N1 SoC contains two dual-core Arm Neoverse N1 processor clusters.

The system demonstrates Arm technology in the context of *Cache-Coherent Interconnect for Accelerators* (CCIX) protocol by:

- Running coherent traffic between the N1 SoC and an accelerator card.
- Coherent communication between two N1 SoCs.
- Enabling development of CCIX-enabled FPGA accelerators.

1.3 The N1 SDP at a glance

The following figures show the PC tower back panel and front panel, and the N1 board.

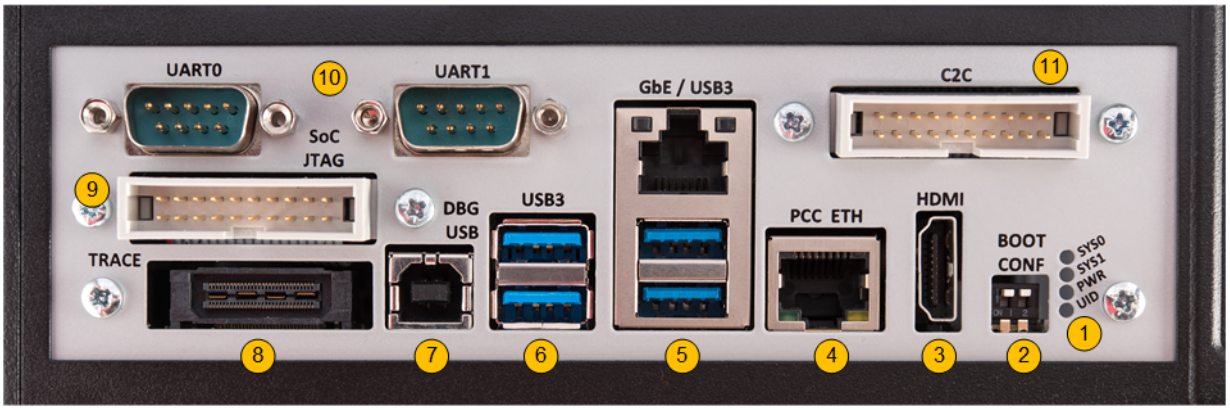


Figure 1-1 Back panel

Figure 1-2 Front panel reset buttons

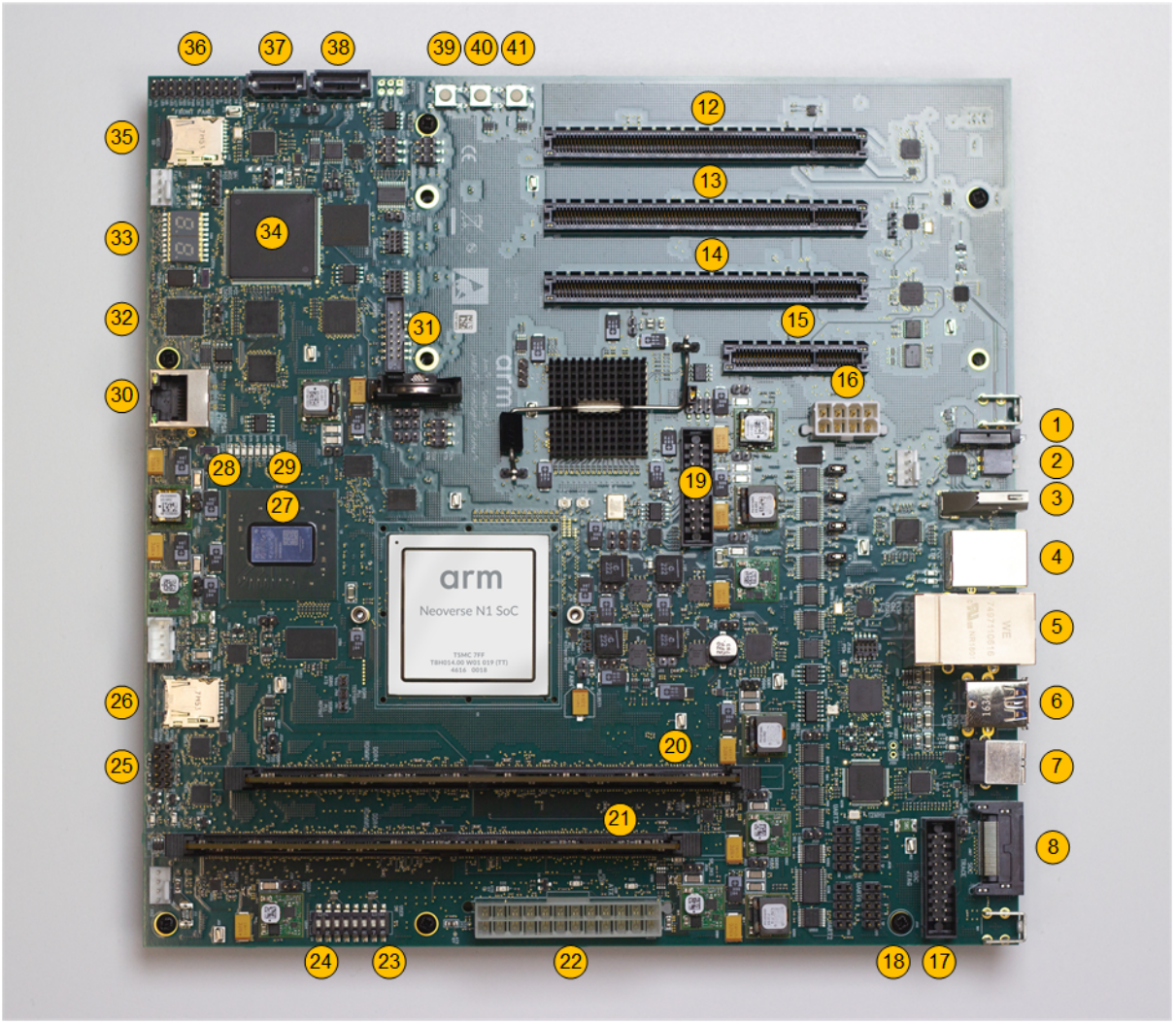


Figure 1-3 N1 board

The following table describes the components, connectors, and push buttons.

Table 1-1 Key to figures

Component number	Component name	Access	Comment
1	System LEDs	Back panel.	-
2	Configuration switches		
3	HDMI port		
4	PCC Ethernet port		
5	GbE port. USB 3.0 ports.		
6	USB 3.0 ports.		
7	DBG USB port		
8	N1 SoC trace port		
9	N1 SoC JTAG port		Ribbon cable to N1 SoC JTAG port, connector 17, on board.
10	UART0 and UART1 DB9 male connectors		Arm supplies the N1 SDP with the following ribbon cable connections: • Header UART0 on board to DB9 connector UART0 on back panel. • Header UART1 on board to DB9 connector UART1 on back panel. The DB9 connectors are logically UARTs but the pins follow the RS232 specification.
11	*Chip-to-Chip* (C2C) Connector		Ribbon cable to *Chip-to-Chip* (C2C) connector, 19, on board.
12	Slot 4: PCIe, CCIX, ×16 connector.	Board. Remove side panel for access.	16 lanes used. Gen 4 link.
13	Slot 3: PCIe ×16 connector.		8 lanes used, 8 lanes unused. Gen 3 link.
14	Slot 2: PCIe ×16 connector.		16 lanes used. Gen 3 link.
15	Slot 1: PCIe ×4 connector.		1 lane used. 3 lanes unused. Gen 3 link.
16	ATX/EPS connector		-
17	N1 SoC JTAG port	Board.	Ribbon cable to N1 SoC JTAG port, connector 9, on back panel.

Table 1-1 Key to figures (continued)

Component number	Component name	Access	Comment
18	UART0, UART1, UART2, and UART3 5×2 way headers, no pin 10.	Board. Remove side panel for access.	Arm supplies the N1 SDP with the following ribbon cable connections: • Header UART0 on board to DB9 connector UART0 on back panel. • Header UART1 on board to DB9 connector UART1 on back panel. **Note** UART2 and UART3 headers are not connected to the back panel. The UART headers are logically UARTs but the header pins follow the RS232 specification.
19	*Chip-to-Chip* (C2C) Connector	Back panel	Ribbon cable to *Chip-to-Chip* (C2C) connector, 11, on back panel.
20	RDIMM1 memory	Board. Remove side panel for access.	-
21	RDIMM0 memory		
22	ATX power connector and power indicator LEDs		
23	User switch SW8		
24	User switch SW1		
25	Reserved for use by Arm		
26	IOFPGA microSD card		
27	IOFPGA		
28	User LED0		
29	User LED7		
30	Reserved for use by Arm		
31	IOFPGA JTAG		
32	*Platform Controller Chip* (PCC)		
33	7-segment display		
34	*Motherboard Configuration Controller* (MCC)		
35	MCC configuration microSD card		
36	Front panel I/O connectors		
37	PCIe SATA0		
38	PCIe SATA1.		
39	Reserved push button	-	

Table 1-1 Key to figures (continued)

Component number	Component name	Access	Comment
40	Hardware reset button, PBRESET	Board. Remove side panel for access.	The front panel I/O connector: • Brings the PBON and PBRESET push button functions to the front panel. • Connects to the power LED.
41	On/Off/Soft reset push button, PBON		
42	Hardware reset button, PBRESET	Front panel	
43	On/Off/Soft reset push button, PBON, and power LED.		
44	HDD activity LED.		Combined signal from SATA0 and SATA1 from front panel I/O connector on board.

1.4 Getting started

The N1 SDP is controlled from a serial terminal that you connect to the DBG USB port. A set of files in the non-volatile *Motherboard Configuration Controller* (MCC) configuration microSD card configures the board. The configuration microSD card is accessible through the DBG USB port.

The board is factory-programmed with the MCC and *Platform Controller Chip* (PCC), *System Control Processor* (SCP), *Manageability Control Processor* (MCP), and *Application Processor* (AP) firmware.

Powering up into the operating state

The minimum actions to boot the N1 SDP are as follows:

1. Connect a serial terminal to the DBG USB port on the back panel. The serial port settings must be:
   - 115.2kBaud.
   - 8N1.
   - No hardware or software flow control.

   By default, the four COM ports are connected to the following devices:
   - COM<n> *Motherboard Configuration Controller* (MCC).
   - COM<n+1> - *Application Processor* (AP).
   - COM<n+2) - *System Control Processor* (SCP).
   - COM<n+3) - *Manageability Control Processor* (MCP).
2. Turn the mains power switch on the PC tower ON. The MCC window command prompt is shown and the system is now in the standby state. Ensure that both configuration switches on the back panel are in the OFF (up) position. See *1.3 The N1 SDP at a glance* on page 1-14 for the location of the configuration switches.
3. To complete the powerup sequence from the standby state, briefly press the PBON button. The system is now fully-powered and in the operating state.

Editing configuration files

The configuration microSD card contains the system configuration files. To modify the system default settings, edit or replace configuration files while the system is in standby state:

1. Ensure that the serial terminal is connected to the DBG USB port on the back panel.
2. Turn the power switch ON. The MCC window command prompt is shown and the system is now in the standby state. Ensure that both configuration switches are in the OFF (up) position.
3. Issue the following command at the MCC command prompt on the serial terminal:
   - `Cmd> usb_on`

   The serial terminal now recognizes the configuration microSD card as a *USB Mass Storage Device* (USBMSD).
4. Edit the existing configuration files, or Drag and Drop new files.
5. Perform a Hardware Reset by pressing the PBRESET button. The system is now in the standby state.
6. Briefly press the PBON button. The system is now fully powered and in the operating state.

Note

See *3.3 Configuration files* on page 3-64 for information about the configuration files.

1.5 Accessing the ATX power cables

The N1 SDP PC tower provides SATA and other ATX power cables that you can use to connect to external hard drives. The power cables are accessed by removing the metal side panel.

——— Warning ———

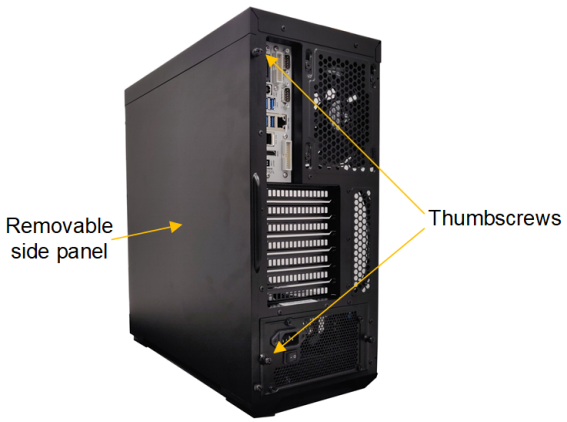
Before accessing the ATX power cables, ensure that the unit is disconnected from the mains power supply.

———————————

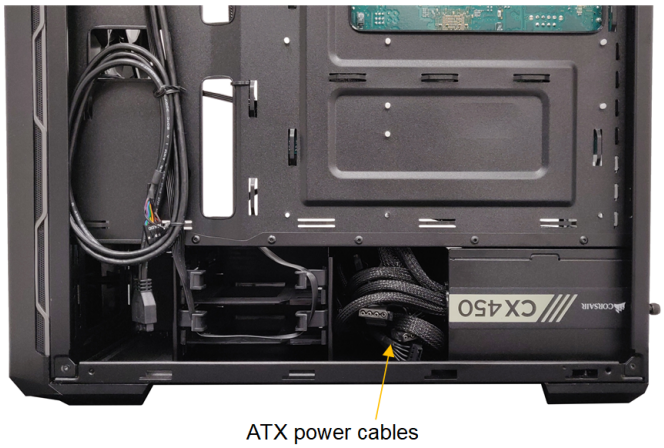
Access the ATX power cables

To access the ATX power cables, you must gain access to the chassis:

1. Remove the large metal side panel:
   - Undo the thumbscrews at the rear of the tower.
   - Slide the side panel away from the tower.



2. The ATX power cables are now accessible, folded up inside the tower. Unfold the power cables to connect them to external hard drives.



Chapter 2
Hardware description

This chapter describes the N1 SDP hardware.

It contains the following sections:

2.1 N1 SDP hardware

The support logic and peripheral interfaces of the N1 SDP support access to the N1 SoC.

Overview of the N1 SDP hardware

The following figure shows a high-level view of the system architecture.

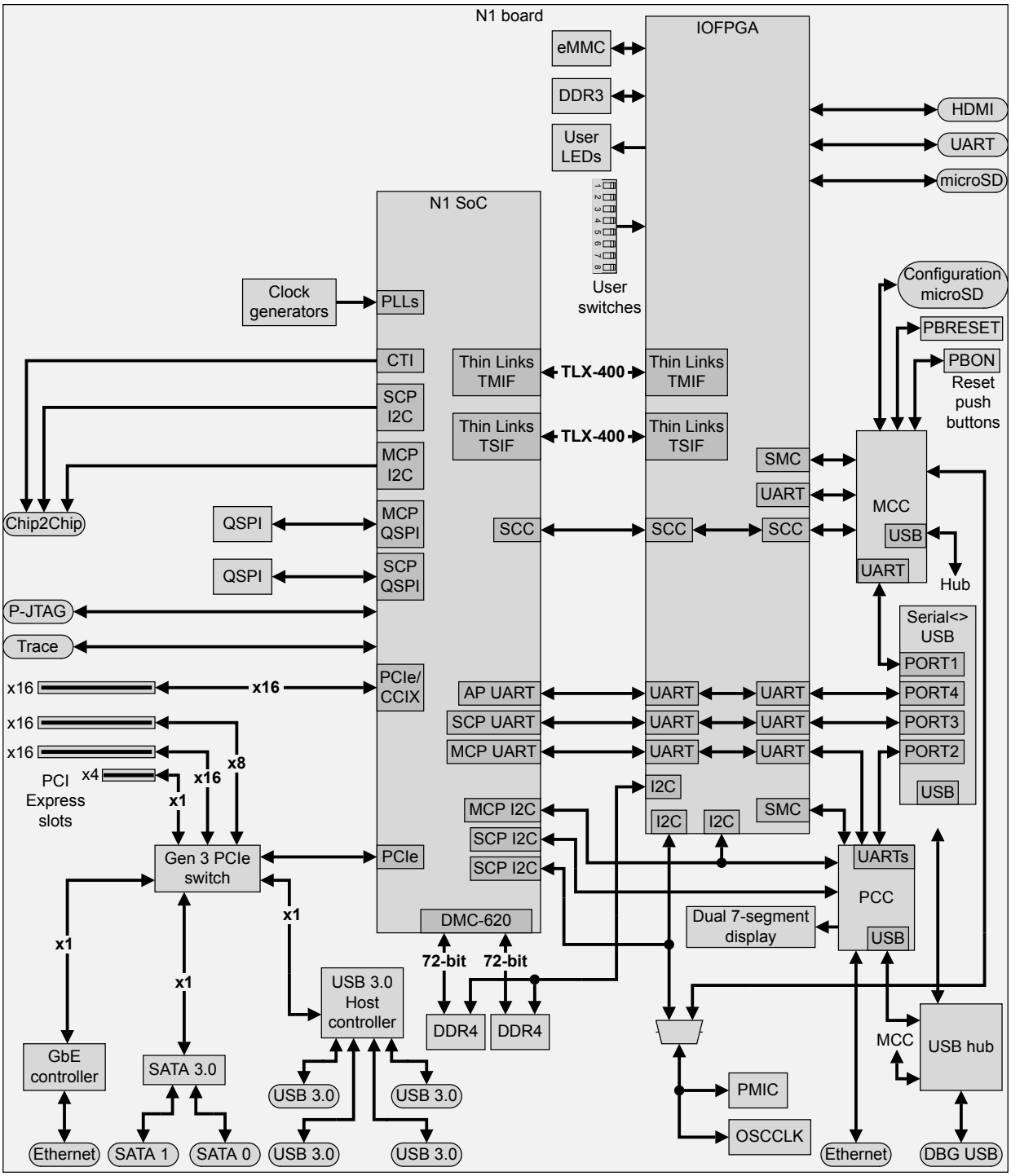


Figure 2-1 N1 SDP architecture

Note

The figure shows the default UART and USB connectivity between the components on the N1 board. The UART system is configurable using the settings in the `config.txt` file on the configuration microSD card. See the following for more information:

- *2.10 UARTs* on page 2-51.
- *3.3.2 `config.txt` board configuration file* on page 3-65.

Components and systems of the N1 SDP

The N1 SDP contains the following components and systems.

- *Motherboard Configuration Controller* (MCC):
  - Cortex-M4 based controller.
  - Controls board powerup, reset, and configuration process.
  - Controls IOFPGA configuration.
  - Enables drag and drop configuration using the DBG USB connector.
  - Always powered up.
  - *Static Memory Bus* (SMB) connection to the IOFPGA.
  - Reads temperature measurements from the N1 SoC and ambient sensors and controls cooling fans.
- *Platform Controller Chip* (PCC):
  - Cortex-M4 based controller.
  - Board and SoC management.
  - Always powered up.
  - *Static Memory Bus* (SMB) connection to the IOFPGA.
  - Dual 7-segment LED display.
- *System Control Processor* (SCP) QSPI memory.
- *Manageability Control Processor* (MCP) QSPI memory.
- DDR4 memory.
- Cache-Coherent Interconnect for Accelerators (CCIX)/PCI Express ×16 Gen 4 slot:
  - Connects to Gen 4 root complex and PHY on the N1 SoC.
- PCI Express 48-lane, 18-port, Gen 3 switch:
  - Gigabit Ethernet controller, ×1 Gen 1 link to PCIe switch.
  - SATA 3.0 controller, ×1 Gen 2 link to PCIe switch.
  - USB 3.0 controller, ×1 Gen 2 link to PCIe switch.
  - ×16 PCIe Gen 3 slot.
  - ×8 PCIe Gen 3 slot.
  - ×1 PCIe Gen 3 slot.
- Four USB 3.0 ports from USB 3.0 controller.
- Two SATA 3.0 ports from SATA 3.0 controller.
- *Chip to Chip* (C2C) connector, sideband signals for N1 SoC to N1 SoC CCIX connectivity.
- IOFPGA:
  - Low-bandwidth peripherals.
  - AXI Thin Links Master (TMIF) and Slave (TSIF) interface to the N1 SoC.
  - APB energy meter registers, for processor voltage control and current monitoring.
  - HDLCD controller, low-resolution output from the N1 cores or the PCC (boot).
  - I^2S audio from HDLCD controller.
- IOFPGA connections to N1 board:
  - HDMI connector, driven by HDLCD controller.
  - DDR3 memory.
  - eMMC, provides user boot memory image storage.
  - microSD card, provides user boot memory image storage.
  - Two UART ports (PL011).
  - System registers, Watchdog and Real Time Clock.
  - Eight user DIP switches.

  - Eight user LEDs.
  - I^3C master connector, for future external expansion.
- Two reset push buttons:
  - On/Off/Soft reset button PBON.
  - Hardware reset button, PBRESET.
- Programmable oscillators.
- JTAG debug port.
- 32-bit Trace port.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.2 N1 SoC

The following figure shows a high-level view of architecture of the N1 SoC.

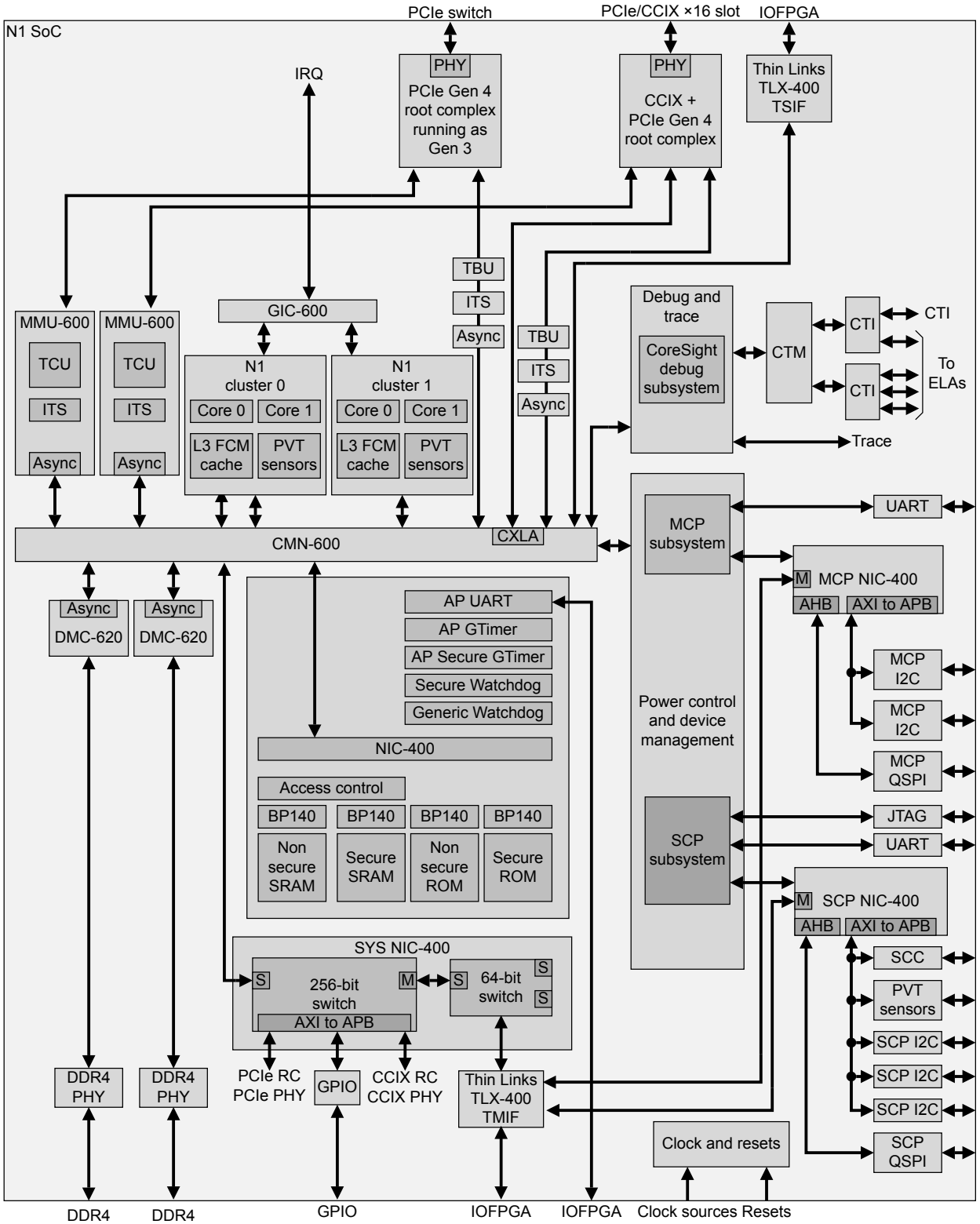


Figure 2-2 N1 SoC

Major components of the N1 SoC

The N1 SoC contains the following components and interfaces:

- Two dual-core N1 clusters. Each cluster has:
  - 64KB private L1 data cache for each core, and 64KB private L1 instruction cache for each core.
  - 1MB private L2 unified cache for each core.
  - 1MB shared L3 unified cache in the *DynamIQ Shared Unit* (DSU) *Flash Cache Module* (FCM).
- CMN-600 interconnect with *Coherent Multichip Link* (CML):
  - Runs from **INTPLLCLK** default 1.6GHz.
  - 1GHz clock, **CXSCLK** for CCIX block in CMN-600 interconnect.

  Note

  Arm recommends that you set the CMN-600 clock, **INTPLLCLK**, to 1.5GHz maximum using the SCC registers. See *2.4.3 Clock programming and control* on page 2-31, *4.5.42 INT_PLL_CTRL0 Register* on page 4-158, and *4.5.43 INT_PLL_CTRL1 Register* on page 4-159.
- Embedded Logic Analyzer (ELA) on the N1 cores and FCM DSU.
- Base element:
  - Secure region. 512KB RAM, 128KB ROM.
  - Non-secure region. 64KB RAM, 4KB ROM
- GIC-600 (GICv3).
- MMU-600 Memory Management Units.
- Cortex-M7 based internal *System Control Processor* (SCP) and *Manageability Control Processor* (MCP):
  - Secure boot, power management, and device management.
- CoreSight debug and trace.
- One *Cache-Coherent Interconnect for Accelerators* (CCIX) Gen 4 root complex and PHY:
  - Connects to one ×16 PCI Express slot.
  - Backwards compatible to PCI Express Gen 4.
- One PCIe Gen 4 root complex and PHY, running as Gen 3. Connects to the following downstream slots and peripherals through a PCI Express Gen 3 switch:
  - One ×16 PCI Express slot.
  - One ×8 PCI Express slot.
  - One ×1 PCI Express slot.
  - One ×1 Gigabit Ethernet controller.
  - One ×1 SATA 3 controller.
  - One ×1 USB 3 controller.
- Master and slave Thin Links (TLX-400) interfaces:
  - Expansion to IOFPGA on the board.
- Two 72-bit DMC-620 DDR4 controllers:
  - Support for one 288-pin RDIMM DDR4 per interface. Up to DDR4-3200 speed.
- Interfaces for AP, SCP, and MCP, routed to the *Platform Controller Chip* (PCC) on the board:
  - Three UART (PL011) interfaces.
  - Three I^2C for SCP and two I^2C interfaces for MCP.
  - Two QSPI interfaces bot bootup, one for SCP, one for MCP.
- 8-bit GPIO (PL061) for on-board I/O and interrupt.
- *Serial Configuration Controller* (SCC) interface to IOFPGA.
- *Process, Voltage, and Temperature* (PVT) sensors.
- 32-bit *Mobile Industry Process Interface* (MIPI-60) Trace port.
- JTAG debug port.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.3 External power

A mains supply in the range 100-240V AC powers the N1 SDP.

This section contains the following subsections:

2.3.1 Overview of power scheme

A standard ATX power supply unit converts the mains power to low DC voltages which power the N1 board. On-board regulators supply power to the N1 board and to the power domains of the N1 SoC.

Power LEDs indicate the active power domains. See *2.11 LEDs, switches, and buttons* on page 2-55 for information on the power LEDs.

2.3.2 Power islands

The N1 board has the following power islands:

- ATX Always-On region:
  - Operates in standby state.
  - Powers the *Motherboard Configuration Controller* (MCC) and *Platform Controller Chip* (PCC) subsystems only.
- Switched region:
  - Main board VIO and all other non-MCC and non-PCC supplies, including the IOFPGA.

This arrangement enables the PCC to receive a request to place the board into standby state over its local Ethernet connection. The following figure shows the N1 board power islands.

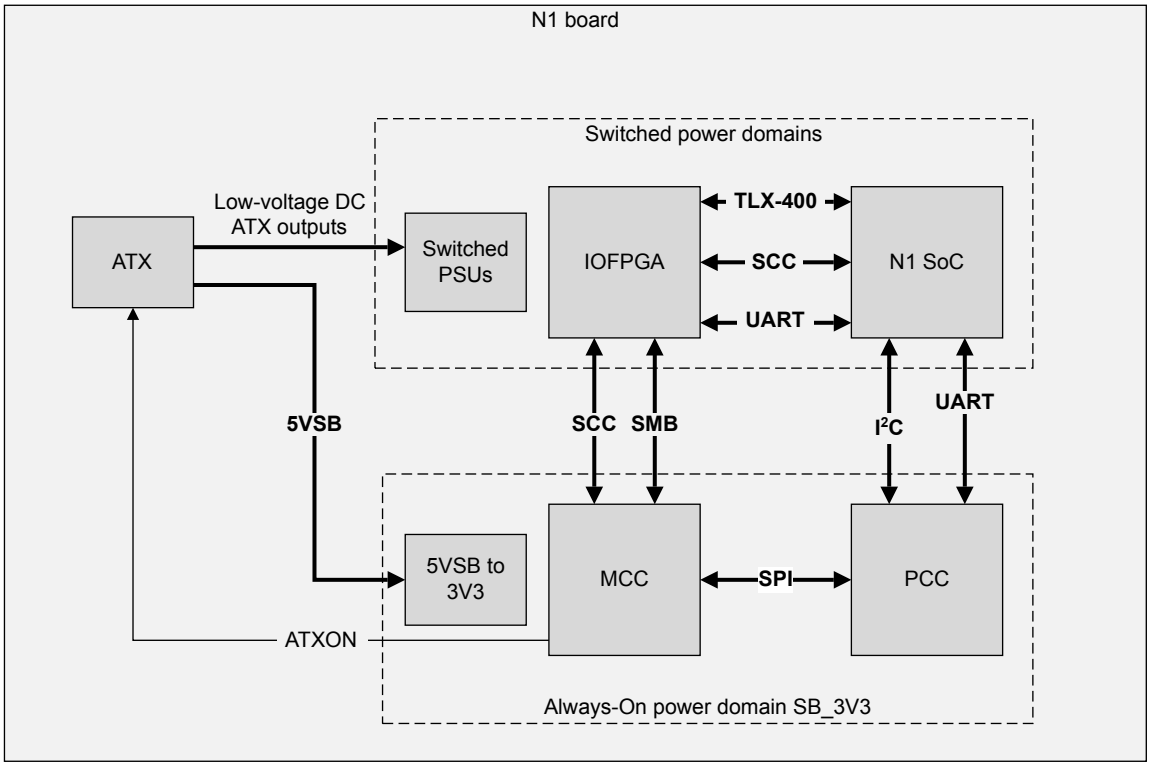


Figure 2-3 N1 board power islands

2.4 Clocks

The N1 SDP clocks drive the board and the N1 SoC.

This section contains the following subsections:

2.4.1 Overview of clocks

Programmable clock generators on the N1 board generate clocks for the board peripherals, internal blocks in the IOFPGA, and the systems in the N1 SoC.

Phase-locked loops (PLLs) generate internal clocks in the N1 SoC for the processor clusters and other systems.

During powerup or reset, the MCC programs the clock generators according to default values defined in the `io_v0.txt` configuration file. You can change the operational clock frequencies by modifying the configuration file. See *3.3.3 Contents of the `MB` directory* on page 3-65 for an example `io_v?.txt` configuration file.

Note

Arm recommends that you operate the N1 board at the default clock frequencies.

2.4.2 SoC clocks

Programmable clock generators on the N1 board drive PLLs in the N1 SoC which generate the internal N1 SoC clocks.

The following figure shows the programmable clock generators on the board, OSC0-OSC6, and the internal clocking scheme of the N1 SoC.

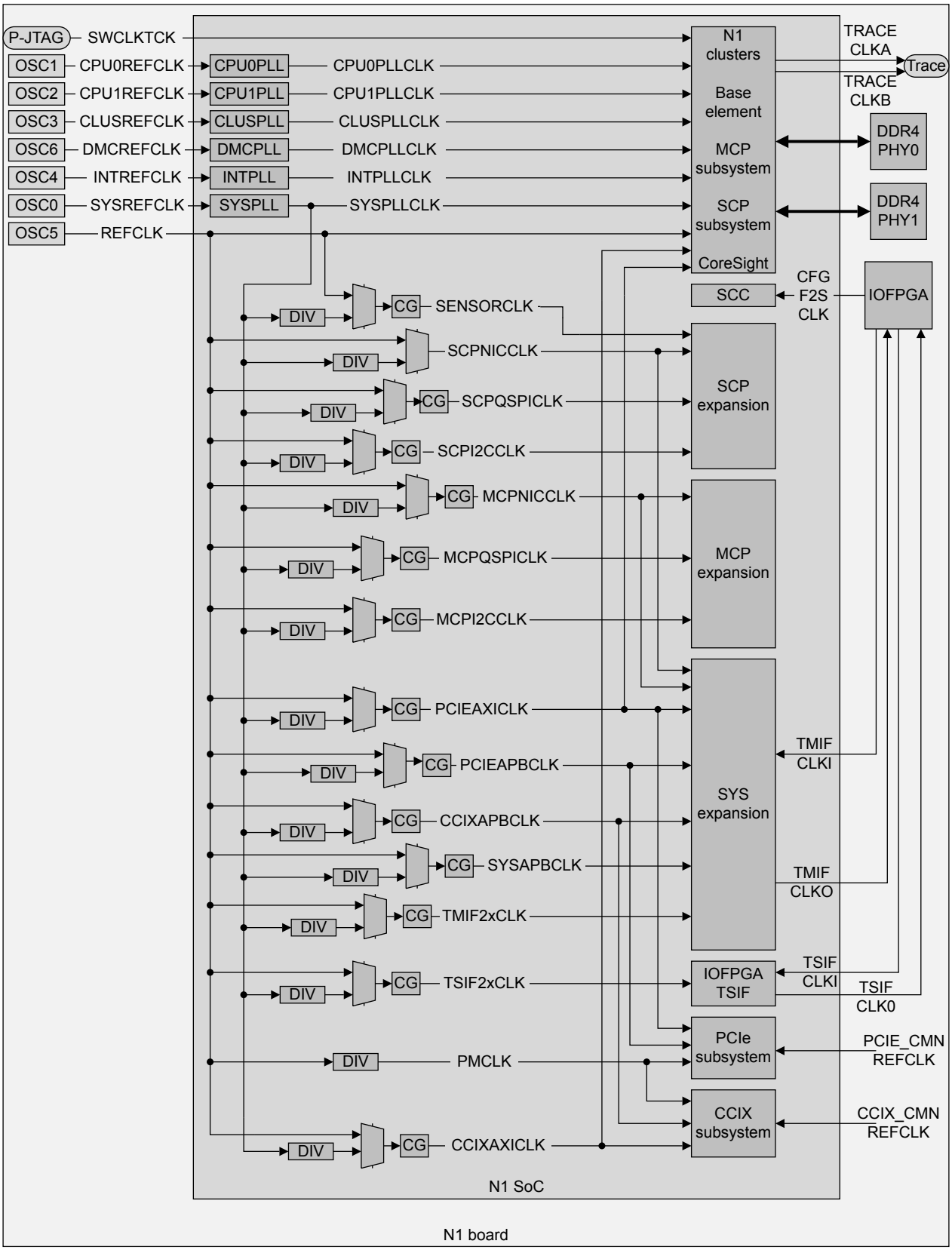


Figure 2-4 N1 SoC clocks

The *System Control Processor* (SCP) configures the PLLs, muliplexers, and dividers in the clock system during bootup.

The following table shows the N1 SoC clocks.

Note

The default clock frequencies in this table represent an example clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in other default frequencies.

Table 2-1 N1 SoC clocks

Clock	Source	Default frequency	Description
SWCLKTCK	External debugger	-	Combined P-JTAG and *Serial Wire Debug* (SWD) clock.
CPU0REFCLK	OSC1	50MHz	Reference clock for CPU0PLL. Generates **CPU0PLLCLK** for cluster 0.
CPU1REFCLK	OSC2	50MHz	Reference clock for CPU1PLL. Generates **CPU1PLLCLK** for cluster 1.
CLUSREFCLK	OSC3	50MHz	Reference clock for CLUSPLL. Generates **CLUSPLLCLK**, a common cluster clock for cluster 0 and cluster 1.
DMCREFCLK	OSC6	50MHz	Reference clock for DMCPLL. Generates **DMCPLLCLK** for the DDR subsystem.
INTREFCLK	OSC4	50MHz	Reference clock for INTPLL. Generates **INTPLLCLK** for the CMN-600 Coherent Mesh Network.
SYSREFCLK	OSC0	50MHz	Reference clock for SYSPLL. Generates the main system clock **SYSPLLCLK**, and other clocks through programmable dividers.
REFCLK	OSC5	50MHz	Always-On reference clock.
CPU0PLLCLK	CPU0PLL	2.4GHz	Cluster-specific clock for cluster 0.
CPU1PLLCLK	CPU1PLL	2.4GHz	Cluster-specific clock for cluster 1.
CLUSPLLCLK	CLUSPLL	1.6GHz	Clock for cluster 0 and cluster 1.
DMCPLLCLK	DMCPLL	1.6GHz	Clock for DDR4 subsystem.
INTPLLCLK	INTPLL	1.6GHz	CMN-600 Coherent Mesh network clock.
SYSPLLCLK	SYSPLL	2.4GHz	Main system clock.

Table 2-1 N1 SoC clocks (continued)

Clock	Source	Default frequency	Description
SENSORCLK	SYSPLL	100MHz	Sensor clock
SCPNICLK		300MHz	SCP NIC-400 clock.
SCPQSPICLK		50MHz	SCP QSPI reference clock
SCPI2CCLK		50MHz	SCP I2C clock
MCPNICCLK		300MHz	MCP NIC-400 clock.
MCPQSPICLK		50MHz	MCP QSPI reference clock
MCPI2CCLK		50MHz	MCP I2C clock
PCIEAXICLK		1.2GHz	PCIe AXI clock
PCIEAPBCLK		200MHz	PCIe APB clock
CCIXAPBCLK		200MHz	CCIX APB clock
SYSAPBCLK		120MHz	System expansion APB peripherals
TMIF2xCLK		120MHz	IOFPGA TMIF 2× clock
TSIF2xCLK		120MHz	IOFPGA TSIF 2× clock
CCIXAXICLK		1.2GHz	CCIX AXI clock
TRACECLKA	TPIU	10MHz	Trace clocks to connector
TRACECLKB			
PMCLK	OSC5, REFCLK	25MHz	Power management clock for PCIe and CCIX
CFG_F2S_CLK	MCC	10MHz	Serial Configuration Controller (SCC) interface clock. This clock is a data strobe, not a free running clock.
TMIF_CLKI	IOFPGA TLX-400 master interface	80MHz	Thin Links-based AXI master interface clock received from IOFPGA with incoming data from IOFPGA.
TMIF_CLKO	N1 SoC TLX-400 master interface	75MHz	Thin Links-based AXI master interface clock exported from N1 SoC with data transmitted from N1 SoC to IOFPGA.
TSIF_CLKI	IOFPGA TLX-400 slave interface	80MHz	Thin Links-based AXI slave interface clock received from IOFPGA with incoming data from IOFPGA.
TSIF_CLKO	N1 SoC TLX-400 slave interface	75MHz	Thin Links-based AXI slave interface clock exported from N1 SoC with data transmitted from N1 SoC to IOFPGA.
PCIE_CMN_REFCLK	Clock buffer	100MHz	Fixed differential reference clock for PCIe U-PHY
CCIX_CMN_REFCLK	Clock buffer	100MHz	Fixed differential reference clock for CCIX U-PHY
CXSCLK	CCIX PCIe PHY	1GHz	CXLA clock in CMN-600

2.4.3 Clock programming and control

The *Serial Configuration Control* (SCC) clock control registers in the N1 SoC control the clock frequencies by modifying the clock PLLs and dividers.

The PLLs generate the internal clocks from the board OSC clock generators according to the formula:

Output clock frequency = (Input clock frequency/REFDIV)×FBDIV/POSTDIV where:

- REFDIV is input frequency division value.
- FBDIV is the PLL feedback division value.
- POSTDIV is the PLL output frequency division value.

The SCC PLL control registers set the values REFDIV, FBDIV, and POSTDIV for each PLL. Other SCC registers control the clock dividers and select the inputs for the internal clocks. See *2.4.2 SoC clocks* on page 2-28.

The following table shows the SCC clock control registers.

Table 2-2 Clock control SCC registers

Register	Register function	Register description
PMCLK_DIV	Sets value of divider value to generate **PMCLK** from **REFCLK**.	See *4.5.2 PMCLK_DIV Register* on page 4-124.
SYSAPBCLK_CTRL	Selects input clock to generate **SYSAPBCLK**.	See *4.5.3 SYSAPBCLK_CTRL Register* on page 4-125.
SYSAPBCLK_DIV	Sets value of divider value to generate **SYSAPBCLK** from **SYSPLLCLK**.	See *4.5.4 SYSAPBCLK _DIV Register* on page 4-126.
TMIF2XCLK_CTRL	Selects input clock to generate **TMIF2XCLK**.	See *4.5.5 IOFPGA_TMIF2XCLK_CTRL Register* on page 4-127.
TMIF2XCLK_DIV	Sets value of divider value to generate **TMIF2XCLK** from **SYSPLLCLK**.	See *4.5.6 IOFPGA_TMIF2XCLK_DIV Register* on page 4-128.
TSIF2XCLK_CTRL	Selects input clock to generate **TSIF2XCLK**.	See *4.5.7 IOFPGA_TSIF2XCLK_CTRL Register* on page 4-128.
TSIF2XCLK_DIV	Sets value of divider value to generate **TSIF2XCLK** from **SYSPLLCLK**.	See *4.5.8 IOFPGA_TSIF2XCLK_DIV Register* on page 4-129.
SCPNICCLK_CTRL	Selects input clock to generate **SCPNICLK**.	See *4.5.9 SCPNICCLK_CTRL Register* on page 4-130.
SCPNICCLK_DIV	Sets value of divider value to generate **SCPNICCLK** from **SYSPLLCLK**.	See *4.5.10 SCPNICCLK_DIV Register* on page 4-131.
SCPI2CCLK_CTRL	Selects input clock to generate **SCPI2CCLK**.	See *4.5.11 SCPI2CCLK_CTRL Register* on page 4-131.
SCPI2CCLK_DIV	Sets value of divider value to generate **SCPI2CCLK** from **SYSPLLCLK**.	See *4.5.12 SCPI2CCLK_DIV Register* on page 4-132.
SCPQSPICLK_CTRL	Selects input clock to generate **SCPQSPICLK**.	See *4.5.13 SCPQSPICLK_CTRL Register* on page 4-133.
SCPQSPICLK_DIV	Sets value of divider value to generate **SCPQSPICLK** from **SYSPLLCLK**.	See *4.5.14 SCPQSPICLK_DIV Register* on page 4-134.
SENSORCLK_CTRL	Selects input clock to generate **SENSORCLK**.	See *4.5.15 SENSORCLK_CTRL Register* on page 4-134.
SENSORCLK_DIV	Sets value of divider value to generate **SENSORCLK** from **SYSPLLCLK**.	See *4.5.16 SENSORCLK_DIV Register* on page 4-135.
MCPNICCLK_CTRL	Selects input clock to generate **MCPNICCLK**.	See *4.5.17 MCPNICCLK_CTRL Register* on page 4-136.
MCPNICCLK_DIV	Sets value of divider value to generate **MCPNICCLK** from **SYSPLLCLK**.	See *4.5.18 MCPNICCLK_DIV Register* on page 4-137.

Table 2-2 Clock control SCC registers (continued)

Register	Register function	Register description
MCPI2CCLK_CTRL	Selects input clock to generate **MCPI2CCLK**.	See *4.5.19 MCPI2CCLK_CTRL Register* on page 4-137.
MCPI2CCLK_DIV	Sets value of divider value to generate **MCPI2CCLK** from **SYSPLLCLK**.	See *4.5.20 MCPI2CCLK_DIV Register* on page 4-138.
MCPQSPICLK_CTRL	Selects input clock to generate **MCPQSPICLK**.	See *4.5.21 MCPQSPICLK_CTRL Register* on page 4-139.
MCPQSPICLK_DIV	Sets value of divider value to generate **MCPQSPICLK** from **SYSPLLCLK**.	See *4.5.22 MCPQSPICLK_DIV Register* on page 4-140.
PCIEAXICLK_CTRL	Selects input clock to generate **PCIEAXICLK**.	See *4.5.23 PCIEAXICLK_CTRL Register* on page 4-140.
PCIEAXICLK_DIV	Sets value of divider value to generate **PCIEAXICLK** from **SYSPLLCLK**.	See *4.5.24 PCIEAXICLK_DIV Register* on page 4-141.
CCIXAXICLK_CTRL	Selects input clock to generate **CCIXAXICLK**.	See *4.5.25 CCIXAXICLK_CTRL Register* on page 4-142.
CCIXAXICLK_DIV	Sets value of divider value to generate **CCIXAXICLK** from **SYSPLLCLK**.	See *4.5.26 CCIXAXICLK_DIV Register* on page 4-143.
PCIEAPBCLK_CTRL	Selects input clock to generate **PCIEAPBCLK**.	See *4.5.27 PCIEAPBCLK_CTRL Register* on page 4-143.
PCIEAPBCLK_DIV	Sets value of divider value to generate **PCIEAPBCLK** from **SYSPLLCLK**.	See *4.5.28 PCIEAPBCLK_DIV Register* on page 4-144.
CCIXAPBCLK_CTRL	Selects input clock to generate **CCIXAPBCLK**.	See *4.5.29 CCIXAPBCLK_CTRL Register* on page 4-145.
CCIXAPBCLK_DIV	Sets value of divider value to generate **CCIXAPBCLK** from **SYSPLLCLK**.	See *4.5.30 CCIXAPBCLK_DIV Register* on page 4-146.
SYS_CLK_EN	Enables or disables internally generated clocks.	See *4.5.31 SYS_CLK_EN Register* on page 4-146.
CPU0_PLL_CTRL0	Control CPU0PLL to generate **CPU0PLLCLK**.	See *4.5.32 CPU0_PLL_CTRL0 Register* on page 4-148.
CPU0_PLL_CTRL1		See *4.5.33 CPU0_PLL_CTRL1 Register* on page 4-149.
CPU1_PLL_CTRL0	Control CPU1PLL to generate **CPU1PLLCLK**.	See *4.5.34 CPU1_PLL_CTRL0 Register* on page 4-150.
CPU1_PLL_CTRL1		See *4.5.35 CPU1_PLL_CTRL1 Register* on page 4-151.
CLUS_PLL_CTRL0	Control CLUSPLL to generate **CLUSPLLCLK**.	See *4.5.36 CLUS_PLL_CTRL0 Register* on page 4-152.
CLUS_PLL_CTRL1		See *4.5.37 CLUS_PLL_CTRL1 Register* on page 4-153.
SYS_PLL_CTRL0	Control SYSPLL to generate **SYSPLLCLK**.	See *4.5.38 SYS_PLL_CTRL0 Register* on page 4-154.
SYS_PLL_CTRL1		See *4.5.39 SYS_PLL_CTRL1 Register* on page 4-155.
DMC_PLL_CTRL0	Control DMCPLL to generate **DMCPLLCLK**.	See *4.5.40 DMC_PLL_CTRL0 Register* on page 4-156.
DMC_PLL_CTRL1		See *4.5.41 DMC_PLL_CTRL1 Register* on page 4-157.
INT_PLL_CTRL0	Control INTPLL to generate **INTPLLCLK**.	See *4.5.42 INT_PLL_CTRL0 Register* on page 4-158.
INT_PLL_CTRL1		See *4.5.43 INT_PLL_CTRL1 Register* on page 4-159.

2.4.4 IOFPGA clocks

Programmable clock generators on the N1 board generate clocks for the internal systems of the IOFPGA.

The IOFPGA Thin Links interfaces generate clocks for data transmitted to the N1 SoC interfaces. The IOFPGA also generates the *Serial Configuration Controller* (SCC) clock data strobe.

The following table shows the IOFPGA clocks.

Table 2-3 IOFPGA clocks

Clock	Source	Frequency	Description
IOFPGA_ACLK	OSC9	60MHz	Boot up clock. Drives IOFPGA OSC0.
IOFPGA_TLXCLK	OSC8	80MHz	IOFPGA Thin Links
IOFPGA_PXLCLK	OSC7	23.75MHz	Drives HDLCDPLL. Low-performance pixel clock output, range 25-100MHz.
IOFPGA_AUDCLK	OSC10	24.576MHz	Drives audio clock **I2SCLK**.
IOFPGA_CLK24M	FPGA_CLK24M	24MHz	Drives MMCM at 100MHz.
IOFPGA_RSVD	OSC11	24MHz	Reserved
S32KCLK	CLK_32K	32.768kHz	Standalone clock for *Real Time Clock* (RTC)
IOFPGA_DDR3_SYSCLK	GTX clock	100MHz	Drives DDR3 controller reference clock at 400MHz.
Thin Links-based AXI master and slave interface clocks between IOFPGA and N1 SoC.	-	75MHz from N1 SoC to IOFPGA. 80MHz from IOFPGA to N1 SoC.	See *2.4.2 SoC clocks* on page 2-28 for descriptions of Thin Links clocks.
SMBM_CLK	MCC	40MHz	SMB clock
SMBP_CLK	PCC	40MHz	SMB clock
CFG_M2F_CLK	MCC	10MHz	Serial Configuration Controller (SCC) interface clock. This clock is a data strobe, not a free running clock.
CFG_CLK	IOFPGA SCC interface	25MHz	Serial Configuration Controller (SCC) interface clock. This clock is a data strobe, not a free running clock.
PCIE_CMN_REFCLK	Clock buffer	100MHz	Fixed differential reference clock for PCIe U-PHY
CCIX_CMN_REFCLK	Clock buffer	100MHz	Fixed differential reference clock for CCIX U-PHY

2.5 Resets

The N1 SDP provides reset signals for the N1 board and N1 SoC.

N1 board resets

The N1 board has the following resets.

Table 2-4 N1 board resets

Reset	Source	Target	Comment
nPBRESET	Powerup reset. Hardware reset user push button PBRESET.	*Motherboard Configuration Controller* (MCC) and entire board	Main board powerup reset and hard reset from the user hardware reset push button. The entire system goes to standby state.
UART0_DSR	External device	MCC and entire board	Remote UART reset. Must be enabled by use of configuration switch SW1. See *2.11.5 Push buttons and switches* on page 2-57.
CB_CFGnRST	MCC	*Platform Controller Chip* (PCC) and entire board	The MCC controls the PCC reset.
IOFPGA_nPOR	MCC	IOFPGA, powerup reset sections.	Enables the IOFPGA internal PLLs to be reset and become stable before release of logic reset.
IOFPGA_nRST	MCC	IOFPGA logic, internal blocks.	Resets main IOFPGA logic blocks.
nPBON	On/Off/Soft reset user push button PBON	MCC and PCC	Push button to power up. By default, this button powers up the system in standby mode. **nPBON** generates an interrupt to either the MCC or PCC to control the powerup sequence.

N1 SoC resets

The N1 SoC has the following resets from the board.

Table 2-5 N1 SoC resets

Reset	Source	Comment
SOC_nPOR	MCC, IOFPGA.	Main powerup reset for the whole system except some SCC logic. De-assertion of this input initiates the powerup sequence.
SOC_nSRST	MCC/IOFPGA/external debug unit.	Debug through reset signal. This signal enables the debug tools to debug Cortex-M7 (SCP, MCP) and the N1 (AP) before the processors leave reset.
nTRST	External debug unit	JTAG reset. Resets the CoreSight DAP.
CFG_nRST	MCC through IOFPGA	Reset signal for the serial interface to the *System Configuration Controller* (SCC).

Reset sequence

The system can operate in two modes:

- Mobile mode:
  - The board and SCP are brought up by the MCC alone.
- Enterprise mode:
  - The MCC brings the board up to standby state and is then under the control of the PCC.

The following figure shows the board and SoC reset sequence.

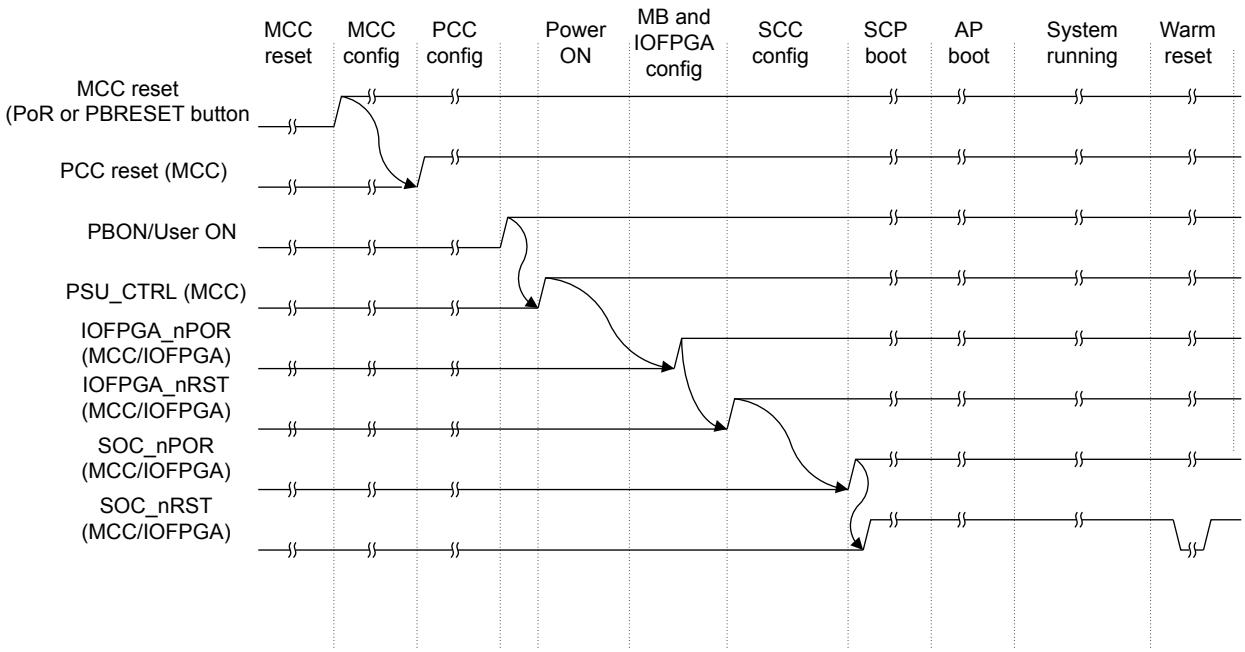


Figure 2-5 Reset sequence

Related information

1.3 The N1 SDP at a glance on page 1-14

2.6 IOFPGA

The IOFPGA provides access to low-bandwidth peripherals that the N1 SoC does not provide. The N1 SoC connects to the IOFPGA through an AXI Thin Links (TLX-400) master and slave interfaces.

This section contains the following subsections:

2.6.1 Overview of IOFPGA

The IOFPGA on the N1 board contains the following blocks and interfaces:

- eMMC device.
- microSD card controller.
- QSPI controller.
- DDR3 controller.
- PL031 *Real Time Clock* (RTC).
- SP804 Timers.
- SP805 Watchdog.
- SP810 System controller.
- PL011 UARTs.
- GIC-400 interrupt controller.
- 1MB SRAM.
- I^2C configuration of PCIe switch and HDMI PHY.
- HDLCD.
- APB mapping to user LEDs and switches.
- APB-mapped energy meter registers.

The following figure shows the internal architecture of the IOFPGA and its connectivity to external peripherals, the N1 SoC, the MCC, and the PCC.

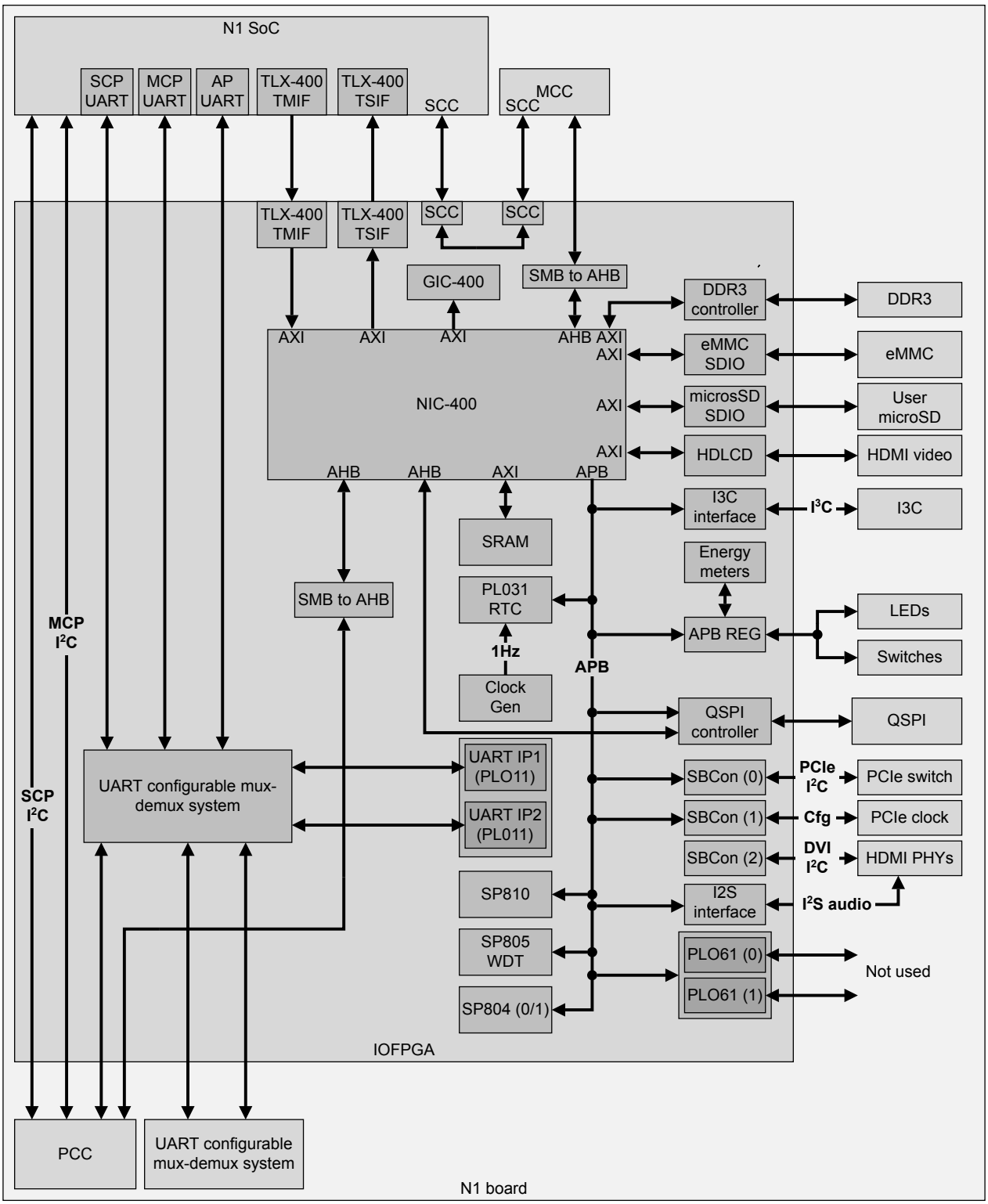


Figure 2-6 IOFPGA internal architecture

Note

The UART system in the IOFPGA and N1 SoC is configurable using the settings in the `config.txt` file. See the following for information on the UART system, and on configuring the UART system.

- *2.10 UARTs* on page 2-51.
- *3.3.2 `config.txt` board configuration file* on page 3-65.

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2.6.2 IOFPGA interrupts

The N1 SoC implements an Arm CoreLink GIC-600 Generic Interrupt Controller.

The IOFPGA implements an Arm CoreLink GIC-400 Generic Interrupt Controller. The IOFPGA:

- Merges the functional interrupts from its internal blocks, and from four external blocks, into three interrupts to the *Application Processor* (AP), *System Control Processor* (SCP, and the *Manageability Control Processor* (MCP), in the N1 SoC.
- Implements a set of interrupt memory mapped registers accessible by the *Application Processors* (AP) over the Thin Links TXL-400 interface to determine the interrupt source. The base address of the interrupt memory mapped registers is `0x1CA0_0000`.

The IOFPGA interrupts are separately combined and driven to the *Platform Controller Chip* (PCC) and *Motherboard Configuration Controller* (MCC).

See *Arm® CoreLink™ GIC-400 Generic Interrupt Controller Technical Reference Manual* for information on the GIC-400 interrupt controller.

The following figure shows the IOFPGA interrupt routing.

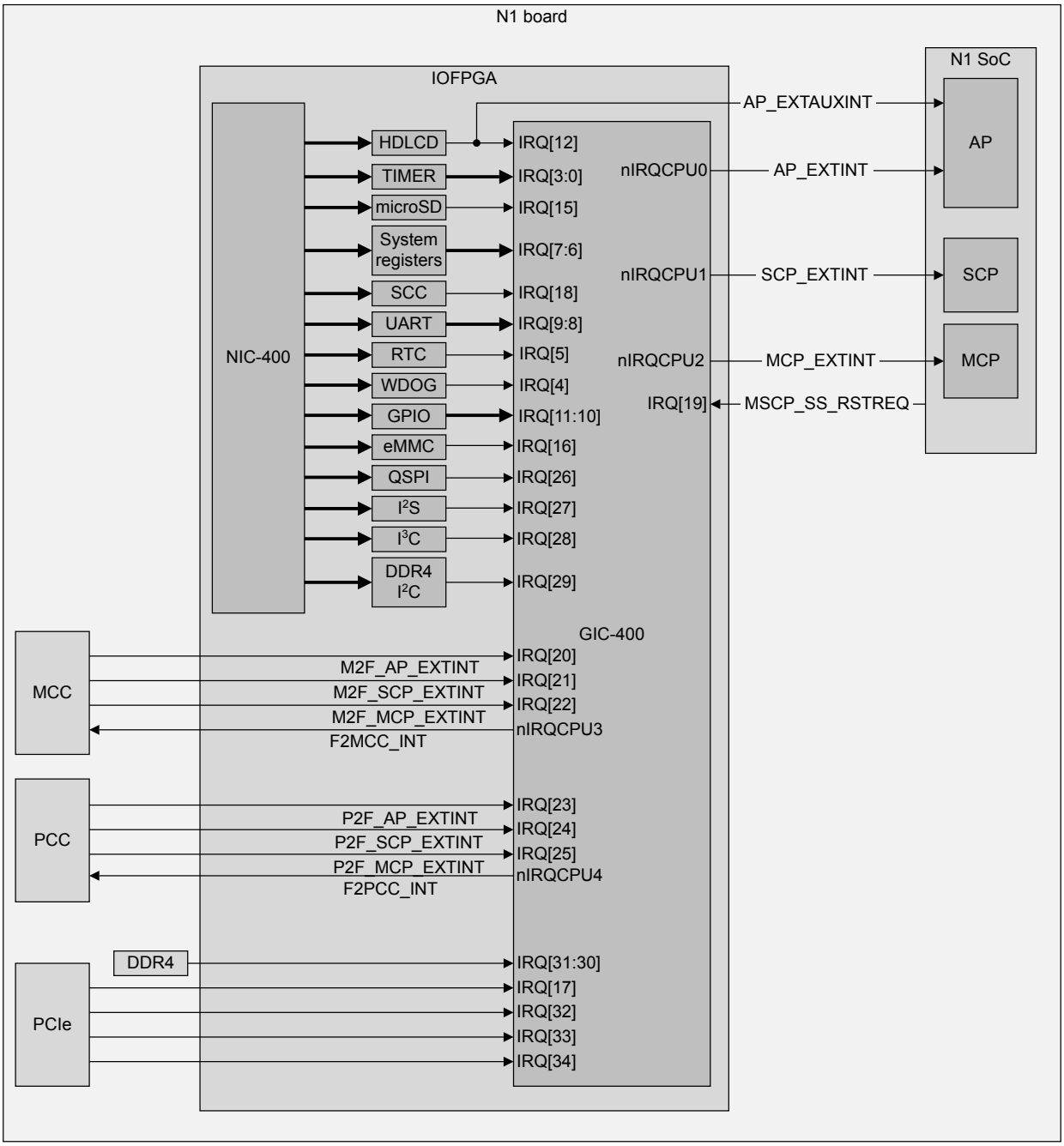

Figure 2-7 IOFPGA interrupt routing

The following table shows the input interrupts to the GIC-400.

Table 2-6 IOFPGA GIC-400 interrupt sources

Interrupt ID	IRQ level	Source	Comment
IRQ[0]	1	Timer 0	-
IRQ[1]	1	Timer 1	-
IRQ[2]	1	Timer 2	-

Table 2-6 IOFPGA GIC-400 interrupt sources (continued)

Interrupt ID	IRQ level	Source	Comment
IRQ[3]	1	Timer 3	-
IRQ[4]	1	Watchdog	-
IRQ[5]	1	Real Time Clock	-
IRQ[6]	1	CFGINT (System)	-
IRQ[7]	1	FUNINT (System)	-
IRQ[8]	1	UART 0	-
IRQ[9]	1	UART 1	-
IRQ[10]	1	GPIO 0	-
IRQ[11]	1	GPIO 1	-
IRQ[12]	1	HDLCD	-
IRQ[13]	-	Reserved	-
IRQ[14]	-	Reserved	-
IRQ[15]	1	User microSD	-
IRQ[16]	1	eMMC	-
IRQ[17]	0	PCIe Switch	-
IRQ[18]	1	CFGINT (SCC)	-
IRQ[19]	1	MSCP_SS_RSTREQ	From N1 SoC
IRQ[20]	1	M2F_AP_EXTINT	MCC to AP
IRQ[21]	1	M2F_SCP_EXTINT	MCC to SCP
IRQ[22]	1	M2F_MCP_EXTINT	MCC to MCP
IRQ[23]	1	P2F_AP_EXTINT	PCC to AP
IRQ[24]	1	P2F_SCP_EXTINT	PCC to SCP
IRQ[25]	1	P2F_MCP_EXTINT	PCC to MCP
IRQ[26]	1	QSPI	-
IRQ[27]	1	I^2S	-
IRQ[28]	1	I^3C	-
IRQ[29]	1	DDR4 EEPROM I^2C	-
IRQ[30]	0	DDR4_nEVENT0	-
IRQ[31]	0	DDR4_nEVENT1	-
IRQ[32]	0	PCIe_nWAKE	-
IRQ[33]	0	CCIX-nWAKE>	-
IRQ[34]	0	FATAL_ERRn from PCIe switch.	-

The following table shows the output interrupts from the GIC-400 to blocks in the N1 SoC and the N1 board.

Table 2-7 IOFPGA output interrupts

Interrupt ID	Target	Comment
nIRQCPU0	*Application Processors* (AP)	N1 SoC
nIRQCPU1	*System Control Processor* (SCP)	N1 SoC
nIRQCPU2	*Manageability Control Processor* (MCP)	N1 SoC
nIRQCPU3	*Motherboard Configuration Controller* (MCC)	N1 board
nIRQCPU4	*Platform Controller Chip* (PCC)	N1 board

2.7 HDLCD video

An Arm HDLCD controller in the IOFPGA and an HDMI transmitter on the N1 board provide video graphics.

The controller is a simple frame buffer which supports all common 24-bit RGB formats. The design supports XGA 1024×768kHz, 50-60Hz, compatible with major Linux distributions GUI installation interfaces.

The IOFPGA implements a single DDR3 ×16 interface operating at 400MHz that acts as a local frame buffer.

The pixel clock is derived from a clock generator on the N1 board and a PLL in the IOFPGA.

The RGB video connects to GPIO drivers in the IOFPGA that drive the HDMI transmitter, PHY, at up to 120MHz. The PHY is a TDA19988 HDMI transmitter which drives the HDMI connector. The *Application Processor* (AP) code configures the HDLCD controller and the *Motherboard Configuration Controller* (MCC) or AP configures the PHY over I^2C from the IOFPGA.

The following figure shows the HDLCD video system on the N1 SDP.

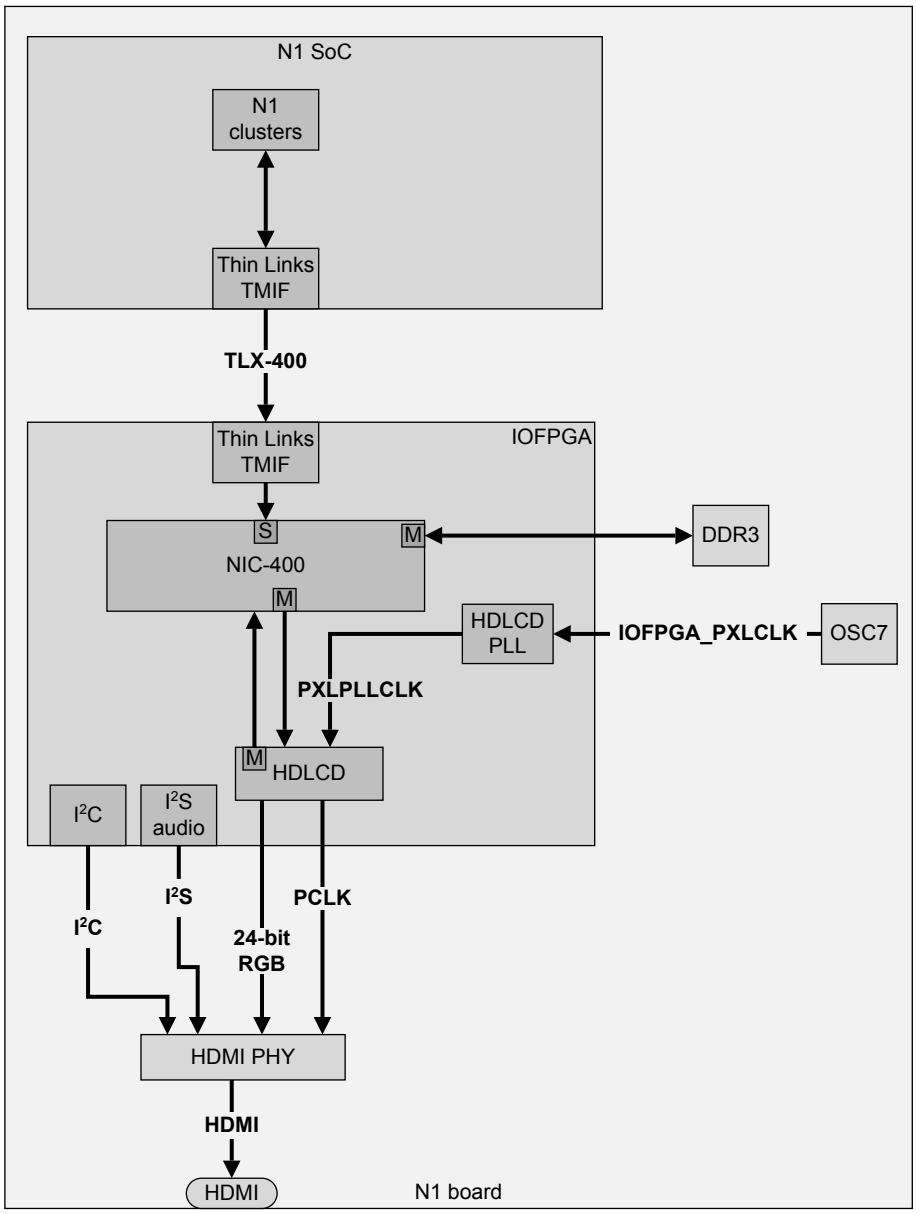

Figure 2-8 HDLCD interface

Related information

1.3 The N1 SDP at a glance on page 1-14

2.8 PCI Express and CCIX systems

The N1 SDP provides PCI Express Gen 4, and *Cache-Coherent Interconnect for Accelerators* (CCIX) expansion.

This section contains the following subsections:

2.8.1 Overview of PCIe and CCIX systems

The N1 SoC provides two PCI Express Gen 4, 16Gbps, independent interfaces. One of the interfaces supports *Cache-Coherent Interconnect for Accelerators* (CCIX) technology. The N1 SoC and N1 board provide the *Chip to Chip* (C2C) sideband signals necessary for CCIX expansion. The CCIX interface also functions as a standard PCIe Gen 4 interface.

One Gen 4 root complex on the N1 SoC connects directly to a Gen 3 switch. Downstream of the switch provides access to three PCIe slots, a four-port USB 3.0 Host Controller, a two-port SATA controller, and one Gigabit Ethernet port.

The other Gen 4 root complex on the N1 SoC provides access through one ×16 CCIX slot which also functions as a standard PCIe Gen 4 interface. The C2C port provides the CCIX sideband signals.

The following figure shows the N1 SDP.

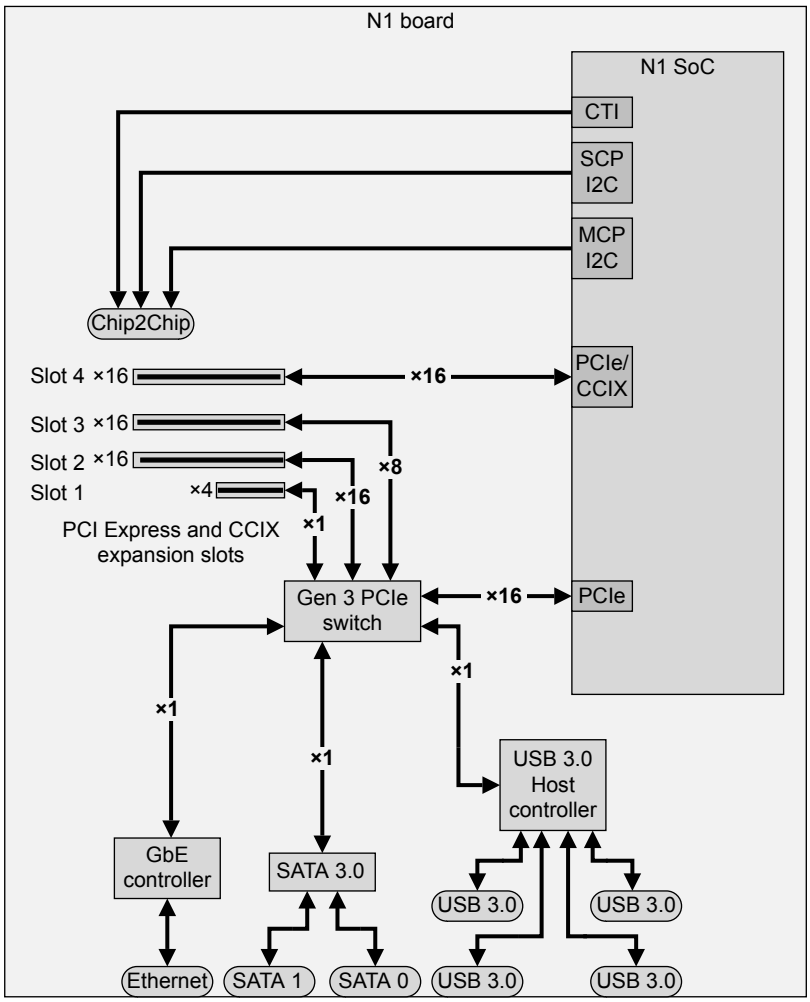

Figure 2-9 PCI Express and CCIX systems

The GbE, USB 3.0, and C2C connectors are accessible on the back panel. The PCIe and CCIX slots, and the SATA ports, are accessible by removing the side panel. See*1.3 The N1 SDP at a glance* on page 1-14.

2.8.2 PCI Express and CCIX expansion slots

The following table shows the PCIe expansion slots on the N1 board.

Table 2-8 PCI Express expansion slots

Slot number	PCIe lane connector size	Number of lanes connected	Unused lanes	Comment
Slot 1	×4	1	3	PCIe
Slot 2	×16	16	0	PCIe
Slot 3	×16	8	8	PCIe
Slot 4	×16	16	0	PCIe CCIX dual-use

Note

- Using slot 2 as the ×16 slot:

  - Enables use of a double slot 150W/300W card which covers slot 3 and makes it unusable.
  - Enables use of a double slot card in slot 1.
- It is not possible to simultaneously use a ×16 Triple-slot card in slot 2 and a ×16 lane CCIX in slot 3.

2.8.3 SATA 3.0 ports

The PCIe switch connects to the SATA 3.0 controller over a ×1 PCIe link.

The SATA 3.0 controller drives two SATA 3.0 ports for hard drives:

- The SATA 3.0 is a Marvell 88SE9170 SATA 3.0 controller with a ×1 Gen 2 link to the PCIe switch.
- The connections between the SATA 3.0 ports and the SATA 3.0 controller have a Serial ATA Generation 3 transfer rate of 6Gbps.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.8.4 Gigabit Ethernet port

The PCIe switch connects to the *Gigabit Ethernet* (GbE) controller over a ×1 Gen 1.1 link.

The GbE controller drives an RJ45 GbE port on the back panel.

- The GbE controller is a RealTek RTL8111GS device.
- The controller provides a 10/100/1000Base-T connection to the GbE port.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.8.5 USB 3.0 ports

The PCI switch connects to a USB 3.0 Host controller over a single-lane PCIe Gen 2 link.

The USB 3.0 Host controller drives four USB 3.0 ports on the back panel:

- The USB 3.0 controller is a Texas Instruments TUSB7340IRKMT device with a Gen 2 link to the PCIe switch.
- The controller operates at USB 3.0, 5Gbps, and is backwards compatible with USB 2.0, 480Mbps.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.9 Chip to Chip communications

Certain connections between master and slave systems are necessary to enable *Cache-Coherent Interconnect* (CCIX) between two N1 SoCs.

Chip to Chip Sideband signals

Various sideband, *Chip to Chip* (C2C), signals are necessary to enable *Cache-Coherent Interconnect* (CCIX) between two N1 SoCs. The N1 System Development Platform connects these sideband signals to a 20-pin *Chip to Chip* (C2C) connector on the back panel. A ribbon cable connects the master and slave N1 System Development Platforms.

C2C interfaces

The sideband interfaces which must be through connected through the C2C connectors are:

- *Cross Trigger Interface* (CTI).
- System counter synchronization.
- **REFCLK** handshaking synchronization.
- SCP I^2C.
- MCP I^2C.
- CoreSight debug JTAG.

The following figure shows the CTI and synchronization signals.

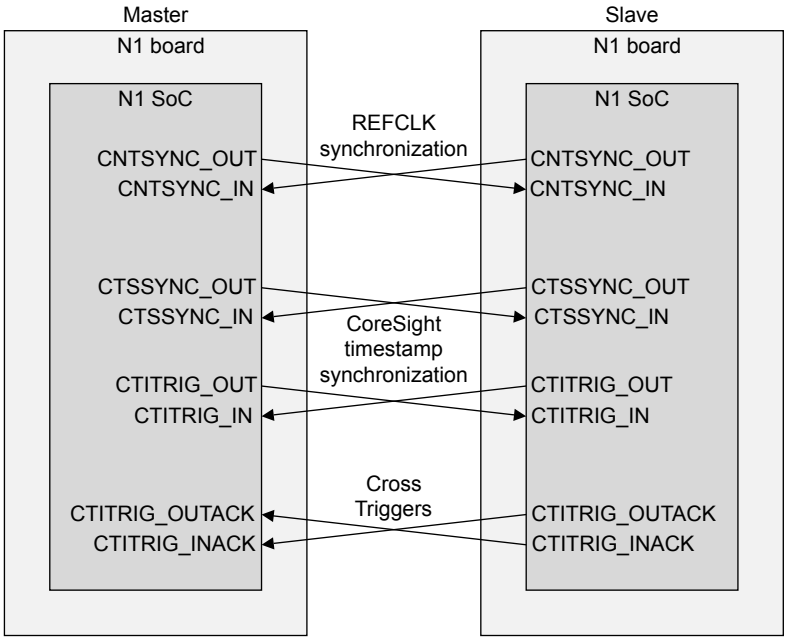

Figure 2-10 CTI and synchronization signals

The following figure shows the C2C SCP and MCP I^2C connections.

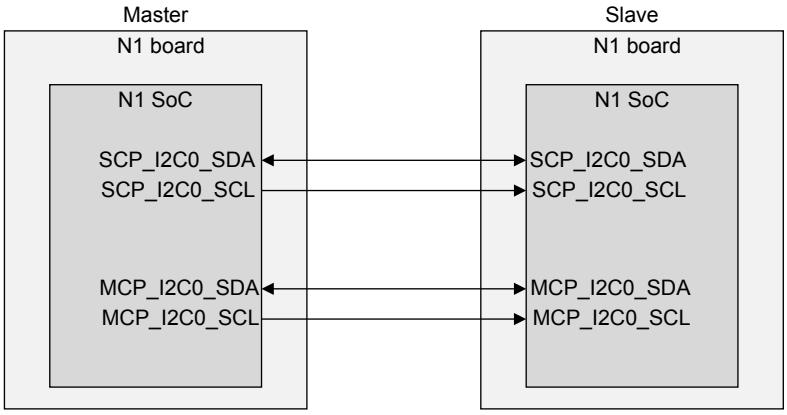

Figure 2-11 C2C SCP and MCP I²C connections

Chip to Chip powerup synchronization

To enable C2C powerup synchronization, the N1 boards must be connected together with the following cables:

- 20-pin ribbon cable connecting the C2C connectors on the back panel.
- PCIe adapter cable for the PCIe links, for example, OSS adapter card.

The MCC microSD card must be configured with the master or slave C2C option.

The powerup sequence is:

1. MCC powers up and reads the C2C and master-slave configurations in the microSD card.
2. MCC reads the C2C_PRESENT input pin, on the C2C connector, to determine the power state of the other system.
3. MCC on the slave side enables the I2C register pullups.
4. MCC updates the SCC registers in the IOFPGA with CHIP_ID and multi-chip support.
5. MCC releases the N1 SoC from reset.
6. The SCP or MCP reads the SCC registers and configures the CCIX root port appropriately:
   - CCIX root complex, master.
   - CCIX endpoint, slave.

   This sequence includes several layers of PCIe and CCIX bring-up across the links to verify the root complex register configurations, set up the links, and initiate virtual-channel support to enable CCIX traffic.

C2C connector ribbon cable

The following table shows the C2C ribbon cable wiring and connectivity between the two connected N1 System Development Platforms.

Table 2-9 C2C connector wiring

Master N1 System Development Platform		Slave N1 System Development Platform	
Pin	Signal	Pin	Signal
1	**SCP_SCL**	1	**SCP_SCL**
2	**SCP_SDA**	2	**SCP_SDA**
3	**GND**	3	**GND**
4	**MCP_SCL**	4	**MCP_SCL**

Table 2-9 C2C connector wiring (continued)

Master N1 System Development Platform		Slave N1 System Development Platform	
5	**MCP_SDA**	5	**MCP_SDA**
6	**PRESENT_IN**	20	**PRESENT_OUT**
7	**GND**	7	**GND**
8	**CTITRIGIN**	18	**CTITRIGOUT**
9	**CTITRIGOUTACK**	17	**CTITRIGINACK**
10	**GND**	10	**GND**
11	**GCNTSYNC_IN**	15	**GCNTSYNC_OUT**
12	**CTSSYNC_IN**	14	**CTSSYNC_OUT**
13	**GND**	13	**GND**
14	**CTSSYNC_OUT**	12	**CTSSYNC_IN**
15	**GCNTSYNC_OUT**	11	**GCNTSYNC_IN**
16	**GND**	16	**GND**
17	**CTITRIGINACK**	9	**CTITRIGOUTACK**
18	**CTITRIGOUT**	8	**CTITRIGIN**
19	**GND**	19	**GND**
20	**PRESENT_OUT**	6	**PRESENT_IN**

Connection between CCIX slots on the master and slave N1 boards

The following are necessary to enable CCIX traffic between the two N1 boards:

- The master exports **REFCLK**.
- The slave is configured to accept **REFCLK** from the master and distribute it locally.
- The slave detects the PCIe reset **nPERST** from the master for the System Control Processor (SCP) to release the local PCIe internal reset. This is done by driving **nPERST** from the slave into one of the SoC GPIO pins. The GPIO is configured to generate an interrupt to the SCP.

Arm supplies adapter boards and connector cables for the master and slave CCIX slots.

2.10 UARTs

The N1 SDP UART system enables access to the N1 SoC and IOFPGA on the N1 board.

Overview of UART system

The following figure shows the N1 SDP UART system and indicates the default and non-default connectivity settings.

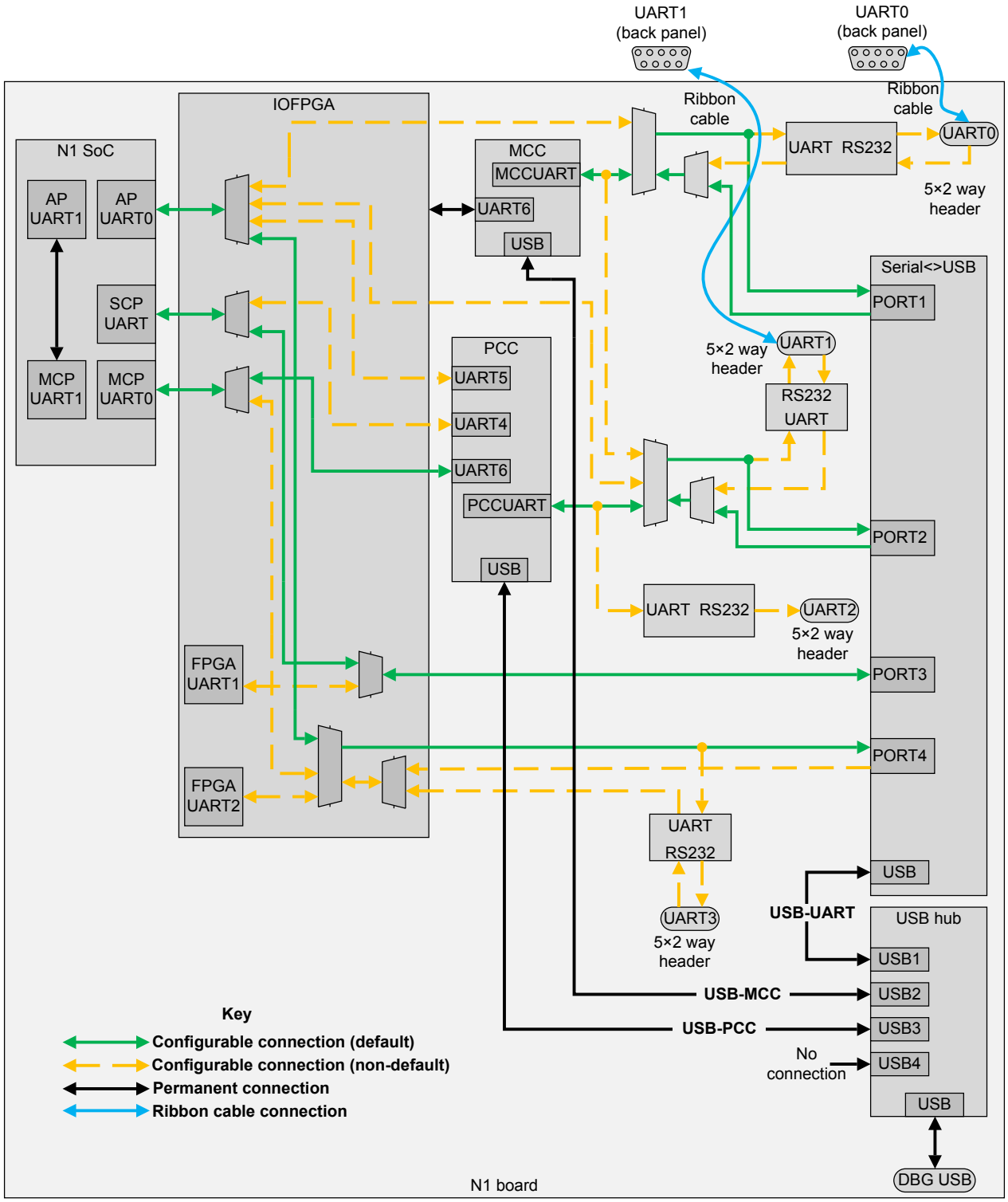

Figure 2-12 UART system

Note

APUART1 is used to communicate through MCPUART1 internally within the SoCand is accessible to the *Application Processor* (AP) cores. MCPUART1 is not accessible to the AP cores.

Default UART settings

The system is configurable using the settings in the `config.txt` file. The following table shows the default UART connectivity settings.

Table 2-10 Default UART connectivity settings in the `config.txt` file

Board component UART	Intermediate connection	Final connection	Comment
APUART0	Serial<>USB bridge, PORT4.	DBG USB connector	-
SCPUART	Serial<>USB bridge, PORT3.		-
MCPUART0	-	UART6 port on PCC	-
MCCUART	Serial<>USB bridge, PORT1.	DBG USB connector	This COM port is visible when a serial terminal display is connected to the DBG USB connector. The command prompt is not visible without mains power to the system.
PCCUART	Serial<>USB bridge, PORT2.		This COM port is visible when a serial terminal display is connected to the DBG USB port.
FPGAUART1	-	-	Not used
FPGAUART2	-	-	Not used

Operation and getting started

When a serial terminal is connected to the DBG USB port, but before mains power is applied:

- The USB powers the USB hub and the Serial<>USB bridge.
- The MCC and PCC UARTS are visible as COM ports.
- The command prompt is not shown.

When mains power is applied, the MCC and PCC are powered and the MCC command prompt is shown. The system is in the standby state waiting for a press of the PBON button to complete the powerup and configuration process. The UART system is configured according to the settings in the `config.txt` file.

See the following sections for more information:

- *1.4 Getting started* on page 1-19.
- *3.3.2 `config.txt` board configuration file* on page 3-65.

Mapping between variables in the `config.txt` file and the UART ports

The following table shows the mapping between the variables in the `config.txt` file and the UART connectors and UART ports:

Table 2-11 `config.txt` file variables

`config.txt` variable	UART interface or connector	Comment
USBPORT1	Serial<>USB bridge PORT1	Serial<>USB bridge connects to DBG USB connector through the USB hub.
USBPORT2	Serial<>USB bridge PORT2	
USBPORT3	Serial<>USB bridge PORT3	
USBPORT4	Serial<>USB bridge PORT4	
UART0	DB9 connector on back panel	A ribbon cable connects the DB9 connector to the 5×2 way header UART0 on the board. The header and DB9 connector pins follow the RS232 specification. No pin 10 on the 5×2 way header.
UART1	DB9 connector on back panel	A ribbon cable connects the DB9 connector to the 5×2 way header UART1 on the board. The header and DB9 connector pins follow the RS232 specification. No pin 10 on the 5×2 way header.
UART2	UART2 5×2 way header on board	The header pins follow the RS232 specification. No pin 10.
UART3	UART3 5×2 way header on board	The header pins follow the RS232 specification. No pin 10.
PCC_UART4	UART4 port on PCC	-
PCC_UART5	UART5 port on PCC	-
PCC_UART6	UART6 port on PCC	-

UART memory addresses

See *4.8 UART memory addresses and control registers* on page 4-225 for information on the UART base memory addresses and control registers.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.11 LEDs, switches, and buttons

There are system LEDs, user LEDs, user system buttons, configuration DIP switches and, user DIP switches on the N1 board.

This section contains the following subsections:

2.11.1 MCC system LEDs

The following table shows the system LEDs associated with the *Motherboard Configuration Controller* (MCC).

Table 2-12 MCC system LEDs

LED	Description	Position	Access	Indicates
Power status	Three color RGY 4-level light pipe	Back panel second from bottom	-	ATX powered or faulty
System LEDs	Green 4-level light pipe	Back panel third from bottom	-	MCC USB activity
	Orange 4-level light pipe	Back panel fourth from bottom		

Related information

1.3 The N1 SDP at a glance on page 1-14

2.11.2 PCC system LEDs

The following table shows the system LEDs associated with the *Platform Controller Chip* (PCC).

Table 2-13 PCC system LEDs

LED	Description	Position	Access	Function
RAS RDIMM LEDs	2×orange	On N1 board. One next to each RDIMM slot	Remove side panel.	Indicates DDR4 configuration issues or that RAS events have occurred.
PCIe status LED	1×green	On N1 board. Near PCC.		Indicates that PCIe is properly configured and link training completed.
CCIX status LED	1×green			Indicates that CCIX is properly configured and virtual channel setup completed.
Chip to Chip (C2C) status LED	1×green			Indicates that C2C link is up and configured to enable C2C traffic.
UID LED	Blue 4-level light pipe	Back panel, first from bottom.	-	Unit Identification Light. Used to physically identify the system in a rack environment.
Numerical LED displays	2×7 green -segment displays	On N1 board, near board edge.	Remove side panel. Not visible through rear I/O opening.	Used by *System Control Processor* (SCP) and MCC to indicate system status through boot. Also used to indicate error conditions during normal run-time operations.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.11.3 IOFPGA LEDs

The IOFPGA drives green LEDs on the N1 board to indicate *Cache-Coherent Interconnect for Accelerators* (CCIX) and *Chip to Chip* (C2C) activity. Removing the side panel provides access to the LEDs which are near the edge of the board.

IOFPGA LEDs

There are eight LEDs and the IOFPGA uses the bottom six to indicate *Link Training and Status State Machine* (LTSSM) status as follows.

Table 2-14 IOFGPA LEDs

LED6	LED5	LED4	LED3	LED2	LED1	Hex LTSSM state number	Indicates
Off	Off	Off	Off	Off	Off	`0x0`	No Linkup and LTSSM in reset
Off	Off	Off	Off	Off	On	`0x1`	×1-Gen 1
Off	Off	Off	Off	On	Off	`0x2`	×1-Gen 2
Off	Off	Off	Off	On	On	`0x3`	×1-Gen 3
Off	Off	Off	On	Off	Off	`0x4`	×1-Gen 4
Off	Off	Off	On	Off	On	`0x5`	×2-Gen 1
Off	Off	Off	On	On	Off	`0x6`	×2-Gen 2
Off	Off	Off	On	On	On	`0x7`	×2-Gen 3
Off	Off	On	Off	Off	Off	`0x8`	×2-Gen 4
Off	Off	On	Off	Off	On	`0x9`	×4-Gen 1
Off	Off	On	Off	On	Off	`0xA`	×4-Gen 2
Off	Off	On	Off	On	On	`0xB`	×4-Gen 3
Off	Off	On	On	Off	Off	`0xC`	×4-Gen 4
Off	Off	On	On	Off	On	`0xD`	×8-Gen 1
Off	Off	On	On	On	Off	`0xE`	×8-Gen 2
Off	Off	On	On	On	On	`0xF`	×8-Gen 3
Off	On	Off	Off	Off	Off	`0x10`	×8-Gen 4
Off	On	On	Off	Off	Off	`0x18`	×16-Gen 1
Off	On	On	On	Off	Off	`0x1C`	×16-Gen 2
Off	On	On	On	On	Off	`0x1E`	×16-Gen 3
Off	On	On	On	On	On	`0x1F`	×16-Gen 4

2.11.4 Miscellaneous LEDs

There are other system LEDs to indicate traffic to and from the N1 board.

The following table shows miscellaneous system LEDs.

Table 2-15 System LEDs

LED	Description	Position	Access	Indicates
Gigabit Ethernet LEDs	1×Yellow	GbE port on back panel	-	GbE activity
	1×green-Orange			Green: 10/100 Link. Orange: 1000 Link.
SATA LEDs	2×green	On N1 board. One next to each SATA connector.	Remove side panel.	SATA activity.
USB 3.0 VBUS LEDs	4×green	On back panel near USB 3.0 connectors	-	USB VBUS
PCC 10/100 Ethernet LEDs	1×yellow	PCC GbE port on back panel	-	PCC GbE activity
	1×green		-	PCC GbE 10/100 Link

Related information

1.3 The N1 SDP at a glance on page 1-14

2.11.5 Push buttons and switches

There are reset push buttons, configuration DIP switches, and user DIP switches on the N1 board.

Reset push buttons

The hardware reset push buttons are:

- PBON, the ON/OFF/Soft Reset button.
- PBRESET, the Hardware reset button.

See *2.5 Resets* on page 2-35 for a description of the functions of the hardware reset push buttons. See *1.3 The N1 SDP at a glance* on page 1-14 for the locations of the hardware reset buttons.

Configuration DIP switches

There are two configuration DIP switches, SW0 and SW1 on the back panel.

The following table shows the functions of the configuration DIP switches.

Table 2-16 Configuration DIP switches

Switch	OFF (Default)	ON
SW0	Reserved	Reserved
SW1	Disabled	Enable MCC hard reset from UART0, **DSR**.

See *3.4.2 Remote UART configuration* on page 3-68 for information on enabling MCC hard reset from UART0, **DSR**.

IOFPGA DIP switches

There are eight DIP switches connected to the IOFPGA.

The IOFPGA DIP switches are reserved for future use.

Related information

1.3 The N1 SDP at a glance on page 1-14

2.12 Debug

The N1 SDP provides on-chip CoreSight debug technology to enable P-JTAG and 32-bit trace debug.

The 20-pin box header on the back panel provides access to JTAG debug.

The trace connector on the back panel provides access to JTAG debug and to 32-bit trace.

See *1.3 The N1 SDP at a glance* on page 1-14 for the location of the JTAG and trace connectors on the back panel.

Related information

1.3 The N1 SDP at a glance on page 1-14

Chapter 3
Configuration

This chapter describes the powerup and configuration process of the N1 SDP.

It contains the following sections:

3.1 Overview of the configuration process

The *Motherboard Configuration Controller* (MCC), the *Platform Controller Chip* (PCC) together with the configuration microSD card, configure the N1 SDP during powerup or reset.

The MCC uses information in the configuration EEPROM and the configuration microSD card during the configuration process, including the board HBI number.

Note

- The HBI number is a unique code that identifies the board. The root directories of the microSD card contain subdirectories in the form *HBI<BoardNumber><BoardRevision>*, for example HBI0316A. HBI0316A is the HBI number of the N1 board.
- If the MCC does not find a configuration directory that matches the HBI number of the board, the configuration process fails and the board reenters the standby state.

The configuration microSD card stores N1 SDP configuration files, including the `board.txt` file.

When power is applied to the N1 board by pressing the power button on the PC case, or the PBON button, preliminary configuration takes place and the board enters the standby state.

The MCC command-line interface is enabled in the standby state. You can connect a workstation to the DBG USB port and edit configuration files or Drag and Drop new configuration files.

Configuration resumes after another press of the power button on the PC tower, or the PBON button. The configuration process then completes without further intervention from the user. The system is then in operating state and application code runs.

A long press of the PBON button, longer than two seconds, initiates a software reset of the system and puts it into the standby state. Pressing the *Hardware Reset* button, PBRESET, initiates a forced reset and puts the system into standby state.

See *1.4 Getting started* on page 1-19.

Related information

1.3 The N1 SDP at a glance on page 1-14
1.4 Getting started on page 1-19

3.2 Powerup and powerdown sequences

The ON/OFF/Soft Reset, PBON, the Hardware Reset button, PBRESET, and powerdown requests from the operating system initiate the powerup and powerdown sequences.

Powerup sequence from powered down state

The powerup sequence of the N1 board is as follows:

1. The PC tower is switched on using the power switch.
2. The *Motherboard Configuration Controller* (MCC) and the *Platform Controller Chip* (PCC) are powered from SB_3V3. All other supplies are powered off.
3. The MCC powers the EEPROM on the board and reads it to determine the HBI code for the board.
4. The system enables the MCC command-line interface on UART0.
5. The system enables the configuration microSD card. You can connect a workstation to the DBG USB port to edit existing configuration files or Drag-and-Drop new configuration files.
6. The system waits in standby state.
7. The PBON button is pressed briefly.
8. The system loads the board configuration file:
   - The MCC reads the generic `config.txt` file.
   - The MCC searches the configuration microSD card MB directory for a directory name that matches the board HBI number.
9. If the MCC finds configuration subdirectories that match the HBI code of the board, configuration continues and the MCC reads the `board.txt` file.
10. If the MCC does not find the correct configuration subdirectories or files, it records the failure to a log file on configuration microSD card. Configuration stops and the system reenters the standby state.
11. The MCC enables the ATXPSU (ATXON).
12. The MCC takes the PCC out of reset in the Enterprise user case.
13. The MCC enables all the supplies, including the board VIO, and the N1 SoC and IOFPGA supplies.
14. The MCC enables the *System Control Processor* (SCP) 32kHZ clock, **REFCLK**, and the board clocks.
15. The MCC reads the FPGA image from the configuration microSD card and loads it into the IOFPGA.
16. The MCC sets the board oscillator frequencies using values from the `board.txt` file.
17. The MCC releases the *Serial Configuration Controller* (SCC) reset, **nCFG_RESET**.
18. If necessary, the MCC programs the IOFPGA and N1 SoC SCC registers as a backup procedure.
19. The MCC programs the SCP and MCP QSPI images from the `images.txt` file.
20. The MCC notifies the PCC that the N1 SoC is coming out of reset and then releases **nSRST**.
21. The MCC releases **nPOR** to the N1 SoC.
22. The MCC enters run state enabling the USBMSD and monitors the MCC UART interface for user commands. It also communicates with the PCC.
23. The SCP and *Manageability Control Processor* (MCP) boot from internal ROM.
24. The SCP and MCP run code from their QSPI flash.
25. The SCP performs the basic N1 SoC setup, PLLs, internal clocks.
26. The SCP releases the *Power Policy Units* (PPUs) to begin the application boot sequence.
27. Application code runs on the N1 SoC. The system is in the operating state.

Powerdown sequence

A long press, greater than two seconds, of the PBON button, initiates the powerdown sequence. The powerdown sequence is as follows:

1. Press the PBON button for longer than two seconds.
2. The PCC detects the power request and sequences the power down with the SCP.
3. The SCP signals the powerdown request to the application processor, that is, one of the N1 clusters.
4. The application cluster goes through its cleanup and shutdown sequence.
5. The application cluster goes to the *Wait for Interrupt* (WFI) state.
6. The PPU sees the WFI state and powers down. The SCP waits for this sequence to complete.
7. The SCP powers down all supplies.
8. The SCP signals the PCC that it is ready for shutdown using the I^2C bus.

9. The PCC requests a powerdown from the MCC using the SPI bus.
10. The MCC asserts **nPOR**, disables the board clocks and the ATXPSU.
11. The system is now in the standby state and waits for a short press of the PBON button.

Related information

1.3 The N1 SDP at a glance on page 1-14

3.3 Configuration files

Configuration files in the configuration microSD card control the board powerup and configuration process.

This section contains the following subsections:

3.3.1 Overview of configuration files and microSD card directory structure

Because the N1 SDP configuration microSD card is non-volatile flash memory, it is only necessary to load new configuration files if you change the system configuration. The configuration microSD card contains default configuration files.

If you connect a workstation to the DBG USB port, the microSD card appears as a *USB Mass Storage Device* (USBMSD) and you can add, edit, or delete files.

You can use a standard text editor that produces DOS line endings to read and edit the board configuration files.

The following figure shows a typical example of the directory structure in the microSD card memory.

Caution

Files names and directory names are in 8.3 format:

- File names that you generate must be in lowercase.
- Directory names must be in uppercase.
- All configuration files must end in DOS line endings, `0x0D`/`0x0A`.

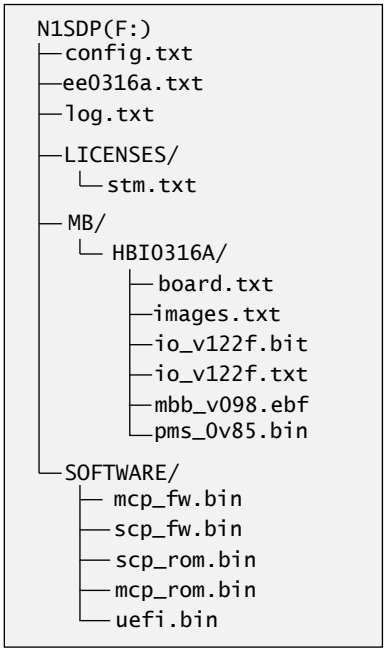

Figure 3-1 Example configuration microSD card directory structure

The directory structure and file name format ensure that each image is matched to the correct target device defined in the N1 SDP configuration EEPROM.

`config.txt` file
Generic configuration file for all motherboards. This file applies to all Arm development boards including the N1 board.

`LICENSES` directory
Contains one license text file.

`MB` directory
Contains one or more HBI subdirectories for board variants. The subdirectory names match the HBI codes for the board variants.

`HBI0316?` subdirectories
Contain pointer files that define BIOS images for the MCC, the *Power Management IC* (PMIC), and the IOFPGA, SCP, and MCP. Other files contain image, and configuration information for the board and IOFPGA.

`SOFTWARE` directory
Contains application files for the SCP and MCP. The `images.txt` file defines the image files.

3.3.2 `config.txt` board configuration file

You can connect a workstation to the DBG USB port to update the generic Arm development board configuration file `config.txt` in the root directory of the microSD card.

The following example shows a typical `config.txt` configuration file in the root directory of the configuration microSD card.

Note

- Colons (:) indicate the end of commands and must be separated by a space character (`0x20`) from the value fields.
- Semicolons (;) indicate comments.

```
BOARD: HBI0316A
TITLE: N1SDP Configuration file

[CONFIGURATION]
TESTMENU: FALSE
AUTORUN: TRUE               ;Auto Run from power on
AUTORUNDELAY: 3             ;Delay in seconds to wait for key press to stop

RTC: TRUE                   ;TRUE = Enable RTC, FALSE = Disable RTC

APUART0: 6                  ;0-Not Used 1-USBPORT1 2-UART0 3-USBPORT2 4-UART1 5-PCC_UART5 6-
USBPORT4 7-UART3
MCCUART: 1                  ;0-Not Used 1-USBPORT1 2-UART0 3-USBPORT2 4-UART1
PCCUART: 1                  ;0-Not Used 1-USBPORT2 2-UART1 3-UART2
SCPUART: 1                  ;0-Not Used 1-USBPORT3 2-PCC_UART4
MCPUART0: 3                 ;0-Not Used 1-USBPORT4 2-UART3 3-PCC_UART6
FPGAUART1: 0                ;0-Not Used 1-USBPORT3
FPGAUART2: 0                ;0-Not Used 1-USBPORT4 2-UART3

DVIMODE: VGA                ;VGA/SVGA/XGA/UXGA or HD1080 (MCC sets OSCCLK5)

USERSWITCH: 10101010        ;Userswitch[7:0] in binary
CONFSWITCH: 01010101        ;Configuration Switch[7:0] in binary

USB_REMOTE: FALSE           ;Selects remote command via USB !TBA
```

See *2.10 UARTs* on page 2-51 for information on configuring the UARTs and UART connectivity.

3.3.3 Contents of the `MB` directory

The `MB` directory contains a configuration `HBI????` subdirectory that matches the HBI code of the N1 board. The `HBI????` subdirectory contains files that relate to the MCC and to other components on the N1 board, but not the N1 SoC.

The HBI subdirectory contains the following:

One `board.txt` file	Points to the BIOS image that the MCC loads during configuration.
One `images.txt` file	Points to the SCP and MCP image files.
Files of the form `io_v???.bit`	IOFPGA image files for different board variants.
File of the form `io_v???.txt`	IOFPGA configuration files for different board variants.
A file of the form `mbb_v???.ebf`.	MCC BIOS image that the `board.txt` file defines.
A file of the form `pms_v???.bin`	BIOS image for the *Power Management IC* (PMIC) on the N1 board.

The following example shows a typical N1 board configuration `board.txt` file.

```
BOARD: HBI0316A
TITLE: N1SDP Motheboard Configuration File

[MCCS]
MBBIOS: mbb_v098.ebf               ;MB BIOS IMAGE

[PCCS]
PCCBIOS: pcc_v050.bin               ;PCC BIOS IMAGE

[PCIE]
MBPCIE: pci_v002.bin               ;MB PCIE

[FPGA]                             ;Please select the required fpga image
APPFILE: io_v122f.txt                 ;N1SDP fpga image
```

The following example shows a typical N1 board `images.txt` file.

```
TITLE: Images Configuration File

[IMAGES]
TOTALIMAGES: 5                     ;Number of Images (Max: 32)

IMAGE0ADDRESS: 0x64000000          ;Please select the required executable program
IMAGE0UPDATE: MCP_AUTO             ;Image Update: NONE/AUTO/FORCE/SCP_AUTO/MCP_AUTO
IMAGE0FILE: \SOFTWARE\mcp_fw.bin   ;Image for test

IMAGE1ADDRESS: 0x64000000          ;Please select the required executable program
IMAGE1UPDATE: SCP_AUTO             ;Image Update:NONE/AUTO/FORCE/SCP_AUTO/MCP_AUTO
IMAGE1FILE: \SOFTWARE\scp_fw.bin   ;Image for test

IMAGE2ADDRESS: 0x60000000          ;Please select the required executable program
IMAGE2UPDATE: FORCE                ;Image Update:NONE/AUTO/FORCE/SCP_AUTO/MCP_AUTO
IMAGE2FILE: \SOFTWARE\scp_rom.bin  ;Image for test

IMAGE3ADDRESS: 0x62000000          ;Please select the required executable program
IMAGE3UPDATE: FORCE                ;Image Update:NONE/AUTO/FORCE/SCP_AUTO/MCP_AUTO
IMAGE3FILE: \SOFTWARE\mcp_rom.bin  ;Image for test

IMAGE4ADDRESS: 0x60200000          ;Please select the required executable program
IMAGE4UPDATE: FORCE                ;Image Update:NONE/AUTO/FORCE/SCP_AUTO/MCP_AUTO
IMAGE4FILE: \SOFTWARE\uefi.bin     ;Image for test
```

The following example shows a typical N1 board configuration file, `io_v122f.txt`.

```
BOARD: HBI0316
TITLE: N1SDP configuration file

[FPGAS]
TOTALFPGAS: 1                      ;Total number of FPGAs
F0FILE: io_v122f.bit               ;FPGA0 Filename
F0MODE: FPGA                       ;FPGA0 Programming Mode

[PMIC]
MBPMIC: pms_0v85.bin               ;MB PMIC

[OSCCLKS]
TOTALOSCCLKS: 12
OSC0:  50.0                        ;OSC0-Y5 - SYS_REF_CLK
OSC1:  50.0                        ;OSC0-Y4 - CPU0_REF_CLK
OSC2:  50.0                        ;OSC0-Y6 - CPU1_REF_CLK
OSC3:  50.0                        ;OSC1-Y2 - CLUS_REF_CLK
OSC4:  50.0                        ;OSC1-Y4 - INT_REF_CLK
OSC5:  50.0                        ;OSC1-Y6 - REF_CLK
OSC6:  50.0                        ;OSC2-Y2 - DMC_REF_CLK
OSC7:  23.75                       ;OSC2-Y4 - IOFPGA_PXLCLK (HDLCD)
OSC8:  80.0                        ;OSC2-Y6 - IOFPGA_TXLCLK
OSC9:  60.0                        ;OSC3-Y2 - IOFPGA_ACLK
```

```
OSC10: 24.576                       ;OSC3-Y4 - IOFPGA_AUDCLK
OSC11: 24.0                         ;OSC3-Y6 - IOFPGA_RSVDCLK

[HARDWARE CONTROL]
;ASSERTNPOR: TRUE                   ;External resets assert nPOR !TBA

[PERIPHERAL SUPPORT]
FPGA_SMB: TRUE                      ;SMB interface is supported (MCC_SMC<>FPGA_SMB)

FPGA_SCC: TRUE                      ;SCC interface is supported
SCCREG:  0x68130000                 ;SCC registers base address

FPGA_DDR: TRUE                      ;DDR interface is supported
DDRBASE: 0x68040000                 ;DDR I2C register address

FPGA_SYSREG: TRUE                   ;System register interface is supported
FPGAREG: 0x68010000                 ;System registers base address

FPGA_HDMI: TRUE                     ;HDMI interface is supported
HDMIBASE: 0x680F0000                ;HDMI I2C register address

FPGA_LAN: TRUE                      ;LAN LAN9220 interface is supported
LANBASE: 0x69100000                 ;LAN LAN9220 base address

FPGA_RTC: TRUE                      ;RTC PL031 interface is supported
RTCBASE: 0x68100000                 ;RTC PL031 base address

FPGA_QSPI: TRUE                     ;QSPI interface is supported
QSPIBASE: 0x680C0000                ;QSPI controller base address
QSPIDATA: 0x64000000                ;QSPI data address

C2C_ENABLE: TRUE                    ;C2C enable TRUE/FALSE
C2C_SIDE: SLAVE                     ;C2C side SLAVE/MASTER

[SCC REGISTERS]
TOTALSYSCONS: 13                    ;Total Number of SCC registers defined
SYSCON: 0x000 0x01234567            ;IOFPGA SCC test entry

SOCCON: 0x1160 0x00000001           ;SoC SCC BOOT_CTL - enable TLX
SOCCON: 0x1164 0x01000000           ;SoC SCC BOOT_CTL_STA (0xX1000000 = MCC OK)
SOCCON: 0x1168 0x00000000           ;SoC SCC SCP_BOOT_ADR
SOCCON: 0x116C 0x00000000           ;SoC SCC MCP_BOOT_ADR
;SOCCON: 0x1170 0x00000000           ;SoC SCC PLATFORM_CTRL
;SOCCON: 0x1174 0x00000000           ;SoC SCC TARGETIDAPP (0x07B00477)
;SOCCON: 0x1178 0x00000000           ;SoC SCC TARGETIDSCP (0x07B10477)
;SOCCON: 0x117C 0x00000000           ;SoC SCC TARGETIDMCP (0x07B20477)
SOCCON: 0x1180 0x00000000           ;SoC SCC BOOT_GPR0
SOCCON: 0x1184 0x00000000           ;SoC SCC BOOT_GPR1
SOCCON: 0x1188 0x00000000           ;SoC SCC BOOT_GPR2
SOCCON: 0x118C 0x00000000           ;SoC SCC BOOT_GPR3
SOCCON: 0x1190 0x00000000           ;SoC SCC BOOT_GPR4
SOCCON: 0x1194 0x00000000           ;SoC SCC BOOT_GPR5
SOCCON: 0x1198 0x00000000           ;SoC SCC BOOT_GPR6
SOCCON: 0x119C 0x00000000           ;SoC SCC BOOT_GPR7
```

3.3.4 Contents of the SOFTWARE subdirectory

The SOFTWARE subdirectory contains applications that you can load into external flash memory.

You can create new applications and load them into the flash memory on the N1 SDP. Application images are typically boot images or demo programs. The system recognizes `.elf`, `.bin`, and `.bit` files.

Typical applications in this subdirectory are:

- `mcp_fw.elf` MCP image file.
- `scp_fw.elf` SCP image file.

3.4 Configuration switches

There are configuration switches SW0 and SW1 on the back panel.

This section contains the following subsections:

3.4.1 Use of configuration switches

The SW0 and SW1 switches affect board initialization.

The `config.txt` configuration file contains *`USERSWITCH`* and *`CONFSWITCH`* entries for the virtual switch register bits SYS_SW[7:0] and SYS_CFGSW[7:0] in the IOFPGA. The configuration system does not use these virtual switches for system configuration, but they are available for the user application and boot monitor.

Note

- The default setting for configuration switches SW0 and SW1 is OFF.
- If the switches are in the up position, they are OFF. See *1.4 Getting started* on page 1-19.

Boot script switch SW0

Reserved.

Remote UART control switch SW1

SW1 in the ON position enables UART control and the flow-control signals on UART0 to control the standby-state. This setting is typically used on test farms.

See the following for information about the configuration switches:

- *1.3 The N1 SDP at a glance* on page 1-14.
- *1.4 Getting started* on page 1-19.

3.4.2 Remote UART configuration

To enable remote UART control:

Switch SW1, on the side panel must be ON, and the correct options must be set in the `config.txt` file to connect the UART0 port to the MCC.

An external controller can toggle the UART0 connector on the side panel **SER0_DSR**, pin 6, HIGH for 100ms to put the N1 SDP into standby-state. This is equivalent to pressing the Hardware Reset button, PBRESET. Power cycling the board also places the system in the standby state.

Note

The duration of the **SER0_DSR** HIGH pulse must be greater than or equal to 100ms.

Remote UART0 control requires a full null modem cable that Arm supplies with the N1 SDP. The following figure shows the cable wiring.

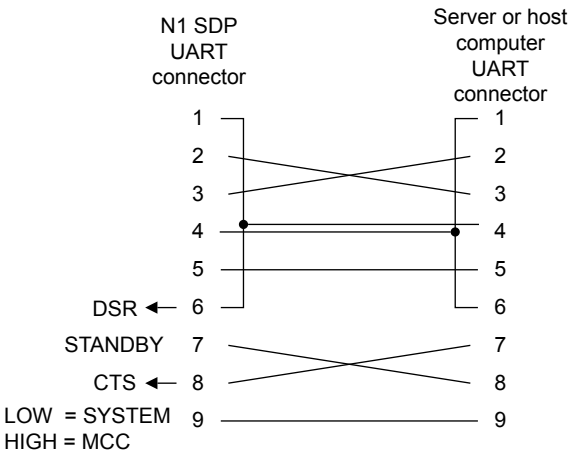

Figure 3-2 Modem cable wiring

You can control the **SER0_DSR** and **SER0_CTS** signals using control logic on the host computer.

Alternatively, you can use a custom terminal program such as `VETerminal.exe` that Arm provides on the N1 SDP DVD. This program integrates the terminal output and control buttons into a single application.

Related information

1.3 The N1 SDP at a glance on page 1-14

3.5 Use of reset push buttons

The On/Off/Soft reset button, PBON, initiates the powerup and powerdown sequences. The Hardware reset button, PBRESET, initiates a hardware reset.

In standby state, press the PBON button briefly, less than two seconds, to initiate the powerup sequence.

In the operating state, press the PBON button for longer than two seconds to initiate the powerdown sequence.

In the operating state, press the PBRESET button to initiate a hardware reset.

See *3.2 Powerup and powerdown sequences* on page 3-62.

Related information

1.3 The N1 SDP at a glance on page 1-14

3.6 Command-line interface

The N1 SDP command-line interface supports system command-line input to the *Motherboard Configuration Controller* (MCC).

This section contains the following subsections:

3.6.1 Overview of the N1 SDP MCC command-line interface

You must connect a workstation to the DBG USB to enter MCC system commands at the MCC USB port.

You must set the *MBLOG* option in the `config.txt` to `TRUE` to enter MCC system commands.

The workstation settings must be:

- 115.2kBaud.
- 8N1 representing 8 data bits, no parity, one stop bit.
- No hardware or software flow control.

Related information

1.3 The N1 SDP at a glance on page 1-14

3.6.2 MCC main command menu

The following table shows the MCC main menu system commands.

Table 3-1 N1 SDP MCC main command menu

Command	Description
CAP *filename* [/A]	Capture serial data to the file *filename*. Use the /A option to append data to an existing file.
COPY *input_filename_1* [*input_filename_2*] *output_filename*	Copy a file *input_filename_1* to *output_filename*. Option *input_filename_2* merges *input_filename_1* and *input_filename_2*.
DEBUG	Change to the debug menu.
DEL *filename*	Delete file *filename*.
DIR [*mask*]	Display a list of files in the directory.
EEPROM	Change to the EEPROM menu.
FILL *filename* [*nnnn*]	Create a file *filename* filled with text. *nnnn* specifies the number of lines to create. The default is 1000.
HELP or ?	Display this help.
REBOOT	Cycle system power and reboot.
REN *filename_1* *filename_2*	Rename a file from *filename_1* to *filename_2*.

Table 3-1 N1 SDP MCC main command menu (continued)

Command	Description
RESET	Reset the N1 SoC using the **SoC_nSRST** reset signal.
SHUTDOWN	Shut down the power supply but leave the MCC running. The board returns to Standby mode.
TYPE *filename*	Display the contents of text file *filename*.
USB_ON	Enable MCC USB configuration port.
USB_OFF	Disable MCC USB configuration port.

3.6.3 MCC debug menu

To switch to the debug submenu enter DEBUG at the main menu. The debug submenu is valid only in operating-state.

The following table shows the debug commands.

Table 3-2 N1 SDP MCC debug command menu

Command	Description
DATE	Display current date.
DEBUG [0|1]	Enable or disable debug printing: 0b0 Disable. 0b1 Enable.
DEPOSIT *address data*	Write word to system memory address.
EXAM *address* [*nnnn*]	Examine system memory address at *address*. *nnnn* is number, in Hex, of words to read.
EXIT or QUIT	Return to main menu.
HELP or ?	Display this help.
TIME	Display current time.

3.6.4 EEPROM menu

To switch to the EEPROM submenu enter EEPROM at the main menu. The contents of the N1 SDP EEPROMs identify the specific board variant and might contain data to load to the other devices on the board.

The following table shows the EEPROM commands.

Caution

You must not modify the EEPROM settings. The settings are programmed with unique values during production and changing them might compromise the function of the board.

Table 3-3 N1 SDP EEPROM commands

Command	Description
CONFIG 0 *filename*	Write configuration file to EEPROM.
EXIT or QUIT	Return to main menu.

Table 3-3 N1 SDP EEPROM commands (continued)

Command	Description
`ERASECON [0]`	Erase configuration section of EEPROM.
`ERASEDEV [0]`	Erase device section of EEPROM.
`ERASERANGE [0] start end`	Erase EEPROM between *start* and *end*.
`ERASEIMAGE image_id`	Erase image, named *image_id*, stored in Motherboard EEPROM.
`ERASEIMAGES`	Erase images stored in Motherboard EEPROM.
`HELP` or `?`	Display this help.
`READIMAGES`	Read images stored in Motherboard EEPROM.
`READCF [0]`	Read configuration EEPROM.
`READRANGE [0]` [*start*] [*end*]	Read EEPROM between *start* and *end*.

Chapter 4
Programmers model

This chapter describes the programmers model of the N1 SDP.

It contains the following sections:

4.1 About this programmers model

The following information applies to all registers in this programmers model:

- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or powerup reset.
  - All register summary tables in this chapter describe register access types as follows:

RW	Read/write.
RO	Read-only.
WO	Write-only.

4.2 N1 SDP memory maps

The N1 SDP contains *Application Processor* (AP), *System Control Processor* (SCP), and *Manageability Control Processor* (MCP) memory maps.

The SCP and MCP memory maps are private. The masters which can access the AP memory map have no access to the components in the SCP and MCP memory maps. Certain areas with the AP memory map are mapped into the SCP and MCP memory maps and the corresponding masters can access them.

This section contains the following subsections:

4.2.1 Application Processor memory map

The following figure shows the N1 SDP Application Processor (AP) memory map.

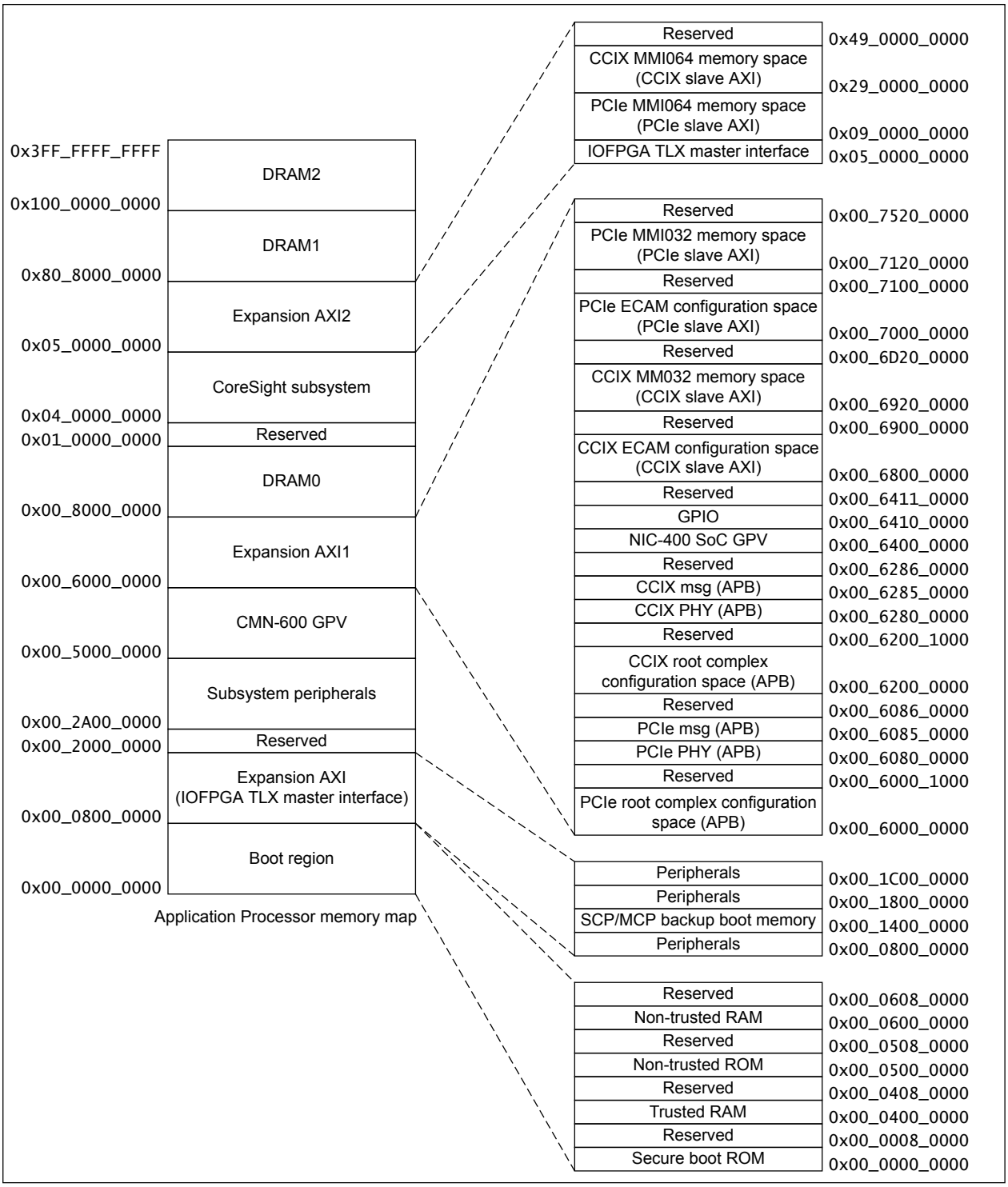

Figure 4-1 AP memory map

The following table shows the N1 SDP AP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-1 AP memory map

Address range		Size	Description
From	To		
0x0_0000_0000	0x0_0007_FFFF	512KB	Boot region-Secure boot ROM
0x0_0400_0000	0x0_0407_FFFF	512KB	Boot region-Trusted RAM
0x0_0500_0000	0x0_0507_FFFF	512KB	Boot region-Non-trusted ROM
0x0_0600_0000	0x0_0607_FFFF	512KB	Boot region-Non-trusted RAM
0x0_0080_0000	0x0_13FF_FFFF	192MB	IOFPGA peripherals
0x0_1400_0000	0x0_17FF_FFFF	64MB	SCP, MCP backup boot memory.
0x0_1800_0000	0x0_1BFF_FFFF	64MB	IOFPGA peripherals
0x0_1C00_0000	0x0_1FFF_FFFF	64MB	IOFPGA peripherals
0x0_2A00_0000	0x0_4FFF_FFFF	608MB	Subsystem peripherals
0x0_5000_0000	0x0_5FFF_FFFF	256MB	CMN-600 GPV
0x0_6000_0000	0x0_6000_0FFF	4KB	PCIe root complex configuration space, APB.
0x0_6080_0000	0x0_6084_FFFF	320KB	PCIe PHY, APB.
0x0_6085_0000	0x0_6085_FFFF	64KB	PCIe msg, (APB.
0x0_6200_0000	0x0_6200_0FFF	4KB	CCIX root complex configuration space, APB.
0x0_6280_0000	0x0_6284_FFFF	320KB	CCIX PHY, APB.
0x0_6285_0000	0x0_6285_FFFF	64KB	CCIX msg, APB.
0x0_6400_0000	0x0_640F_FFFF	1MB	NIC-400 N1 SoC GPV
0x0_6410_0000	0x0_6410_FFFF	64KB	GPIO
0x0_6800_0000	0x0_68FF_FFFF	16MB	CCIX ECAM configuration space. CCIX slave AXI.
0x0_6920_0000	0x0_6D1F_FFFF	64MB	CCIX MMO32 memory space. CCIX slave AXI.
0x0_7000_0000	0x0_70FF_FFFF	16MB	PCIe ECAM configuration space. PCIe slave AXI.
0x0_7120_0000	0x0_751F_FFFF	64MB	PCIe MMI032 memory space. PCIe slave AXI.
0x0_8000_0000	0x0_FFFF_FFFF	2GB	DRAM0
0x04_0000_0000	0x04_FFFF_FFFF	4GB	CoreSight subsystem
0x05_0000_0000	0x08_FFFF_FFFF	16GB	IOFPGA TLX master interface
0x09_0000_0000	0x28_FFFF_FFFF	128GB	PCIe MMI064 memory space. PCIe slave AXI.

Table 4-1 AP memory map (continued)

Address range		Size	Description
From	To		
0x29_0000_0000	0x48_FFFF_FFFF	128GB	CCIX MMI064 memory space. CCIX slave AXI.
0x80_8000_0000	0xFF_FFFF_FFFF	510GB	DRAM1
0x100_0000_0000	0x3FF_FFFF_FFFF	3TB	DRAM2

4.2.2 Application Processor subsystem peripherals memory map

The *Application Processor* (AP) memory map of the N1 SDP contains a region associated with the subsystem peripherals.

The following figure shows the subsystem peripherals region of the AP memory map.

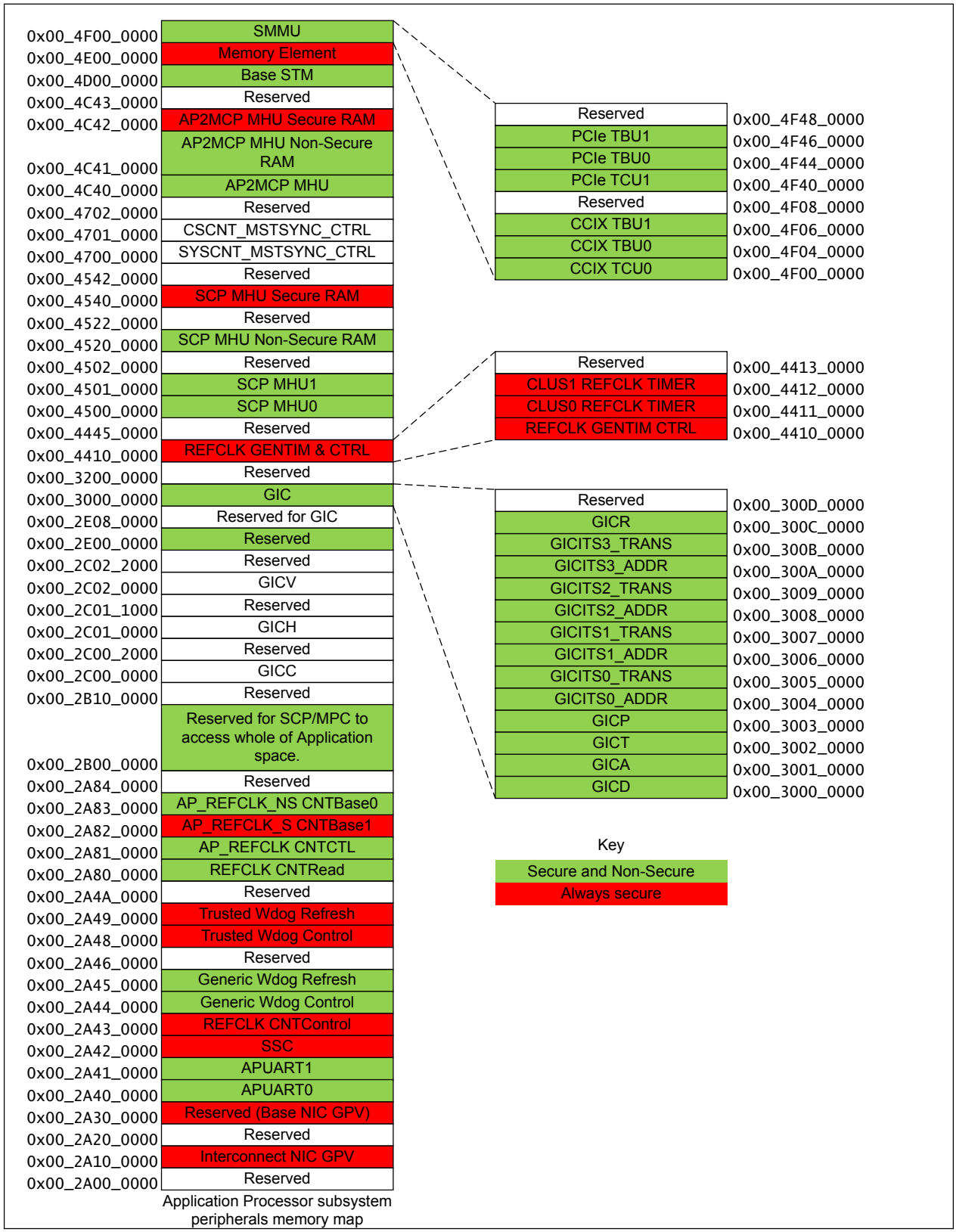

Figure 4-2 Application Processor subsystem peripherals memory map

The following table shows the subsystem peripherals region of the AP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-2 AP peripherals memory map

Address range		Size	Description
From	To		
0x00_2A00_0000	0x00_2A0F_FFFF	1MB	Reserved
0x00_2A10_0000	0x00_2A1F_FFFF	1MB	Interconnect NIC GPV
0x00_2A30_0000	0x00_2A3F_FFFF	1MB	Reserved (Base NIC GPV)
0x00_2A40_0000	0x00_2A40_FFFF	64KB	APUART0
0x00_2A41_0000	0x00_2A41_FFFF	64KB	APUART1
0x00_2A42_0000	0x00_2A42_FFFF	64KB	SSC
0x00_2A43_0000	0x00_2A43_FFFF	64KB	REFCLK CNTControl
0x00_2A44_0000	0x00_2A44_FFFF	64KB	Generic Watchdog Control
0x00_2A45_0000	0x00_2A45_FFFF	64KB	Generic Watchdog Refresh
0x00_2A48_0000	0x00_2A48_FFFF	64KB	Trusted Watchdog Control
0x00_2A49_0000	0x00_2A49_FFFF	64KB	Trusted Watchdog Refresh
0x00_2A80_0000	0x00_2A80_FFFF	64KB	REFCLK CNTRead
0x00_2A81_0000	0x00_2A81_FFFF	64KB	AP_REFCLK CNTCTL
0x00_2A82_0000	0x00_2A82_FFFF	64KB	AP_REFCLK_S CNTBase1
0x00_2A83_0000	0x00_2A83_FFFF	64KB	AP_REFCLK_NS CNTBase0
0x00_2B00_0000	0x00_2B0F_FFFF	1MB	Reserved for SCP/MCP to access whole of application space.
0x00_2C00_0000	0x00_2C00_1FFF	8KB	GICC registers
0x00_2C01_0000	0x00_2C01_0FFF	4KB	GICH registers
0x00_2C02_0000	0x00_2C02_1FFF	8KB	GICV registers
0x00_2E08_0000	0x00_2FFF_FFFF	32256KB	Reserved for GIC
0x00_3000_0000	0x00_3000_FFFF	64KB	GICD registers
0x00_3001_0000	0x00_3001_FFFF	64KB	GICA registers
0x00_3002_0000	0x00_3002_FFFF	64KB	GICT registers
0x00_3003_0000	0x00_3003_FFFF	64KB	GICP registers
0x00_3004_0000	0x00_3004_FFFF	64KB	GICITS0 ITS address
0x00_3005_0000	0x00_3005_FFFF	64KB	GICITS0 translater
0x00_3006_0000	0x00_3006_FFFF	64KB	GICITS1 address
0x00_3007_0000	0x00_3007_FFFF	64KB	GICITS1 translater
0x00_3008_0000	0x00_3008_FFFF	64KB	GICITS2 address
0x00_3009_0000	0x00_3009_FFFF	64KB	GICITS2 translater
0x00_300A_0000	0x00_300A_FFFF	64KB	GICITS3 address
0x00_300B_0000	0x00_300B_FFFF	64KB	GICITS3 address

Table 4-2 AP peripherals memory map (continued)

Address range		Size	Description
From	To		
0x00_300C_0000	0x00_300C_FFFF	64KB	GICR registers
0x00_4410_0000	0x00_4410_FFFF	64KB	REFCLK general timer control
0x00_4411_0000	0x00_4411_FFFF	64KB	Cluster 0 time frame
0x00_4412_0000	0x00_4412_FFFF	64KB	Cluster 1 time frame
0x00_4500_0000	0x00_4500_FFFF	64KB	SCP *Message Handling Unit0* (MHU0)
0x00_4501_0000	0x00_4501_FFFF	64KB	SCP MHU1
0x00_4520_0000	0x00_4521_FFFF	128KB	SCP MHU Non-secure RAM
0x00_4540_0000	0x00_4541_FFFF	128KB	SCP MHU Secure RAM
0x00_4700_0000	0x00_4700_FFFF	64KB	SYSCNT_MSTSYN_CTRL
0x00_4701_0000	0x00_4701_FFFF	64KB	CSCNT_MSTSYNC_CTRL
0x00_4C40_0000	0x00_4C40_FFFF	64KB	AP2MCP MHU
0x00_4C41_0000	0x00_4C41_FFFF	64KB	AP2MCP MHU Non-Secure RAM
0x00_4C42_0000	0x00_4C42_FFFF	64KB	AP2MCP MHU Secure RAM
0x00_4D00_0000	0x00_4DFF_FFFF	16MB	Base STM
0x00_4E00_0000	0x00_4EFF_FFFF	16MB	Memory Element
0x00_4F00_0000	0x00_4F03_FFFF	256KB	*Translation Control Unit0* (TCU0) for CCIX root port.
0x00_4F04_0000	0x00_4F05_FFFF	128KB	*Translation Buffer Unit0* (TBU0) for CCIX root port.
0x00_4F06_0000	0x00_4F07_FFFF	128KB	*Translation Buffer Unit1* (TBU1) for CCIX root port.
0x00_4F40_0000	0x00_4F43_FFFF	256KB	*Translation Control Unit1* (TCU0) for PCIe root port.
0x00_4F44_0000	0x00_4F45_FFFF	128KB	*Translation Buffer Unit0* (TBU0) for PCIe root port.
0x00_4F46_0000	0x00_4F47_FFFF	128KB	*Translation Buffer Unit1* (TBU1) for PCIe root port.

4.2.3 Manageability Control Processor memory map

The following figure shows the N1 SDP Manageability Control Processor (MCP) memory map.

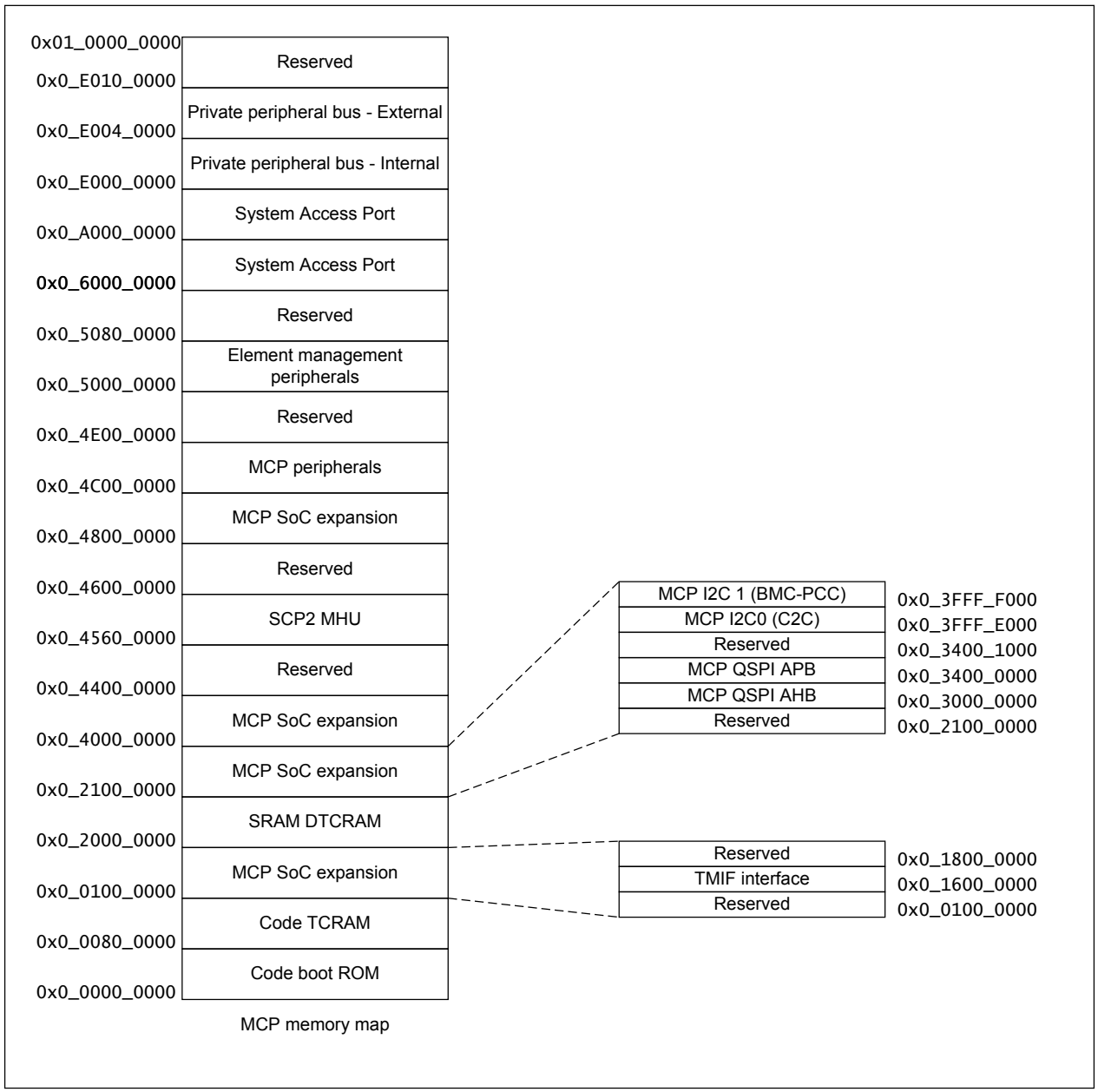

Figure 4-3 MCP memory map

The following table shows the N1 SDP MCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-3 MCP memory map

Address range		Size	Description
From	To		
0x0_0000_0000	0x0_007F_FFFF	8MB	Code boot ROM
0x0_0080_0000	0x0_00FF_FFFF	8MB	Code TCRAM
0x0_0100_0000	0x0_15FF_FFFF	336MB	Reserved part of MCP SoC expansion memory
0x0_1600_0000	0x0_17FF_FFFF	32MB	TMIF interface
0x0_1800_0000	0x0_1FFF_FFFF	128MB	Reserved part of MCP SoC expansion memory
0x0_2000_0000	0x0_20FF_FFFF	16MB	SRAM DTCRAM
0x0_2100_0000	0x0_2FFF_FFFF	240MB	Reserved part of MCP SoC expansion memory
0x0_3000_0000	0x0_33FF_FFFF	64MB	MCP QSPI AHB
0x0_3400_0000	0x0_3400_0FFF	4KB	MCP QSPI APB
0x0_3400_1000	0x0_3FFF_DFFF	191MB	Reserved part of MCP SoC expansion memory
0x0_3FFF_E000	0x0_3FFF_EFFF	4KB	MCP I2C0 (C2C)
0x0_3FFF_F000	0x0_3FFF_FFFF	4KB	MCP I2C 1 (BMC-PCC)
0x0_4000_0000	0x0_43FF_FFFF	64MB	MCP SoC expansion
0x0_4400_0000	0x0_455F_FFFF	22MB	Reserved
0x0_4560_0000	0x0_45FF_FFFF	10MB	SCP2 MHU
0x0_4600_0000	0x0_47FF_FFFF	32MB	Reserved
0x0_4800_0000	0x0_4BFF_FFFF	64MB	MCP SoC expansion
0x0_4C00_0000	0x0_4DFF_FFFF	32MB	MCP peripherals
0x0_4E00_0000	0x0_4FFF_FFFF	32MB	Reserved
0x0_5000_0000	0x0_507F_FFFF	8MB	Element management peripherals
0x0_5080_0000	0x0_5FFF_FFFF	248MB	Reserved
0x0_6000_0000	0x0_9FFF_FFFF	1GB	System Access Port. Translated to 0x0_4000_0000 to 0x0_7FFF_FFFF of AP memory map.
0x0_A000_0000	0x0_DFFF_FFFF	1GB	System Access Port. Translated to 0x0_0000_0000 to 0x0_3FFF_FFFF of AP memory map with debug address translation not enabled. Translated to 0x4_0000_0000 to 0x4_3FFF_FFFF of AP memory map with debug address translation enabled.
0x0_E000_0000	0x0_E003_FFFF	256KB	Private peripheral bus - Internal.
0x0_E004_0000	0x0_E00F_FFFF	768KB	Private peripheral bus - External.
0x0_E010_0000	0x0_FFFF_FFFF	511MB	Reserved

4.2.4 Manageability Control Processor peripherals memory map

The *Manageability Control Processor* (MCP) memory map of the N1 SDP contains a region associated with the MCP peripherals.

The following figure shows the peripherals region of the MCP memory map.

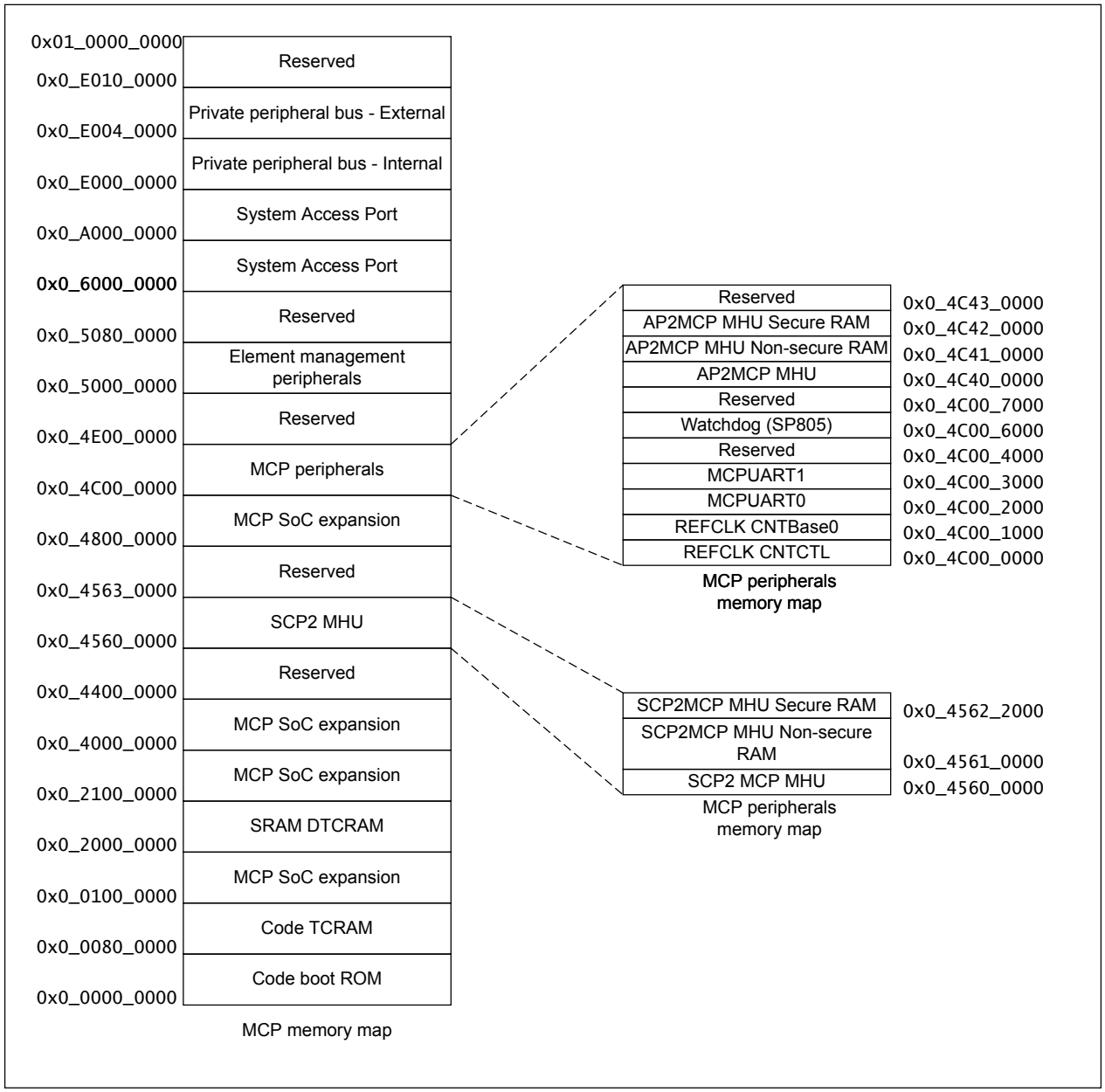

Figure 4-4 MCP peripherals memory map

The following table shows the peripherals region of the MCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-4 MCP peripherals memory map

Address range		Size	Description
From	To		
0x00_4560_0000	0x00_4560_FFFF	64KB	SCP2 MCP *Message Handling Unit* (MHU)
0x00_4561_0000	0x00_4561_FFFF	64KB	SCP2 MCP MHU Non-secure RAM

Table 4-4 MCP peripherals memory map (continued)

Address range		Size	Description
From	To		
0x00_4562_0000	0x00_4562_FFFF	64KB	SCP2 MCP MHU Secure RAM
0x00_4C00_0000	0x00_4C00_0FFF	4KB	REFCLK CNTCTL
0x00_4C00_1000	0x00_4C00_1FFF	4KB	REFCLK CNTBase0
0x00_4C00_2000	0x00_4C00_2FFF	4KB	MCPUART0
0x00_4C00_3000	0x00_4C00_3FFF	4KB	MCPUART1
0x00_4C00_6000	0x00_4C00_6FFF	4KB	Watchdog (SP805)
0x00_4C40_0000	0x00_4C40_FFFF	64KB	AP2 MCP MHU
0x00_4C41_0000	0x00_4C41_FFFF	64KB	AP2 MCP MHU Non-secure RAM
0x00_4C42_0000	0x00_4C42_FFFF	64KB	AP2 MCP MHU Secure RAM

4.2.5 System Control Processor memory map

The following figure shows the N1 SDP System Control Processor (SCP) memory map.

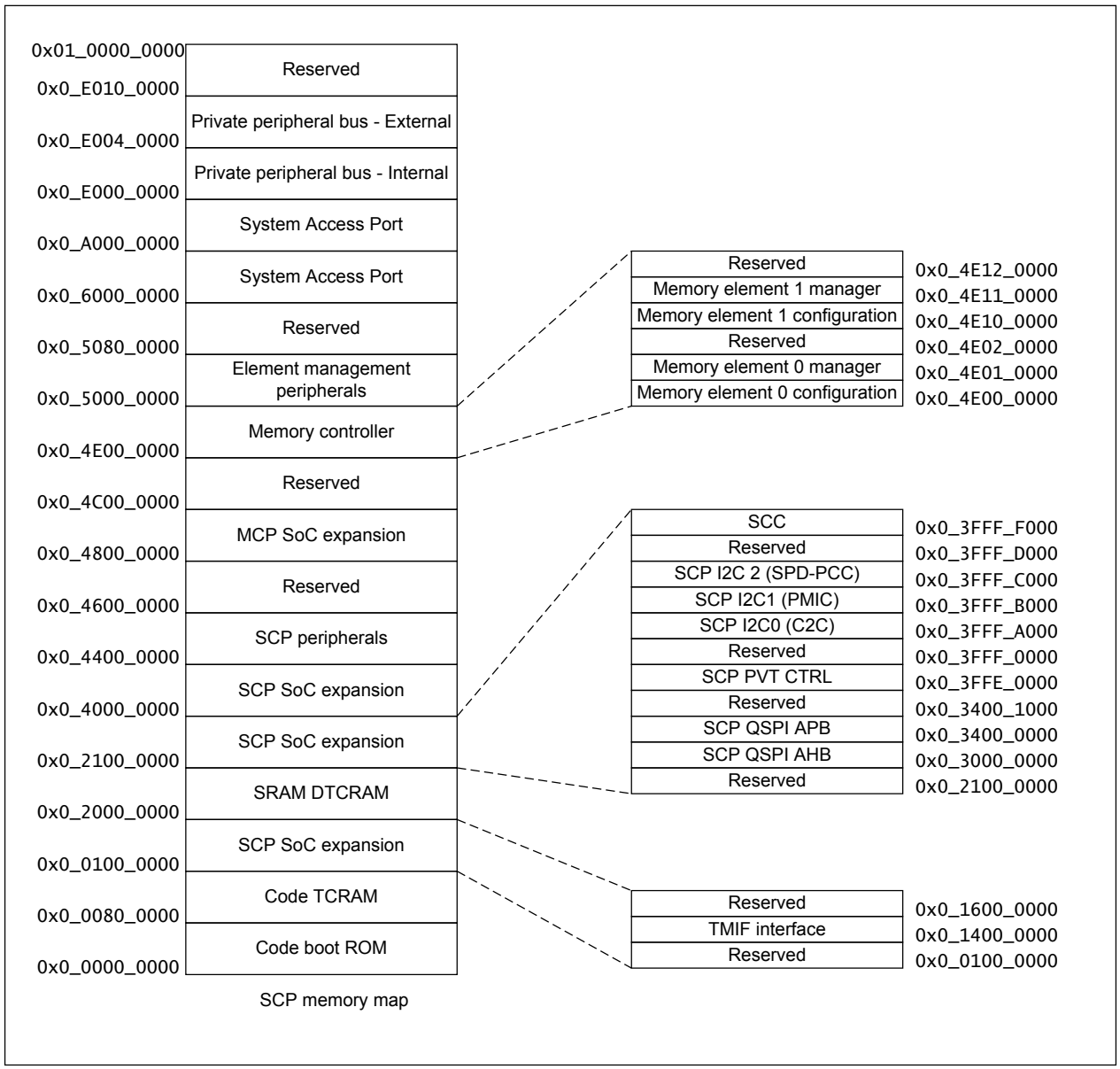

Figure 4-5 SCP memory map

The following table shows the N1 SDP SCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-5 SCP memory map

Address range		Size	Description
From	To		
0x0_0000_0000	0x0_007F_FFFF	8MB	Code boot ROM
0x0_0080_0000	0x0_00FF_FFFF	8MB	Code TCRAM

Table 4-5 SCP memory map (continued)

Address range		Size	Description
From	To		
0x0_0100_0000	0x0_13FF_FFFF	304MB	Reserved part of SCP SoC expansion memory
0x0_1400_0000	0x0_15FF_FFFF	32MB	TMIF interface
0x0_1600_0000	0x0_1FFF_FFFF	160MB	Reserved part of SCP SoC expansion memory
0x0_2000_0000	0x0_20FF_FFFF	16MB	SRAM DTCRAM
0x0_2100_0000	0x0_2FFF_FFFF	240MB	Reserved part of SCP SoC expansion memory
0x0_3000_0000	0x0_33FF_FFFF	64MB	SCP QSPI AHB
0x0_3400_0000	0x0_3400_0FFF	4KB	SCP QSPI APB
0x0_3400_1000	0x0_3FFD_FFFF	191MB	Reserved part of SCP SoC expansion memory
0x0_3FFE_0000	0x0_3FFE_FFFF	64KB	SCP PVT CTRL
0x0_3FFF_0000	0x0_3FFF_9FFF	40KB	Reserved part of SCP SoC expansion memory
0x0_3FFF_A000	0x0_3FFF_AFFF	4KB	SCP I2C0 (C2C)
0x0_3FFF_B000	0x0_3FFF_BFFF	4KB	SCP I2C1 (PMIC)
0x0_3FFF_C000	0x0_3FFF_CFFF	4KB	SCP I2C2 (SPD-PCC)
0x0_3FFF_D000	0x0_3FFF_EFFF	8KB	Reserved part of SCP SoC expansion memory
0x0_3FFF_F000	0x0_3FFF_FFFF	4KB	SCC registers
0x0_4000_0000	0x0_43FF_FFFF	64MB	SCP SoC expansion
0x0_4400_0000	0x0_45FF_FFFF	32MB	SCP peripherals
0x0_4600_0000	0x0_47FF_FFFF	32MB	Reserved
0x0_4800_0000	0x0_4BFF_FFFF	64MB	MCP SoC expansion
0x0_4C00_0000	0x0_4DFF_FFFF	32MB	Reserved
0x0_4E00_0000	0x0_4E00_FFFF	64KB	Memory element 0 configuration
0x0_4E01_0000	0x0_4E01_FFFF	64KB	Memory element 0 manager
0x0_4E10_0000	0x0_4E10_FFFF	64KB	Memory element 1 configuration
0x0_4E11_0000	0x0_4E11_FFFF	64KB	Memory element 1 manager
0x0_5000_0000	0x0_507F_FFFF	8MB	Element management peripherals
0x0_5080_0000	0x0_5FFF_FFFF	248MB	Reserved
0x0_6000_0000	0x0_9FFF_FFFF	1GB	System Access Port. Translated to 0x0_4000_0000 to 0x0_7FFF_FFFF of AP memory map.
0x0_A000_0000	0x0_DFFF_FFFF	1GB	System Access Port. Translated to 0x0_0000_0000 to 0x0_3FFF_FFFF of AP memory map with debug address translation not enabled. Translated to 0x4_0000_0000 to 0x4_3FFF_FFFF of AP memory map with debug address translation enabled.
0x0_E000_0000	0x0_E003_FFFF	256KB	Private peripheral bus - Internal.

Table 4-5 SCP memory map (continued)

Address range		Size	Description
From	To		
0x0_E004_0000	0x0_E00F_FFFF	768KB	Private peripheral bus - External.
0x0_E010_0000	0x0_FFFF_FFFF	511MB	Reserved

4.2.6 System Control Processor peripherals memory map

The *System Control Processor* (SCP) memory map of the N1 SDP contains a region associated with the SCP peripherals.

The following figure shows the peripherals region of the SCP memory map.

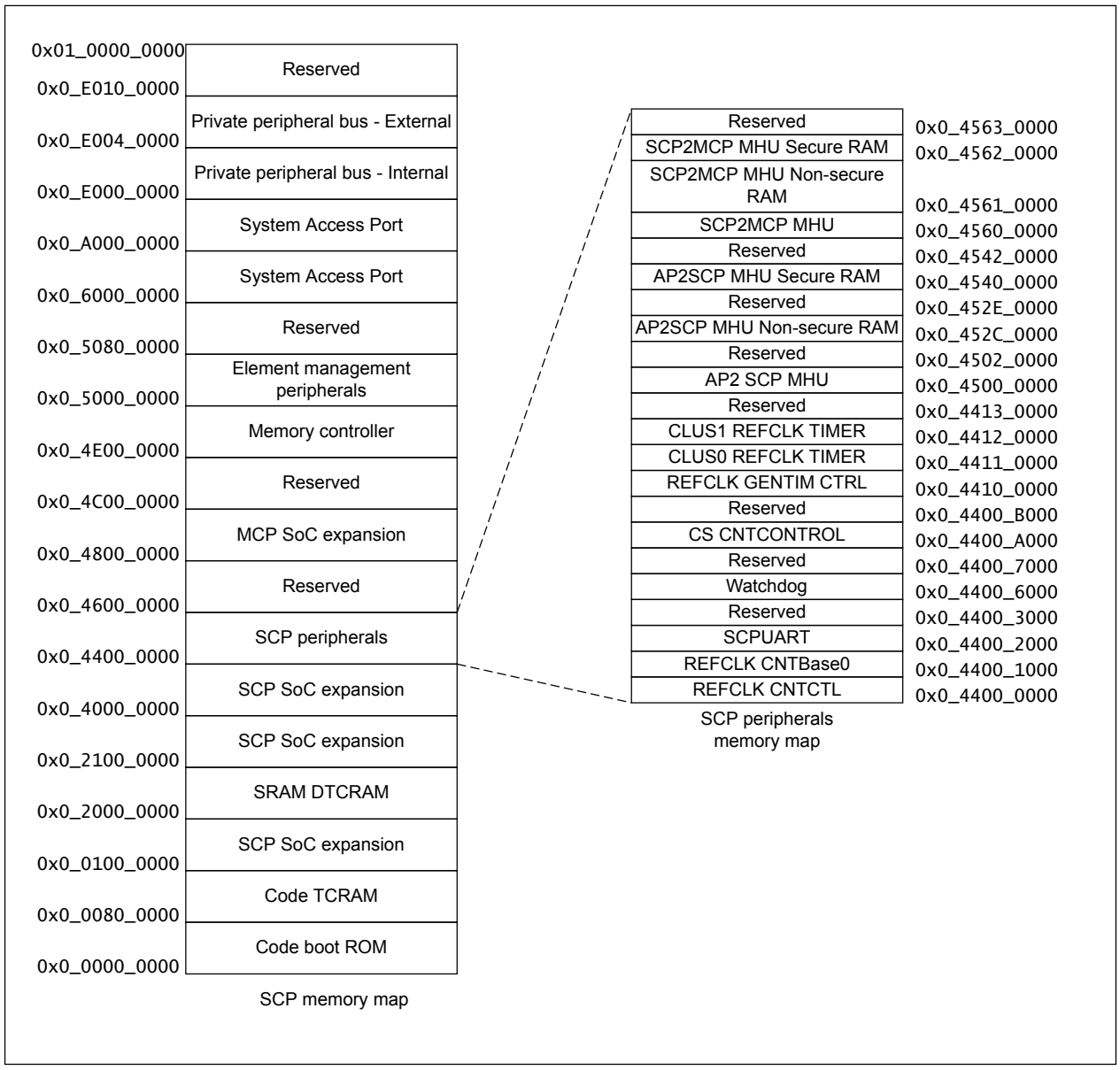

Figure 4-6 SCP peripherals memory map

The following table shows the peripherals region of the N1 SDP SCP memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-6 SCP peripherals memory map

Address range		Size	Description
From	To		
0x00_4400_0000	0x00_4400_0FFF	4KB	REFCLK CNTCTL
0x00_4400_1000	0x00_4400_1FFF	4KB	REFCLK CNTBase0
0x00_4400_2000	0x00_4400_2FFF	4KB	SCPUART
0x00_4400_6000	0x00_4400_6FFF	4KB	Watchdog (SP805)
0x00_4400_A000	0x00_4400_AFFF	4KB	CS CNTCONTROL
0x00_4410_0000	0x00_4C10_FFFF	64KB	REFCLK general timer control
0x00_4411_0000	0x00_4C41_FFFF	64KB	Cluster 0 time frame
0x00_4412_0000	0x00_4C12_FFFF	64KB	Cluster 1 time frame
0x00_4500_0000	0x00_4501_FFFF	128KB	AP2SCP *Message Handling Unit* (MHU)
0x00_452C_0000	0x00_452D_FFFF	128KB	AP2SCP MHU Non-secure RAM
0x00_4540_0000	0x00_4541_FFFF	128KB	AP2SCP MHU Secure RAM
0x00_4560_0000	0x00_4560_FFFF	64KB	SCP2MCH MHU
0x00_4561_0000	0x00_4561_FFFF	64KB	SCP2MCP MHU Non-secure RAM
0x00_4562_0000	0x00_4562_FFFF	64KB	SCP2MCP MHU Secure RAM
0x00_4563_0000	0x00_45FF_FFFF	64KB	Reserved

4.2.7 CoreSight™ system memory map

The N1 SDP Application Processor (AP) memory map contains a region that is associated with the CoreSight debug and trace.

The following figure shows the CoreSight debug and trace memory map.

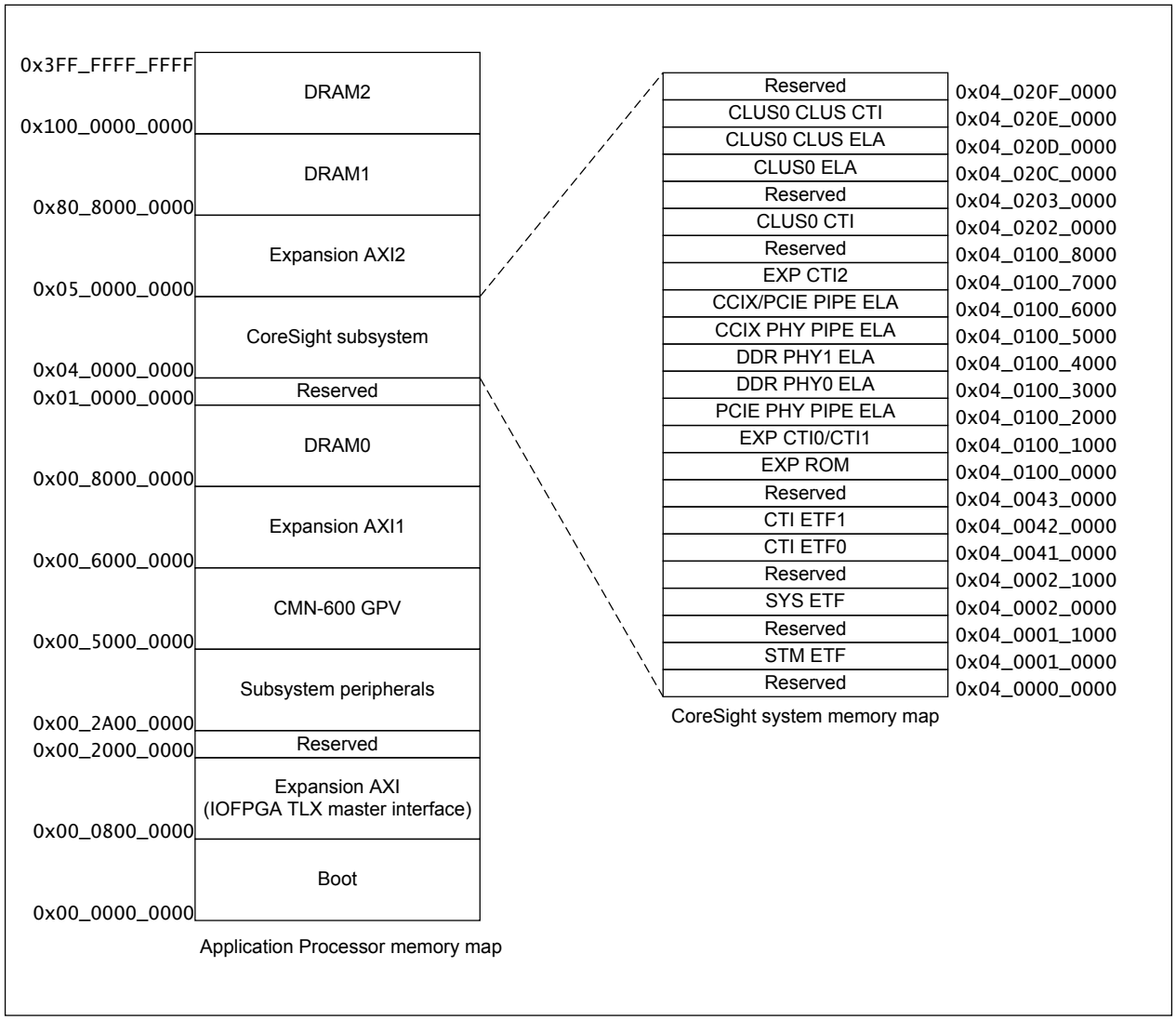

Figure 4-7 CoreSight system memory map

The following table shows the peripherals region of the N1 SDP CoreSight debug and trace memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-7 CoreSight debug and trace memory map

Address range		Size	Description
From	To		
0x04_0000_0000	0x04_0000_FFFF	64KB	Reserved
0x04_0001_0000	0x04_0001_0FFF	4KB	STM ETF
0x04_0002_0000	0x04_0002_0FFF	4KB	SYS ETF
0x04_0041_0000	0x04_0041_FFFF	64KB	CTI ETF0
0x04_0042_0000	0x04_0042_FFFF	64KB	CTI ETF1
0x04_0100_0000	0x04_0100_0FFF	4KB	EXP ROM

Table 4-7 CoreSight debug and trace memory map (continued)

Address range		Size	Description
From	To		
0x04_0100_1000	0x04_0100_1FFF	4KB	EXP CTI0/CTI1
0x04_0100_2000	0x04_0100_2FFF	4KB	PCIE PHY PIPE ELA
0x04_0100_3000	0x04_0100_3FFF	4KB	DDR PHY0 ELA
0x04_0100_4000	0x04_0100_4FFF	4KB	DDR PHY1 ELA
0x04_0100_5000	0x04_0100_5FFF	4KB	CCIX PHY PIPE ELA
0x04_0100_6000	0x04_0100_6FFF	4KB	CCIX/PCIE PIPE ELA
0x04_0100_7000	0x04_0100_7FFF	4KB	EXP CTI2
0x04_0202_0000	0x04_0202_FFFF	64KB	CLUS0 CTI
0x04_020C_0000	0x04_020C_FFFF	64KB	CLUS0 ELA
0x04_020D_0000	0x04_020D_FFFF	64KB	CLUS0 CLUS ELA
0x04_020E_0000	0x04_020E_FFFF	64KB	CLUS0 CLUS CTI

4.2.8 IOFPGA memory map

The following figure shows the memory map of the peripherals inside the IOFPGA.

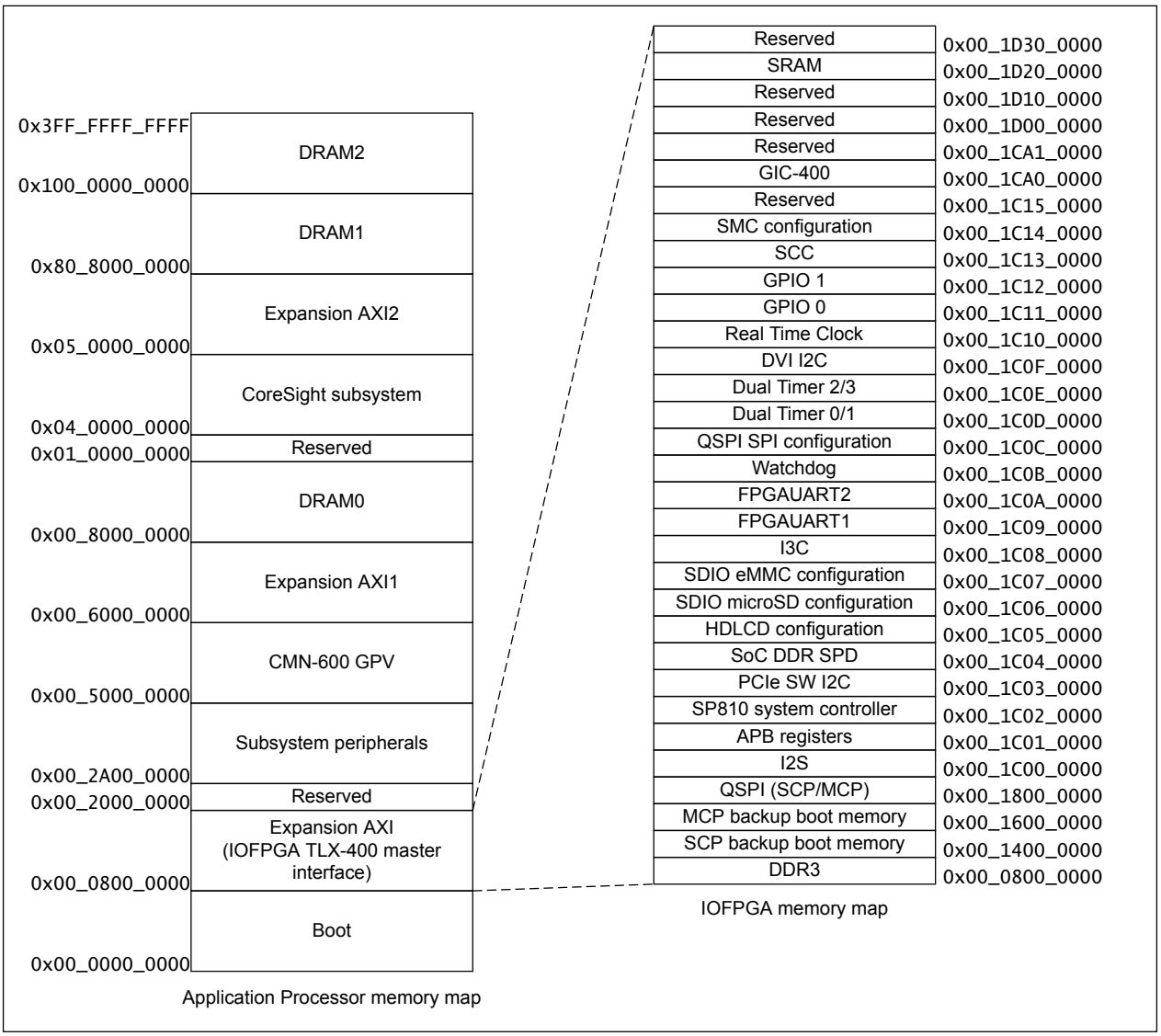

Figure 4-8 IOFPGA memory map

The following table shows the IOFPGA memory map. Undefined locations of the memory map are reserved. Software must not attempt to access these locations.

Table 4-8 IOFPGA memory map

Address range		Size	Description
From	To		
0x0800_0000	0x13FF_FFFF	192MB	DDR3
0x1400_0000	0x15FF_FFFF	32MB	SCP backup boot memory
0x1600_0000	0x17FF_FFFF	32MB	MCP backup boot memory
0x1800_0000	0x1BFF_FFFF	32MB	QSPI (SCP/MCP)

Table 4-8 IOFPGA memory map (continued)

Address range		Size	Description
From	To		
0x1C00_0000	0x1C00_FFFF	64MB	I2S
0x1C01_0000	0x1C01_FFFF	64KB	System registers
0x1C02_0000	0x1C02_FFFF	64KB	System control
0x1C03_0000	0x1C03_FFFF	64KB	PCIe SW I2C
0x1C04_0000	0x1C04_FFFF	64KB	SoC DDR SPD
0x1C05_0000	0x1C05_FFFF	64KB	HDLCD configuration
0x1C06_0000	0x1C06_FFFF	64KB	SDIO microSD configuration
0x1C07_0000	0x1C07_FFFF	64KB	SDIO eMMC configuration
0x1C08_0000	0x1C08_FFFF	64K	I3C
0x1C09_0000	0x1C09_FFFF	64KB	FPGAUART1
0x1C0A_0000	0x1C0A_FFFF	64KB	FPGAUART2
0x1C0B_0000	0x1C0B_FFFF	64KB	Watchdog
0x1C0C_0000	0x1C0C_FFFF	64KB	QSPI SPI configuration
0x1C0D_0000	0x1C0D_FFFF	64KB	Dual Timer 0/1
0x1C0E_0000	0x1C0E_FFFF	64KB	Dual Timer 2/3
0x1C0F_0000	0x1C0F_FFFF	64KB	DVI I2C
0x1C10_0000	0x1C10_FFFF	64KB	Real Time Clock
0x1C11_0000	0x1C11_FFFF	64KB	GPIO 0
0x1C12_0000	0x1C12_FFFF	64KB	GPIO 1
0x1C13_0000	0x1C13_FFFF	64KB	SCC
0x1C14_0000	0x1C14_FFFF	64KB	SMC configuration
0x1C15_0000	0x1C9F_FFFF	8MB	Reserved
0x1CA0_0000	0x1CA0_FFFF	64KB	GIC-400
0x1CA1_0000	0x1D1F_FFFF	8MB	Reserved
0x1D20_0000	0x1D2F_FFFF	1MB	SRAM
0x1D30_0000	0x1FFF_FFFF	45MB	Reserved

4.3 N1 SoC interrupt maps

The N1 SoC contains three independent interrupt maps for the *Application Processors* (APs), the *System Control Processor* (SCP), and the *Manageability Control Processor* (MCP).

This section contains the following subsections:

4.3.1 Application Processor interrupt map

The GIC-600 implements two types of interrupt. Private Peripheral Interrupts (PPIs) exist separately for each core. Shared Peripheral Interrupts (SPIs) are shared between all cores.

The following table shows the Private Peripheral Interrupts (PPI) for the application processors. The map repeats for each core in the subsystem.

Table 4-9 Private peripheral interrupts

ID	Source	Description
20-16	-	Reserved
21	PMBIRQn	SPE interrupt request
22	COMMIRQn	Debug Communications Channel receive or transmit request
23	PMUIRQn	PMU interrupt
24	CTIIRQ	CTI Interrupt
25	VCPUMNTIRQn	Virtual Maintenance Interrupt (PPI6)
26	CNTHPIRQn	Non-secure PL2 Timer event (PPI5)
27	CNTVIRQn	Virtual Timer event (PPI4)
28	CNTHVIRQn	-
29	CNTPSIRQn	Secure PL1 Physical Timer event (PPI1)
30	CNTPNSIRQn	Non-secure PL1 Physical Timer event (PPI2)
31	-	Reserved

The following table shows the Shared Peripheral Interrupts (SPI) for the application processors.

Table 4-10 Shared peripheral interrupts

ID	Source	Description
32	DMC0_pmuirq	PMU event interrupt from DMC0
33	DMC0_comb_err_oflow	Combined Error interrupt overflow from DMC0
34	DMC0_failed_access_int	TZ access error interrupt from DMC0
35	DMC0_ecc_err	ECC Error from DMC0
36	DMC1_pmuirq	PMU event interrupt from DMC1
37	DMC1_comb_err_oflow	Combined Error interrupt overflow from DMC1
38	DMC1_failed_access_int	TZ access error interrupt from DMC1

Table 4-10 Shared peripheral interrupts (continued)

ID	Source	Description
39	DMC1_ecc_err	ECC Error from DMC1
66-40	-	Reserved
67	MCP2APMHU_NS	MHU Non-secure interrupt
68	-	Reserved
69	MCP2APMHU_S	MHU secure interrupt
70	CATU	CATUADDRERROR interrupt
71	ETR	ETRBUFINT interrupt
77-72	-	Reserved
78	CMN600_ INTREQPMU_DTC0	PMU Count Overflow Interrupt
82-79	-	Reserved
83	STM-500	STM-500 Synchronization Interrupt
84	CTI	CTI Trigger output 6 from CTI2
85	CTI	CTI Trigger output 7 from CTI2
86	Trusted Watchdog	Trusted Watchdog interrupt(WS0)
90-87	-	Reserved
91	AP_REFCLK Generic Timer (Secure)	AP_REFCLK Generic Timer Interrupt (Secure)
92	AP_REFCLK Generic Timer (Non-secure)	AP_REFCLK Generic Timer Interrupt (Non-secure)
93	Generic Watchdog	Watchdog WS0 Interrupt
94	Generic Watchdog	Watchdog WS1 Interrupt
95	AP_UART0	AP UART0 interrupt
96	AP_UART1	AP UART1 interrupt
127-97	-	Reserved
128	N1 board	AP external IRQ (AP_EXT_INT)
129	N1 board	AP external Ethernet IRQ (AP_EXT_ETHERNET_INT)
167-130	-	Reserved
168	N1 SoC	GPIO combined IRQ
176-169	N1 SoC	GPIO individual IRQ [7:0]
200-177	-	Reserved
201	N1 SoC	pcie_inta_out
202	N1 SoC	pcie_intb_out
203	N1 SoC	pcie_intc_out
204	N1 SoC	pcie_intd_out
205	N1 SoC	pcie_phy_interrupt_out
206	N1 SoC	pcie_aer_interrupt
207	N1 SoC	pcie_link_down_reset_out

Table 4-10 Shared peripheral interrupts (continued)

ID	Source	Description
208	N1 SoC	pcie_local_interrupt_reset
209	N1 SoC	pcie_performance_data_threshold
210	N1 SoC	pcie_negotiated_speed_change
211	N1 SoC	pcie_link_training_done
212	N1 SoC	pcie_pll_status_rise
213	N1 SoC	pcie_message_fifo_interrupt
214	N1 SoC	pcie_local_interrupt_ras
231-215	-	Reserved
232	N1 SoC	ccix_bus_device_change_irq
233	N1 SoC	ccix_inta_out
234	N1 SoC	ccix_intb_out
235	N1 SoC	ccix_intc_out
236	N1 SoC	ccix_intd_out
237	N1 SoC	ccix_phy_interrupt_out
238	N1 SoC	ccix_aer_interrupt
239	N1 SoC	ccix_link_down_reset_out
240	N1 SoC	ccix_local_interrupt_reset
241	N1 SoC	ccix_performance_data_threshold
242	N1 SoC	ccix_negotiated_speed_change
243	N1 SoC	ccix_link_training_done
244	N1 SoC	ccix_pll_status_rise
245	N1 SoC	ccix_message_fifo_interrupt
246	N1 SoC	ccix_local_interrupt_ras
247	N1 SoC	ccix_hot_reset_irq
248	N1 SoC	ccix_flr_reset_irq
249	N1 SoC	ccix_power_state_change_irq
255-250	-	Reserved
256	MMUTCU1_PMU_IRPT	PMU interrupt
257	MMUTCU1_EVENT_Q_IRPT_S	Event Queue Secure interrupt, indicating Event Queue Non-Empty or Overflow
258	MMUTCU1_CMD_SYNC_IRPT_S(	SYNC Complete Secure interrupt
259	MMUTCU1_GLOBAL_IRPT_S	Global Secure interrupt
260	MMUTCU1_EVENT_Q_IRPT_NS	Event Queue non-Secure interrupt, indicating Event Queue Non-Empty or Overflow
261	MMUTCU1_CMD_SYNC_IRPT_NS	SYNC Complete Non-secure interrupt
262	MMUTCU1_GLOBAL_IRPT_NS	Global Non-secure interrupt

Table 4-10 Shared peripheral interrupts (continued)

ID	Source	Description
263	MMUTCU2_PMU_IRPT	PMU interrupt
264	MMUTCU2_EVENT_Q_IRPT_S	Event Queue Secure interrupt, indicating Event Queue Non-Empty or Overflow
265	MMUTCU2_CMD_SYNC_IRPT_S	SYNC Complete Secure interrupt
266	MMUTCU2_GLOBAL_IRPT_S	Global Secure interrupt
267	MMUTCU2_EVENT_Q_IRPT_NS	Event Queue non-Secure interrupt, indicating Event Queue Non-Empty or Overflow
268	MMUTCU2_CMD_SYNC_IRPT_NS	SYNC Complete Non-secure interrupt
269	MMUTCU2_GLOBAL_IRPT_NS	Global Non-secure interrupt
319-270	-	Reserved
323-320	MMUTBU_PMU_IRPT[3:0]	TBU PMU Interrupt. Allocated to 4 TBUs in the system.
511-324	-	Reserved
512	CLUSTER0SCP ->AP MHU Non-secure	-
513	CLUSTER0SCP ->AP MHU secure	-
514	CLUSTER1SCP ->AP MHU Non-secure	-
515	CLUSTER1SCP ->AP MHU secure	-
575-516	-	Reserved
576	P0_REFCLK_GENTIM	Pn_REFCLK Generic Secure Timer interrupts
577	P0_REFCLK_GENTIM	Pn_REFCLK Generic Secure Timer interrupts
640-578	-	Reserved

4.3.2 System Control Processor interrupt map

The *System Control Processor* (SCP) receives interrupts from several sources.

The sources of the interrupts to the SCP are:

- Application Processor system wakeup interrupts
- CoreSight power and reset request interrupts
- Internal SCP subsystem interrupts
- Expansion SCP interrupts

The interrupts are routed to the Nested Vector Interrupt Controllers in Cortex-M7 processors where they can be managed by software.

The following table shows the SCP interrupts.

Table 4-11 SCP interrupts

ID	Source	Description
NMI	SCP Generic Watchdog	SCP Watchdog(WS0)
0	-	Reserved

Table 4-11 SCP interrupts (continued)

ID	Source	Description
1	CoreSight	CoreSight debug power up request (If there is a separate debug power domain). **Note** SCP Firmware must support optional debug power up rail.
2	CoreSight	CoreSight system power up request
3	CoreSight	CoreSight debug reset request
4	GIC expansion interrupt	External GIC wakeup interrupt. Generated by the logical OR of all the GIC Expansion Interrupts.
15-5	-	Reserved
16	SCP external IRQ (SCP_EXT_INT)	SCP external IRQ (SCP_EXT_INT)
17	GPIO	GPIO combined IRQ
25-18	GPIO	GPIO individual IRQ [7:0]
32-26	-	Reserved
33	SCP REFCLK Generic Timer	REFCLK Physical Timer interrupt
34	GENTIM_SYNC	System generic timer synchronization interrupt
35	CSTS_SYNC	Coresight Time stamp synchronization interrupt
36	-	Reserved
37	CTI	CTI Trigger 0
38	CTI	CTI Trigger 1
39	GICECCFATAL	GIC Fatal ECC failure
40	GICAXIMERR	GIC Fatal AXI Master error
41	-	Reserved
42	AON_UART_INT	Always-on UART interrupt
43	-	Reserved
44	Generic Watchdog	Generic Watchdog timer interrupt WS0
45	Generic Watchdog	Generic Watchdog timer interrupt WS1
46	Trusted Watchdog	Trusted Watchdog timer interrupt WS0
47	Trusted Watchdog	Trusted Watchdog timer interrupt WS1
48	APPS_UART_INT	Applications UART interrupt
49	-	Reserved
50	CPU Core Power Policy Units	Consolidated CPU PPU Interrupt for cores
53-51	-	Reserved
54	CPU Cluster Power Policy Units	Consolidated CPU cluster PPU Interrupt for clusters 0-1
55	CPU Core PLLs	Consolidated CPU PLL Lock for PLLs

Table 4-11 SCP interrupts (continued)

ID	Source	Description
58-56	-	Reserved
59	CPU Core Fault Indicator	Consolidated nFaultIRQ for both clusters
63-60	-	Reserved
64	CPU ECC error interrupts	Consolidated nERRIRQ for both clusters
68-64	-	Reserved
69	Cluster PLLs	Consolidated lock interrupt for cluster PLLs
70	Cluster PLLs	Consolidated unlock interrupt for cluster PLLs
81-71	-	Reserved
82	AP2SCP MHU Non-secure interrupt	Consolidated MHU High Priority Non-Secure interrupt
83	AP2SCP MHU Secure interrupt	Consolidated MHU Secure interrupt for both clusters
84	MCP2SCP MHU Non-secure Interrupt	MCP2SCP MHU High Priority Interrupt
85	MCP2SCP MHU Secure Interrupt	MCP2SCP MHU High Priority Interrupt
89-86	-	Reserved
90	Pn_REFCLK_GENTIM_1_2	Consolidated Pn REFCLK Timer Interrupt for both clusters
93-91	-	Reserved
94	CONS_MMU_TCU_RASIRPT	Consolidated MMU RAS for the interrupt coming from multiple TCUs
95	CONS_MMU_TBU_RASIRPT[NUM_TBUS-1:0]	Consolidated TBU for the interrupts coming from various TBUs
96	INTREQPPU	PPU interrupt from CMN-600
97	INTREQERRNS	Non Secure error handling interrupt from CMN-600
98	INTREQERRS	Secure error handling interrupt from CMN-600
99	INTREQFAULTS	Secure Fault handling interrupt from CMN-600
100	INTREQFAULTNS	Non Secure Fault handling interrupt from CMN-600
101	INTREQPMU	PMU count overflow interrupt
119-102	-	Reserved
127-120	DBGCH[0-7]_PPU_INT	-
129	-	Reserved
130	Power Integration Kit	Debug PIK Interrupt
131	LOGIC_PPU_INT	LOGIC_PPU_INT
134-132	-	Reserved
135	SRAM_PPU_INT	SRAM PPU Interrupt
138-136	-	Reserved
139	MCP WS1	MCP Watchdog reset
140	SYSPLL_LOCK	Sys PLL Lock
141	SYSPLL_UNLOCK	Sys PLL Unlock
142	INTPLL_LOCK	Interconnect PLL Lock

Table 4-11 SCP interrupts (continued)

ID	Source	Description
143	INTPLL_UNLOCK	Interconnect PLL UnLock
173-144	-	Reserved
174	DMC_PLL_LOCK	DMC PLL Lock
175	DMC_PLL_UNLOCK	DMC PLL Unlock
179-176	-	Reserved
180	DMC0 Interrupts	DMC0 _misc oflow
181		DMC0 _err_oflow
182		DMC0 _ecc_err_int
183		DMC0 _misc_access_int
184		DMC0 _temperature_event_int
185		DMC0 _failed_access_int
186		DMC0 _mgr_int
187	DMC1 Interrupts	DMC1 _misc oflow
188		DMC1 _err_oflow
189		DMC1 _ecc_err_int
190		DMC1 _misc_access_int
191		DMC1 _temperature_event_int
192		DMC1 _failed_access_int
193		DMC1 _mgr_int
208	SCP C2C I2C	SCP C2C I2C interrupt (I2C0)
209	SCP PMIC I2C	SCP PMIC I2C interrupt (I2C1)
210	SCP SPD-PCC I2C	SCP SPD-PCC I2C interrupt (I2C2)
211	SCP-QSPI	SCP QSPI interrupt
212	PVT controller	PVT controller interrupt
218-213	-	Reserved
219	ccix_bus_device_change_irq	ccix_bus_device_change_irq
220	ccix_inta_out	ccix_inta_out
221	ccix_intb_out	ccix_intb_out
222	ccix_intc_out	ccix_intc_out
223	ccix_intd_out	ccix_intd_out
224	ccix_phy_interrupt_out	ccix_phy_interrupt_out
225	ccix_aer_interrupt	ccix_aer_interrupt
226	ccix_link_down_reset_out	ccix_link_down_reset_out
227	ccix_local_interrupt_reset	ccix_local_interrupt_reset
228	ccix_performance_data_threshold	ccix_performance_data_threshold

Table 4-11 SCP interrupts (continued)

ID	Source	Description
229	ccix_negotiated_speed_change	ccix_negotiated_speed_change
230	ccix_link_training_done	ccix_link_training_done
231	ccix_pll_status_rise	ccix_pll_status_rise
232	ccix_message_fifo_interrupt	ccix_message_fifo_interrupt
233	ccix_local_interrupt_ras	ccix_local_interrupt_ras
234	ccix_hot_reset_irq	ccix_hot_reset_irq
235	ccix_flr_reset_irq	ccix_flr_reset_irq
236	ccix_power_state_change_irq	ccix_power_state_change_irq
237	pcie_aer_interrupt	pcie_aer_interrupt
238	pcie_local_interrupt_reset	pcie_local_interrupt_reset
239	pcie_local_interrupt_ras	pcie_local_interrupt_ras

4.3.3 Manageability Control Processor interrupt map

The *Manageability Control Processor* (MCP) receives interrupts from several sources.

The sources of the interrupts to the MCP are:
- Application Processor system wakeup interrupts
- CoreSight power and reset request interrupts
- Internal MCP subsystem interrupts
- Expansion MCP interrupts

The interrupts are routed to the Nested Vector Interrupt Controllers in Cortex-M7 processors where they can be managed by software.

The following table shows the MCP interrupts.

Table 4-12 MCP interrupts

ID	Source	Description
NMI	MCP Generic Watchdog	MCP Watchdog(WS0)
0	-	Reserved
1	CoreSight	CoreSight debug power up request (If there is a separate debug power domain). ——— **Note** ——— MCP Firmware must support optional debug power up rail. ———
2	CoreSight	CoreSight system power up request
3	CoreSight	CoreSight debug reset request
4	GIC expansion interrupt	External GIC wakeup interrupt. Generated by the logical OR of all the GIC Expansion Interrupts.
15-5	-	Reserved
16	MCP external IRQ (MCP_EXT_INT)	MCP external IRQ (MCP_EXT_INT)
17	GPIO	GPIO combined IRQ

Table 4-12 MCP interrupts (continued)

ID	Source	Description
25-18	GPIO	GPIO individual IRQ [7:0]
32-26	-	Reserved
33	MCP REFCLK Generic Timer	REFCLK Physical Timer interrupt
34	Non-secure AP2MCP MHU	MHU Non-Secure interrupt
35	-	Reserved
36	AP2MCP Secure MHU	MHU Secure interrupt
37	CTI	CTI Trigger 0
38	CTI	CTI Trigger 1
41-39	-	Reserved
42	MCP_UART0_INT	Always-on UART interrupt
83-43	MCP_UART1_INT	Always-on UART interrupt
84	MCP2SCP MHU Non-secure Interrupt	MCP2SCP MHU High Priority Interrupt
85	MCP2SCP MHU Secure Interrupt	MCP2SCP MHU High Priority Interrupt
93-86	-	Reserved
94	MMU_TBU_RASIRPT[NUM_TBUS-1:0]	Consolidated MMU RAS for the interrupt coming from multiple TCUs
95	MMU_TBU_RASIRPT[NUM_TBUS-1:0]	Consolidated TBU for the interrupts coming from multiple TBUs
96	INTREQPPU	PPU interrupt from CMN-600
97	INTREQERRNS	Non-secure error handling interrupt from CMN-600
98	INTREQERRS	Secure error handling interrupt from CMN-600
99	INTREQFAULTS	Secure Fault handling interrupt from CMN-600
100	INTREQFAULTNS	Non-secure Fault handling interrupt from CMN-600
101	INTREQPMU	PMU count overflow interrupt
138-102	-	Reserved
139	MCP WS1	MCP Watchdog reset
179-140	SYSPLL_LOCK	Sys PLL Lock
180	DMC0 Interrupts	DMC0 _misc oflow
181		DMC0 _err_oflow
182		DMC0 _ecc_err_int
183		DMC0 _misc_access_int
184		DMC0 _temperature_event_int
185		DMC0 _failed_access_int
186		DMC0 _mgr_int

Table 4-12 MCP interrupts (continued)

ID	Source	Description
187	DMC1 Interrupts	DMC1 _misc oflow
188		DMC1 _err_oflow
189		DMC1 _ecc_err_int
190		DMC1 _misc_access_int
191		DMC1 _temperature_event_int
192		DMC1 _failed_access_int
193		DMC1 _mgr_int
208	MCP C2C I2C	MCP C2C I2C interrupt (I2C0)
209	MCP BMC-PCC I2C	MCP BMC-PCC I2C interrupt (I2C1)
210	MCP-QSPI	MCP QSPI interrupt
219-211	-	Reserved
220	pcie_aer_interrupt	pcie_aer_interrupt
221	pcie_local_interrupt_reset	pcie_local_interrupt_reset
222	pcie_local_interrupt_ras	pcie_local_interrupt_ras
223	ccix_aer_interrupt	ccix_aer_interrupt
224	ccix_local_interrupt_reset	ccix_phy_interrupt_out
225	ccix_local_interrupt_ras	ccix_aer_interrupt
239-226	ccix_link_down_reset_out	ccix_link_down_reset_out

4.4 System Security Control registers

The *System Security Control* (SSC) interface in the N1 SoC controls system-wide security features.

These features include the following:

- Selection of and internal sources for Debug Authentication signals
- General Purpose register for secure state storage

The registers are in the Always-on power domain so their states are maintained when the system is powered down except when VSYS is powered down.

This section contains the following subsections:

4.4.1 System Security Control registers summary

The base memory address of the SSC registers is `0x0_2A42_0000` in the subsystem peripherals region of the *Application Processor* (AP) memory map.

The following table shows the SSC registers in offset order from the base memory address. Undefined registers are reserved. Software must not attempt to access these registers.

Table 4-13 SCC registers summary

Offset	Name	Type	Reset	Width	Description
`0x0010`	SSC_DBGCFG_STAT	RO	`0x0001_0000`	32	Debug authentication configuration status See *4.4.2 SSC_DBGCFG_STAT Register* on page 4-107.
`0x0014`	SSC_DBGCFG _SET	WO	N/A	32	Debug authentication configuration set. See *4.4.3 SSC_DBGCFG _SET Register* on page 4-108.
`0x0018`	SSC_DBGCFG _CLR	WO	N/A	32	Debug authentication configuration clear. See *4.4.4 SSC_DBGCFG _CLR Register* on page 4-109.

Table 4-13 SCC registers summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0028	SSC_AUXDBGCFG	RW	0x0000_0000	32	Auxiliary debug authentication register. See *4.4.5 SSC_AUXDBGCFG Register* on page 4-110.
0x0030	SSC_GPRETN	RW	0x0000_0000	32	General purpose secure retention status. See *4.4.6 SSC_GPRETN Register* on page 4-111.
0x0040	SSC_VERSION	RO	0x1004_17B0	32	Version register See *4.4.7 SSC_VERSION Register* on page 4-112.
0x0100-0x017C	SSC_SW_SCRATCH[31:0]	RW	0x0000_0000	32	Software defined scratch registers See *4.4.8 SSC_SW_SCRATCH Registers* on page 4-112.
0x0200-0x02FC	SSC_SW_CAP[63:0]	RW	0x0000_0000	32	Software defined CAP registers. See *4.4.9 SSC_SW_CAP Registers* on page 4-112.
0x0300	SSC_SW_CAPCTRL	RW	0x0000_0000	32	Software defined CAP control registers. See *4.4.10 SSC_SW_CAPCTRL Register* on page 4-113.
0x0500	SSC_CHIPID_ST	RO	0x0000_0000	32	CHIPID status register. See *4.4.11 SSC_CHIPID_ST Register* on page 4-113.
0x0FD0	SSC_PID4	RO	0x0000_0004	32	Peripheral ID4 register See *4.4.12 SSC_PID4 Register* on page 4-114.
0x0FE0	SSC_PID0	RO	0x0000_0044	32	Peripheral ID0 register See *4.4.13 SSC_PID0 Register* on page 4-115.
0x0FE4	SSC_PID1	RO	0x0000_00B8	32	Peripheral ID1 register See *4.4.14 SSC_PID1 Register* on page 4-115.
0x0FE8	SSC_PID2	RO	0x0000_000B	32	Peripheral ID2 register See *4.4.15 SSC_PID2 Register* on page 4-116.
0x0FF0	COMPID0	RO	0x0000_000D	32	Component ID0 register See *4.4.16 SSC_COMPID0 Register* on page 4-116.
0x0FF4	COMPID1	RO	0x0000_00F0	32	Component ID1 register See *4.4.17 SSC_COMPID1 Register* on page 4-117.

Table 4-13 SCC registers summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0FF8	COMPID2	RO	0x0000_0005	32	Component ID2 register See *4.4.18 SSC_COMPID2 Register* on page 4-117.
0x0FFC	COMPID3	RO	0x0000_00B1	32	Component ID3 register See *4.4.19 SSC_COMPID3 Register* on page 4-118.

4.4.2 SSC_DBGCFG_STAT Register

The SSC_DBGCFG_STAT Register characteristics are:

Purpose

Controls how the Debug Authentication signals are to be driven, either from an external source, or internally using build-in register bits, also implemented using this register.
Defines the values of the Debug Authentication signals when they are configured to be internally driven.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_DBGCFG_STAT Register bit assignments.

Table 4-14 SSC_DBGCFG_STAT Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7]	SPIDEN_SEL_STAT	RO	Selects between SPIDEN external or internal drive: 0b0: External. 0b1: Internal. If external mode is selected SPIDEN is driven by top-level configuration input SPIDEN_CFG. Reset value 0b0.
[6]	SPIDEN_INT_STAT	RO	SPIDEN internal drive value Reset value 0b0.

Table 4-14 SSC_DBGCFG_STAT Register bit assignments (continued)

Bits	Name	Type	Function
[5]	SPNIDEN_SEL_STAT	RO	Selects between SPNIDEN external or internal drive: `0b0`: External. `0b1`: Internal. If external mode is selected SPNIDEN is driven by top-level configuration input. Reset value `0b0`.
[4]	SPNIDEN_INT_STAT	RO	SPNIDEN internal drive value Reset value `0b0`.
[3]	DEVICEEN_SEL_STAT	RO	Selects between DEVICEEN external or internal drive: `0b0`: External. `0b1`: Internal. If external mode is selected DEVICEEN is driven by top-level configuration input. Reset value `0b0`.
[2]	DEVICEEN_INT_STAT	RO	DEVICEEN internal drive value Reset value `0b0`.
[1:0]	-	-	Reserved.

4.4.3 SSC_DBGCFG _SET Register

The SSC_DBGCFG _SET Register characteristics are:

Purpose

The SSC_DBGCFG _SET register is a Secure access only write-only memory mapped register. This register is associated with the SSC_DBGCFG _STAT register. Writing `0b1` to a particular field in the SSC_DBGCFG _SET register sets the corresponding bit in the SSC_DBGCFG _STAT register to `0b1`.

Usage constraints

This register is write-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_DBGCFG _SET Register bit assignments.

Table 4-15 SSC_DBGCFG_SET Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7]	SPIDEN_SEL_SET	RO	Sets SPIDEN_SEL_STAT to `0b1`: `0b0`: No effect. `0b1`: Set SPIDEN_SEL_STAT to `0b1`.
[6]	SPIDEN_INT_SET	RO	Sets SPIDEN_INT_STAT to `0b1`: `0b0`: No effect. `0b1`: Set SPIDEN_INT_STAT to `0b1`.
[5]	SPNIDEN_SEL_SET	RO	Sets SPNIDEN_SEL_STAT to `0b1`: `0b0`: No effect. `0b1`: Set SPNIDEN_INT_STAT to `0b1`.
[4]	SPNIDEN_INT_SET	RO	Sets SPNIDEN_INT_STAT to `0b1`: `0b0`: No effect. `0b1`: Set SPNIDEN_INT_STAT to `0b1`.
[3]	DEVICEEN_SEL_SET	RO	Sets DEVICEEN_SEL_STAT to `0b1`: `0b0`: No effect. `0b1`: Set DEVICEEN_SEL_STAT to `0b1`.
[2]	DEVICEEN_INT_SET	RO	Sets DEVICEEN_INT_STAT to `0b1`: `0b0`: No effect. `0b1`: Set DEVICEEN_INT_STAT to `0b1`.
[1:0]	-	-	Reserved.

4.4.4 SSC_DBGCFG _CLR Register

The SSC_DBGCFG _CLR Register characteristics are:

Purpose

The SSC_DBGCFG _CLR register is a Secure access only write-only memory mapped register. This register is associated with the SSC_DBGCFG _STAT register. Writing`0b1` to a particular field in the SSC_DBGCFG _CLR register clears the corresponding bit in the SSC_DBGCFG _STAT register to `0b0`.

Usage constraints

This register is write-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_DBGCFG _CLR Register bit assignments.

Table 4-16 SSC_DBGCFG_CLR Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7]	SPIDEN_SEL_CLR	RO	Clears SPIDEN_SEL_STAT to `0b1`: `0b0`: No effect. `0b1`: Clear SPIDEN_SEL_STAT to `0b0`.
[6]	SPIDEN_INT_CLR	RO	Clears SPIDEN_INT_STAT to `0b1`: `0b0`: No effect. `0b1`: Clear SPIDEN_INT_STAT to `0b0`.
[5]	SPNIDEN_SEL_CLR	RO	Clears SPNIDEN_SEL_STAT to `0b1`: `0b0`: No effect. `0b1`: Clear SPNIDEN_INT_STAT to `0b0`.
[4]	SPNIDEN_INT_CLR	RO	Clears SPNIDEN_INT_STAT to `0b1`: `0b0`: No effect. `0b1`: Clear SPNIDEN_INT_STAT to `0b0`.
[3]	DEVICEEN_SEL_CLR	RO	Clears DEVICEEN_SEL_STAT to `0b1`: `0b0`: No effect. `0b1`: Clear DEVICEEN_SEL_STAT to `0b0`.
[2]	DEVICEEN_INT_CLR	RO	Clears DEVICEEN_INT_STAT to `0b0`: `0b0`: No effect. `0b1`: Clear DEVICEEN_INT_STAT to `0b0`.
[1:0]	-	-	Reserved.

4.4.5 SSC_AUXDBGCFG Register

The SSC_AUXDBGCFG Register characteristics are:

Purpose

The SSC_AUXDBGCFG register is a Secure access only read-write register. The register provides override control of the debug authentication signals **DBGEN** and **NIDEN**

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_AUXDBGCFG Register bit assignments.

Table 4-17 SSC_AUXDBGCFG Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1:0]	INTERNAL_DEBUG_OVERRIDE	RW	`0b00`: Enable Non-secure self-hosted debug. **DBGEN** and **NIDEN** inputs to the application processors are HIGH. `0b01`: Disable Invasive, Non-secure self-hosted debug. Enable Non-invasive, Non-secure self-hosted debug. **DBGEN** inputs to the application processors are LOW and **NIDEN** inputs to the application processors are HIGH. `0b1`: Disable Non-secure self-hosted debug. **DBGEN** and **NIDEN** inputs to the application processors are LOW. Reset value `0b00`.

Note

Arm strongly recommends that this register is not used, and that you leave both bits at their reset value.

4.4.6 SSC_GPRETN Register

The SSC_GPRETN Register characteristics are:

Purpose

The SSC_GPRETN register is a secure access read/write memory mapped register that provides 16 bit general storage for security purposes. The register resets only on system powerup reset.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_GPRETN Register bit assignments.

Table 4-18 SSC_GPRETN Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:0]	GPRETN	RW	General-purpose register for Secure state storage. Reset value `0x0000`.

4.4.7 SSC_VERSION Register

The SSC_VERSION Register characteristics are:

Purpose

The SSC_VERSION register is a Secure access read-only memory mapped register that specifies the N1 SoC version ID for security purposes.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_VERSION Register bit assignments.

Table 4-19 SSC_VERSION Register bit assignments

Bits	Name	Type	Function
[31:28]	CONFIGURATION	RO	Equals `0b0001` on N1 SoC.
[27:24]	MAJOR_REVISION	RO	Equals `0b0000` on N1 SoC.
[23:20]	MINOR_REVISION	RO	Equals `0b0000` on N1 SoC.
[19:12]	DESIGNER_ID	RO	Equals Arm identifier `0x41` on N1 SoC.
[11:0]	PART_NUMBER	RO	Equals Arm identifier `0x7B0` on N1 SoC.

4.4.8 SSC_SW_SCRATCH Registers

The SSC_SW_SCRATCH Register characteristics are:

Purpose

The SSC_SW_SCRATCH registers are scratch registers for use by software.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_SW_SCRATCH Register bit assignments.

Table 4-20 SSC_SW_SCRATCH Register bit assignments

Bits	Name	Type	Function
[31:0]	SCRATCH	RW	Software scratch values Reset value `0x0000_0000`

4.4.9 SSC_SW_CAP Registers

The SSC_SW_CAP Register characteristics are:

Purpose

The SSC_SW_CAP registers are capability registers used by the System Control Processor (SCP) software to record the design configuration.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_SW_CAP Register bit assignments.

Table 4-21 SSC_SW_CAP Register bit assignments

Bits	Name	Type	Function
[31:0]	SW_CAP	RW	SCP software defined capability registers. Reset value `0x0000_0000`

4.4.10 SSC_SW_CAPCTRL Register

The SSC_SW_CAPCTRL Register characteristics are:

Purpose

The SSC_SW_CAPCTRL register contains a stick bit to enable writing to the SSC_SW_CAP registers.

Usage constraints

Once set, the active bit, bit[0] cannot be cleared until **SoC_nPOR** is asserted.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_SW_CAPCTRL Register bit assignments.

Table 4-22 SSC_SW_CAPCTRL Register bit assignments

Bits	Name	Type	Function
[31:1]	-	-	Reserved.
[0]	SW_CAP_WR_EN	RO	Sticky bit to enable writing to SSC_SW_CAP registers. `0b0`: Enable writes. `0b1`: Disable writes. Once set to `0b1`, this bit cannot be cleared until **SoC_nPOR** is asserted. Reset value `0b0`.

4.4.11 SSC_CHIPID_ST Register

The SSC_CHIPID_ST Register characteristics are:

Purpose

The SSC_CHIPID_ST register stores the CHIPID status for the node when there are multiple sockets.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_CHIPID_ST Register bit assignments.

Table 4-23 SSC_CHIPID_ST Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[8]	MULTI_CHIP_MODE	RO	Multi-chip mode tie-off value. `0b0`: Single chip. `0b1`: Multi-chip. Reset value `0b0`.
[7:6]	-	-	Reserved.
[5:0]	CHIP_ID	RO	Tie-off value in multi-chip mode. This is `0b0` for single chip mode. Reset value `0b000000`

4.4.12 SSC_PID4 Register

The SSC_PID4 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_PID4 Register bit assignments.

Table 4-24 SSC_PID4 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:4]	SIZE	RO	LOG2 of the number of 4KB blocks occupied by the interface. Reset value `0x0`.
[3:0]	DES_2	RO	JEP106 continuation code to identify designer Reset value `0x4` for Arm

4.4.13 SSC_PID0 Register

The SSC_PID0 Register characteristics are:

Purpose
Stores peripheral identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_PID0 Register bit assignments.

Table 4-25 SSC_PID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PART_0	RO	Bits [7:0] of part number Reset value `0x44`.

4.4.14 SSC_PID1 Register

The SSC_PID1 Register characteristics are:

Purpose
Stores peripheral identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_PID1 Register bit assignments.

Table 4-26 SSC_PID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:4]	DES_0	RO	Bits[3:0] of JEP identity. Reset value `0xB`.
[3:0]	PART_1	RO	Bits[11:8] of part number. Reset value `0x8`.

4.4.15 SSC_PID2 Register

The SSC_PID2 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_PID2 Register bit assignments.

Table 4-27 SSC_PID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:4]	REVISION	RO	Revision number. Reset value `0x0`.
[3]	JEDEC	RO	JEDEC ID. Reset value `0b1`.
[2:0]	DES_1	RO	Designer ID. Reset value `0b011`.

4.4.16 SSC_COMPID0 Register

The SSC_COMPID0 Register characteristics are:

Purpose

The SSC_COMPID0 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_COMPID0 Register bit assignments.

Table 4-28 SSC_COMPID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID0	RO	Component ID 0 information. Reset value `0x0D`.

4.4.17 SSC_COMPID1 Register

The SSC_COMPID1 Register characteristics are:

Purpose

The SSC_COMPID1 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_COMPID1 Register bit assignments.

Table 4-29 SSC_COMPID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID1	RO	Component ID 1 information. Reset value `0xF0`.

4.4.18 SSC_COMPID2 Register

The SSC_COMPID2 Register characteristics are:

Purpose

The SSC_COMPID2 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_COMPID2 Register bit assignments.

Table 4-30 SSC_COMPID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID2	RO	Component ID 2 information. Reset value `0x05`.

4.4.19 SSC_COMPID3 Register

The SSC_COMPID3 Register characteristics are:

Purpose

The SSC_COMPID3 register stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.4.1 System Security Control registers summary* on page 4-105.

The following table shows the SSC_COMPID3 Register bit assignments.

Table 4-31 SSC_COMPID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SSC_COMPID3	RO	Component ID 3 information. Reset value `0xB1`.

4.5 Serial Configuration Control registers

The *Serial Configuration Control* (SCC) registers contain the initial settings of blocks before bootup. Write and read accesses to these registers during run-time enable software to alter and to read block settings.

This section contains the following subsections:

4.5.1 Serial Configuration Control registers summary

The base memory address of the SCC registers in the N1 SDP is `0x0_3FFF_F000` in the *System Control Processor* (SCP) SoC expansion region of the SCP memory map.

The following table shows the SCC registers in offset order from the base memory address. Undefined registers are reserved. Software must not attempt to access these registers.

Table 4-32 SCC registers summary

Offset	Name	Type	Reset	Width	Description
0x0004	PMCLK_DIV	RW/RO	0x0001_0001	32	See *4.5.2 PMCLK_DIV Register* on page 4-124.
0x000C	SYSAPBCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.3 SYSAPBCLK_CTRL Register* on page 4-125.
0x0010	SYSAPBCLK_DIV	RW/RO	0x0013_0013	32	See *4.5.4 SYSAPBCLK _DIV Register* on page 4-126.
0x0018	IOFPGA_TMIF2XCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.5 IOFPGA_TMIF2XCLK_CTRL Register* on page 4-127.
0x001C	IOFPGA_TMIF2XCLK_DIV	RW/RO	0x0000_0000	32	See *4.5.6 IOFPGA_TMIF2XCLK_DIV Register* on page 4-128.
0x0024	IOFPGA_TSIF2XCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.7 IOFPGA_TSIF2XCLK_CTRL Register* on page 4-128.
0x0028	IOFPGA_TSIF2XCLK_DIV	RW/RO	0x000B_000B	32	See *4.5.8 IOFPGA_TSIF2XCLK_DIV Register* on page 4-129.
0x0030	SCPNICCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.9 SCPNICCLK_CTRL Register* on page 4-130 .
0x0034	SCPNICCLK_DIV	RW/RO	0x0000_0000	32	See *4.5.10 SCPNICCLK_DIV Register* on page 4-131.
0x003C	SCPI2CCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.11 SCPI2CCLK_CTRL Register* on page 4-131.
0x0040	SCPI2CCLK_DIV	RW/RO	0x000F_000F	32	See *4.5.12 SCPI2CCLK_DIV Register* on page 4-132.
0x0048	SCPQSPICLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.13 SCPQSPICLK_CTRL Register* on page 4-133.
0x004C	SCPQSPICLK_DIV	RW/RO	0x0000_0000	32	See *4.5.14 SCPQSPICLK_DIV Register* on page 4-134.
0x0054	SENSORCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.15 SENSORCLK_CTRL Register* on page 4-134.
0x0058	SENSORCLK_DIV	RW/RO	0x0017_0017	32	See *4.5.16 SENSORCLK_DIV Register* on page 4-135.
0x0060	MCPNICCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.17 MCPNICCLK_CTRL Register* on page 4-136.
0x0064	MCPNICCLK_DIV	RW/RO	0x0000_0000	32	See *4.5.18 MCPNICCLK_DIV Register* on page 4-137.
0x006C	MCPI2CCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.19 MCPI2CCLK_CTRL Register* on page 4-137.
0x0070	MCPI2CCLK_DIV	RW/RO	0x0017_0017	32	See *4.5.20 MCPI2CCLK_DIV Register* on page 4-138.
0x0078	MCPQSPICLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.21 MCPQSPICLK_CTRL Register* on page 4-139.
0x007C	MCPQSPICLK_DIV	RW/RO	0x0000_0000	32	See *4.5.22 MCPQSPICLK_DIV Register* on page 4-140.
0x0084	PCIEAXICLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.23 PCIEAXICLK_CTRL Register* on page 4-140.

Table 4-32 SCC registers summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0088	PCIEAXICLK_DIV	RW/RO	0x0001_0001	32	See *4.5.24 PCIEAXICLK_DIV Register* on page 4-141.
0x0090	CCIXAXICLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.25 CCIXAXICLK_CTRL Register* on page 4-142.
0x0094	CCIXAXICLK_DIV	RW/RO	0x0001_0001	32	See *4.5.26 CCIXAXICLK_DIV Register* on page 4-143.
0x009C	PCIEAPBCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.27 PCIEAPBCLK_CTRL Register* on page 4-143.
0x00A0	PCIEAPBCLK_DIV	RW/RO	0x000B_000B	32	See *4.5.28 PCIEAPBCLK_DIV Register* on page 4-144.
0x00A8	CCIXAPBCLK_CTRL	RW/RO	0x0000_0101	32	See *4.5.29 CCIXAPBCLK_CTRL Register* on page 4-145.
0x00AC	CCIXAPBCLK_DIV	RW/RO	0x000B_000B	32	See *4.5.30 CCIXAPBCLK_DIV Register* on page 4-146.
0x00F0	SYS_CLK_EN	RW	0x0000_3FF7	32	See *4.5.31 SYS_CLK_EN Register* on page 4-146.
0x0100	CPU0_PLL_CTRL0	RW	0x8010_3000	32	See *4.5.32 CPU0_PLL_CTRL0 Register* on page 4-148.
0x0104	CPU0_PLL_CTRL1	RW/RO	0x9100_0000	32	See *4.5.33 CPU0_PLL_CTRL1 Register* on page 4-149.
0x0108	CPU1_PLL_CTRL0	RW	0x8010_3000	32	See *4.5.34 CPU1_PLL_CTRL0 Register* on page 4-150.
0x010C	CPU1_PLL_CTRL1	RW/RO	0x9100_0000	32	See *4.5.35 CPU1_PLL_CTRL1 Register* on page 4-151.
0x0110	CLUS_PLL_CTRL0	RW	0x8010_2000	32	See *4.5.36 CLUS_PLL_CTRL0 Register* on page 4-152.
0x0114	CLUS_PLL_CTRL1	RW/RO	0x9100_0000	32	See *4.5.37 CLUS_PLL_CTRL1 Register* on page 4-153.
0x0118	SYS_PLL_CTRL0	RW	0x8010_3000	32	See *4.5.38 SYS_PLL_CTRL0 Register* on page 4-154.
0x011C	SYS_PLL_CTRL1	RW/RO	0x9100_0000	32	See *4.5.39 SYS_PLL_CTRL1 Register* on page 4-155.
0x0120	DMC_PLL_CTRL0	RW	0x8020_2000	32	See *4.5.40 DMC_PLL_CTRL0 Register* on page 4-156.
0x0124	DMC_PLL_CTRL1	RW/RO	0x9100_0000	32	See *4.5.41 DMC_PLL_CTRL1 Register* on page 4-157.
0x0128	INT_PLL_CTRL0	RW	0x8010_2000	32	See *4.5.42 INT_PLL_CTRL0 Register* on page 4-158.
0x012C	INT_PLL_CTRL1	RW/RO	0x9100_0000	32	See *4.5.43 INT_PLL_CTRL1 Register* on page 4-159.
0x0150	SYS_MAN_RESET	RW	0x0000_0C00	32	See *4.5.44 SYS_MAN_RESET Register* on page 4-160.
0x0160	BOOT_CTL	RW/RO	0x0000_0000	32	See *4.5.45 BOOT_CTL Register* on page 4-162.
0x0164	BOOT_CTRL_STA	RW/RO	0x0000_0000	32	See *4.5.46 BOOT_CTRL_STA Register* on page 4-163.

Table 4-32 SCC registers summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0168	SCP_BOOT_ADR	RW/RO	0x0000_0000	32	See *4.5.47 SCP_BOOT_ADR Register* on page 4-163.
0x016C	MCP_BOOT_ADR	RW/RO	0x0000_0000	32	See *4.5.48 MCP_BOOT_ADR Register* on page 4-164.
0x0170	PLATFORM_CTRL	RW/RO	0x0000_0000	32	See *4.5.49 PLATFORM_CTRL Register* on page 4-164.
0x0174	TARGETIDAPP	RW/RO	0x07B0_0477	32	See *4.5.50 TARGETIDAPP Register* on page 4-165.
0x0178	TARGETIDSCP	RW/RO	0x07B1_0477	32	See *4.5.51 TARGETIDSCP Register* on page 4-165.
0x017C	TARGETIDMCP	RW/RO	0x07B2_0477	32	See *4.5.52 TARGETIDMCP Register* on page 4-166.
0x0180	BOOT_GPR0	RW/RO	0x0000_0000	32	See *4.5.53 BOOT_GPR0 Register* on page 4-166.
0x0184	BOOT_GPR1	RW/RO	0x0000_0000	32	See *4.5.54 BOOT_GPR1 Register* on page 4-167.
0x0188	BOOT_GPR2	RW/RO	0x0000_0000	32	See *4.5.55 BOOT_GPR2 Register* on page 4-167.
0x018C	BOOT_GPR3	RW/RO	0x0000_0000	32	See *4.5.56 BOOT_GPR3 Register* on page 4-167.
0x0190	BOOT_GPR4	RW/RO	0x0000_0000	32	See *4.5.57 BOOT_GPR4 Register* on page 4-168.
0x0194	BOOT_GPR5	RW/RO	0x0000_0000	32	See *4.5.58 BOOT_GPR5 Register* on page 4-168.
0x0198	BOOT_GPR6	RW/RO	0x0000_0000	32	See *4.5.59 BOOT_GPR6 Register* on page 4-169.
0x019C	BOOT_GPR7	RW/RO	0x0000_0000	32	See *4.5.60 BOOT_GPR7 Register* on page 4-169.
0x01A0	INSTANCE_ID	RW/RO	0x0000_0000	32	See *4.5.61 INSTANCE_ID Register* on page 4-170.
0x01A4	PCIE_BOOT_CTRL	RW	0x0000_0003	32	See *4.5.62 PCIE_BOOT_CTRL Register* on page 4-170.
0x01B4	DBG_AUTHN_CTRL	RW	0x0000_0007	32	See *4.5.63 DBG_AUTHN_CTRL Register* on page 4-171.
0x01B8	CTI0_CTRL	RW	0x0000_0000	32	See *4.5.64 CTI0_CTRL Register* on page 4-172.
0x01BC	CTI1_CTRL	RW	0x0000_0000	32	See *4.5.65 CTI1_CTRL Register* on page 4-172.
0x01C0	CTI0TO3_CTRL	RW	0x0000_0000	32	See *4.5.66 CTI0TO3_CTRL Register* on page 4-173.
0x01C4	MCP_WDOGCTI_CTRL	RW	0x0000_0000	32	See *4.5.67 MCP_WDOGCTI_CTRL Register* on page 4-173.
0x01C8	SCP_WDOGCTI_CTRL	RW	0x0000_0000	32	See *4.5.68 SCP_WDOGCTI_CTRL Register* on page 4-174.
0x01CC	DBGEXPCTI_CTRL	RW	0x0000_0000	32	See *4.5.69 DBGEXPCTI_CTRL Register* on page 4-174.
0x01D0	PCIE_PM_CTRL	RW/RO	0x0000_0000	32	See *4.5.70 PCIE_PM_CTRL Register* on page 4-175.
0x01D4	CCIX_PM_CTRL	RW/RO	0x0000_0000	32	See *4.5.71 CCIX_PM_CTRL Register* on page 4-175.

Table 4-32 SCC registers summary (continued)

Offset	Name	Type	Reset	Width	Description
0x01D8	SCDBG_CTRL	RW/RO	0x0000_0000	32	See *4.5.72 SCDBG_CTRL Register* on page 4-176.
0x01DC	EXP_IF_CTRL	RW	0x0000_0000	32	See *4.5.73 EXP_IF_CTRL Register* on page 4-178.
0x01E4	RO_CTRL	RW	0x0000_0001	32	See *4.5.74 RO_CTRL Register* on page 4-179.
0x01E8	CMN_CCIX_CTRL	RW/RO	0x0101_0000	32	See *4.5.75 CMN_CCIX_CTRL Register* on page 4-180.
0x01EC	STM_CTRL	RW	0x0000_0000	32	See *4.5.76 STM_CTRL Register* on page 4-181.
0x01F0	AXI_OVRD_PCIE	RW	0x0030_3030	32	See *4.5.77 AXI_OVRD_PCIE Register* on page 4-182.
0x01F4	AXI_OVRD_CCIX	RW	0x0030_3030	32	See *4.5.78 AXI_OVRD_CCIX Register* on page 4-183.
0x01F8	AXI_OVRD_TSIF	RW	0x0000_3030	32	See *4.5.79 AXI_OVRD_TSIF Register* on page 4-184.
0x0200	TRACE_PAD_CTRL0	RW	0x1111_1111	32	See *4.5.80 TRACE_PAD_CTRL0 Register* on page 4-184.
0x0204	TRACE_PAD_CTRL1	RW	0x0000_1111	32	See *4.5.81 TRACE_PAD_CTRL1 Register* on page 4-187.
0x0208	IOFPGA_TMIF_PAD_CTRL	RW	0x0011_1111	32	See *4.5.82 IOFPGA_TMIF_PAD_CTRL Register* on page 4-188.
0x020C	IOFPGA_TSIF_PAD_CTRL	RW	0x0011_1111	32	See *4.5.83 IOFPGA_TSIF_PAD_CTRL Register* on page 4-189.
0x0E00	APB_CTRL_CLR	RW	0xXXXX_XXXX	32	See *4.5.84 APB_CTRL_CLR Register* on page 4-191.
0x0FD0	PID4	RO	0x0000_0004	32	See *4.5.85 PID4 Register* on page 4-191.
0xFE0	PID0	RO	0x0000_00AF	32	See *4.5.86 PID0 Register* on page 4-192.
0xFE4	PID1	RO	0x0000_00B0	32	See *4.5.87 PID1 Register* on page 4-192.
0xFE8	PID2	RO	0x0000_000B	32	See *4.5.88 PID2 Register* on page 4-193.
0xFEC	PID3	RO	0x0000_0000	32	See *4.5.89 PID3 Register* on page 4-193.
0xFF0	CID0	RO	0x0000_000D	32	See *4.5.90 CID0 Register* on page 4-194.
0xFF4	CID1	RO	0x0000_00F0	32	See *4.5.91 CID1 Register* on page 4-194.
0xFF8	CID2	RO	0x0000_0005	32	See *4.5.92 CID2 Register* on page 4-195.
0xFFC	CID3	RO	0x0000_00B1	32	See *4.5.93 CID3 Register* on page 4-195.

4.5.2 PMCLK_DIV Register

The PMCLK_DIV Register characteristics are:

Purpose

Controls the **PMCLK** division value from **REFCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PMCLK_DIV Register bit assignments.

Table 4-33 PMCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKSEL_CUR+1. Reset value `0b00001`, division value=2.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKSEL_CUR+1. Reset value `0b00001`, division value=2.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.3 SYSAPBCLK_CTRL Register

The SYSAPBCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SYSAPBCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SYSAPBCLK_CTRL Register bit assignments.

Table 4-34 SYSAPBCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **SYSAPBCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **SYSAPBCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.4 SYSAPBCLK _DIV Register

The SYSAPBCLK _DIV Register characteristics are:

Purpose

Controls the **SYSAPBCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SYSAPBCLK _DIV Register bit assignments.

Table 4-35 SYSAPBCLK _DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.

Table 4-35 SYSAPBCLK _DIV Register bit assignments (continued)

Bits	Name	Type	Function
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b10011`, division value=20.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.5 IOFPGA_TMIF2XCLK_CTRL Register

The IOFPGA_TMIF2XCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **TMIF2XCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the IOFPGA_TMIF2XCLK_CTRL Register bit assignments.

Table 4-36 IOFPGA_TMIF2XCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **TMIF2XCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **TMIF2XCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.6 IOFPGA_TMIF2XCLK_DIV Register

The IOFPGA_TMIF2XCLK_DIV Register characteristics are:

Purpose

Controls the **TMIF2XCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the IOFPGA_TMIF2XCLK_DIV Register bit assignments.

Table 4-37 IOFPGA_TMIF2XCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b10011`, division value=20.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.7 IOFPGA_TSIF2XCLK_CTRL Register

The IOFPGA_TSIF2XCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **TSIF2XCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the IOFPGA_TSIF2XCLK_CTRL Register bit assignments.

Table 4-38 IOFPGA_TSIF2XCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **TSIF2XCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **TSIF2XCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.8 IOFPGA_TSIF2XCLK_DIV Register

The IOFPGA_TSIF2XCLK_DIV Register characteristics are:

Purpose

Controls the **TSIF2XCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the IOFPGA_TSIF2XCLK_DIV Register bit assignments.

Table 4-39 IOFPGA_TSIF2XCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.

Table 4-39 IOFPGA_TSIF2XCLK_DIV Register bit assignments (continued)

Bits	Name	Type	Function
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b10011`, division value=20.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.9 SCPNICCLK_CTRL Register

The SCPNICCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SCPNICCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCPNICCLK_CTRL Register bit assignments.

Table 4-40 SCPNICCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **SCPNICCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **SCPNICCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.10 SCPNICCLK_DIV Register

The SCPNICCLK_DIV Register characteristics are:

Purpose

Controls the **SCPNICCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCPNICCLK_DIV Register bit assignments.

Table 4-41 SCPNICCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00111`, division value=8.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.11 SCPI2CCLK_CTRL Register

The SCPI2CCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SCPI2CCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCPI2CCLK_CTRL Register bit assignments.

Table 4-42 SCPI2CCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **SCPI2CCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RO	Select source for **SCPI2CCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0001`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.12 SCPI2CCLK_DIV Register

The SCPI2CCLK_DIV Register characteristics are:

Purpose

Controls the **SCPI2CCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCPI2CCLK_DIV Register bit assignments.

Table 4-43 SCPI2CCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.

Table 4-43 SCPI2CCLK_DIV Register bit assignments (continued)

Bits	Name	Type	Function
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00000`, division value=1.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.13 SCPQSPICLK_CTRL Register

The SCPQSPICLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SCPQSPICLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCPQSPICLK_CTRL Register bit assignments.

Table 4-44 SCPQSPICLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **SCPQSPICLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **SCPQSPICLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0001`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.14 SCPQSPICLK_DIV Register

The SCPQSPICLK_DIV Register characteristics are:

Purpose

Controls the **SCPQSPICLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCPQSPICLK_DIV Register bit assignments.

Table 4-45 SCPQSPICLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00000`, division value=1.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.15 SENSORCLK_CTRL Register

The SENSORCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **SENSORCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SENSORCLK_CTRL Register bit assignments.

Table 4-46 SENSORCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **SENSORCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **SENSORCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.16 SENSORCLK_DIV Register

The SENSORCLK_DIV Register characteristics are:

Purpose

Controls the **SENSORCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SENSORCLK_DIV Register bit assignments.

Table 4-47 SENSORCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.

Table 4-47 SENSORCLK_DIV Register bit assignments (continued)

Bits	Name	Type	Function
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b10111`, division value=24.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.17 MCPNICCLK_CTRL Register

The MCPNICCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **MCPNICCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCPNICCLK_CTRL Register bit assignments.

Table 4-48 MCPNICCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **MCPNICCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **MCPNICCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.18 MCPNICCLK_DIV Register

The MCPNICCLK_DIV Register characteristics are:

Purpose

Controls the **MCPNICCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCPNICCLK_DIV Register bit assignments.

Table 4-49 MCPNICCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00111`, division value=8.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.19 MCPI2CCLK_CTRL Register

The MCPI2CCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **MCPI2CCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCPI2CCLK_CTRL Register bit assignments.

Table 4-50 MCPI2CCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **MCPI2CCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **MCPI2CCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0001`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.20 MCPI2CCLK_DIV Register

The MCPI2CCLK_DIV Register characteristics are:

Purpose

Controls the **MCPI2CCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCPI2CCLK_DIV Register bit assignments.

Table 4-51 MCPI2CCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.

Table 4-51 MCPI2CCLK_DIV Register bit assignments (continued)

Bits	Name	Type	Function
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00000`, division value=1.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.21 MCPQSPICLK_CTRL Register

The MCPQSPICLK_CTRL Register characteristics are:

Purpose

Selects source for clock **MCPQSPICLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCPQSPICLK_CTRL Register bit assignments.

Table 4-52 MCPQSPICLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **MCPQSPICLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **MCPQSPICLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0001`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.22 MCPQSPICLK_DIV Register

The MCPQSPICLK_DIV Register characteristics are:

Purpose

Controls the **MCPQSPICLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCPQSPICLK_DIV Register bit assignments.

Table 4-53 MCPQSPICLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00000`, division value=1.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.23 PCIEAXICLK_CTRL Register

The PCIEAXICLK_CTRL Register characteristics are:

Purpose

Selects source for clock **PCIEAXICLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PCIEAXICLK_CTRL Register bit assignments.

Table 4-54 PCIEAXICLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **PCIEAXICLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **PCIEAXICLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.24 PCIEAXICLK_DIV Register

The PCIEAXICLK_DIV Register characteristics are:

Purpose

Controls the **PCIEAXICLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PCIEAXICLK_DIV Register bit assignments.

Table 4-55 PCIEAXICLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.

Table 4-55 PCIEAXICLK_DIV Register bit assignments (continued)

Bits	Name	Type	Function
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00001`, division value=2.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.25 CCIXAXICLK_CTRL Register

The CCIXAXICLK_CTRL Register characteristics are:

Purpose

Selects source for clock **CCIXAXICLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CCIXAXICLK_CTRL Register bit assignments.

Table 4-56 CCIXAXICLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **CCIXAXICLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **CCIXAXICLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.26 CCIXAXICLK_DIV Register

The CCIXAXICLK_DIV Register characteristics are:

Purpose

Controls the **CCIXAXICLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CCIXAXICLK_DIV Register bit assignments.

Table 4-57 CCIXAXICLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b00001`, division value=2.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.27 PCIEAPBCLK_CTRL Register

The PCIEAPBCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **PCIEAPBCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PCIEAPBCLK_CTRL Register bit assignments.

Table 4-58 PCIEAPBCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **PCIEAPBCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **PCIEAPBCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.28 PCIEAPBCLK_DIV Register

The PCIEAPBCLK_DIV Register characteristics are:

Purpose

Controls the **PCIEAPBCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PCIEAPBCLK_DIV Register bit assignments.

Table 4-59 PCIEAPBCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.

Table 4-59 PCIEAPBCLK_DIV Register bit assignments (continued)

Bits	Name	Type	Function
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b01011`, division value=12.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.29 CCIXAPBCLK_CTRL Register

The CCIXAPBCLK_CTRL Register characteristics are:

Purpose

Selects source for clock **CCIXAPBCLK**.

Usage constraints

Bits[11:8] are read-only. Bits[3:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CCIXAPBCLK_CTRL Register bit assignments.

Table 4-60 CCIXAPBCLK_CTRL Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:8]	CLKSEL_CUR	RO	Current value of source for **CCIXAPBCLK**: `0b0001`: Source is **REFCLK**. `0b0010`: Source is divided **SYSPLLCLK**.
[7:4]	-	-	Reserved.
[3:0]	CLKSEL	RW	Select source for **CCIXAPBCLK**: `0b0001`: Select **REFCLK**. `0b0010`: Select divided **SYSPLLCLK**. Reset value `0b0010`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.30 CCIXAPBCLK_DIV Register

The CCIXAPBCLK_DIV Register characteristics are:

Purpose

Controls the **CCIXAPBCLK** division value from **SYSPLLCLK**.

Usage constraints

Bits[20:16] are read-only. Bits[4:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CCIXAPBCLK_DIV Register bit assignments.

Table 4-61 CCIXAPBCLK_DIV Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20:16]	CLKDIV_CUR	RO	Current clock divider value. Division value=CLKDIV_CUR+1.
[15:5]	-	-	Reserved.
[4:0]	CLKDIV	RW	Sets clock division value. Division value=CLKDIV_CUR+1. Reset value `0b01011`, division value=12.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.31 SYS_CLK_EN Register

The SYS_CLK_EN Register characteristics are:

Purpose

Enables or disables internally generated clocks.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SYS_CLK_EN Register bit assignments.

Table 4-62 SYS_CLK_EN Register bit assignments

Bits	Name	Type	Function
[31:14]	-	-	Reserved.
[13]	CCIXAPBCLKEN	RW	Enable clock **CCIXAPBCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
12	CCIXAXICLKEN	RW	Enable clock **CCIXAXICLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
11	PCIEAPBCLKEN	RW	Enable clock **PCIEAPBCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
10	PCIEAXICLKEN	RW	Enable clock **PCIEAXICLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
9	MCPQSPICLKEN	RW	Enable clock **MCPQSPICLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
8	MCPI2CCLKEN	RW	Enable clock **MCPI2CCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
7	MCPNICCLKEN	RW	Enable clock **MCPNICCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.

Table 4-62 SYS_CLK_EN Register bit assignments (continued)

Bits	Name	Type	Function
6	SENSORCLKEN	RW	Enable clock **SENSORCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
5	SCPQSPICLKEN	RW	Enable clock **SCPQSPICLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
4	SCPI2CCLKEN	RW	Enable clock **SCPI2CCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
3	-	-	Reserved.
2	IOFPGA_TSIF2XCLKEN	RW	Enable clock **TSIF2XCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
1	IOFPGA_TMIF2XCLKEN	RW	Enable clock **TMIF2XCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.
0	SYSAPBCLKEN	RW	Enable clock **SYSAPBCLK**: `0b0`: Clock disabled. `0b1`: Clock enabled. Reset value `0b1`.

4.5.32 CPU0_PLL_CTRL0 Register

The CPU0_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register CPU0_PLL_CTRL1, control the settings of clock control PLL CPU0PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CPU0_PLL_CTRL0 Register bit assignments.

Table 4-63 CPU0_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to `0b1`: `0x0`: PLL disabled. `0x1`: PLL disabled. Reset value `0x1`.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value `0b1`.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value `0x30`, division value=48.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS	RW	Bypasses PLL to drive input clock directly into the SoC: `0x0`: PLL not bypassed. `0x1`: PLL bypassed. Reset value `0b0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.33 CPU0_PLL_CTRL1 Register

The CPU0_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register CPU0_PLL_CTRL0, control the settings of clock control PLL CPU0PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CPU0_PLL_CTRL1 Register bit assignments.

Table 4-64 CPU0_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value `0b1`.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value `0b1`.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction=FRAC/2^24. Reset value `0x0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.34 CPU1_PLL_CTRL0 Register

The CPU1_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register CPU1_PLL_CTRL1, control the settings of clock control PLL CPU1PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CPU1_PLL_CTRL0 Register bit assignments.

Table 4-65 CPU1_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to `0b1`: `0x0`: PLL disabled. `0x1`: PLL enabled. Reset value `0x1`.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value `0b1`.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value `0x30`, division value=48.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS	RW	Bypasses PLL to drive input clock directly into the SoC: `0x0`: PLL not bypassed. `0x1`: PLL bypassed. Reset value `0b0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.35 CPU1_PLL_CTRL1 Register

The CPU1_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register CPU1_PLL_CTRL0, control the settings of clock control PLL CPU1PLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CPU1_PLL_CTRL1 Register bit assignments.

Table 4-66 CPU1_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value `0b1`.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value `0b1`.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction=FRAC/2^24. Reset value `0x0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.36 CLUS_PLL_CTRL0 Register

The CLUS_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register CLUS_PLL_CTRL1, control the settings of clock control PLL CLUSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CLUS_PLL_CTRL0 Register bit assignments.

Table 4-67 CLUS_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to `0b1`: `0b0`: PLL disabled. `0b1`: PLL enable. Reset value `0x1`.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value `0b1`.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value `0x20`, division value=32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS		Bypasses PLL to drive input clock directly into the SoC: `0b0`: PLL not bypassed.. `0b1`: PLL bypassed. Reset value `0b0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.37 CLUS_PLL_CTRL1 Register

The CLUS_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register CLUS_PLL_CTRL0, control the settings of clock control PLL CLUSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CLUS_PLL_CTRL1 Register bit assignments.

Table 4-68 CLUS_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value `0b1`.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value `0b1`.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction=FRAC/2^24. Reset value `0x0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.38 SYS_PLL_CTRL0 Register

The SYS_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register SYS_PLL_CTRL1, control the settings of clock control PLL SYSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SYS_PLL_CTRL0 Register bit assignments.

Table 4-69 SYS_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to `0b1`: `0b0`: PLL disabled. `0b1`: PLL enabled. Reset value `0x1`.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value `0b1`.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value `0x30`, division value=48.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS		Bypasses PLL to drive input clock directly into the SoC: `0b0`: PLL not bypassed. `0b1`: PLL bypassed. Reset value `0b0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.39 SYS_PLL_CTRL1 Register

The SYS_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register SYS_PLL_CTRL0, control the settings of clock control PLL SYSSPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SYS_PLL_CTRL1 Register bit assignments.

Table 4-70 SYS_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value `0b1`.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value `0b1`.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction=FRAC/2^24. Reset value `0x0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.40 DMC_PLL_CTRL0 Register

The DMC_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register DMC_PLL_CTRL1, control the settings of clock control PLL DMCPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the DMC_PLL_CTRL0 Register bit assignments.

Table 4-71 DMC_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to `0b1`: `0b0`: PLL disabled. `0b1`: PLL enabled. Reset value `0x1`.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock divider value. Reset value `0b1`.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value `0x20`, division value=32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS	RW	Bypasses PLL to drive input clock directly into the SoC: `0b0`: PLL not bypassed. `0b1`: PLL bypassed. Reset value `0b0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.41 DMC_PLL_CTRL1 Register

The DMC_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register DMC_PLL_CTRL0, control the settings of clock control PLL DMCPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the DMC_PLL_CTRL1 Register bit assignments.

Table 4-72 DMC_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value `0b1`.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value `0b1`.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction=FRAC/2^24. Reset value `0x0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.42 INT_PLL_CTRL0 Register

The INT_PLL_CTRL0 Register characteristics are:

Purpose

This register, and register INT_PLL_CTRL1, control the settings of clock control PLL INTPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the INT_PLL_CTRL0 Register bit assignments.

Table 4-73 INT_PLL_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31]	PLLEN	RW	PLL global enable. After SoC bootup, the PLL is disabled until this bit is set to `0b1`: `0b0`: PLL disabled. `0b1`: PLL enabled. Reset value `0b0`.
[30:26]	-	-	Reserved.
[25:20]	REFDIV	RW	PLL reference, input clock, divider value. Reset value `0b1`.
[19:8]	FBDIV	RW	PLL feedback divider value. Reset value `0x20`, division value=32.
[7:1]	-	-	Reserved.
[0]	HARD_BYPASS		Bypasses PLL to drive input clock directly into the SoC: `0b0`: PLL not bypassed. `0b1`: PLL bypassed. Reset value `0b0`.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.43 INT_PLL_CTRL1 Register

The INT_PLL_CTRL1 Register characteristics are:

Purpose

This register, and register INT_PLL_CTRL0, control the settings of clock control PLL INTPLL.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the INT_PLL_CTRL1 Register bit assignments.

Table 4-74 INT_PLL_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31]	-	-	Reserved.
[30:28]	POSTDIV2	RW	Second post-divide value. Post-divide value=POSTDIV2. Reset value `0b1`.
[27]	-	-	Reserved.
[26:24]	POSTDIV1	RW	First post-divide value. Post-divide value=POSTDIV1. Reset value `0b1`.
[23:0]	FRAC	RW	Fractional part of feedback divide value. Fraction=FRAC/2^24.

Note

The example values in this register, and the clock frequency they generate, are part of a clock configuration which enables correct operation of the N1 SoC. Further SoC testing and measurement, by Arm or by other developers, might result in new register values.

4.5.44 SYS_MAN_RESET Register

The SYS_MAN_RESET Register characteristics are:

Purpose

Controls the manual resets of the internal resets at SoC level.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SYS_MAN_RESET Register bit assignments.

Table 4-75 SYS_MAN_RESET Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11]	FORCE_CCIX_APB_RST	RW	CCIX APB reset, CCIX top reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b1`.

Table 4-75 SYS_MAN_RESET Register bit assignments (continued)

Bits	Name	Type	Function
[10]	FORCE_PCIE_APB_RST		PCIe APB reset, PCIe top reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b1`.
[9:8]	-	-	Reserved.
[7]	FORCE_MCP_QSPI_RST		**MCPQSPICLK** manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.
[6]	FORCE_MCP_I2C_RST		**MCP I2CCLK** clock manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.
[5]	FORCE_SCP_SENSOR_RST		**SENSORCLK** manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.
[4]	FORCE_SCP_QSPI_RST		**SCPQSPICLK** manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.
[3]	FORCE_SCP_I2C_RST		**SCP I2CCLK** manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.
[2]	FORCE_IOFPGA_TSIF_RST		**TSIF2XCLK** manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.

Table 4-75 SYS_MAN_RESET Register bit assignments (continued)

Bits	Name	Type	Function
[1]	FORCE_IOFPGA_TMIF_RST		**TMIF2XCLK** manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.
[0]	FORCE_SYS_APB_RST		**SYSAPBCLK** manual reset: `0b0`: Not reset. `0b1`: Reset. Reset value `0b0`.

4.5.45 BOOT_CTL Register

The BOOT_CTL Register characteristics are:

Purpose

Controls powerup reset hold and MSCP bootup type.

Usage constraints

This register is read-only from APB interface and read/write from serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_CTL Register bit assignments.

Table 4-76 BOOT_CTL Register bit assignments

Bits	Name	Type	Function
[31]	PORESET_HOLD	RO from APB interface. RW from serial interface.	Powerup reset hold: `0b0`: Do not hold powerup reset. `0b1`: Hold powerup reset. Reset value `0b0`. **Note** This bit is valid only when MSCP_BOOT_TYPE=`0b1`.
[30:1]	-		Reserved.
[0]	MSCP_BOOT_TYPE	RO from APB interface. RW from serial interface.	MSCP bootup type: `0b0`: Boot from QSPI. `0b1`: Boot from TLX master interface. Reset value `0b0`.

4.5.46 BOOT_CTRL_STA Register

The BOOT_CTRL_STA Register characteristics are:

Purpose

Stores bootup statuses.

Usage constraints

Bits[31:24 are read/write. Bits[6:0] are read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_CTRL_STA Register bit assignments.

Table 4-77 BOOT_CTRL_STA Register bit assignments

Bits	Name	Type	Function
[31:24]	MSCP_BOOT_STATUS	RW	SCP can use this field to store MSCP bootup status for MCC to read. Reset value `0x00`.
[23:7]	-	-	Reserved.
[6]	MCP_ACG_QDENY	RO	MCP ACG **QDENYn**. Reset value `0b0`.
[5]	MCP_ACG_QACCEPT	RO	MCP ACG **QACCEPTn** Reset value `0b0`.
[4]	MCP_QACTIVE	RO	MCP ACG **QACTIVE** Reset value `0b0`.
[3]	-	RO	Reserved.
[2]	SCP_ACG_QDENY	RO	SCP ACG **QDENYn**
[1]	SCP_QACCEPT	RO	SCP ACG **QACCEPTn** Reset value `0b0`.
[0]	SCP_ACG_QACTIVE	RO	SCP ACG **QACTIVE** Reset value `0b0`.

4.5.47 SCP_BOOT_ADR Register

The SCP_BOOT_ADR Register characteristics are:

Purpose

Stores the SCP bootup address.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCP_BOOT_ADR Register bit assignments.

Table 4-78 SCP_BOOT_ADR Register bit assignments

Bits	Name	Type	Function
[31:0]	ADDRESS	RO from APB interface. RW from serial interface.	Bootup address of SCP. Reset value `0x00000000`.

4.5.48 MCP_BOOT_ADR Register

The MCP_BOOT_ADR Register characteristics are:

Purpose
Stores the MCP bootup address.

Usage constraints
This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCP_BOOT_ADR Register bit assignments.

Table 4-79 MCP_BOOT_ADR Register bit assignments

Bits	Name	Type	Function
[31:0]	ADDRESS	RO from APB interface. RW from serial interface.	Bootup address of MCP. Reset value `0x00000000`.

4.5.49 PLATFORM_CTRL Register

The PLATFORM_CTRL Register characteristics are:

Purpose
N1 SoC platform control.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PLATFORM_CTRL Register bit assignments.

Table 4-80 PLATFORM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:9]	-	-	Reserved.
[8]	MULTI_CHIP_MODE	RO from APB interface. RW from serial interface.	Multi-chip tie-off value: `0b0`: Single chip. `0b1`: Multi-chip. Reset value `0b0`.
[7:6]	-	-	Reserved.
[5:0]	CHIPID	RO from APB interface. RW from serial interface.	CHIP ID tie-off value in multichip mode. This value is `0b00000` for single chip mode.

4.5.50 TARGETIDAPP Register

The TARGETIDAPP Register characteristics are:

Purpose
CoreSight target ID of *Application Processor* (AP).

Usage constraints
This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the TARGETIDAPP Register bit assignments.

Table 4-81 TARGETIDAPP Register bit assignments

Bits	Name	Type	Function
[31:0]	ID	RO from APB interface. RW from serial interface.	CoreSight target ID of AP. Reset value `0x07B00477`.

4.5.51 TARGETIDSCP Register

The TARGETIDSCP Register characteristics are:

Purpose
Stores the SCP bootup address.

Usage constraints
This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCP_BOOT_ADR Register bit assignments.

Table 4-82 SCP_BOOT_ADR Register bit assignments

Bits	Name	Type	Function
[31:0]	ID	RO from APB interface. RW from serial interface.	CoreSight target ID of SCP. Reset value `0x07B10477`.

4.5.52 TARGETIDMCP Register

The TARGETIDMCP Register characteristics are:

Purpose
Stores the MCP bootup address.

Usage constraints
This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the TARGETIDMCP Register bit assignments.

Table 4-83 TARGETIDMCP Register bit assignments

Bits	Name	Type	Function
[31:0]	ID	RO from APB interface. RW from serial interface.	CoreSight target ID of MCP. Reset value `0x07B20477`.

4.5.53 BOOT_GPR0 Register

The BOOT_GPR0 Register characteristics are:

Purpose
Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints
This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR0 Register bit assignments.

Table 4-84 BOOT_GPR0 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 0. Reset value `0x00000000`.

4.5.54 BOOT_GPR1 Register

The BOOT_GPR1 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR1 Register bit assignments.

Table 4-85 BOOT_GPR1 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 1. Reset value `0x00000000`.

4.5.55 BOOT_GPR2 Register

The BOOT_GPR2 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR2 Register bit assignments.

Table 4-86 BOOT_GPR2 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 2. Reset value `0x00000000`.

4.5.56 BOOT_GPR3 Register

The BOOT_GPR3 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR3 Register bit assignments.

Table 4-87 BOOT_GPR3 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 3. Reset value `0x00000000`.

4.5.57 BOOT_GPR4 Register

The BOOT_GPR4 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR4 Register bit assignments.

Table 4-88 BOOT_GPR4 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 4. Reset value `0x00000000`.

4.5.58 BOOT_GPR5 Register

The BOOT_GPR5 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR5 Register bit assignments.

Table 4-89 BOOT_GPR5 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 5. Reset value `0x00000000`.

4.5.59 BOOT_GPR6 Register

The BOOT_GPR6 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR6 Register bit assignments.

Table 4-90 BOOT_GPR6 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 6. Reset value `0x00000000`.

4.5.60 BOOT_GPR7 Register

The BOOT_GPR7 Register characteristics are:

Purpose

Bootup general-purpose register. This register enables an external controller to pass bootup configuration information into the N1 SoC before the release of the powerup reset. The register does not export any control from the SCC.

Usage constraints

This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the BOOT_GPR7 Register bit assignments.

Table 4-91 BOOT_GPR7 Register bit assignments

Bits	Name	Type	Function
[31:0]	REG	RO from APB interface. RW from serial interface.	Bootup general-purpose register 7. Reset value `0x00000000`.

4.5.61 INSTANCE_ID Register

The INSTANCE_ID Register characteristics are:

Purpose
SWJ-DP instance ID register.

Usage constraints
This register is read-only from the APB interface and read/write from the serial interface.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the INSTANCE_ID Register bit assignments.

Table 4-92 INSTANCE_ID Register bit assignments

Bits	Name	Type	Function
[31:4]	-	-	Reserved.
[3:0]	ID	RO from APB interface. RW from serial interface.	SWJ-DP instance ID register. Reset value `0b0000`.

4.5.62 PCIE_BOOT_CTRL Register

The PCIE_BOOT_CTRL Register characteristics are:

Purpose
Enables reset of sticky bits in the PCIe and CCIX controllers during reset of the PCIe and CCIX controllers.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PCIE_BOOT_CTRL Register bit assignments.

Table 4-93 PCIE_BOOT_CTRL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	CCIX_STICKY_RST_EN	RW	Enable reset of all sticky bits in the CCIX controller during CCIX controller reset: `0b0`: Not enable reset of sticky bits. `0b1`: Enable reset of sticky bits. Reset value `0b1`.
[0]	PCIE_STICKY_RST_EN	RW	Enable reset of all sticky bits in the PCIe controller during PCIe controller reset: `0b0`: Not enable reset of sticky bits. `0b1`: Enable reset of sticky bits. Reset value `0b1`.

4.5.63 DBG_AUTHN_CTRL Register

The DBG_AUTHN_CTRL Register characteristics are:

Purpose

Drives the CoreSight authentication external interface.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the DBG_AUTHN_CTRL Register bit assignments.

Table 4-94 DBG_AUTHN_CTRL Register bit assignments

Bits	Name	Type	Function
[31:3]	-	-	Reserved.
[2]	DBG_SPNIDEN	RW	Secure non-invasive debug enable: `0b0`: Disable. `0b1`: Enable. Reset value `0b1`.

Table 4-94 DBG_AUTHN_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[1]	DBG_SPIDEN	RW	Secure invasive debug enable: `0b0`: Disable. `0b1`: Enable. Reset value `0b1`.
[0]	DBG_DEVICEEN	RW	Global external debug enable: `0b0`: Disable. `0b1`: Enable. Reset value `0b1`.

4.5.64 CTI0_CTRL Register

The CTI0_CTRL Register characteristics are:

Purpose
CTI trigger mask register.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CTI0_CTRL Register bit assignments.

Table 4-95 CTI0_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value `0x00`.
[7:0]	TINIDENSEL	RW	CTI TINIDENSEL input. Reset value `0x00`.

4.5.65 CTI1_CTRL Register

The CTI1_CTRL Register characteristics are:

Purpose
CTI trigger mask register.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CTI1_CTRL Register bit assignments.

Table 4-96 CTI1_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value `0x00`.
[7:0]	TINIDENSEL	RW	CTI TINIDENSEL input. Reset value `0x0`.

4.5.66 CTI0TO3_CTRL Register

The CTI0TO3_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CTI0TO3_CTRL Register bit assignments.

Table 4-97 CTI0TO3_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value `0x00`.
[7:0]	TINIDENSEL	RW	CTI TINIDENSEL input. Reset value `0x00`.

4.5.67 MCP_WDOGCTI_CTRL Register

The MCP_WDOGCTI_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the MCP_WDOGCTI_CTRL Register bit assignments.

Table 4-98 MCP_WDOGCTI_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value `0x00`.
[7:0]	-	-	Reserved.

4.5.68 SCP_WDOGCTI_CTRL Register

The SCP_WDOGCTI_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCP_WDOGCTI_CTRL Register bit assignments.

Table 4-99 SCP_WDOGCTI_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	-	-	Reserved.
[15:8]	TODBGENSEL	RW	CTI TODBGENSEL input. Reset value `0x00`.
[7:0]	-	-	Reserved.

4.5.69 DBGEXPCTI_CTRL Register

The DBGEXPCTI_CTRL Register characteristics are:

Purpose

CTI trigger mask register.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the DBGEXPCTI_CTRL Register bit assignments.

Table 4-100 DBGEXPCTI_CTRL Register bit assignments

Bits	Name	Type	Function
[31:24]	TODBGENSEL2	RW	CTI2 TODBGENSEL input. Reset value `0x00`.
[23:16]	TINIDENSEL2	RW	CTI2 TINIDENSEL input. Reset value `0x00`.
[15:8]	TODBGENSEL1	RW	CTI1 TODBGENSEL input. Reset value `0x00`.
[7:0]	TINIDENSEL1	RW	CTI1 TINIDENSEL input. Reset value `0x00`.

4.5.70 PCIE_PM_CTRL Register

The PCIE_PM_CTRL Register characteristics are:

Purpose
PCIe power control register.

Usage constraints
Bit[1] is read-only. Bit[0] is read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PCIE_PM_CTRL Register bit assignments.

Table 4-101 PCIE_PM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	PM_ACK	RO	PCIe powerup acknowledgement: `0b0`: Not acknowledge. `0b1`: Acknowledge. Reset value `0b0`.
[0]	PM_REQ	RW	PCIe powerup request: `0b0`: No effect. `0b1`: Request powerup. Reset value `0b0`.

4.5.71 CCIX_PM_CTRL Register

The CCIX_PM_CTRL Register characteristics are:

Purpose
CCIX power control register.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CCIX_PM_CTRL Register bit assignments.

Table 4-102 CCIX_PM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	PM_ACK	RO	CCIX powerup acknowledgement: `0b0`: Not acknowledge. `0b1`: Acknowledge. Reset value `0b0`.
[0]	PM_REQ	RW	CCIX powerup request: `0b0`: No effect. `0b1`: Request powerup. Reset value `0b0`.

4.5.72 SCDBG_CTRL Register

The SCDBG_CTRL Register characteristics are:

Purpose
SCC scan-based debug control register.

Usage constraints
Bits[9:8] and bits[5:4] are read-only. Bits[15:0] are reserved. All other bits are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the SCDBG_CTRL Register bit assignments.

Table 4-103 SCDBG_CTRL Register bit assignments

Bits	Name	Type	Function
[31:16]	MANUAL_TRIG_DELAY	RW	Number of **REFCLK** cycles to wait after a write to MANUAL_TRIGGER register. Default `0x0000`. Maximum `0xFFFF`. Reset value `0x0000`.
[15:10]	-	-	Reserved.

Table 4-103 SCDBG_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[9]	SOC_ELAOUTUT0	RO	Or-ed SoC ELA EALOUTPUT[0]. Reset value `0b0`.
[8]	MODE_STATUS	RO	Sticky signal which indicates that the N1 SoC has entered Scan-based debug mode: `0b0`: Not Scan-based debug mode. `0b1`: Scan-based debug mode. Reset value `0b0`.
[7]	MANUAL_TRIG	RW	Triggers scan-based dump if TRIG_MANUAL is enabled: `0b0`: No effect. `0b1`: Trigger scan-based dump. Reset value `0b0`.
[6]	TRIG_MANUAL	RW	Include manual trigger: `0b0`: No effect. `0b1`: Include manual trigger. Reset value `0b0`.
[5]	TRIG_ELA_SOC	RO	Or-ed Logic Analyzer, ELA, STOPCLOCK trigger from all N1 SoC ELAs. Reset value `0b0`.
[4]	TRIG_ELA_AP	RO	Or-ed Logic Analyzer, ELA, STOPCLOCK trigger from both N1clusters. Reset value `0b0`.
[3]	TRIG_CTHALT_C1	RW	Include N1 cluster 1 cross trigger halt event, OR function of all PE cross trigger halt events. Reset value `0b0`.
[2]	TRIG_CTHALT_C0	RW	Include N1 cluster 0 cross trigger halt event, OR function of all PE cross trigger halt events. Reset value `0b0`.

Table 4-103 SCDBG_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[1]	TRIG_SS_RESETREQ	RW	Include *Manageability Control Processor* (MC) and *System Control Processor* (SCP) subsystem reset request. Reset value `0b0`.
[0]	MASTER_EN	RW	Scan-based debug master enable. This bit must be `0b1` to enter SCD mode. `0b0`: Not enable. `0b1`: Enable. Reset value `0b0`.

4.5.73 EXP_IF_CTRL Register

The EXP_IF_CTRL Register characteristics are:

Purpose
Controls certain CCIX and PCIe activity.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the EXP_IF_CTRL Register bit assignments.

Table 4-104 EXP_IF_CTRL Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:16]	TSIF_WIN_ADDR	RW	Controls the location of the TSIF 1TB address window inside the Application Processor memory map: 0-4TB for single chip system. 0-8TB for two chip system. This field should be set before the first transaction from any TSIF masters and should not be changed afterwards. Reset value `0x0000_0000`.
[15:2]	-	-	Reserved.

Table 4-104 EXP_IF_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[1]	ROUNDROBIN_TBU_CCIX	RW	Defines the Micro TLB entry replacement policy for the PCIe AXI expansion interface. `0b0`: The Micro TLB uses a pseudo *Least Recently Used* (LRU) replacement policy. This policy typically provides the best average performance. However, when multiple translations are prefetched using a StashTranslation transaction, they might evict each other. `0b1`: The Micro TLB uses a round-robin replacement policy. This policy enables prefetch multiple translations using a StashTranslation transaction without evictions if the Micro TLB size is not exceeded. To avoid evictions, set this bit to `0b1` if a real-time upstream master prefetches translations.
[0]	ROUNDROBIN_TBU_PCIE	RW	Defines the Micro TLB entry replacement policy for the CCIX AXI expansion interface. `0b0`: The Micro TLB uses a pseudo *Least Recently Used* (LRU) replacement policy. This policy typically provides the best average performance. However, when multiple translations are prefetched using a StashTranslation transaction, they might evict each other. `0b1`: The Micro TLB uses a round-robin replacement policy. This policy enables prefetch multiple translations using a StashTranslation transaction without evictions if the Micro TLB size is not exceeded. To avoid evictions, set this bit to `0b1` if a real-time upstream master prefetches translations.

4.5.74 RO_CTRL Register

The RO_CTRL Register characteristics are:

Purpose

Enables ring oscillator to directly measure silicon liveliness.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the RO_CTRL Register bit assignments.

Table 4-105 RO_CTRL Register bit assignments

Bits	Name	Type	Function
[31:1]	-	-	Reserved.
[0]	RO_EN	RW	Enables and disables ring oscillator: `0b0`: Disable ring oscillator. `0b1`: Enable ring oscillator. Reset value `0b1`.

4.5.75 CMN_CCIX_CTRL Register

The CMN_CCIX_CTRL Register characteristics are:

Purpose

CCIX control register.

Usage constraints

Bits[27:2] and bits[19:17] are read-only. Bit[24] and bits[16:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CMN_CCIX_CTRL Register bit assignments.

Table 4-106 CMN_CCIX_CTRL Register bit assignments

Bits	Name	Type	Function
[31:28]	-	-	Reserved.
[27]	CXLA_CXSCLK _QDENY	RO	QDENY of CXLA CXSCLK control Q channel at CXS interface side. Reset value `0b0`.
[26]	CXLA_CXSCLK _QACCEPT	RO	QACCEPTn of CXLA CXSCLK control Q channel at CXS interface side. Reset value `0b0`.
[25]	CXLA_CXSCLK _QACTIVE	RO	QACTIVE of CXLA CXSCLK control Q channel at CXS interface side. Reset value `0b0`.

Table 4-106 CMN_CCIX_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[24]	CXLA_CXSCLK _QREQ	RW	QREQn of CXLA CXSCLK control Q channel at CXS interface side. This bit maintains its reset value while the CCIX subsystem is operating. It is only used to complete Q-channel clock down handshake when the CCIX subsystem, CCIX PCIe controller, needs reset while the main part of CMN-600 is running. This is useful for CCIX subsystem error clearance. Reset value `0b1`.
[23:20]	-	-	Reserved.
[19]	CXLA_PWR_QDENY	RO	QDENY of CXLA power control Q channel at CXS interface side.
[18]	CXLA_PWR_QACCEPT	RO	QACCEPTN of CXLA power control Q channel at CXS interface side.
[17]	CXLA_PWR_QACTIVE	RO	QACTIVE of CXLA power control Q channel at CXS interface side.
[16]	CXLA_PWR_QREQ	RW	QREQn of CXLA power control Q channel at CXS interface side. This bit maintains its reset value while the CCIX subsystem is operating. It is only used to complete Q-channel power down handshakes when the CCIX subsystem, CCIX PCIe controller, needs reset while the main part of CMN-600 is running. This is useful for CCIX subsystem error clearance. Reset value `0b1`.
[15:0]	PCIE_BUS_NUM	RW	The PCIe ID{BUS_NUM[15:8], DEVICE_NUM[7:3], FUNCTION_NUM[2:0]} used for CMN-600 to form its PCIe header. When the CCIX is configured as RP, this field must be set to `0x0`. When the CCIX is configured as EP, the SCP reads the End Point Bus and Device Number Register of CCIX enabled PCIe controller and set the value accordingly. Interrupt **ccix_bus_device_change_irq** indicates a change of value in the controller.

4.5.76 STM_CTRL Register

The STM_CTRL Register characteristics are:

Purpose

Non-secure guaranteed access control.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the STM_CTRL Register bit assignments.

Table 4-107 STM_CTRL Register bit assignments

Bits	Name	Type	Function
[31:1]	-	-	Reserved.
[0]	NSGUAREN	RW	The top level static configuration port, NSGUAREN, controls the behavior of the the *System Trace Macrocell* (STM) for Non-secure guaranteed AXI accesses: `0b0`: Non-secure guaranteed accesses behave like invariant timing accesses, that is, the AXI does not stall. `0b1`: Non-secure guaranteed accesses are enabled, that is, the AXI can stall and the trace output is guaranteed. Reset value `0b0`.

4.5.77 AXI_OVRD_PCIE Register

The AXI_OVRD_PCIE Register characteristics are:

Purpose
Controls PCIe AXI slave expansion interface override.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the AXI_OVRD_PCIE Register bit assignments.

Table 4-108 AXI_OVRD_PCIE Register bit assignments

Bits	Name	Type	Function
[31:22]	-	-	Reserved.
[21:20]	AWDOMAIN_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value `0b11`.

Table 4-108 AXI_OVRD_PCIE Register bit assignments (continued)

Bits	Name	Type	Function
[19:16]	AWCACHE_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value `0b0000`.
[15:14]	-	-	Reserved.
[13:12]	ARDOMAIN	RW	Override value of ARCACHE. Reset value `0b11`.
[11:8]	ARCACHE	RW	Override value of AWCACHE. Reset value `0b0000`.
[7:6]	-	-	Reserved.
[5:4]	AWDOMAIN	RW	Override value of AWCACHE when TPH values are not present. Reset value `0b11`.
[3:0]	AWCACHE	RW	Override value of AWCACHE when TPH values are not present. Reset value `0b0000`.

4.5.78 AXI_OVRD_CCIX Register

The AXI_OVRD_CCIX Register characteristics are:

Purpose

Controls CCIX AXI slave expansion interface override.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the AXI_OVRD_CCIX Register bit assignments.

Table 4-109 AXI_OVRD_CCIX Register bit assignments

Bits	Name	Type	Function
[31:22]	-	-	Reserved.
[21:20]	AWDOMAIN_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value `0b11`.
[19:16]	AWCACHE_TPH	RW	Override value of AWCACHE when TPH values are present. Reset value `0b0000`.

Table 4-109 AXI_OVRD_CCIX Register bit assignments (continued)

Bits	Name	Type	Function
[15:14]	-	-	Reserved.
[13:12]	ARDOMAIN	RW	Override value of ARCACHE. Reset value `0b11`.
[11:8]	ARCACHE	RW	Override value of AWCACHE. Reset value `0b0000`.
[7:6]	-	-	Reserved.
[5:4]	AWDOMAIN	RW	Override value of AWCACHE when TPH values are not present. Reset value `0b11`.
[3:0]	AWCACHE	RW	Override value of AWCACHE when TPH values are not present. Reset value `0b0000`.

4.5.79 AXI_OVRD_TSIF Register

The AXI_OVRD_TSIF Register characteristics are:

Purpose
Controls TSIF AXI slave expansion interface override.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the AXI_OVRD_TSIF Register bit assignments.

Table 4-110 AXI_OVRD_CCIX Register bit assignments

Bits	Name	Type	Function
[31:14]	-	-	Reserved.
[13:12]	ARDOMAIN	RW	Override value of ARCACHE. Reset value `0b11`.
[11:6]	-	-	Reserved.
[5:4]	AWDOMAIN	RW	Override value of AWCACHE. Reset value `0b11`.
[3:0]	-	-	Reserved.

4.5.80 TRACE_PAD_CTRL0 Register

The TRACE_PAD_CTRL0 Register characteristics are:

Purpose

Controls the drive strengths and slew rates of trace data output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the TRACE_PAD_CTRL0 Register bit assignments.

Table 4-111 TRACE_PAD_CTRL0 Register bit assignments

Bits	Name	Type	Function
[31:29]	-	-	Reserved.
[28]	IO_SR_TRACE_DATA 3	RW	Slew rate control of trace port output pads TRACE_DATA[31:24]: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[27:26]	-	-	Reserved.
[25:24]	IO_DS_TRACE_DATA 3	RW	Drive strength control of trace port output pads TRACE_DATA[31:24]: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.
[23:21]	-	-	Reserved.
[20]	IO_SR_TRACE_DATA 2	RW	Slew rate control of trace port output pads TRACE_DATA[23:16]: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[19:18]	-	-	Reserved.

Table 4-111 TRACE_PAD_CTRL0 Register bit assignments (continued)

Bits	Name	Type	Function
[17:16]	IO_DS_TRACE_DATA 2	RW	Drive strength control of trace port output pads TRACE_DATA[23:16]: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.
[15:13]	-	-	Reserved.
[12]	IO_SR_TRACE_DATA 1	RW	Slew rate control of trace port output pads TRACE_DATA[15:8]: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[11:10]	-	-	Reserved.
[9:8]	IO_DS_TRACE_DATA 1	RW	Drive strength control of trace port output pads TRACE_DATA[15:8]: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.
[7:5]	-	-	Reserved.
[4]	IO_SR_TRACE_DATA 0	RW	Slew rate control of trace port output pads TRACE_DATA[7:0]: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[3:2]	-	-	Reserved.
[1:0]	IO_DS_TRACE_DATA 0	RW	Drive strength control of trace port output pads TRACE_DATA[7:0]: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.

4.5.81 TRACE_PAD_CTRL1 Register

The TRACE_PAD_CTRL1 Register characteristics are:

Purpose

Controls the drive strengths and slew rates of the trace clock output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the TRACE_PAD_CTRL1 Register bit assignments.

Table 4-112 TRACE_PAD_CTRL1 Register bit assignments

Bits	Name	Type	Function
[31:13]	-	-	Reserved.
[12]	IO_SR_TRACE_CLK_B	RW	Slew rate control of trace port output pad TRACE_CLK_B: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[11:10]	-	-	Reserved.
[9:8]	IO_DS_TRACE_CLK_B	RW	Drive strength control of trace port output pad TRACE_CLK_B: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.
[7:5]	-	-	Reserved.
[4]	IO_SR_TRACE_CLK_A	RW	Slew rate control of trace port output pad TRACE_CLK_A: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.

Table 4-112 TRACE_PAD_CTRL1 Register bit assignments (continued)

Bits	Name	Type	Function
[3:2]	-	-	Reserved.
[1:0]	IO_DS_TRACE_CLK_A	RW	Drive strength control of trace port output pad TRACE_CLK_A: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.

4.5.82 IOFPGA_TMIF_PAD_CTRL Register

The IOFPGA_TMIF_PAD_CTRL Register characteristics are:

Purpose

Controls the drive strengths and slew rates of IOFPGA AXI TMIF output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the IOFPGA_TMIF_PAD_CTRL Register bit assignments.

Table 4-113 IOFPGA_TMIF_PAD_CTRL Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20]	IO_SR_IOFPGA_AXI_TMIF_CLK	RW	Slew rate control of IOFPGA AXI TMIF output pad IOFPGA_TMIF_CLK_O: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[19:18]	-	-	Reserved.
[17:16]	IO_DS_IOFPGA_AXI_TMIF_CLK	RW	Drive strength control of IOFPGA AXI TMIF output pad IOFPGA_TMIF_CLK_O: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.

Table 4-113 IOFPGA_TMIF_PAD_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[15:13]	-	-	Reserved.
[12]	IO_SR_IOFPGA_AXI_TMIF_CTL	RW	Slew rate control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_VALID_O and IOFPGA_TMIF_CTL_O: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[11:10]	-	-	Reserved.
[9:8]	IO_DS_IOFPGA_AXI_TMIF_CTL	RW	Drive strength control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_VALID_O and IOFPGA_TMIF_CTL_O: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.
[7:5]	-	-	Reserved.
[4]	IO_SR_IOFPGA_AXI_TMIF_DATA	RW	Slew rate control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_DATA_O[7:0]: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[3:2]	-	-	Reserved.
[1:0]	IO_DS_IOFPGA_AXI_TMIF_DATA	RW	Drive strength control of IOFPGA AXI TMIF output pads IOFPGA_TMIF_DATA_O[7:0]: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.

4.5.83 IOFPGA_TSIF_PAD_CTRL Register

The IOFPGA_TSIF_PAD_CTRL Register characteristics are:

Purpose

Controls the drive strengths and slew rates of IOFPGA AXI TSIF output pads.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the IOFPGA_TSIF_PAD_CTRL Register bit assignments.

Table 4-114 IOFPGA_TSIF_PAD_CTRL Register bit assignments

Bits	Name	Type	Function
[31:21]	-	-	Reserved.
[20]	IO_SR_IOFPGA_AXI_TSIF_CLK	RW	Slew rate control of IOFPGA AXI TSIF output pad IOFPGA_TSIF_CLK_O: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[19:18]	-	-	Reserved.
[17:16]	IO_DS_IOFPGA_AXI_TSIF_CLK	RW	Drive strength control of IOFPGA AXI TSIF output pad IOFPGA_TSIF_CLK_O: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.
[15:13]	-	-	Reserved.
[12]	IO_SR_IOFPGA_AXI_TSIF_CTL	RW	Slew rate control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_VALID_O and IOFPGA_TSIF_CTL_O[1:0]: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[11:10]	-	-	Reserved.
[9:8]	IO_DS_IOFPGA_AXI_TSIF_CTL	RW	Drive strength control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_VALID_O and IOFPGA_TSIF_CTL_O[1:0]: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.
[7:5]	-	-	Reserved.

Table 4-114 IOFPGA_TSIF_PAD_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[4]	IO_SR_IOFPGA_AXI_TSIF_DATA	RW	Slew rate control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_DATA_O[7:0]: `0b0`: Fast. `0b1`: Slow. Reset value `0b1`.
[3:2]	-	-	Reserved.
[1:0]	IO_DS_IOFPGA_AXI_TSIF_DATA	RW	Drive strength control of IOFPGA AXI TSIF output pads IOFPGA_TSIF_DATA_O[7:0]: `0b00`: 2mA. `0b01`: 8mA. `0b10`: 4mA. `0b11`: 12mA. Reset value `0b01`.

4.5.84 APB_CTRL_CLR Register

The APB_CTRL_CLR Register characteristics are:

Purpose
Controls reversion to serial control of the register at the specified base address.

Usage constraints
There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the APB_CTRL_CLR Register bit assignments.

Table 4-115 APB_CTRL_CLR Register bit assignments

Bits	Name	Type	Function
[31:12]	NUMBER	RW	Writing `0xA50F5` to this field sets the register, whose base address bits[11:0] specify, to serial control.
[11:0]	BASE_ADDRESS	RW	Base address of register which reverts to serial control when `0xA50F5` is written to bits[31:12].

4.5.85 PID4 Register

The PID4 Register characteristics are:

Purpose
Stores peripheral identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PID4 Register bit assignments.

Table 4-116 PID4 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID4	RO	Peripheral ID 4 identification. Reset value `0x04`.

4.5.86 PID0 Register

The PID0 Register characteristics are:

Purpose
Stores peripheral identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PID0 Register bit assignments.

Table 4-117 PID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID0	RO	Peripheral ID 0 identification. Reset value `0xAF`.

4.5.87 PID1 Register

The PID1 Register characteristics are:

Purpose
Stores peripheral identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PID1 Register bit assignments.

Table 4-118 PID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID1	RO	Peripheral ID 1 identification. Reset value `0xB0`.

4.5.88 PID2 Register

The PID2 Register characteristics are:

Purpose
Stores peripheral identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PID2 Register bit assignments.

Table 4-119 PID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID2	RO	Peripheral ID 2 identification. Reset value `0x0B`.

4.5.89 PID3 Register

The PID3 Register characteristics are:

Purpose
Stores peripheral identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the PID3 Register bit assignments.

Table 4-120 PID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	PID3	RO	Peripheral ID 3 identification. Reset value `0x00`.

4.5.90 CID0 Register

The CID0 Register characteristics are:

Purpose
Stores component identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CID0 Register bit assignments.

Table 4-121 CID0 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID3	RO	Component ID 3 identification. Reset value `0x0D`.

4.5.91 CID1 Register

The CID1 Register characteristics are:

Purpose
Stores component identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CID1 Register bit assignments.

Table 4-122 CID1 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID1	RO	Component ID 1 identification. Reset value `0xF0`.

4.5.92 CID2 Register

The CID2 Register characteristics are:

Purpose
Stores component identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CID2 Register bit assignments.

Table 4-123 CID2 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID2	RO	Component ID 2 identification. Reset value `0x05`.

4.5.93 CID3 Register

The CID3 Register characteristics are:

Purpose
Stores component identification information.

Usage constraints
This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value
See *4.5.1 Serial Configuration Control registers summary* on page 4-120.

The following table shows the CID3 Register bit assignments.

Table 4-124 CID3 Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	CID3	RO	Component ID 3 identification. Reset value `0xB1`.

4.6 APB system registers

The IOFPGA contains the APB system registers.

This section contains the following subsections:

4.6.1 APB system register summary

The base memory address of the APB system registers in the IOFPGA is `0x1C01_0000`.

The following table shows the registers in address offset order from the base memory address.

Table 4-125 N1 SDP APB system register summary

Offset	Name	Type	Reset	Width	Description
`0x0000`	SYS_ID	RO	`0xXXXXXXXX`	32	See *4.6.2 SYS_ID Register* on page 4-198.
`0x0004`	SYS_SW	RO/RW	`0xX00000XX`	32	See *4.6.3 SYS_SW Register* on page 4-198.
`0x0008`	SYS_LED	RO/RW	`0x000000XX`	32	See *4.6.4 SYS_LED Register* on page 4-199.
`0x0024`	SYS_100HZ	RO/RW	`0xXXXXXXXX`	32	See *4.6.5 SYS_100HZ Register* on page 4-199.
`0x0030`	SYS_FLAG	RO	`0x00000000`	32	See *4.6.6 SYS_FLAG Registers* on page 4-200.
`0x0030`	SYS_FLAGSSET	WO	-	32	See *4.6.6 SYS_FLAG Registers* on page 4-200
`0x0034`	SYS_FLAGSCLR	WO	-	32	See *4.6.6 SYS_FLAG Registers* on page 4-200.
`0x0038`	SYS_NVFLAGS	RO	`0x00000000`	32	See *4.6.6 SYS_FLAG Registers* on page 4-200.
`0x0038`	SYS_NVFLAGSSET	WO	-	32	See *4.6.6 SYS_FLAG Registers* on page 4-200.
`0x003C`	SYS_NVFLAGSCLR	WO	-	32	See *4.6.6 SYS_FLAG Registers* on page 4-200.
`0x0058`	SYS_CFGSW	RO/RW	`0x000000XX`	32	See *4.6.7 SYS_CFGSW Register* on page 4-201.
`0x005C`	SYS_24MHZ	RO	`0xXXXXXXXX`	32	See *4.6.8 SYS_24MHZ Register* on page 4-201.
`0x0070`	SYS_PCIE_CNTL	RW	`0x0000000X`	32	See *4.6.9 SYS_PCIE_CNTL Register* on page 4-202.
`0x0074`	SYS_PCIE_GBE_L	RO	`0xXXXXXXXX`	32	See *4.6.10 SYS_PCIE_GBE Register* on page 4-202.
`0x0078`	SYS_PCIE_GBE_H	RO	`0x0000XXXX`	32	See *4.6.10 SYS_PCIE_GBE Register* on page 4-202.

Table 4-125 N1 SDP APB system register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0084	SYS_PROC_ID0	RW	0x0X000000	32	See *4.6.11 SYS_PROC_ID0 Register* on page 4-203.
0x0120	SYS_FAN_SPEED	RW	0x00000000	32	See *4.6.12 SYS_FAN_SPEED Register* on page 4-203.

4.6.2 SYS_ID Register

The SYS_ID Register characteristics are:

Purpose

Contains information about the N1 SDP and the bus and image versions inside the IOFPGA.

Usage constraints

The SYS_ID Register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-126 SYS_ID Register bit assignments

Bits	Name	Type	Function
[31:28]	Rev	RO	Board revision: 0x0: Rev A board. This is the prototype board and contains the N1 SoC.
[26:16]	HBI	RO	HBI board number in BCD: 0x316: HBI0316.
[15:12]	Build	RO	Build variant of board: 0xF: All builds.
[11:8]	Arch	RO	IOFPGA bus architecture: 0x4: AHB. 0x5: AXI.
[7:0]	FPGA	RO	FPGA build in BCD. The actual value that is read depends on the FPGA build.

4.6.3 SYS_SW Register

The SYS_SW Register characteristics are:

Purpose

Stores the 8 user DIP switches on the N1 board. A bit set to 0b1 indicates that the switch is ON.

Usage constraints

Bits[29:28] are read-only. Bits[7:0] are read/write.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-127 SYS_SW Register bit assignments

Bits	Name	Type	Function
[31:30]	-	-	Reserved.
[29]	nUART0CTS	RO	UART0 CTS signal.
[28]	nUART0DSR	RO	UART0 DSR signal.
[27:8]	-	-	Reserved.
[7:0]	HARDWARE_USER_SW.	RW	State of the 8 user DIP switches on the board. Application software can read these switch settings: `0b0`: OFF. `0b1`: ON.

4.6.4 SYS_LED Register

The SYS_LED Register characteristics are:

Purpose

Controls the eight user LEDs on the N1 SDP. All LEDs are turned OFF at reset. The Boot Monitor updates the LED value.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-128 SYS_LED Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	LED[7:0]	RW	Set or read the user LED states: `0b0`: OFF. `0b1`: ON.

4.6.5 SYS_100HZ Register

The SYS_100HZ Register characteristics are:

Purpose

A 32-bit counter that updates at 100Hz. The input clock derives from the 24MHz clock generator on the N1 board.

Usage constraints

The SYS_100HZ Register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-129 SYS_100HZ Register bit assignments

Bits	Name	Type	Function
[31:0]	100HZ_COUNT	RO	Contains the count, at 100Hz, since the last **CB_nRST** reset.

4.6.6 SYS_FLAG Registers

The SYS_FLAG Registers characteristics are:

Purpose

Provide two 32-bit registers, SYS_FLAGS and SYS_NVFLAGS, that contain general-purpose flags. The application software defines the meaning of the flags. You use the SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET, and SYS_NVFLAGSCLR registers to set and clear the bits in the Flag Registers.

Usage constraints

The SYS_FLAGS and SYS_NVFLAGS Registers are read-only.

The SYS_FLAGSSET, SYS_FLAGSCLR, SYS_NVFLAGSSET, and SYS_NVFLAGSCLR Registers are write-only.

Configurations

Available in all N1 SDP configurations.

SYS_FLAGS Register

The SYS_FLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_FLAGS Register is volatile, that is, a reset signal from the reset push button resets the SYS_FLAGS Register.

You use the SYS_FLAGSSET Register to set bits in the SYS_FLAGS Register. Write `0b1` to set the associated flag. Write `0b0` to leave the associated flag unchanged.

You use the SYS_FLAGSCLR Register to clear bits in the SYS_FLAGS Register. Write `0b1` to clear the associated flag. Write `0b0` to leave the associated flag unchanged.

SYS_NVFLAGS Register

The SYS_NVFLAGS Register is one of the two flag registers. It contains the current states of the flags.

The SYS_NVFLAGS Register is non-volatile, that is, a reset signal from the reset push button does not reset the SYS_FLAGS Register. Only **CB_nPOR** resets the SYS_NVFLAGS Register.

You use the SYS_NVFLAGSSET Register to set bits in the SYS_NVFLAGS Register. Write `0b1` to set the associated flag. Write `0b0` to leave the associated flag unchanged.

You use the SYS_NVFLAGSCLR Register to clear bits in the SYS_NVFLAGS Register. Write `0b1` to clear the associated flag. Write `0b0` to leave the associated flag unchanged.

4.6.7 SYS_CFGSW Register

The SYS_CFGSW Register characteristics are:

Purpose

Contains the value of *`CONFSWITCH`* in the `config.txt` file.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-130 SYS_CFGSW Register bit assignments

Bits	Name	Type	Function
[31:8]	-	-	Reserved.
[7:0]	SOFT_CONFIG_SWITCH	RW	Software applications can read these switch settings. The application software defines the meanings of the switch settings. The reset signals set these bits to the value of *`CONFSWITCH`* in the `config.txt` file. **Note** The configuration system does not use the contents of this register for board configuration.

4.6.8 SYS_24MHZ Register

The SYS_24MHZ Register characteristics are:

Purpose

A 32-bit counter that updates at 24MHz. The clock source is the 24MHz clock generator on the N1 SDP.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-131 SYS_24MHZ Register bit assignments

Bits	Name	Type	Function
[31:0]	24MHZ_COUNT	RO	Contains the count, at 24MHz, from the last **CB_nRST** reset. **CB_nRST** sets the register to zero and then the count resumes.

4.6.9 SYS_PCIE_CNTL Register

The SYS_PCIE_CNTL Register characteristics are:

Purpose

Error signal from PCIe switch and reset signal to PCIe Express slots.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-132 SYS_PCIE_CNTL Register bit assignments

Bits	Name	Type	Function
[31:2]	-	-	Reserved.
[1]	PCIE_RSTHALT	RW	Error signal from PCIe switch.
[0]	PCIE_nPERST	RW	Reset signal to PCIe expansion slots.

4.6.10 SYS_PCIE_GBE Register

The SYS_PCIE_GBE Register characteristics are:

Purpose

Contains the 48-bit PCI Express Ethernet MAC address.

Usage constraints

Bits[47:0] are read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-133 SYS_PCI_GBE Register bit assignments

Bits	Name	Type	Function
[63:48]	-	-	Reserved.
[47:32]	SYS_PCIE_GBE_H	RO	Most significant 16 bits of the PCI Express Ethernet MAC address.
[31:0]	SYS_PCIE_GBE_L	RO	Least significant 32 bits of the PCI Express Ethernet MAC address.

4.6.11 SYS_PROC_ID0 Register

The SYS_PROC_ID0 Register characteristics are:

Purpose

Identifies the active clusters in the N1 SoC.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-134 SYS_PROC_ID0 Register bit assignments

Bits	Name	Type	Function
[31:24]	PROC_ID0	RW	Denotes active clusters.
[23:0]	-	-	Reserved.

4.6.12 SYS_FAN_SPEED Register

The SYS_FAN_SPEED Register characteristics are:

Purpose

Contains a value that represents the fan operating speed. The MCC uses this value to moderate the speed of the cooling fan on the N1 SDP.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-135 SYS_FAN_SPEED Register bit assignments

Bits	Name	Type	Function
[31]	UPDATE_FAN_SPEED	RW	Set this bit to `0b1` when updating the fan speed control bits [4:0]. The system clears this bit to `0b0` after updating the fan speed. The default value is `0b0`.
[30:5]	-	-	Reserved.
[4:0]	FAN_SPEED	RW	Indicates and controls the speed of the board cooling fan. The fan has 30 speed settings: `0b00010`: Minimum fan speed. `0b11111`: Maximum fan speed. **Note** `0b00000` and `0b00001` are invalid settings. Do not use them.

4.6.13 SP810_CTRL Register

The SP810_CTRL Register characteristics are:

Purpose

This register in the SP810 system controller selects the source clocks for the four SP804 timers in the IOFPGA.

Usage constraints

There are no usage constraints.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.6.1 APB system register summary* on page 4-197.

The following table shows the bit assignments.

Table 4-136 SP810_CTRL Register bit assignments

Bits	Name	Type	Function
[31:22]	-		Reserved.
[21]	TimerEn3Sel		Selects the source clock for SP804 3 timer clock **TIM_CLK[3]**: `0b0` **TIM_CLK[3] = 32kHz**. `0b1` **TIM_CLK[3] = 1MHz**. **Note** The default is `0b0`.

Table 4-136 SP810_CTRL Register bit assignments (continued)

Bits	Name	Type	Function
[20]	-		Reserved.
[19]	TimerEn2Sel		Selects the source clock for SP804 2 timer clock **TIM_CLK[2]**: `0b0` **TIM_CLK[2] = 32kHz**. `0b1` **TIM_CLK[2] = 1MHz**. **Note** The default is `0b0`.
[18]	-		Reserved.
[17]	TimerEn1Sel		Selects the source clock for SP804 1 timer clock **TIM_CLK[1]**: `0b0` **TIM_CLK[1] = 32kHz**. `0b1` **TIM_CLK[1] = 1MHz**. **Note** The default is `0b0`.
[16]	-		Reserved.
[15]	TimerEn0Sel		Selects the source clock for SP804 0 timer clock **TIM_CLK[0]**: `0b0` **TIM_CLK[0] = 32kHz**. `0b1` **TIM_CLK[0] = 1MHz**. **Note** The default is `0b0`.
[14:0]	-		Reserved.

4.7 APB energy meter registers

The IOFPGA contains the APB energy meter registers.

This section contains the following subsections:

4.7.1 APB energy meter registers summary

The base memory address of the APB energy meter registers in the IOFPGA is `0x1C01_0000`.

The APB energy meter registers contain values that represent supply currents, supply voltages, and power consumption in the N1 SoC.

The IOFPGA energy registers relate to the following parts of the N1 SoC:

- N1 clusters, 1 and 0.
- CCIX and PCIe PHY cluster.
- The fabric of the N1 SoC outside the clusters, that is, the parts of the chip that operate from the VSYS power supply.

The IOFPGA energy registers measure the following values of each block:

- Instantaneous current consumption.
- Instantaneous voltage supplies.
- Instantaneous power consumption.
- Cumulative energy consumption.

- N1 clusters, 1 and 0.
- CCIX and PCIe PHY cluster.
- The fabric of the N1 SoC outside the clusters, that is, the parts of the chip that operate from the VSYS power supply.

Note

The current, power, and energy meter registers are provisional and subject to characterization on the RevB boards.

The following table shows the registers in address offset order from the base memory address.

Table 4-137 N1 SDP APB system register summary

Offset	Name	Type	Reset	Width	Description
0x00D0	SYS_I_SYS	RO	0x0000_0000	32	See *4.7.2 SYS_I_SYS Register* on page 4-208.
0x00D4	SYS_I_CL0	RO	0x0000_0000	32	See *4.7.3 SYS_I_CL0 Register* on page 4-208.
0x00D8	SYS_I_PCIE	RO	0x0000_0000	32	See *4.7.4 SYS_I_PCIE Register* on page 4-209.
0x00DC	SYS_I_CL1	RO	0x0000_0000	32	See *4.7.5 SYS_I_CL1 Register* on page 4-210.
0x00E0	SYS_V_SYS	RO	0x0000_0000	32	See *4.7.6 SYS_V_SYS Register* on page 4-210.
0x00E4	SYS_V_ CL0	RO	0x0000_0000	32	See *4.7.7 SYS_V_CL0 Register* on page 4-211.
0x00E8	SYS_V_PCIE	RO	0x0000_0000	32	See *4.7.8 SYS_V_PCIE Register* on page 4-211.
0x00EC	SYS_V_ CL1	RO	0x0000_0000	32	See *4.7.9 SYS_V_CL1 Register* on page 4-212.
0x00F0	SYS_POW_SYS	RO	0x0000_0000	32	See *4.7.10 SYS_POW_SYS Register* on page 4-213.
0x00F4	SYS_POW_ CL0	RO	0x0000_0000	32	See *4.7.11 SYS_POW_CL0 Register* on page 4-213.
0x00F8	SYS_POW_PCIE	RO	0x0000_0000	32	See *4.7.12 SYS_POW_PCIE Register* on page 4-214.
0x00FC	SYS_POW_ CL1	RO	0x0000_0000	32	See *4.7.13 SYS_POW_CL1 Register* on page 4-214.
0x0100	SYS_ENM_L_SYS	RW	0x0000_0000	32	See *4.7.14 SYS_ENM_SYS Register* on page 4-215.
0x0104	SYS_ENM_H_SYS	RW	0x0000_0000	32	See *4.7.14 SYS_ENM_SYS Register* on page 4-215.
0x0108	SYS_ENM_L_CL0	RW	0x0000_0000	32	See *4.7.15 SYS_ENM_CL0 Register* on page 4-216.
0x010C	SYS_ENM_H_ CL0	RW	0x0000_0000	32	See *4.7.15 SYS_ENM_CL0 Register* on page 4-216.
0x0110	SYS_ENM_L_PCIE		0x0000_0000	32	See *4.7.16 SYS_ENM_PCIE Register* on page 4-217.
0x0114	SYS_ENM_H_PCIE	RW	0x0000_0000	32	See *4.7.16 SYS_ENM_PCIE Register* on page 4-217.
0x0118	SYS_ENM_L_CL1	RW	0x0000_0000	32	See *4.7.17 SYS_ENM_CL1 Register* on page 4-218.
0x011C	SYS_ENM_H_CL1	RW	0x0000_0000	32	See *4.7.17 SYS_ENM_CL1 Register* on page 4-218.
0x0120	SYS_I_DDR0	RO	0x0000_0000	32	See *4.7.18 SYS_I_DDR0 Register* on page 4-219.
0x0124	SYS_I_DDR1	RO	0x0000_0000	32	See *4.7.19 SYS_I_DDR1 Register* on page 4-220.
0x0128	SYS_V_ DDR0	RO	0x0000_0000	32	See *4.7.20 SYS_V_DDR0 Register* on page 4-220.
0x012C	SYS_V_ DDR1	RO	0x0000_0000	32	See *4.7.21 SYS_V_DDR1 Register* on page 4-221.

Table 4-137 N1 SDP APB system register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x0130	SYS_POW_ DDR0	RO	0x0000_0000	32	See *4.7.22 SYS_POW_DDR0 Register* on page 4-221.
0x0134	SYS_POW_ DDR1	RO	0x0000_0000	32	See *4.7.23 SYS_POW_DDR1 Register* on page 4-222.
0x0138	SYS_ENM_L_ DDR0	RW	0x0000_0000	32	See *4.7.24 SYS_ENM_DDR0 Register* on page 4-223.
0x013C	SYS_ENM_H_ DDR0	RW	0x0000_0000	32	See *4.7.24 SYS_ENM_DDR0 Register* on page 4-223.
0x0140	SYS_ENM_L_ DDR1	RW	0x0000_0000	32	See *4.7.25 SYS_ENM_DDR1 Register* on page 4-224.
0x0144	SYS_ENM_H_ DDR1	RW	0x0000_0000	32	See *4.7.25 SYS_ENM_DDR1 Register* on page 4-224.

4.7.2 SYS_I_SYS Register

The SYS_I_SYS Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous current consumption of the parts of the N1 SoC, outside the clusters, that operate from the VSYS power supply.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-138 SYS_I_SYS Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_I_SYS	RO	12-bit representation of the instantaneous current consumption of the parts of the N1 SoC, outside the clusters, that operate from the VSYS power supply: • Full scale measurement, 4096, represents 5A. Full scale is 0xFFF. • Measured current = (SYS_I_SYS+1)/761 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.3 SYS_I_CL0 Register

SYS_I_CL0 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous current consumption of N1 cluster 0.

Usage constraints

This register is read-only. You must use one of the cluster 1 cores to read this register.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-139 SYS_I_CL0 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_I_CL0	RO	12-bit representation of the instantaneous current consumption of N1 cluster 0: • Full scale measurement, 4096, represents 10A. Full scale is `0xFFF`. • Measured current = (SYS_I_CL0+1)/381 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.4 SYS_I_PCIE Register

The SYS_I_PCIE Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous current consumption of the PCIe cluster.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-140 SYS_I_PCIE Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_I_PCIE	RO	12-bit representation of the instantaneous current consumption of the PCIe cluster: • Full scale measurement, 4096, represents 10A. Full scale is `0xFFF`. • Measured current = (SYS_I_PCIE+1)/381 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.5 SYS_I_CL1 Register

The SYS_I_CL1 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous current consumption of N1 cluster 1.

Usage constraints

This register is read-only. You must use one of the cluster 0 cores to read this register.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-141 SYS_I_CL1 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_I_CL1	RO	12-bit representation of current consumption of N1 cluster 1: • Full scale measurement, 4096, represents 5A. Full scale is `0xFFF`. • Measured current = (SYS_I_CL1+1)/761 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.6 SYS_V_SYS Register

The SYS_V_SYS Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of the parts of the N1 SoC, outside the clusters, that operate from the VSYS power supply.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

The following table shows the bit assignments.

Table 4-142 SYS_V_SYS Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_V_SYS	RO	12-bit representation of the instantaneous supply voltage of the parts of the N1 SoC, outside the clusters, that operate from the VSYS power supply: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_SYS+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.7 SYS_V_CL0 Register

The SYS_V_CL0 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of N1 SoC cluster 0.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

The following table shows the bit assignments.

Table 4-143 SYS_V_CL0 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_V_CL0	RO	12-bit representation of the instantaneous supply voltage of N1 SoC cluster 0: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_CL0+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.8 SYS_V_PCIE Register

The SYS_V_PCIE Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of the PCIe cluster.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

The following table shows the bit assignments.

Table 4-144 SYS_V_PCIE Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_V_PCIE	RO	12-bit representation of the instantaneous supply voltage of the PCIe cluster: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_PCIE+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.9 SYS_V_CL1 Register

The SYS_V_CL1 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of N1 SoC cluster 1.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

The following table shows the bit assignments.

Table 4-145 SYS_V_CL1 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_V_CL1	RO	12-bit representation of the instantaneous supply voltage of N1 SoC cluster 1: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_CL1+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.10 SYS_POW_SYS Register

The SYS_POW_SYS Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of the parts of the N1 SoC, outside the clusters, that operate from the VSYS power supply.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-146 SYS_POW_SYS Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:0]	SYS_POW_SYS	RO	24-bit representation of the instantaneous power consumption of the parts of the N1 SoC, outside the clusters, that operate from the VSYS power supply: • The value of these bits represents [SYS_I_SYS(I) × SYS_V_SYS(V)]/1234803 watts. • Measured power consumption=(SYS_POW_SYS)/1234803 • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.11 SYS_POW_CL0 Register

The SYS_POW_CL0 Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of N1 SoC cluster 0.

Usage constraints

This register is read-only. You must use one of the cluster 1 cores to read this register.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-147 SYS_POW_CL0 Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:0]	SYS_POW_CL0	RO	24-bit representation of the instantaneous power consumption of N1 SoC cluster 0: • The value of these bits represents [SYS_I_CL0(I) × SYS_V_CL0(V)]/617402 watts. • Measured power consumption=[SYS_POW_CL0]/617402 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.12 SYS_POW_PCIE Register

The SYS_POW_PCIE Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of the PCIe cluster.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-148 SYS_POW_PCIE Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:0]	SYS_POW_PCIE	RO	24-bit representation of the instantaneous power consumption of PCIe cluster: • The value of these bits represents [SYS_I_PCIE(I) × SYS_V_PCIE(V)]/617402 watts. • Measured power consumption=[SYS_POW_PCIE]/617402 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.13 SYS_POW_CL1 Register

The SYS_POW_CL1 Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of N1 SoC cluster 1.

Usage constraints

This register is read-only. You must use one of the cluster 0 cores to read this register.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-149 SYS_POW_CL1 Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:0]	SYS_POW_CL1	RO	24-bit representation of the instantaneous power consumption of N1 SoC cluster 1: • The value of these bits represents [SYS_I_CL1(I) × SYS_V_CL1(V)]/1234803 watts. • Measured power consumption=[SYS_POW_CL1]/1234803 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.14 SYS_ENM_SYS Register

The SYS_ENM_SYS Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of the fabric of the N1 SoC outside the clusters.

Usage constraints

Writing to this register clears the 64-bit value.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-150 SYS_ENM_SYS Register bit assignments

Bits	Name	Type	Function
[63:32]	SYS_ENM_H_SYS	RW	Most significant 32 bits of a 64-bit representation of the accumulated energy energy consumption of the fabric of the N1 SoC outside the clusters: • The memory address offset of these bits is `0x0104`. • Accumulated energy = (SYS_ENM_CH0_H_SYS:SYS_ENM_L_SYS)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_SYS	RW	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the fabric of the N1 SoC outside the clusters: • The memory address offset of these bits is `0x0100`. • Accumulated energy = (SYS_ENM_CH0_H_SYS:SYS_ENM_L_SYS)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.15 SYS_ENM_CL0 Register

The SYS_ENM_CL0 Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of the N1 SoC cluster 0.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-151 SYS_ENM_CL0 Register bit assignments

Bits	Name	Type	Function
[63:32]	SYS_ENM_H_CL0	RO	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of the N1 SoC cluster 0: • The memory address offset of these bits is `0x010C`. • Accumulated energy = (SYS_ENM_H_CL0:SYS_ENM_L_CL0)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_CL0	RO	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the N1 SoC cluster 0: • The memory address offset of these bits is `0x0108`. • Accumulated energy = (SYS_ENM_H_CL0:SYS_ENM_L_CL0)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.16 SYS_ENM_PCIE Register

The SYS_ENM_PCIE Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of the PCIE cluster 0.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-152 SYS_ENM_PCIE Register bit assignments

Bits	Name	Type	Function
[63:32]	SYS_ENM_H_PCIE	RO	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of the N1 SoC cluster 0: • The memory address offset of these bits is `0x0114`. • Accumulated energy = (SYS_ENM_H_PCIE:SYS_ENM_L_PCIE)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_PCIE	RO	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of the N1 SoC cluster 0: • The memory address offset of these bits is `0x0110`. • Accumulated energy = (SYS_ENM_H_PCIE:SYS_ENM_L_PCIE)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.17 SYS_ENM_CL1 Register

The SYS_ENM_CL1 Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of N1 SoC cluster 1.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-153 SYS_ENM_CL1 Register bit assignments

Bits	Name	Type	Function
[63:32]	SYS_ENM_H_CL1	RO	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of N1 SoC cluster 1: • The memory address offset of these bits is `0x011C`. • Accumulated energy = (SYS_ENM_H_CL1:SYS_ENM_L_CL1)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_CL1	RO	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of N1 SoC cluster 1: • The memory address offset of these bits is `0x0118`. • Accumulated energy = (SYS_ENM_H_CL1:SYS_ENM_L_CL1)/12348030000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.18 SYS_I_DDR0 Register

SYS_I_DDR0 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous current consumption of DDR 0.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-154 SYS_I_DDR0 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_I_DDR0	RO	12-bit representation of the instantaneous current consumption of DDR 0: • Full scale measurement, 4096, represents 10A. Full scale is `0xFFF`. • Measured current = (SYS_I_DDR0+1)/381 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.19 SYS_I_DDR1 Register

SYS_I_DDR1 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous current consumption of DDR 1.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-155 SYS_I_DDR1 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_I_DDR1	RO	12-bit representation of the instantaneous current consumption of DDR 1: • Full scale measurement, 4096, represents 10A. Full scale is `0xFFF`. • Measured current = (SYS_I_DDR 1+1)/381 amperes. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.20 SYS_V_DDR0 Register

The SYS_V_DDR0 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of DDR 0.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

The following table shows the bit assignments.

Table 4-156 SYS_V_DDR0 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_V_DDR0	RO	12-bit representation of the instantaneous supply voltage of DDR 0: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_DDR0+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.21 SYS_V_DDR1 Register

The SYS_V_DDR1 Register characteristics are:

Purpose

Contains a 12-bit representation of the instantaneous supply voltage of DDR 1.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

The following table shows the bit assignments.

Table 4-157 SYS_V_DDR1 Register bit assignments

Bits	Name	Type	Function
[31:12]	-	-	Reserved.
[11:0]	SYS_V_DDR1	RO	12-bit representation of the instantaneous supply voltage of DDR 1: • Full scale measurement, 4096, represents 2V5. Full scale is `0xFFF`. • Measured voltage = (SYS_V_DDR1+1)/1622 volts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.22 SYS_POW_DDR0 Register

The SYS_POW_DDR0 Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of DDR 0.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-158 SYS_POW_DDR0 Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:0]	SYS_POW_DDR0	RO	24-bit representation of the instantaneous power consumption of DDR 0: • The value of these bits represents [SYS_I_DDR0(I) × SYS_V_DDR0(V)]/617402 watts. • Measured power consumption=[SYS_POW_DDR0]/617402 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.23 SYS_POW_DDR1 Register

The SYS_POW_DDR1 Register characteristics are:

Purpose

Contains a 24-bit representation of the instantaneous power consumption of DDR 1.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-159 SYS_POW_DDR1 Register bit assignments

Bits	Name	Type	Function
[31:24]	-	-	Reserved.
[23:0]	SYS_POW_DDR1	RO	24-bit representation of the instantaneous power consumption of DDR 1: • The value of these bits represents [SYS_I_DDR1(I) × SYS_V_DDR1(V)]/617402 watts. • Measured power consumption=[SYS_POW_DDR1]/617402 watts. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.24 SYS_ENM_DDR0 Register

The SYS_ENM_DDR0 Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of DDR 0.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-160 SYS_ENM_DDR0 Register bit assignments

Bits	Name	Type	Function
[63:32]	SYS_ENM_H_DDR0	RO	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of DDR 0: • The memory address offset of these bits is `0x013C`. • Accumulated energy = (SYS_ENM_H_DDR0:SYS_ENM_L_DDR0)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_DDR0	RO	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of DDR 0: • The memory address offset of these bits is `0x0138`. • Accumulated energy = (SYS_ENM_H_DDR0:SYS_ENM_L_DDR0)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.7.25 SYS_ENM_DDR1 Register

The SYS_ENM_DDR1 Register characteristics are:

Purpose

Contains a 64-bit representation of the accumulated energy consumption of DDR 1.

Usage constraints

This register is read-only.

Configurations

Available in all N1 board configurations.

Memory offset and full register reset value

See *4.7.1 APB energy meter registers summary* on page 4-206.

Note

The value measured by this register is provisional and subject to characterization on the RevB boards.

The following table shows the bit assignments.

Table 4-161 SYS_ENM_DDR1 Register bit assignments

Bits	Name	Type	Function
[63:32]	SYS_ENM_H_DDR1	RO	Most significant 32 bits of a 64-bit representation of the accumulated energy consumption of DDR 1: • The memory address offset of these bits is `0x0144`. • Accumulated energy = (SYS_ENM_H_DDR1:SYS_ENM_L_DDR1)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.
[31:0]	SYS_ENM_L_DDR1	RO	Least significant 32 bits of a 64-bit representation of the accumulated energy consumption of DDR 1: • The memory address offset of these bits is `0x0140`. • Accumulated energy = (SYS_ENM_H_DDR1:SYS_ENM_L_DDR1)/6174020000 joules. • The **CB_nRST** reset signal resets the register to zero. The register then updates every 100µs after the reset.

4.8 UART memory addresses and control registers

The N1 SoC and IOFPGA contain registers that control the UARTs in the N1 System Development Platform.

The following table shows the N1 SDP UART memory addresses.

Table 4-162 UART memory locations

UART	Memory address	Comment
APUART0	`0x00_2A40_0000`	AP peripherals memory map. See *4.2.2 Application Processor subsystem peripherals memory map* on page 4-79.
APUART1	`0x00_2A41_0000`	AP peripherals memory. See *4.2.2 Application Processor subsystem peripherals memory map* on page 4-79.
SCPUART	`0x00_4400_2000`	SCP peripherals memory map. See *4.2.6 System Control Processor peripherals memory map* on page 4-89.
MCPUART0	`0x00_4C00_2000`	MCP peripherals memory map. See *4.2.4 Manageability Control Processor peripherals memory map* on page 4-84.
MCPUART1	`0x00_4400_3000`	MCP peripherals memory map. See *4.2.4 Manageability Control Processor peripherals memory map* on page 4-84.
FPGAUART1	`0x00_1C09_0000`	IOFPGA memory map. *4.2.8 IOFPGA memory map* on page 4-93.
FPGAUART2	`0x00_1C0A_0000`	IOFPGA memory map. *4.2.8 IOFPGA memory map* on page 4-93.

Note

APUART1 is used to communicate with the MCP through MCPUART1 and is accessible to the *Application Processor* (AP) cores. MCPUART1 is not accessible to the AP cores.

The following table, from the PL011 Technical Reference Manual, shows the UART0 and UART1 control registers in address offset order from the base memory address. In the table, UART0 and UART1 refer to:

- APUART0 and APUART1 respectively.
- MCPUART0 and MCPUART1 respectively.
- FPGAUART1 and FPGAUART2 respectively.

UART0 refers to SCPUART.

Undefined registers are reserved. Software must not attempt to access these registers.

Table 4-163 UART control registers summary

Offset	Name	Type	Reset value	Width	Function
0x0000	UART0DR	RW	-	32	Data Register.
0x0004	UART0RSR/UART0ECR	RW	0x0000_0000	32	Receive Status Register/Error Clear Register.
0x0018	UART0FR	RO	0x0000_0012	32	Flag Register.
0x0020	UART0ILPR	RW	0x0000_0000	32	IrDA Low-Power Counter Register.
0x0024	UART0IBRD	RW	0x0000_0000	32	Integer Baud Rate Register.
0x0028	UART0FBRD	RW	0x0000_0000	32	Fractional Baud Rate Register.
0x002C	UART0LCR_H	RW	0x0000_0000	32	Line Control Register.
0x0030	UART0CR	RW	0x0000_0300	32	Control Register.
0x0034	UART0IFLS	RW	0x0000_0012	32	Interrupt FIFO Level Select Register.
0x0038	UART0IMSC	RW	0x0000_0000	32	Interrupt Mask Set/Clear Register.
0x003C	UART0RIS	RO	0x0000_0000	32	Raw Interrupt Status Register.
0x0040	UART0MIS	RO	0x0000_0000	32	Masked Interrupt Status Register.
0x0044	UART0ICR	WO	-	32	Interrupt Clear Register.
0x0048	UART0DMACR	RW	0x0000_0000	32	DMA Control Register.
0x0FE0	UART0PeriphID0	RO	0x0000_0011	32	UART0 peripheral ID Register 0.
0x0FE4	UART0PeriphID1	RO	0x0000_0010	32	UART0 peripheral ID Register 1.
0x0FE8	UART0PeriphID2	RO	0x0000_0004	32	UART0 peripheral ID Register 2.
0x0FEC	UART0PeriphID3	RO	0x0000_0000	32	UART0 peripheral ID Register 3.
0x0FF0	UART0PCellID0	RO	0x0000_000D	32	UART0 component ID Register 0.
0x0FF4	UART0PCellID1	RO	0x0000_00F0	32	UART0 component ID Register 1.
0x0FF8	UART0PCellID2	RO	0x0000_0005	32	UART0 component ID Register 2.
0x0FFC	UART0PCellID3	RO	0x0000_00B1	32	UART0 component ID Register 3.
0x1000	UART1DR	RW	-	32	Data Register.
0x1004	UART1RSR/UART1ECR	RW	0x0000_0000	32	Receive Status Register/Error Clear Register.
0x1018	UART1FR	RO	0x0000_0012	32	Flag Register.
0x1020	UART1ILPR	RW	0x0000_0000	32	IrDA Low Power Counter Register.
0x1024	UART1IBRD	RW	0x0000_0000	32	Integer Baud Rate Register.
0x1028	UART1FBRD	RW	0x0000_0000	32	Fractional Baud Rate Register.

Table 4-163 UART control registers summary (continued)

Offset	Name	Type	Reset value	Width	Function
0x102C	UART1LCR_H	RW	0x0000_0000	32	Line Control Register.
0x1030	UART1CR	RW	0x0000_0300	32	Control Register.
0x1034	UART1IFLS	RW	0x0000_0012	32	Interrupt FIFO Level Select Register.
0x1038	UART1IMSC	RW	0x0000_0000	32	Interrupt Mask Set/Clear Register.
0x103C	UART1RIS	RO	0x0000_0000	32	Raw Interrupt Status Register.
0x1040	UART1MIS	RO	0x0000_0000	32	Masked Interrupt Status Register.
0x1044	UART1ICR	WO	-	32	Interrupt Clear Register.
0x1048	UART1DMACR	RW	0x0000_0000	32	DMA Control Register.
0x1FE0	UART1PeriphID0	RO	0x0000_0011	32	UART1 peripheral ID Register 0.
0x1FE4	UART1PeriphID1	RO	0x0000_0010	32	UART1 peripheral ID Register 1.
0x1FE8	UART1PeriphID2	RO	0x0000_0004	32	UART1 peripheral ID Register 2.
0x1FEC	UART1PeriphID3	RO	0x0000_0000	32	UART1 peripheral ID Register 3.
0x1FF0	UART1PCellID0	RO	0x0000_000D	32	UART1 component ID Register 0.
0x1FF4	UART1PCellID1	RO	0x0000_00F0	32	UART1 component ID Register 1.
0x1FF8	UART1PCellID2	RO	0x0000_0005	32	UART1 component ID Register 2.
0x1FFC	UART1PCellID3	RO	0x0000_00B1	32	UART1 component ID Register 3.

See the *Arm® PrimeCell UART(PL011) Technical Reference Manual* for more information.

Appendix A
Signal descriptions

This appendix describes the signals that are present at the N1 SDP ports.

It contains the following sections:

A.1 UART headers

There are four 5×2 way, no pin 10, UART headers on the N1 board.

The settings in the `config.txt` define the connectivity of the UART system. See *3.3.2 `config.txt` board configuration file* on page 3-65 and *2.10 UARTs* on page 2-51 for information on configuring the UART system.

Note

The headers are logical UART channels but the header pins follow the RS232 electrical specification.

The following table shows the pin mapping of the UART headers, UART0-UART3.

Table A-1 UART0 header signal list

Pin	Signal	Pin	Signal
1	No connection	2	**DSR**
3	**RX**	4	**RTS**
5	**TX**	6	**CTS**
7	**DTR**	8	No connection
9	**GND**	-	-

Arm supplies the N1 SDP with a ribbon cable connecting the UART0 header to the UART0 DB9 connector on the back panel.

Table A-2 UART1 header signal list

Pin	Signal	Pin	Signal
1	No connection	2	No connection
3	**RX**	4	No connection
5	**TX**	6	No connection
7	No connection	8	No connection
9	**GND**	-	-

Arm supplies the N1 SDP with a ribbon cable connecting the UART1 header to the UART1 DB9 connector on the back panel.

Table A-3 UART2 header signal list

Pin	Signal	Pin	Signal
1	No connection	2	No connection
3	**RX**	4	No connection
5	**TX**	6	No connection
7	No connection	8	No connection
9	**GND**	-	-

Table A-4 UART3 header signal list

Pin	Signal	Pin	Signal
1	No connection	2	No connection
3	**RX**	4	No connection
5	**TX**	6	No connection
7	No connection	8	No connection
9	**GND**	-	-

Related information

1.3 The N1 SDP at a glance on page 1-14

A.2 UART DB9 connectors

There are two DB9 connectors on the back panel that connect to logical UART channels UART0 and UART1.

The settings in the `config.txt` define the connectivity of the UART system. See *3.3.2 `config.txt` board configuration file* on page 3-65 and *2.10 UARTs* on page 2-51 for information on configuring the UART system.

Note

The DB9 connectors connect to logical UART channels but the connector pins follow the RS232 electrical specification.

The following tables show the pin mapping of the DB9 connectors, UART0 and UART1, on the back panel.

Table A-5 UART0 DB9 connector signal list

Pin	Signal	Pin	Signal
1	No connection	2	**RX**
3	**TX**	4	**DTR**
5	**GND**	6	**DSR**
7	**RTS**	8	**CTS**
9	No connection	-	-

Table A-6 UART1 DB9 connector signal list

Pin	Signal	Pin	Signal
1	No connection	2	**RX**
3	**TX**	4	No connection
5	**GND**	6	No connection
7	No connection	8	No connection
9	No connection	-	-

Arm supplies the N1 SDP with ribbon cables making the following connections:

- DB9 connector UART0 on the back panel to header UART0 on the board.
- DB9 connector UART1 on the back panel to header UART1 on the board.

Related information

1.3 The N1 SDP at a glance on page 1-14

A.3 N1-SoC JTAG connector

There is one 20-pin JTAG box header connector on the back panel.

The I/O voltage of the JTAG connector is 1V8.

The following table shows the pin mapping of the P-JTAG connector.

Table A-7 N1-SoC P-JTAG connector signal list

Pin	Signal	Pin	Signal
1	**VTREF**	2	No connection
3	**nTRST**	4	**GND**
5	**TDI**	6	**GND**
7	**TMS**	8	**GND**
9	**TCK**	10	**GND**
11	**RTCK**	12	**GND**
13	**TDO**	14	**GND**
15	**nSRSTI**	16	**GND**
17	**DBGRQ**	18	**GND**
19	**DBGACK**	20	**GND**

Note

- Pin 1 is the lower left pin of the connector. Pin 2 is the upper left pin of the connector.
- Pins 1, 5, 7, 13, 15, and 19 have pullup resistors to 1V8.
- Pins 3, 9, 11, and 17 have pulldown resistors to **GND**.

Related information

1.3 The N1 SDP at a glance on page 1-14

A.4 Trace connector

There is a Samtec QSH 60-pin plug connector on the back panel which supports 32-bit trace, JTAG debug, and *Serial Wire Debug* (SWD).

The I/O voltage for the connector is 1V8.

The following table shows the pin mapping of the trace connector.

Table A-8 Trace connector pin mapping

Pin	Signal	Pin	Signal
1	**DEBUG_VTREF**	2	**SOC_TMS**
3	**SOC_TCK**	4	**SOC_TDO**
5	**SOC_TDI**	6	**CS_nTRSTI**
7	**SOC_RTCK**	8	**SOC_nTRST**
9	**SOC_nTRST**	10	**DBGRQ**
11	**DBGACK**	12	**TRACE_VTREF**
13	**TRACE_CLKA**	14	**TRACE_CLKB**
15	**GND**	16	**GND**
17	**TRACE_CTL**	18	**TRACE_DATA19**
19	**TRACE_DATA0**	20	**TRACE_DATA20**
21	**TRACE_DATA1**	22	**TRACE_DATA21**
23	**TRACE_DATA2**	24	**TRACE_DATA22**
25	**TRACE_DATA3**	26	**TRACE_DATA23**
27	**TRACE_DATA4**	28	**TRACE_DATA24**
29	**TRACE_DATA5**	30	**TRACE_DATA25**
31	**TRACE_DATA6**	32	**TRACE_DATA26**
33	**TRACE_DATA7**	34	**TRACE_DATA27**
35	**TRACE_DATA8**	36	**TRACE_DATA28**
37	**TRACE_DATA9**	38	**TRACE_DATA29**
39	**TRACE_DATA10**	40	**TRACE_DATA30**
41	**TRACE_DATA11**	42	**TRACE_DATA31**
43	**TRACE_DATA12**	44	No connection
45	**TRACE_DATA13**	46	No connection
47	**TRACE_DATA14**	48	No connection
49	**TRACE_DATA15**	50	No connection
51	**TRACE_DATA16**	52	No connection
53	**TRACE_DATA17**	54	No connection
55	**TRACE_DATA18**	56	No connection

Table A-8 Trace connector pin mapping (continued)

Pin	Signal	Pin	Signal
57	**GND**	58	**GND**
59	No connection	60	No connection

Note

Pin 17, **TRACE_CTL**, is not used and has a pulldown resistor to **GND**.

Related information

1.3 The N1 SDP at a glance on page 1-14

A.5 Front panel I/O header

There is a 20-pin header, 10×2, on the N1 board near the front panel. The header provides connectivity for LEDs and switches between the front panel and the board.

Some signals are not brought out to the front panel but are available on the header but are available for use at the connector. The following table shows the pin mapping of the front panel I/O header.

Table A-9 Front panel I/O header pin mapping

Pin	Polarity	Pin	Polarity	Description
1	+	2	-	Connects PBON button on board to PBON button on front panel.
3	+	4	-	Connects PBRESET button on board to PBRESET button on front panel.
5	+	6	-	Reserved
7	-	8	+	Connects to orange LED in 4-level light pipe, fourth from bottom, on back panel. Denotes MCC USB activity. These pins are not brought out to the front panel.
9	-	10	+	Connects to green LED in 4-level light pipe, third from bottom, on back panel. Denotes MCC USB activity. These pins are not brought out to the front panel.
11	-	12	+	Power LED embedded in PBON button on front panel.
13	-	14	+	HDD activity LED on front panel. This signal is a combined signal from SATA0 and SATA1.
15	-	16	+	Connects to the GbE activity LED embedded in the GbE connector and denotes GbE traffic. These pins are not brought out to the front panel.
17	-	18	+	Connects to blue LED in 4-level light pipe, first from bottom. Denotes UID activity. These pins are not brought out to the front panel.
19	N/A	20	N/A	No connection

Related information

1.3 The N1 SDP at a glance on page 1-14

A.6 PCI Express and CCIX slots

There are two 16-lane PCIe slots, one 4-lane PCIe slot, and one dual-use 16-lane PCIe-*Cache-Coherent Interconnect for Accelerators* (CCIX) slot on the N1 board.

The following table shows the PCIe slots and the number of lanes implemented.

Table A-10 PCI Express expansion slots

Slot number	PCIe lane connector size	Used lanes	Unused lanes	Comment
Slot 1	×4	1	3	PCIe
Slot 2	×16	16	0	PCIe
Slot 3	×16	8	8	PCIe
Slot 4	×16	16	0	PCIe CCIX dual-use

Related information

1.3 The N1 SDP at a glance on page 1-14

A.7 C2C connector

The N1 System Development Platform provides a *Chip-to-Chip* (C2C) connector on the back panel.

The C2C enables N1 SoC to N1 SoC CCIX connectivity. Arm supplies adapter boards and connector cables for the master and slave CCIX slots. See *2.9 Chip to Chip communications* on page 2-48.

Related information

1.3 The N1 SDP at a glance on page 1-14

A.8 Power connectors

There are an ATX 24-pin power connector and an ATX/EPS 8-pin secondary connector on the N1 board.

The ATX 24-pin power connector has the standard ATXv2.2 pin connections.

The following table shows the ATX/EPS connector pin mapping.

Table A-11 ATX/EPS pin mapping

Pin	Connection
1	**GND**
2	**GND**
3	**GND**
4	**GND**
5	**12V**
6	**12V**
7	**12V**
8	**12V**

Related information

1.3 The N1 SDP at a glance on page 1-14

Appendix B
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- *B.1 Revisions* on page Appx-B-240.

B.1 Revisions

The following table lists the technical changes between released issues of this book.

Table B-1 Issue 101489_0000_00

Change	Location	Affects
No changes, first release.	-	-

Table B-2 Differences between issue 101489_0000_00 and issue 101489_0000_01

Change	Location	Affects
Added *Cache-Coherent Interconnect for Accelerators* (CCIX) information.	Throughout document	All board versions
Added SCC registers descriptions.	*4.5 Serial Configuration Control registers* on page 4-119	All board versions
Added APB system register information.	*4.6 APB system registers* on page 4-197	All board versions
Added APB voltage register information.	*4.7 APB energy meter registers* on page 4-206	All board versions
Added APB current, power, and energy register provisional information.	*4.7 APB energy meter registers* on page 4-206	RevA boards
Changed variable names in `config.txt` file variables table. Changed variable names in example `config.tx` file.	*2.10 UARTs* on page 2-51 *3.3.2 `config.txt` board configuration file* on page 3-65	All board versions
Added peripheral memory maps.	*4.2.2 Application Processor subsystem peripherals memory map* on page 4-79. *4.2.4 Manageability Control Processor peripherals memory map* on page 4-84. *4.2.6 System Control Processor peripherals memory map* on page 4-89. *4.2.7 CoreSight™ system memory map* on page 4-90.	All board versions
Added N1 SoC internal UARTs to UART system diagram.	*2.10 UARTs* on page 2-51	All board versions
Added UART memory locations and register information.	*4.8 UART memory addresses and control registers* on page 4-225	All board versions

Table B-2 Differences between issue 101489_0000_00 and issue 101489_0000_01 (continued)

Change	Location	Affects
Added AP, SCP, and MCP interrupt information.	*4.3.1 Application Processor interrupt map* on page 4-95 *4.3.2 System Control Processor interrupt map* on page 4-98 *4.3.3 Manageability Control Processor interrupt map* on page 4-102	All board versions
Added system register information.	*4.4 System Security Control registers* on page 4-105	All board versions

Table B-3 Differences between issue 101489_0000_01 and issue 101489_0000_02

Change	Location	Affects
Added description of how to gain access to ATX power cables for external hard drives.	*1.5 Accessing the ATX power cables* on page 1-20	All board versions
Clarified description of private L2 unified cache in each cluster to say that it is 1MB for each core.	*2.2 N1 SoC* on page 2-25	All board versions
Added details of boot region in Application Processor memory map.	*4.2.1 Application Processor memory map* on page 4-76	All board versions
Clarified PCIe and CCIX information in Application Processor memory map.	*4.2.1 Application Processor memory map* on page 4-76	All board versions
Added GICR to Application Processor subsystem peripherals memory map.	*4.2.2 Application Processor subsystem peripherals memory map* on page 4-79	All board versions
Added details of memory controller to System Control Processor memory map.	*4.2.5 System Control Processor memory map* on page 4-87	All board versions
Modified register names.	*4.4.12 SSC_PID4 Register* on page 4-114 *4.4.13 SSC_PID0 Register* on page 4-115 *4.4.14 SSC_PID1 Register* on page 4-115 *4.4.15 SSC_PID2 Register* on page 4-116 *4.4.16 SSC_COMPID0 Register* on page 4-116 *4.4.17 SSC_COMPID1 Register* on page 4-117 *4.4.18 SSC_COMPID2 Register* on page 4-117 *4.4.19 SSC_COMPID3 Register* on page 4-118	All board versions
Updated CE Conformance Notice.	*Conformance Notices* on page 3	All board versions