Arm® SSE-123 Example Subsystem

Revision: r0p0

Technical Overview

arm

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Arm® SSE-123 Example Subsystem

Technical Overview

Release Information

Document History

Issue	Date	Confidentiality	Change
0000-00	22 March 2019	Non-Confidential	First release for r0p0
0000-01	10 April 2020	Non-Confidential	Second release for r0p0

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Product Status

The information in this document is Final, that is for a developed product.

Web Address

www.arm.com

Contents

Arm® SSE-123 Example Subsystem Technical Overview

Preface

This preface introduces the *Arm® SSE-123 Example Subsystem Technical Overview*.

It contains the following:

About this book

This book is for the Arm® SSE-123 Example Subsystem.

Product revision status

The r*m*p*n* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*m* Identifies the major revision of the product, for example, r1.

p*n* Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the SSE-123.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter provides an overview of the SSE-123 Example Subsystem.

Chapter 2 Hardware
This chapter describes the SSE-123 hardware.

Chapter 3 Software
This chapter describes the software that runs on the SSE-123.

Appendix A Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`mono`space
Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
Denotes language keywords when used outside example code.

`<and>`

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

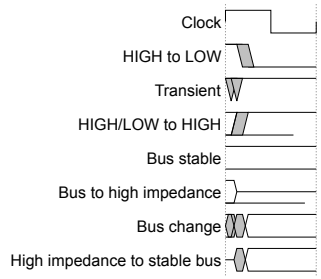

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

Additional reading

Arm publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *Arm® SSE-123 Example Subsystem Technical Reference Manual* (101370).
- *Arm®v8-M Architecture Reference Manual* (DDI 0553).

The following confidential books are only available to licensees:

- *Arm® SSE-123 Example Subsystem Configuration and Integration Manual* (101372).
- *Arm® SSE-123 Example Subsystem Release Note* (PJDOC-1779577084-12680).
- *Arm® SSE-123 Example Subsystem Analysis Report* (PJDOC-1779577084-12626).
- *Arm® SSE-123 Example Subsystem Verification Summary Report* (PJDOC-1779577084-12347).

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *Arm SSE-123 Example Subsystem Technical Overview*.
- The number 101371_0000_01_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

Note

Arm tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Chapter 1
Introduction

This chapter provides an overview of the SSE-123 Example Subsystem.

It contains the following sections:

1.1 About the SSE-123 Example Subsystem

The SSE-123 Example Subsystem integrates a subsystem of key Arm components that implement core functionality of a system targeting *Internet of Things* (IoT) *System on Chip* (SoC) designs.

The subsystem can be implemented as a standalone single core system or as part of a multiprocessor system.

The following figure shows a block diagram of the SSE-123 Example Subsystem.

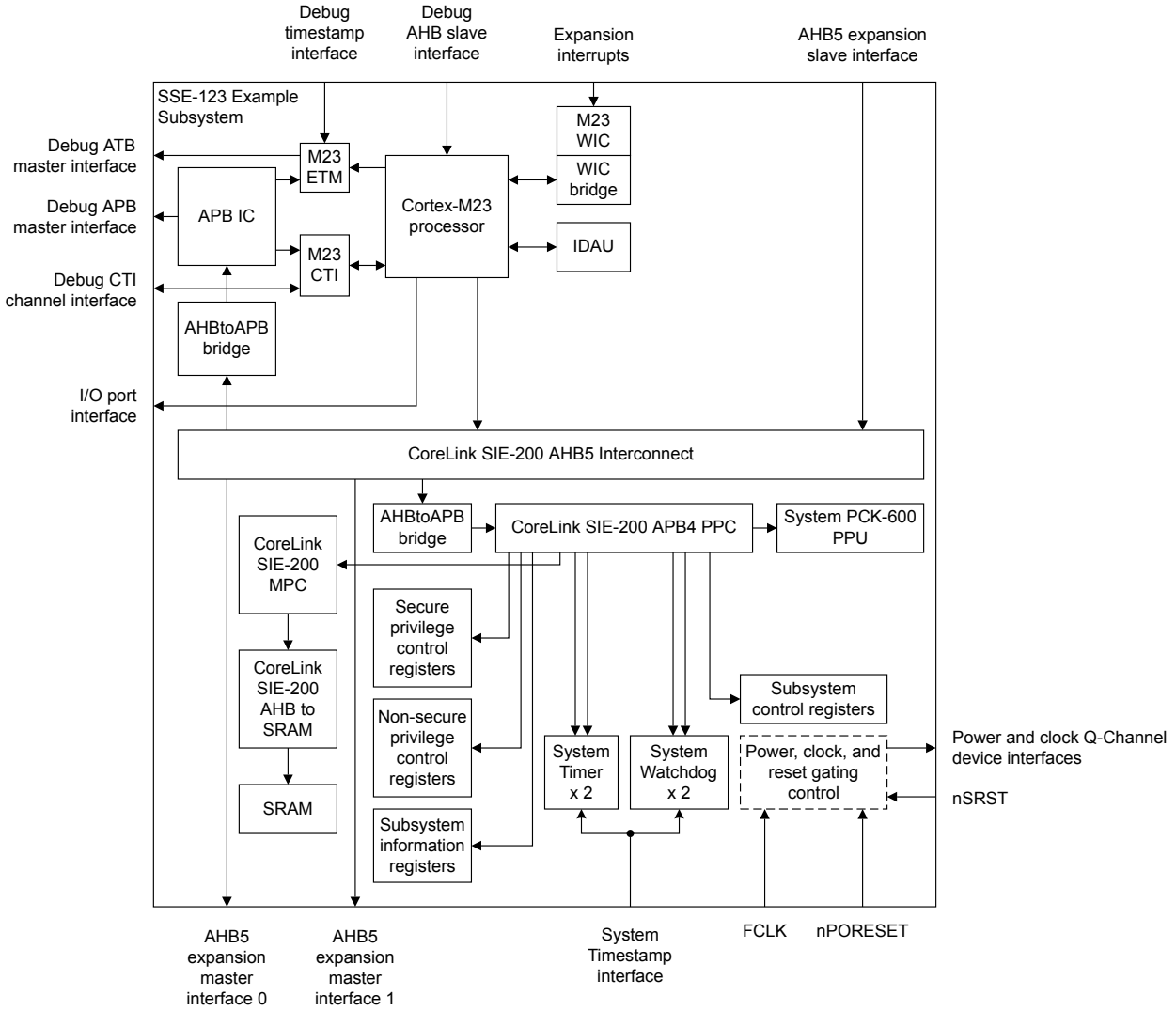

Figure 1-1 SSE-123 Example Subsystem block diagram

The block diagram shows all the key integrated components and interfaces.

1.2 About IoT System on Chip implementations

The SSE-123 Example Subsystem must be extended to create an IoT SoC. A complete system typically contains the following components:

Compute subsystem
The compute subsystem consists of a single Cortex®-M23 processor and associated bus, debug, controller, peripherals, and interface logic supplied by Arm.

Reference system memory and peripherals
SRAM is part of the SSE-123 Example Subsystem, but an SoC requires extra memory, control, and peripheral components beyond the minimum subsystem components. Flash memory, for example, is not provided with the SSE-123 Example Subsystem.

Communication interface
The endpoint must have some way of communicating with other nodes or masters in the system. This interface could be WiFi, Bluetooth, or a wired connection.

Sensor or control component
To be useful as an endpoint, the reference design is typically extended by adding sensors or control logic such as temperature input or motor control output.

Software development environment

Arm provides a complete software development environment which includes the Mbed™ operating system, Arm or GNU (GCC) compilers and debuggers, and firmware.

Custom peripherals typically require corresponding third-party firmware that can be integrated into the software stack.

This section contains the following subsection:
- *1.2.1 IoT hardware and software* on page 1-11.

1.2.1 IoT hardware and software

The following figure shows a block diagram of the hardware and software in an IoT system.

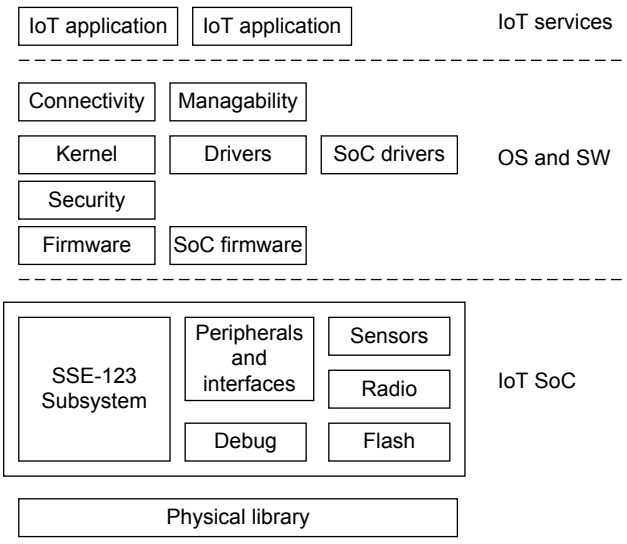

Figure 1-2 Hardware and software solution

1.3 Compliance

The SSE-123 Example Subsystem complies with, or implements, the specifications that this section describes. This document complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

This section contains the following subsections:

1.3.1 Arm architecture

The Cortex-M23 processor in the subsystem implements the Armv8-M Baseline Architecture with Security Extension.

See the *Arm®v8-M Architecture Reference Manual*.

1.3.2 Security architecture

The SSE-123 is designed to facilitate implementation of a TBSA-M compliant system.

See the *Arm® Platform Security Architecture - Trusted Base System Architecture for Armv8-M*.

1.3.3 Interrupt controller architecture

The SSE-123 implements Arm *Nested Vector Interrupt Controller* (NVIC) and Arm *Wakeup Interrupt Controller* (WIC).

See the *Arm® Cortex®-M23 Processor Technical Reference Manual*.

1.3.4 Advanced Microcontroller Bus Architecture (AMBA®)

The SSE-123 implements the following interface protocol architectures:

- *Advanced High-Performance Bus 5* (AHB5). See the *AMBA® 5 AHB Protocol Specification*.
- *Advanced Peripheral Bus 4* (APB4). See the *AMBA® APB Protocol Specification Version: 2.0*.
- *Low-Power Interface* (LPI), Q-Channel, and- P-Channel. See the *AMBA® Low Power Interface Specification*.

1.3.5 Debug architecture

The SSE-123 implements the Arm *Debug Interface Architecture 5* (ADIv5)-compliant debug interfaces.

See the *Arm® Debug Interface Architecture Specification, ADIv5.0 to ADIv5.2*.

1.3.6 Power control architecture

The SSE-123 implements the framework for system power control that the Arm *Power Control System Architecture* (PCSA) Version 2.0 specification defines.

See the *Arm® Power Control System Architecture Specification Version 2.0*.

1.4 Product documentation

This section describes the SSE-123 product documentation in relation to the design flow.

This section contains the following subsection:

- *1.4.1 Documentation* on page 1-13.

1.4.1 Documentation

The SSE-123 Example Subsystem documentation is as follows:

Technical Overview

The *Technical Overview* (TO) provides a high-level overview of the SSE-123 Example Subsystem:

- Hardware.
- Software.

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of the SSE-123 Example Subsystem. It is required at all stages of the design flow. The choices that are made in the design flow can mean that some behaviors that are described in the TRM are not relevant. If you are programming the SSE-123, then contact:

- The implementer to determine:
  - The build configuration of the implementation.
  - The integration, if any, that was performed before implementing the SSE-123.
- The integrator to determine the pin configuration of the device that you are using.

Configuration and Integration Manual

The *Configuration and Integration Manual* (CIM) describes:

- The available build configuration options and related issues in selecting them.
- Guidelines on how to integrate the SSE-123 Example Subsystem into an SoC.
- The SSE-123 Integration component, providing examples of integration with Arm eFlash and debug products.
- The processes to sign off the configuration, integration, and physical implementation of the design.

The CIM is a confidential book that is only available to licensees.

Verification Summary Report

The *Verification Summary Report* (VSR) describes:

- An overview of verification performed on the SSE-123 Example Subsystem.
- The verification quality definition for the subsystem.
- Configurations of the subsystem verified.
- A summary of verification results.

The VSR is a confidential book that is only available to licensees.

Subsystem Analysis Report

The *Subsystem Analysis Report* (SAR) describes:

- Performance characteristics of the SSE-123 Example Subsystem.
- Processor performance analysis and benchmark results.
- Performance analysis of memory system bandwidth and latency.

The SAR is a confidential book that is only available to licensees.

1.5 Product revisions

This section describes the differences in functionality between product revisions:

r0p0 First release.

Chapter 2
Hardware

This chapter describes the SSE-123 hardware.

It contains the following section:

2.1 Features of SSE-123

The SSE-123 Example Subsystem provides the following features:

- A Cortex-M23 processor, including Armv8-M Security Extensions.
- A single bank of system SRAM.
- CoreLink™ SIE-200 System IP for Embedded:
  - AHB5 bus matrix.
  - *Memory Protection Controller* (MPC).
  - *Peripheral Protection Controller* (PPC).
  - AHB5 to APB4 bridge.
  - AHB5 to SRAM controller.
- CoreLink PCK-600 Power Control Kit:
  - *Power Policy Unit* (PPU).
  - Clock controller.
  - Low-Power Distributor Q-Channel (LPD-Q).
- *Implementation Defined Attribution Unit* (IDAU).
- Cortex-M23 processor *Wakeup Interrupt Controller* (WIC).
- System Timer and Watchdog.
- System Control and Security Control Registers.
- Optional Cortex-M23 processor Debug components:
  - *Embedded Trace Macrocell* (ETM).
  - *Cross Trigger Interface* (CTI).
  - Debug APB interconnect.

Chapter 3
Software

This chapter describes the software that runs on the SSE-123.

It contains the following section:

3.1 About the software

Application processor firmware, which is available separately, consists of the code that is required to boot the subsystem up to the point where the OS execution starts. Contact your Arm representative for details on the software and its location.

The firmware contains:

- Trusted Firmware for M-class (TF-M) that separates the Secure and Non-secure execution environment.
- *Cortex Microcontroller Software Interface Standard* (CMSIS) compliant drivers.
- Mbed OS driver support and code for applicable peripherals.

Note

For more information on Mbed, see *mbed.com*.

Appendix A
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

- *A.1 Revisions* on page Appx-A-20.

A.1 Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue 0000-00

Change	Location	Affects
First release	-	-

Table A-2 Differences between issue 0000-00 and issue 0000-01

Change	Location	Affects
No technical chages.	-	-