CoreSight™ ETM™-R7

Revision: r0p1

Technical Reference Manual

ARM®

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CoreSight ETM-R7
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
21 March 2012	A	Non-Confidential	First release for r0p0
28 September 2012	B	Non-Confidential	First release for r0p1

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

Web Address

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CoreSight ETM-R7 Technical Reference Manual

Preface

This preface introduces the *CoreSight ETM-R7 Technical Reference Manual*. It contains the following sections:

About this book

This book is for the CoreSight *Embedded Trace Macrocell* (ETM) for the Cortex™-R7 MPCore™ processor, the ETM-R7.

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

Intended audience

This book is written for:

- Designers of development tools providing support for ETM functionality. Implementation-specific behavior is described in this document. You can find complementary information in the *Embedded Trace Macrocell Architecture Specification v4*.
- Hardware and software engineers integrating the macrocell into an ASIC that includes a Cortex-R7 MPCore processor. You can find complementary information in the *Cortex-R7 MPCore Integration Manual*.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the functionality of the macrocell.

Chapter 2 *Functional Description*

Read this for a description of the interfaces, operation, clocking and resets of the macrocell.

Chapter 3 *Programmers Model*

Read this for a description of the programmers model for the macrocell.

Appendix A *Signal Descriptions*

Read this for a description of the signals used in the macrocell.

Appendix B *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The ARM glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary*, http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html.

Conventions

Conventions that this book can use are described in:

- *Typographical conventions*.
- *Timing diagrams*.
- *Signals* on page viii.

Typographical conventions

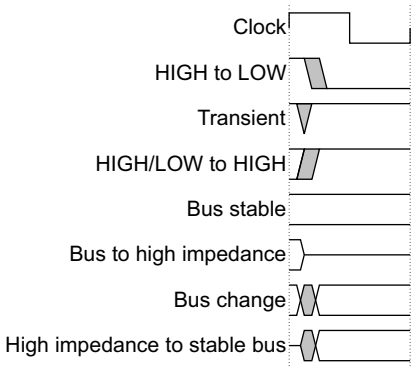
The following table describes the typographical conventions:

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace`	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace italic`	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Enclose replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter, http://infocenter.arm.com, for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:
- *Embedded Trace Macrocell Architecture Specification ETMv4* (ARM IHI 0064).
- *Cortex-R7 MPCore Technical Reference Manual* (ARM DDI 0458).
- *Cortex-R7 MPCore Configuration and Sign-off Guide (*ARM DII 0251).
- *Cortex-R7 MPCore Integration Manual* (ARM DIT 0030).
- *CoreSight SoC Technical Reference Manual* (ARM DDI 0480).
- *CoreSight SoC User Guide* (ARM DUI 0563).
- *CoreSight Architecture Specification* (ARM IHI 0029).
- *CoreSight Technology System Design Guide* (ARM DGI 0016).
- *ARM Reference Peripheral Specification* (ARM DDI 0062).
- *AMBA® 3 APB Protocol Specification* (ARM IHI 0024).
- *AMBA 3 ATB Protocol Specification* (ARM IHI 0032).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- The title.
- The number, ARM DDI 0459B.
- The page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

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Chapter 1
Introduction

This chapter introduces the CoreSight ETM-R7. It contains the following sections:

1.1 About the ETM-R7

The ETM-R7 provides real-time instruction trace and data trace for the Cortex-R7 MPCore processor. The ETM-R7 generates information that trace software tools use to reconstruct the execution of all or part of a program.

For full reconstruction of program execution, the ETM-R7 is able to trace:

- All instructions, including condition code pass/fail.
- Load/store address and data values.
- Values of context-ID.
- Target addresses of taken direct and indirect branch operations.
- Exceptions.
- Changes in processor instruction set state.
- Entry to and return from Debug state when Halting Debug-mode is enabled.
- Cycle counts relating to instruction execution.

The ETM-R7 contains logic, known as resources, that enables you to control tracing by specifying the exact set of triggering and filtering conditions required for a particular application. Resources include address comparators and data value comparators, counters, and a sequencer.

The ETM-R7 is a CoreSight component. For more information about CoreSight, see the *CoreSight Architecture Specification* and *CoreSight Technology System Design Guide*. For more information about the ETM architecture, see the *Embedded Trace Macrocell Architecture Specification*.

1.1.1 The CoreSight debug environment

The ETM-R7 is designed for use with CoreSight, an extensible, system-wide debug and trace architecture from ARM. See the *CoreSight SoC User Guide* for more information about how to use the ETM-R7 in a full CoreSight system.

A software debugger provides the user interface to the ETM-R7. You can use this interface to:

- Configure ETM-R7 facilities such as filtering.
- Configure optional trace features such as cycle accurate tracing.
- Configure the other CoreSight components such as the *Trace Port Interface Unit* (TPIU).
- Access the processor debug and performance monitor units.

A CoreSight system can provide memory-mapped access from the processor to its own debug and trace components.

The ETM-R7 outputs its trace stream to the AMBA 3 *Advanced Trace Bus* (ATB) interfaces. The CoreSight infrastructure provides the following options:

- Export the trace information through a trace port. An external *Trace Port Analyzer* (TPA) captures the trace information as Figure 1-1 on page 1-3 shows.
- Write the trace information directly to an on-chip *Embedded Trace Buffer* (ETB) or to system memory. You can read out the trace at low speed using a JTAG or Serial Wire interface when the trace capture is complete as Figure 1-1 on page 1-3 shows.

The debugger extracts the executed image from memory and the captured trace information from the TPA or ETB and decompresses the image to provide full disassembly, with symbols, of the code that was executed. The trace information generated by the ETM-R7 gives the debugger the capability to link this data back to the original high-level source code, to provide a visualization of how the code was executed on the Cortex-R7 MPCore processor.

Figure 1-1 shows how the ETM-R7 fits into a CoreSight debug environment to provide full trace capabilities in a single processor system. In this example, the external debug software configures the trace and debug components through the *Debug Access Port* (DAP). The ROM table contains a unique identification code for the SoC and the base addresses of the components connected to the debug APB. The trace stream from the ETM-R7 is replicated to provide on-chip storage using the CoreSight ETB or output off-chip using the TPIU. Cross-triggering operates through the *Cross Trigger Interface* (CTI) and *Cross Trigger Matrix* (CTM) components.

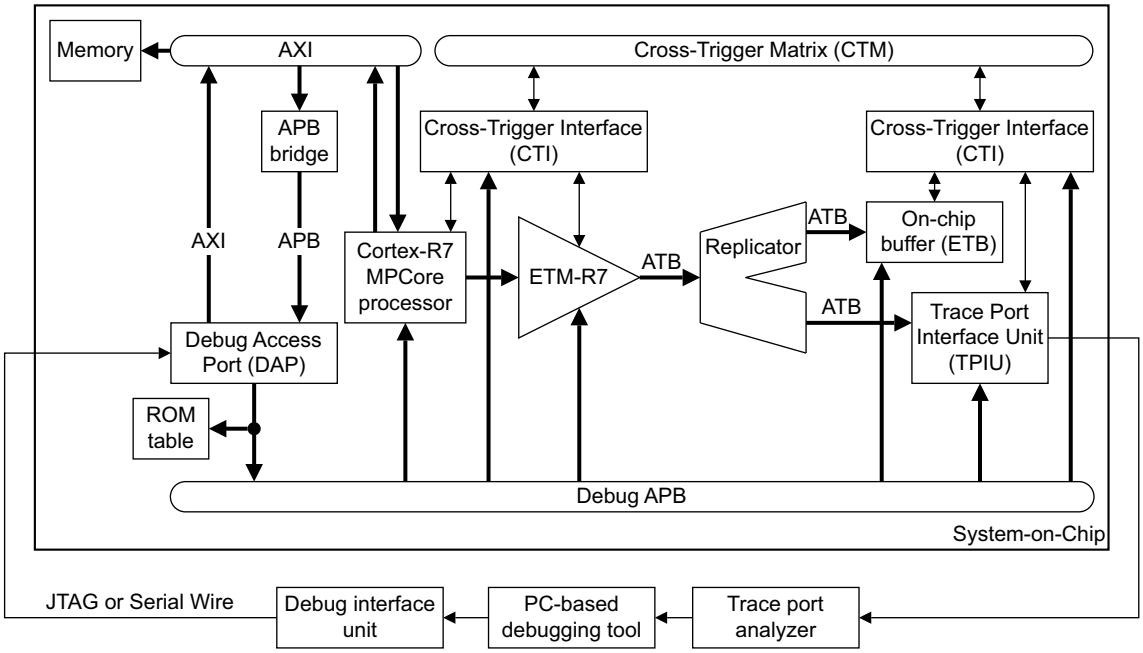

Figure 1-1 ETM-R7 system diagram

Note

In Figure 1-1, the arrows on the thick lines show the transaction direction on busses, from master to slave port. Each bus contains individual signals that go from master to slave and other signals that go from slave to master.

For a Cortex-R7 MPCore processor implementation with two processors, the following options are available:

- One ETM, statically shared between the processors.
- Two ETMs, one dedicated to each processor.

1.2 Compliance

The ETM-R7 complies with, or implements, the specifications described in:

- *Trace macrocell*.
- *Advanced Microcontroller Bus Architecture*.

This TRM complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

1.2.1 Trace macrocell

The ETM-R7 implements the ETM architecture version 4. See the *Embedded Trace Macrocell Architecture Specification ETMv4*.

1.2.2 Advanced Microcontroller Bus Architecture

The ETM-R7 complies with the *Advanced Microcontroller Bus Architecture* (AMBA) 3 *Advanced Peripheral Bus* (APB) and *Advanced Trace Bus* (ATB) protocols. See the *AMBA 3 APB Protocol Specification* and *AMBA 3 ATB Protocol Specification*.

1.3 Features

ETM-R7 supports tracing of 32-bit ARM instructions, and 16-bit and 32-bit Thumb instructions.

See the *Embedded Trace Macrocell Architecture Specification ETMv4* for information about:

- The trace protocol.
- The features of ETMv4.
- Controlling tracing using triggering and filtering resources.
- ETM sharing.

Table 1-1 shows the features of the ETM-R7 that are implementation-defined, in terms of either:

- The number of times the feature is implemented.
- The size of the feature.

Table 1-1 ETM-R7 features with implementation-defined number of instances or size

Feature	ETM-R7 value	Notes
Address comparators	4 pairs	See bits[3:0] of the *ID Register 4* on page 3-42
Data value comparators	2	See bits[7:4] of the *ID Register 4* on page 3-42
Context ID comparators	1	See bits[27:24] of the *ID Register 4* on page 3-42
Single-Shot comparator resource	2, one for instruction, one for data	See bits[2:0] of the *Single-Shot Comparator Status Registers 0-1* on page 3-46
Counters	2	See bits[30:28] of the *ID Register 5* on page 3-43
Cycle count size	12	See bits[28:25] of the *ID Register 2* on page 3-40
Sequencer	1	One four-state sequencer. See bits[27:25] of the *ID Register 5* on page 3-43.
Processor comparator inputs	Not implemented	See bits[15:12] of the *ID Register 4* on page 3-42
External inputs	64	See bits[8:0] of the *ID Register 5* on page 3-43
External outputs	4	See bits[3:0] of the *Event Control 1 Register* on page 3-18
External input selectors	4	See bits[11:9] of the *ID Register 5* on page 3-43
Resource selector pairs	8	See bits[19:16] of the *ID Register 4* on page 3-42
Instruction trace port size	32-bit	-
Data trace port size	64-bit	-
Instruction FIFO[a]	128 byte with 32-bit output	Uses ATB
Data FIFO	256 byte with 64-bit output	Uses ATB
Claim tag bits	4	See bits[3:0] of the *Claim Tag Set Register* on page 3-56

a. Instruction trace can be configured to take priority over data trace. See bit[10] of the TRCSTALLCTLR.

Table 1-2 shows the optional features of the ETM architecture that the ETM-R7 implements.

Table 1-2 ETM-R7 implementation of optional features

Feature	Implemented?	Notes
Configurable FIFO	No	-
Trace Start/Stop block	Yes	*ViewInst Start/Stop Control Register* on page 3-25
Trace all branches option	Yes	See bit[5] of the *ID Register 0* on page 3-38
Trace of conditional instructions	Yes	See bits[13:12] and bit [6] of the *ID Register 0* on page 3-38, using the full CPSR value
Cycle counting in instruction trace	Yes	See bit[7] of the *ID Register 0* on page 3-38
Data trace supported	Yes	See bits[4:3] of the *ID Register 0* on page 3-38
Data address comparison	Yes	See bit[8] of the *ID Register 4* on page 3-42
OS Lock mechanism	Yes	*OS Lock Access Register* on page 3-47
Secure non-invasive debug	No	The Cortex-R7 MPCore processor does not implement the Security Extensions
Context ID tracing	Yes	See bits[9:5] of the *ID Register 2* on page 3-40
Trace output	Yes	ATB
Timestamp size (48/64)	System configurable	See bits[28:24] of the *ID Register 0* on page 3-38
Memory mapped access to ETM registers	Yes	-
System instruction access to ETM registers	No	-
VMID comparator support	No	See bits[31:28] of the *ID Register 4* on page 3-42
ATB trigger support	Yes	See bit[22] of the *ID Register 5* on page 3-43

See Appendix A *Signal Descriptions* for information about the macrocell signals.

1.4 Interfaces

The ETM-R7 has the following main interfaces:

- Processor trace.
- ATB.
- Debug APB.
- Test.

Interfaces on page 2-4 describes the ETM-R7 interfaces in more detail.

1.5 Configurable options

The ETM-R7 includes the following configuration inputs:

- **NUMPROC**.
- **SYSSTALL**.
- **TSSIZE**.

See the *Embedded Trace Macrocell Architecture Specification ETMv4* for more information.

1.6 Test features

The ETM-R7 provides the **DFTSE** input for testing the implemented device. See the *Cortex-R7 MPCore Integration Manual*.

See also *Integration Test Registers* on page 3-65 for information about the integration test registers, provided for testing the ETM-R7 integration in a SoC and performing CoreSight topology detection.

1.7 Product documentation and design flow

This section describes the ETM-R7 books, how they relate to the design flow, and the relevant architectural standards and protocols.

See *Additional reading* on page viii for more information about the books described in this section.

1.7.1 Documentation

The ETM-R7 documentation is as follows:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of the ETM-R7. It is required at all stages of the design flow. Some behavior described in the TRM might not be relevant because of the way that the ETM-R7 is implemented and integrated.

Configuration and Sign-off Guide

The *Cortex-R7 MPCore Configuration and Sign-off Guide* (CSG) describes the processes to test and sign off the implemented design.

The ARM product deliverables include reference scripts and information about using them to implement your design. Reference methodology flows supplied by ARM are example reference implementations. Contact your EDA vendor for EDA tool support.

The CSG is a confidential book that is only available to licensees.

Integration Manual

The *Cortex-R7 MPCore Integration Manual* (IM) describes how to integrate the ETM-R7 into a SoC. It includes a description of the pins that the integrator must tie off, to configure the macrocell for the required integration.

The IM is a confidential book that is only available to licensees.

1.7.2 Design flow

The ETM-R7 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following process:

Implementation

The implementer configures and synthesizes the RTL to produce a hard macrocell. This might include integrating RAMs into the design.

Integration The integrator connects the implemented design into a SoC. This includes connecting it to a memory system and peripherals.

Programming

This is the last process. The system programmer develops the software required to configure and initialize the ETM-R7, and tests the required application software.

Each stage of the process:

- Can be performed by a different party.
- Can include implementation and integration choices that affect the behavior and features of the ETM-R7.

The operation of the final device depends on:

Build configuration

The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting macrocell.

Configuration inputs

The integrator configures some features of the ETM-R7 by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software configuration

The programmer configures the ETM-R7 by programming particular values into registers. This affects the behavior of the ETM-R7.

See Chapter 3 *Programmers Model* for information on the ETM-R7 registers.

Note

This manual refers to implementation-defined features that are applicable to build configuration options. Reference to a feature that is included means that the appropriate build and pin configuration options are selected. Reference to an enabled feature means one that has also been configured by software.

1.8 Product revisions

This section describes the differences in functionality between product revisions:

r0p0 First release.

r0p0-r0p1 The following changes have been made in this release:

- ID register values changed to reflect product revision status:

  ID Register 1 `0x4100F401`.
- Number of P0 keys increased from 32 to 64. See Table 3-40 on page 3-36.
- Various engineering errata fixes.

Chapter 2
Functional Description

This chapter describes the interfaces, operation, clocking and resets of the ETM-R7. It contains the following sections:

2.1 About the functions

Figure 2-1 shows the main functional blocks of the ETM-R7.

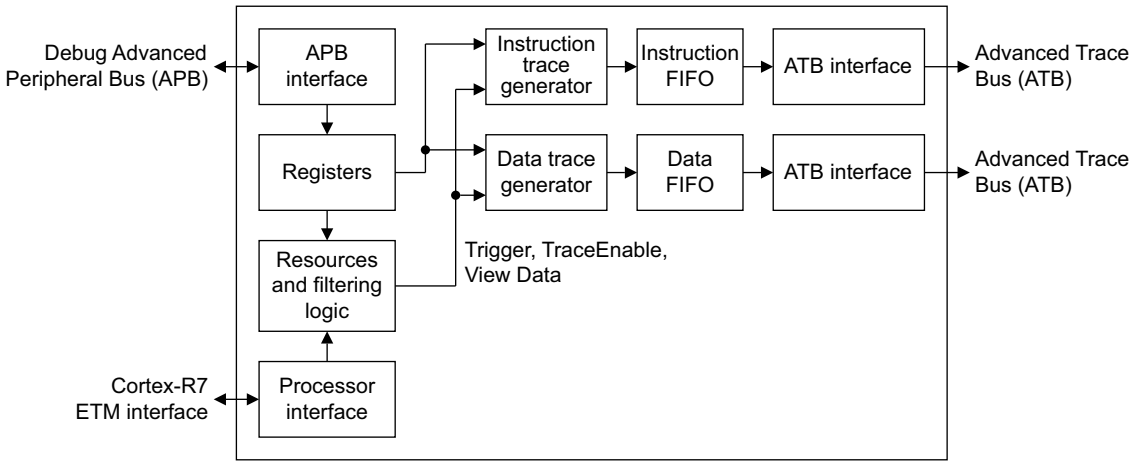

Figure 2-1 ETM-R7 block diagram

2.1.1 Processor interface

This block connects to the ETM-R7 interface. It tracks the execution and speculation information from the processor, decodes the control signals and passes on the information to the internal interfaces.

2.1.2 Instruction trace generator

This block generates the trace packets that are a compressed form of the execution information provided by the Cortex-R7 MPCore processor trace generation. The trace packets are then passed to the FIFO.

2.1.3 Data trace generator

This block generates trace packets that are a compressed form of the external data transfer provided by the Cortex-R7 MPCore processor trace generation. The trace packets are then passed to the FIFO.

2.1.4 FIFO

This block buffers bursts of trace packets. Separate FIFOs are provided for instruction and data trace streams.

2.1.5 Resources and filtering logic

These blocks contain various comparators and state machines that are programmed by trace software to trigger and filter the trace information. They start and stop trace generation, depending on the conditions that have been set.

2.1.6 ATB interface

This block reads up to four or eight bytes of packet information from the FIFO and sends them over the ATB interface.

2.1.7 APB interface

This block implements the interface to the APB, that provides access to the programmable registers. It provides address decoding and pipelining of the address and data to and from the APB.

2.1.8 Global timestamping

The ETM-R7 supports connection to a global timestamp source. This provides a 48 or 64 bit timestamp which can be used for coarse-grained profiling, and correlation of trace sources. ARM recommends that the timestamp counter is no slower than 10% of the processor clock.

Note

Decompression of data trace relies on the presence of a global timestamp count.

2.2 Interfaces

The ETM-R7 has the following interfaces:

ATB Two ATB interfaces, one 32 bits and one 64 bits wide, used for trace output from the macrocell. These interfaces have handshaking signals that indicate when trace data is valid and when the receiving component is ready to accept data. There are also signals to request and acknowledge a flush of the trace information and to indicate when a trigger condition has occurred.

See the *AMBA 3 ATB Protocol Specification* for more information about these interfaces.

APB An APB interface that provides access to the programmable registers in the ETM-R7 and connects to the system Debug APB. This interface is used to configure the ETM-R7 for a trace session.

See the *AMBA 3 APB Protocol Specification* for more information about this interface.

Processor trace

The Cortex-R7 MPCore processor passes its execution information to the ETM-R7 over the processor trace interface. This interface provides both instruction and data execution history and contains address, data, and control information. The information carried on the control bus includes:

- The number of instructions executed in the same cycle.
- Changes in program flow.
- The current processor instruction state.
- The addresses of memory locations accessed by load and store instructions.
- The data values transferred by load and store instructions.
- The type, direction, and size of a transfer.
- Condition code information.
- Exception information.
- Current context ID.

There is also a context ID bus that indicates the current context ID value of the processor.

This interface also includes:

- The **ETMEVENT** bus. See *CPU PMU connectivity* on page 2-5.
- Wait for interrupt state information signals.
- A signal from the ETM to power up the interface.

Miscellaneous

The ETM-R7 has other interface signals that:

- Configure the ETM. See *Configurable options* on page 1-8.
- Input and output external resource information that controls triggering and filtering of the trace stream.
- Control which core is enabled, as the trace source, on the processor trace interface of the ETM.
- Enable invasive and non-invasive debug.

Test This interface contains the scan enable signal used in production testing of the ETM-R7.

2.2.1 CPU PMU connectivity

Table 2-1 shows the connection of the **ETMEVENT** inputs. These come from the CTI, the processor *Performance Monitoring Unit* (PMU), and ECC monitoring logic, if present..

Table 2-1 ETMEVENT connections

Bits	Description
[63]	ECC Fatal processor 1, if present
[62]	ECC Fatal processor 0, if present
[61:60]	Spare
[59:4]	Processor performance monitor events
[3:0]	CTITRIGOUT

For details of the mapping of processor performance monitor events, see the *Cortex-R7 MPCore Technical Reference Manual*.

Note

When a single ETM is shared between two processors, the PMU event pins are driven from the relevant processor, but the CTI connections for the ETM are always to CTI0, regardless of which processor is being traced.

The ETM output resources, **ETMEXTOUT**, are connected to the CTI and also as inputs to the processor PMU, as Table 2-2 shows.

Table 2-2 ETM EXTOUT connections to CTI and processor PMU

ETM output	CTI input	PMU input
ETMEXTOUT[0]	**CTITRIGIN[2]**	-
ETMEXTOUT[1]	**CTITRIGIN[3]**	**PMUEXTIN[0]**
ETMEXTOUT[2]	**CTITRIGIN[4]**	**PMUEXTIN[1]**
ETMEXTOUT[3]	**CTITRIGIN[5]**	-

2.3 Clocking and resets

The following sections describe the ETM-R7 clocks and resets:

- *ETM-R7 clock*.
- *ETM-R7 low power control*.
- *ETM-R7 reset*.
- *Access permissions and power domains*.

2.3.1 ETM-R7 clock

The ETM-R7 has one clock, **CLK**. This clock is synchronous to the **CLK** input of the Cortex-R7 MPCore processor.

2.3.2 ETM-R7 low power control

The ETM-R7 has outputs to indicate if the debugger expects power to be maintained, and also an output to indicate when tracing is inactive. The use of these signals is implementation specific.

The ETM can be configured to remain active even if the Cortex-R7 MPCore processor enters a low power state. See bit[23] of the *ID Register 5* on page 3-43.

2.3.3 ETM-R7 reset

The ETM-R7 has a single reset, **nRESET**, and must only be reset by a debug reset event.

Note

The programming state must be reconfigured after a reset.

2.3.4 Access permissions and power domains

To determine the access permissions as described in the ETM Architecture v4, the ETM implements a SinglePower domain. The ETM (debug) power domain is typically separate from the processor power domain.

2.4 Operation

This section describes the implementation-defined features of the ETM-R7 macrocell. It contains the following sections:

- *Implementation-defined registers*.
- *Precise TraceEnable events*.
- *Parallel instruction execution*.
- *Context ID tracing* on page 2-8.
- *Trace and comparator features* on page 2-8.
- *Data address range filtering* on page 2-8.
- *Interaction with the PMU* on page 2-8.
- *Packet formats* on page 2-9.
- *Resource selection* on page 2-9.
- *Trace flush behavior* on page 2-10.
- *Low power state behavior* on page 2-10.
- *Cycle counter* on page 2-10.
- *Micro-architectural exceptions* on page 2-10.
- *Synchronization* on page 2-11.

See the *Embedded Trace Macrocell Architecture Specification ETMv4* for more information about the operation of the ETM-R7.

2.4.1 Implementation-defined registers

There are two groups of ETM registers:

- Registers that are completely defined by the *Embedded Trace Macrocell Architecture Specification ETMv4*.
- registers that are at least partly implementation-defined.

See Chapter 3 *Programmers Model* for more information about the ETM registers.

2.4.2 Precise TraceEnable events

The *Embedded Trace Macrocell Architecture Specification ETMv4* states that **ViewInst** and **ViewData** are imprecise under certain conditions, with some implementation-defined exceptions. The only condition which ensures that **ViewInst** and **ViewData** are precise is that the enabling event condition is TRUE.

2.4.3 Parallel instruction execution

The Cortex-R7 MPCore processor supports parallel instruction execution. This means the macrocell is capable of tracing two instructions per cycle.

Although the **ViewInst** is evaluated for each instruction as required, the macrocell does not trace one instruction without the other. In other words, if one instruction is specified to be traced, the instruction it is paired with is always traced as well. If **ViewData** is active, any data associated with the paired instruction is also traced. If **ViewData** selects only one transfer of a multiple load or store, both transfers which are issued by the core as a 64-bit transfer are traced.

2.4.4 Context ID tracing

The ETM-R7 detects updates to the Context ID register and, when the context change sequence is completed with an ISB or exception, traces the appropriate number of bytes as a context ID packet as part of the instruction trace stream. Coprocessor register transfers never generate data trace.

2.4.5 Trace and comparator features

In ETM Architecture v4, it is implementation-defined whether an ETM supports a number of trace and comparator features. This section specifies the implementation of these features on the ETM-R7:

- *Trace features*.
- *Comparator features*.

Trace features

The ETM-R7 implements all of the ETMv4 trace features. This means it supports:

- Data value and data address tracing.
- Data suppression.
- Cycle-accurate tracing.
- Timestamping.

See the *Embedded Trace Macrocell Architecture Specification ETMv4* for descriptions of these features.

Comparator features

The ETM-R7 implements data address comparison. See the *Embedded Trace Macrocell Architecture Specification ETMv4* for a description of data address comparison.

2.4.6 Data address range filtering

When data address range filtering is used to include both loads and stores, or no data address include ranges are selected, an address range is set to exclude loads or stores, but not both. When a SWP matches for both the include and exclude ranges, both the load and store transfers are traced.

2.4.7 Interaction with the PMU

The Cortex-R7 MPCore processor includes a *Performance Monitoring Unit* (PMU) that enables events, such as cache misses and instructions executed, to be counted over a period of time. The macrocell can still use these events by means of the extended external input facility. Each bit in the **ETMEVENT[63:0]** input is mapped to the corresponding extended external input. See the *Cortex-R7 MPCore Technical Reference Manual* for details of the mapping of PMU events to bits in this bus.

Bits[3:0] of **ETMEVENT** are reserved for cross trigger connections. PMU event signals use bits[50:4], ECC signals use bits[63:62] if implemented, and the remainder are free for system specific use if implemented. Any four of the external inputs can be selected for further use in the resource logic.

PMU event number 8, Executed instruction count, is presented by the core as a 6-bit vector which the ETM is not able to count. These are ORed together for connection to the ETM and the ETM is not able to count instruction execution directly.

The Cortex-R7 PMU can count two of the ETM external outputs as additional events. These events are not provided back to the macrocell as extended external inputs.

These facilities enable additional filtering of the system events using ETM resources, such as instruction address ranges or the start/stop resource, before they are passed back to the PMU for counting. To do this:

- Configure the ETM external input selectors to the system events you want to count.
- Configure the required ETM filtering resource as appropriate.
- Configure the ETM external outputs and the required ETM filtering resource.
- Select the ETM external outputs as the events to be counted in the Cortex-R7 PMU.

2.4.8 Packet formats

See the *Embedded Trace Macrocell Architecture Specification ETMv4* for descriptions of the trace packet formats generated by the ETM-R7.

2.4.9 Resource selection

The ETM-R7 uses event selectors to control the following resources:

- Trace events (triggers and markers in the trace stream).
- Timestamp event.
- ViewInst event.
- ViewData event.
- Counter control.
- Sequencer state transitions.

Each event selector is configured to be sensitive to a resource selector pair, and one resource selector pair can be used to control more than one event selector.

The ETM provides one fixed resource selector pair, with static values of 0 and 1, and seven configurable selector pairs. A resource selector pair provides a bitfield OR selector for resources in two different groups, with each group and a configurable boolean combination provided.

Table 2-3 shows the resources which can be selected.

Table 2-3 Resource selection

Group	Select	Resource
b0000	0-3	External input selector 0-3
b0010	0-1	Counter at zero 0-1
	4-7	Sequencer states 0-3
b0011	0-1	Single-Shot comparator 0-1
b0100	0-7	Single address comparator 0-7
b0101	0-3	Address range comparator 0-3
b0110	0	Context ID comparator 0

As an example, Figure 2-2 on page 2-10 shows the steps necessary to use a single address comparator to generate a trigger event and an ATB trigger. This example uses the first single resource selector which can be user-configured.

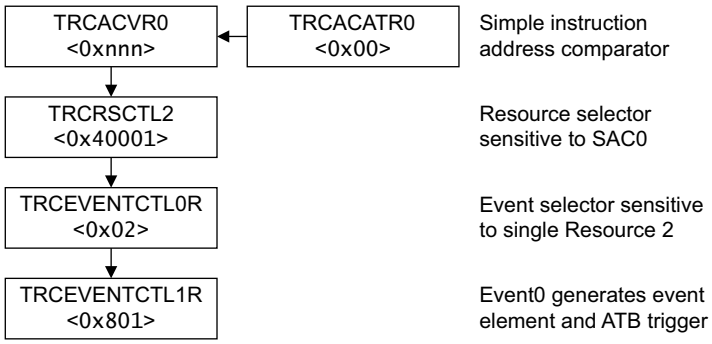

Figure 2-2 Trigger event resource selection

2.4.10 Trace flush behavior

Events which have been observed by the ETM can be confirmed to have reached the trace bus output with the use of the ATB flush protocol. Both ATB ports must be flushed if all trace is required. The ETM internally flushes instruction and data trace together whenever either flush request is seen but does not guarantee that the trace data has drained from the ETM. When the processor enters a low power state, this also causes all trace to be output from the ETM.

If the processor enters a low-power state while an ATB flush request is in progress, the flush is acknowledged only after all instructions presented to the ETM have been traced.

2.4.11 Low power state behavior

When the processor enters a low power state, the ETM resources become inactive after a delay which allows the last instruction executed to trigger a comparator, update the counter or sequencer, and then cause an event packet to be inserted in the trace stream. This event packet is presented on the trace bus before the ETM itself enters a low power state. If an event packet is generated for a different reason, it is not guaranteed to be output before the ETM enters a low power state, but is traced when the processor leaves the low power state, if the ETM logic is not reset before this can occur.

This low power behavior can be disabled, in which case the ETM resources remain active.

2.4.12 Cycle counter

The cycle counter is a 12 bit counter. It does not count when non-invasive debug is disabled, or when the processor is in a low power state.

2.4.13 Micro-architectural exceptions

These exception encodings are intended to permit trace decompression rather than to trace the underlying cause of instruction replay.

The ETM indicates exceptions for the following micro-architectural behaviors using the following TYPE encodings:

b10000 Execution replay resulting from incorrect decode prediction.

b10001 Execution replay resulting from ECC error detection.

2.4.14 Synchronization

All sources of synchronization are combined before being used to generate synchronization in both trace streams, provided that data trace is active.

Periodic synchronization of the data trace stream is aligned with synchronization in the instruction stream. If the ETM is configured to trace only events in the data stream, it is also necessary to configure the instruction trace stream to contain sufficient elements to permit the required data trace stream synchronization.

Chapter 3
Programmers Model

This chapter describes the programmers model. It contains the following sections:

3.1 About the programmers model

This chapter describes the mechanisms for programming the registers used to set up the trace and triggering facilities of the macrocell. The programmers model enables you to use the ETM registers to control the macrocell.

3.2 Modes of operation and execution

The following sections describes how to control ETM programming.

3.2.1 Controlling ETM programming

When programming the ETM registers, you must enable all the changes at the same time. For example, if the counter is reprogrammed, it might start to count based on incorrect events, before the trigger condition has been correctly set up.

You must use the ETM main enable in the TRCPRGCTLR to disable all trace operations during programming. See *Programming Control Register* on page 3-13. Figure 3-1 shows the procedure to follow.

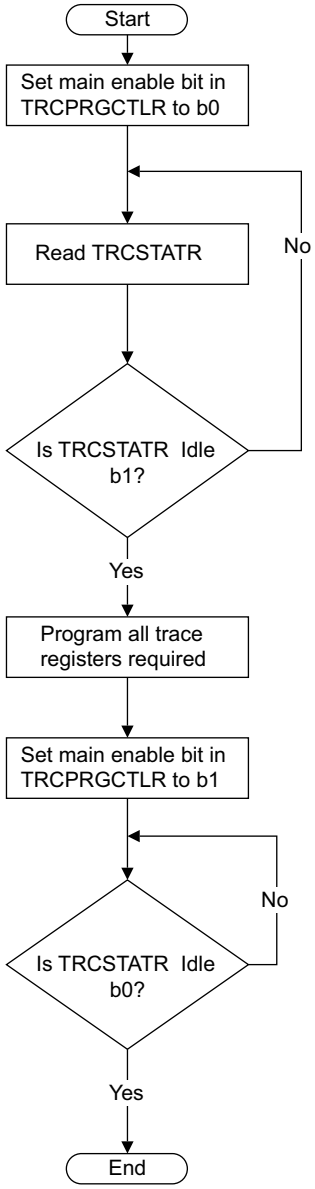

Figure 3-1 Programming ETM-R7 registers

The Cortex-R7 MPCore processor does not have to be in the debug state while you program the ETM registers.

3.2.2 Programming and reading ETM registers

You program and read the ETM registers using the Debug APB interface. This provides a direct method of programming the ETM-R7.

3.3 Register summary

This section summarizes the ETM registers. For full descriptions of the ETM registers, see:

- *Register descriptions* on page 3-13, for the implementation-defined registers.
- the *Embedded Trace Macrocell Architecture Specification ETMv4*, for the other registers.

Table 3-1 shows the ETM registers in numerical order and describes each register.

The macrocell registers are listed by functional group in *Functional grouping of registers* on page 3-8. The functional group register tables include additional information about each register:

- The register access type. This is read-only, write-only or read and write.
- The base offset address of the register. The base address of a register is always four times its register number.
- Additional information about the implementation of the register, where appropriate.

Note

- Registers not listed here are not implemented. Reading a non-implemented register address returns 0. Writing to a non-implemented register address has no effect.
- In Table 3-1:
  - The Reset value column shows the value of the register immediately after an ETM reset. For read-only registers, every read of the register returns this value.
  - Access type is described as follows:

    RW Read and write.

    RO Read only.

    WO Write only.

All ETM registers are 32 bits wide.

Table 3-1 ETM-R7 register summary

Register number	Base offset	Name	Type	Reset value	Description
1	0x004	TRCPRGCTLR	RW	0x00000000	*Programming Control Register* on page 3-13
2	0x008	TRCPROCSELR	RW	0x00000000	*Processor Select Control Register* on page 3-13
3	0x00C	TRCSTATR	RO	-	*Status Register* on page 3-14
4	0x010	TRCCONFIGR	RW	-	*Trace Configuration Register* on page 3-15
6	0x018	TRCAUXCTLR	RW	0x00000000	*Auxiliary Control Register* on page 3-16
8	0x020	TRCEVENTCTL0R	RW	-	*Event Control 0 Register* on page 3-17
9	0x024	TRCEVENTCTL1R	RW	-	*Event Control 1 Register* on page 3-18
11	0x02C	TRCSTALLCTLR	RW	-	*Stall Control Register* on page 3-19
12	0x030	TRCTSCTLR	RW	-	*Global Timestamp Control Register* on page 3-20
13	0x034	TRCSYNCPR	RW	-	*Synchronization Period Register* on page 3-21
14	0x038	TRCCCCTLR	RW	-	*Cycle Count Control Register* on page 3-22

Table 3-1 ETM-R7 register summary (continued)

Register number	Base offset	Name	Type	Reset value	Description
15	0x03C	TRCBBCTLR	RW	-	*Branch Broadcast Control Register* on page 3-22
16	0x040	TRCTRACEIDR	RW	-	*Trace ID Register* on page 3-23
32	0x080	TRCVICTLR	RW	-	*ViewInst Main Control Register* on page 3-24
33	0x084	TRCVIIECTLR	RW	-	*ViewInst Include/Exclude Control Register* on page 3-25
34	0x088	TRCVISSCTLR	RW	-	*ViewInst Start/Stop Control Register* on page 3-25
40	0x0A0	TRCVDCTLR	RW	-	*ViewData Main Control Register* on page 3-26
41	0x0A4	TRCVDSACCTLR	RW	-	*ViewData Include/Exclude Single Address Comparator Register* on page 3-27
42	0x0A8	TRCVDARCCTLR	RW	-	*ViewData Include/Exclude Address Range Comparator Register* on page 3-28
64-66	0x100-0x108	TRCSEQEVRn	RW	-	*Sequencer State Transition Control Registers 0-2* on page 3-29
70	0x118	TRCSEQRSTEVR	RW	-	*Sequencer Reset Control Register* on page 3-29
71	0x11C	TRCSEQSTR	RW	-	*Sequencer State Register* on page 3-30
72	0x120	TRCEXTINSELR	RW	-	*External Input Select Register* on page 3-31
80-81	0x140-0x144	TRCCNTRLDVRn	RW	-	*Counter Reload Value Registers 0-1* on page 3-32
84	0x150	TRCCNTCTLR0	RW	-	*Counter Control Register 0* on page 3-32
85	0x154	TRCCNTCTLR1	RW	-	*Counter Control Register 1* on page 3-33
88-89	0x160-0x164	TRCCNTVRn	RW	-	*Counter Value Registers 0-1* on page 3-34
96	0x180	TRCIDR8	RO	0x00000040	*ID Register 8-13* on page 3-35
97	0x184	TRCIDR9	RO	0x00000040	
98	0x188	TRCIDR10	RO	0x00000040	
99	0x18C	TRCIDR11	RO	0x00000011	
100	0x190	TRCIDR12	RO	0x00000020	
101	0x194	TRCIDR13	RO	0x00000000	
112	0x1C0	TRCIMSPEC0	RW	0x00000000	*Implementation Specific Register 0* on page 3-37
120	0x1E0	TRCIDR0	RO	0xXX001EFF	*ID Register 0* on page 3-38
121	0x1E4	TRCIDR1	RO	0x4100F401	*ID Register 1* on page 3-39
122	0x1E8	TRCIDR2	RO	0x00420084	*ID Register 2* on page 3-40
123	0x1EC	TRCIDR3	RO	0xXX090004	*ID Register 3* on page 3-41
124	0x1F0	TRCIDR4	RO	0x01270124	*ID Register 4* on page 3-42
125	0x1F4	TRCIDR5	RO	0x28C70840	*ID Register 5* on page 3-43
130-140	0x208-0x240	TRCRSCTLRn	RW	-	*Resource Selection Registers 2-16* on page 3-44

Table 3-1 ETM-R7 register summary (continued)

Register number	Base offset	Name	Type	Reset value	Description
160-161	0x280-0x284	TRCSSCCRn	RW	-	*Single-Shot Comparator Control Registers 0-1* on page 3-45
168-169	0x2A0-0x2A4	TRCSSCSRn	RW	-	*Single-Shot Comparator Status Registers 0-1* on page 3-46
192	0x300	TRCOSLAR	WO	-	*OS Lock Access Register* on page 3-47
193	0x304	TRCOSLSR	RO	-	*OS Lock Status Register* on page 3-48
196	0x310	TRCPDCR	RW	0x00000000	*Power Down Control Register* on page 3-49
197	0x314	TRCPDSR	RO	0x00000023	*Power Down Status Register* on page 3-49
256-271	0x400-0x43C	TRCACVRn	RW	-	*Address Comparator Value Registers 0-7* on page 3-50
288-303	0x480-0x4BC	TRCACATRn	RW	-	*Address Comparator Access Type Registers 0-7* on page 3-51
320-321	0x500-0x504	TRCDVCVRn	RW	-	*Data Value Comparator Value Registers 0-1* on page 3-53
352-359	0x580-0x59C	TRCDVCMRn	RW	-	*Data Value Comparator Mask Registers 0-1* on page 3-53
384	0x600	TRCCIDCVR0	RW	-	*Context ID Comparator Value Register 0* on page 3-54
951	0xEDC	TRCITMISCOUTR	RW	-	*Integration Miscellaneous Outputs Register* on page 3-66
952	0xEE0	TRCITMISCINR	RO	-	*Integration Miscellaneous Inputs Register* on page 3-67
953	0xEE4	TRCITATBIDR	RW	-	*Integration ATB Identification Register* on page 3-68
954	0xEE8	TRCIRDDATAR	RW	-	*Integration Data ATB Data Register* on page 3-69
955	0xEEC	TRCITIDATAR	RW	-	*Integration Instruction ATB Data Register* on page 3-69
956	0xEF0	TRCITDATBINR	RO	-	*Integration Data ATB In Register* on page 3-70
957	0xEF4	TRCITIATBINR	RO	-	*Integration Instruction ATB In Register* on page 3-71
958	0xEF8	TRCITDATBOUTR	RW	-	*Integration Data ATB Out Register* on page 3-71
959	0xEFC	TRCITIATBOUTR	RW	-	*Integration Instruction ATB Out Register* on page 3-72
960	0xF00	TRCITCTRL	RW	0x00000000	*Integration Mode Control Register* on page 3-55
1000	0xFA0	TRCCLAIMSET	RW	0x00000000	*Claim Tag Set Register* on page 3-56
1001	0xFA4	TRCCLAIMCLR	RW	0x00000000	*Claim Tag Clear Register* on page 3-56
1002	0xFA8	TRCDEVAFF0	RO	-	*Device Affinity Register* on page 3-57
1004	0xFB0	TRCLAR	WO	-	*Software Lock Access Register* on page 3-58
1005	0xFB4	TRCLSR	RO	-	*Software Lock Status Register* on page 3-58
1006	0xFB8	TRCAUTHSTATUS	RO	-	*Authentication Status Register* on page 3-59
1007	0xFBC	TRCDEVARCH	RO	0x47704A17	*Device Architecture Register* on page 3-60
1010	0xFC8	TRCDEVID	RO	0x00000000	*Device ID Register* on page 3-61

Table 3-1 ETM-R7 register summary (continued)

Register number	Base offset	Name	Type	Reset value	Description
1011	0xFCC	TRCDEVTYPE	RO	0x00000013	*Device Type Register* on page 3-61
1012-1019	0xFD0-0xFEC	TRCPIDRn	RO	-	*Peripheral Identification Registers* on page 3-62
1020-1023	0xFF0-0xFFC	TRCCIDRn	RO	-	*Component Identification Registers* on page 3-64

3.3.1 Functional grouping of registers

This section shows the macrocell registers by functional group, as follows:

- *General control and ID registers*.
- *Trace filtering control registers* on page 3-9.
- *Derived resource registers* on page 3-9.
- *Implementation-specific and identification registers* on page 3-10.
- *Resource selection registers* on page 3-10.
- *Single-Shot comparator registers* on page 3-10.
- *OS lock and power control registers* on page 3-11.
- *Comparator registers* on page 3-11.
- *Integration Test registers* on page 3-11.
- *CoreSight management registers* on page 3-12.

These functional groups include all of the registers.

General control and ID registers

Table 3-2 shows the general control and ID registers in numerical order.

Table 3-2 General control and ID registers

Register number	Name	Base offset	Description
1	TRCPRGCTLR	0x004	*Programming Control Register* on page 3-13
2	TRCPROCSELR	0x008	*Processor Select Control Register* on page 3-13
3	TRCSTATR	0x00C	*Status Register* on page 3-14
4	TRCCONFIGR	0x010	*Trace Configuration Register* on page 3-15
6	TRCAUXCTLR	0x018	*Auxiliary Control Register* on page 3-16
8	TRCEVENTCTL0R	0x020	*Event Control 0 Register* on page 3-17
9	TRCEVENTCTL1R	0x024	*Event Control 1 Register* on page 3-18
11	TRCSTALLCTLR	0x02C	*Stall Control Register* on page 3-19
12	TRCTSCTLR	0x030	*Global Timestamp Control Register* on page 3-20
13	TRCSYNCPR	0x034	*Synchronization Period Register* on page 3-21

Table 3-2 General control and ID registers (continued)

Register number	Name	Base offset	Description
14	TRCCCCTLR	0x038	*Cycle Count Control Register* on page 3-22
15	TRCBBCTLR	0x03C	*Branch Broadcast Control Register* on page 3-22
16	TRCTRACEIDR	0x040	*Trace ID Register* on page 3-23

Trace filtering control registers

Table 3-3 shows the trace filtering control registers in numerical order.

Table 3-3 Trace filtering control registers

Register number	Name	Base offset	Description
32	TRCVICTLR	0x080	*ViewInst Main Control Register* on page 3-24
33	TRCVIIECTLR	0x084	*ViewInst Include/Exclude Control Register* on page 3-25
34	TRCVISSCTLR	0x088	*ViewInst Start/Stop Control Register* on page 3-25
40	TRCVDCTLR	0x0A0	*ViewData Main Control Register* on page 3-26
41	TRCVDSACCTLR	0x0A4	*ViewData Include/Exclude Single Address Comparator Register* on page 3-27
42	TRCVDARCCTLR	0x0A8	*ViewData Include/Exclude Address Range Comparator Register* on page 3-28

Derived resource registers

Table 3-4 shows the derived resource registers in numerical order. These registers control:

- The two counters, and associated events.
- The sequencer, and associated state change events.
- Trigger events.
- EXTOUT (External Output) events.
- Extended External Input selection.

Table 3-4 Derived resource registers

Register number	Name	Base offset	Description
64-66	TRCSEQVRn	0x100-0x108	*Sequencer State Transition Control Registers 0-2* on page 3-29
70	TRCSEQRSTEVR	0x118	*Sequencer Reset Control Register* on page 3-29
71	TRCSEQSTR	0x11C	*Sequencer State Register* on page 3-30
72	TRCEXTINSELR	0x120	*External Input Select Register* on page 3-31
80-81	TRCCNTRLDVRn	0x140-0x144	*Counter Reload Value Registers 0-1* on page 3-32
84	TRCCNTCTLR0	0x150	*Counter Control Register 0* on page 3-32
85	TRCCNTCTLR1	0x154	*Counter Control Register 1* on page 3-33
88-89	TRCCNTVRn	0x160-0x164	*Counter Value Registers 0-1* on page 3-34

Implementation-specific and identification registers

Table 3-5 shows the implementation-specific and identification registers in numerical order.

Table 3-5 Implementation-specific and identification registers

Register number	Name	Base offset	Description
96	TRCIDR8	0x180	*ID Register 8-13* on page 3-35
97	TRCIDR9	0x184	
98	TRCIDR10	0x188	
99	TRCIDR11	0x18C	
100	TRCIDR12	0x190	
101	TRCIDR13	0x194	
112	TRCIMSPEC0	0x1C0	*Implementation Specific Register 0* on page 3-37
120	TRCIDR0	0x1E0	*ID Register 0* on page 3-38
121	TRCIDR1	0x1E4	*ID Register 1* on page 3-39
122	TRCIDR2	0x1E8	*ID Register 2* on page 3-40
123	TRCIDR3	0x1EC	*ID Register 3* on page 3-41
124	TRCIDR4	0x1F0	*ID Register 4* on page 3-42
125	TRCIDR5	0x1F4	*ID Register 5* on page 3-43

Resource selection registers

Table 3-6 shows the resource selection registers in numerical order.

Table 3-6 Resource selection registers

Register number	Name	Base offset	Description
130-140	TRCRSCTLRn	0x208-0x240	*Resource Selection Registers 2-16* on page 3-44

Single-Shot comparator registers

Table 3-7 shows the Single-Shot comparator registers in numerical order.

Table 3-7 Single-Shot Comparator registers

Register number	Name	Base offset	Description
160-161	TRCSSCCRn	0x280-0x284	*Single-Shot Comparator Control Registers 0-1* on page 3-45
168-169	TRCSSCSRn	0x2A0-0x2A4	*Single-Shot Comparator Status Registers 0-1* on page 3-46

OS lock and power control registers

Table 3-8 shows the OS lock and power control registers in numerical order.

Table 3-8 OS lock and power control registers

Register number	Name	Base offset	Description
192	TRCOSLAR	0x300	*OS Lock Access Register* on page 3-47
193	TRCOSLSR	0x304	*OS Lock Status Register* on page 3-48
196	TRCPDCR	0x310	*Power Down Control Register* on page 3-49
197	TRCPDSR	0x314	*Power Down Status Register* on page 3-49

Comparator registers

Table 3-9 shows the comparator registers in numerical order.

Table 3-9 Comparator registers

Register number	Name	Base offset	Description
256-271	TRCACVRn	0x400-0x43C	*Address Comparator Value Registers 0-7* on page 3-50
288-303	TRCACATRn	0x480-0x4BC	*Address Comparator Access Type Registers 0-7* on page 3-51
320-321	TRCDVCVRn	0x500-0x504	*Data Value Comparator Value Registers 0-1* on page 3-53
352-359	TRCDVCMRn	0x580-0x59C	*Data Value Comparator Mask Registers 0-1* on page 3-53
384	TRCCIDCVR0	0x600	*Context ID Comparator Value Register 0* on page 3-54

Integration Test registers

Table 3-10 shows the Integration Test registers in numerical order.

Table 3-10 Integration Test registers

Register number	Name	Base offset	Description
951	Integration Miscellaneous Outputs Register	0xEDC	*Integration Miscellaneous Outputs Register* on page 3-66
952	Integration Miscellaneous Inputs Register	0xEE0	*Integration Miscellaneous Inputs Register* on page 3-67
953	Integration ATB Identification Register	0xEE4	*Integration ATB Identification Register* on page 3-68
954	Integration Data ATB Data Register	0xEE8	*Integration Data ATB Data Register* on page 3-69
955	Integration Instruction ATB Data Register	0xEEC	*Integration Instruction ATB Data Register* on page 3-69
956	Integration Data ATB In Register	0xEF0	*Integration Data ATB In Register* on page 3-70
957	Integration Instruction ATB In Register	0xEF4	*Integration Instruction ATB In Register* on page 3-71
958	Integration Data ATB Out Register	0xEF8	*Integration Data ATB Out Register* on page 3-71
959	Integration Instruction ATB Out Register	0xEFC	*Integration Instruction ATB Out Register* on page 3-72

CoreSight management registers

Table 3-11 shows the CoreSight management registers in numerical order.

Table 3-11 CoreSight management registers

Register number	Name	Base offset	Description
960	TRCITCTRL	0xF00	*Integration Mode Control Register* on page 3-55
1000	TRCCLAIMSET	0xFA0	*Claim Tag Set Register* on page 3-56
1001	TRCCLAIMCLR	0xFA4	*Claim Tag Clear Register* on page 3-56
1002	TRCDEVAFF0	0xFA8	*Device Affinity Register* on page 3-57
1004	TRCLAR	0xFB0	*Software Lock Access Register* on page 3-58
1005	TRCLSR	0xFB4	*Software Lock Status Register* on page 3-58
1006	TRCAUTHSTATUS	0xFB8	*Authentication Status Register* on page 3-59
1007	TRCDEVARCH	0xFBC	*Device Architecture Register* on page 3-60
1010	TRCDEVID	0xFC8	*Device ID Register* on page 3-61
1011	TRCDEVTYPE	0xFCC	*Device Type Register* on page 3-61
1012-1019	TRCPIDRn	0xFD0-0xFEC	*Peripheral Identification Registers* on page 3-62
1020-1023	TRCCIDRn	0xFF0-0xFFC	*Component Identification Registers* on page 3-64

3.4 Register descriptions

This section describes ETM-R7 registers.

3.4.1 Programming Control Register

The TRCPRGCTLR characteristics are:

Purpose Enables the ETM-R7.

Usage constraints See *Controlling ETM programming* on page 3-3.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-2 shows the TRCPRGCTLR bit assignments.

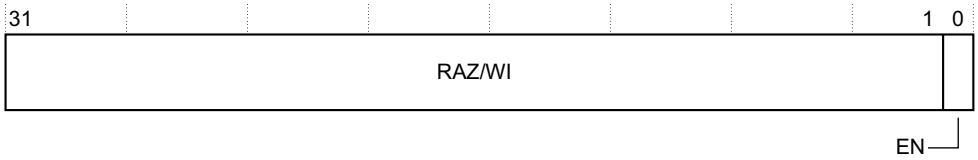

Figure 3-2 TRCPRGCTLR bit assignments

Table 3-12 shows the TRCPRGCTLR bit assignments.

Table 3-12 TRCPRGCTLR bit assignments

Bits	Name	Function
[31:1]	-	RAZ/WI
[0]	EN	Trace program enable: `0` The external pin **ETMIFEN** is LOW, and clocks are only enabled when necessary to process APB accesses, or drain any already generated trace. Writes to most registers are ignored. This is the reset value. `1` The external pin **ETMIFEN** is HIGH, and clocks are enabled except for when the **CPUACTIVE** input is deasserted and all trace has been drained.

3.4.2 Processor Select Control Register

The TRCPROCSELR characteristics are:

Purpose Controls a multiplexer to select trace information from the connected Cortex-R7 processors.

Usage constraints See the *Embedded Trace Macrocell Architecture Specification ETMv4*.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-3 on page 3-14 shows the TRCPROCSELR bit assignments.

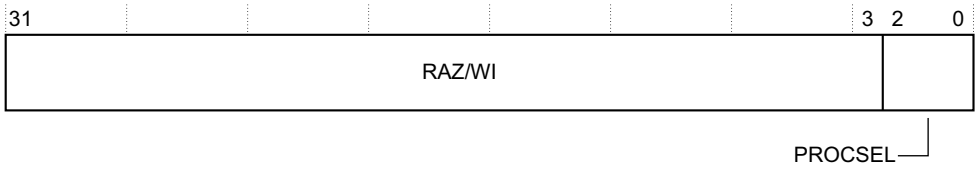

Figure 3-3 TRCPROCSELR bit assignments

Table 3-13 shows the TRCPROCSELR bit assignments.

Table 3-13 TRCPROCSELR bit assignments

Bits	Name	Function
[31:3]	-	RAZ/WI
[2:0]	PROCSEL	Drives the **PROCSEL[2:0]** pin

3.4.3 Status Register

The TRCSTATR characteristics are:

Purpose Indicates the ETM-R7 status.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-4 shows the TRCSTATR bit assignments.

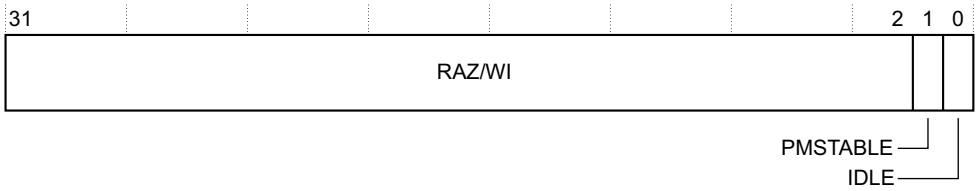

Figure 3-4 TRCSTATR bit assignments

Table 3-14 shows the TRCSTATR bit assignments.

Table 3-14 TRCSTATR bit assignments

Bits	Name	Function
[31:2]	-	RAZ/WI
[1]	PMSTABLE	Indicates whether the ETM-R7 registers are stable and can be read: 0 The programmers model is not stable. 1 The programmers model is stable.
[0]	IDLE	Idle status: 0 The ETM-R7 is not idle. 1 The ETM-R7 is idle.

3.4.4 Trace Configuration Register

The TRCCONFIGR characteristics are:

Purpose Sets the basic tracing options for the trace unit.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-5 shows the TRCCONFIGR bit assignments.

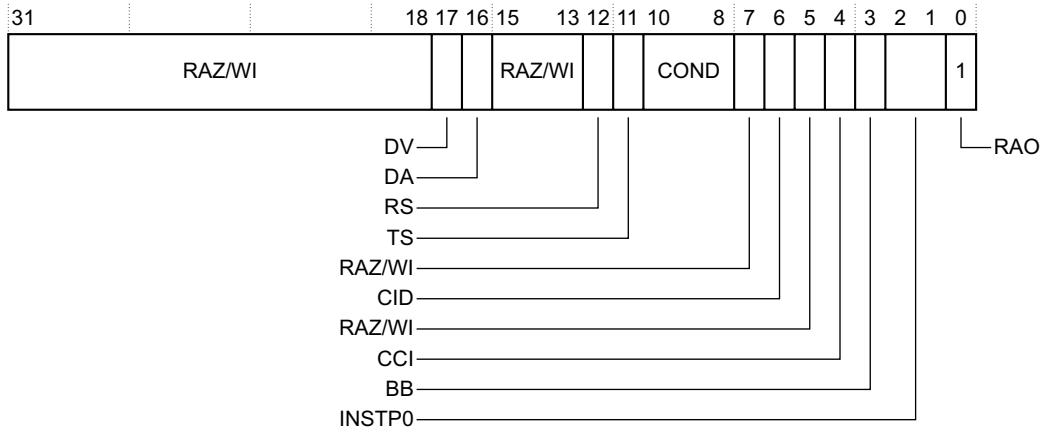

Figure 3-5 TRCCONFIGR bit assignments

Table 3-15 shows the TRCCONFIGR bit assignments.

Table 3-15 TRCCONFIGR bit assignments

Bits	Name	Function
[31:18]	-	RAZ/WI
[17]	DV	Data value tracing: 0 Data value tracing disabled. 1 Data value tracing enabled.
[16]	DA	Data address tracing: 0 Data address tracing disabled. 1 Data address tracing enabled.
[15:13]	-	RAZ/WI
[12]	RS	Return stack enable: 0 Return stack disabled. 1 Return stack enabled.
[11]	TS	Global timestamp tracing: 0 Global timestamp tracing disabled. 1 Global timestamp tracing enabled. For more global timestamping options, see *Global Timestamp Control Register* on page 3-20.

Table 3-15 TRCCONFIGR bit assignments (continued)

Bits	Name	Function
[10:8]	COND	Conditional instruction tracing: `b000` Conditional instruction tracing disabled. `b001` Conditional load instructions are traced. `b010` Conditional store instructions are traced. `b011` Conditional load and store instructions are traced. `b111` All conditional instructions are traced. All other values are Reserved.
[7]	-	RAZ/WI
[6]	CID	Context ID tracing: `0` Context ID tracing disabled. `1` Context ID tracing enabled.
[5]	-	RAZ/WI
[4]	CCI	Cycle counting in instruction trace: `0` Cycle counting in instruction trace disabled. `1` Cycle counting in instruction trace. For more cycle counting options, see *Cycle Count Control Register* on page 3-22.
[3]	BB	Branch broadcast mode: `0` Branch broadcast mode disabled. `1` Branch broadcast mode trace. For more branch broadcast mode options, see *Branch Broadcast Control Register* on page 3-22.
[2:1]	INSTP0	Determines the instructions which are P0 instructions: `b00` Only branches are P0 instructions. `b01` Load instructions and branches are P0 instructions. `b10` Store instructions and branches are P0 instructions. `b11` Load and store instructions and branches are P0 instructions.
[0]	-	RAO

3.4.5 Auxiliary Control Register

The TRCAUXCTLR characteristics are:

Purpose Provides additional controls for the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-6 on page 3-17 shows the TRCAUXCTLR bit assignments.

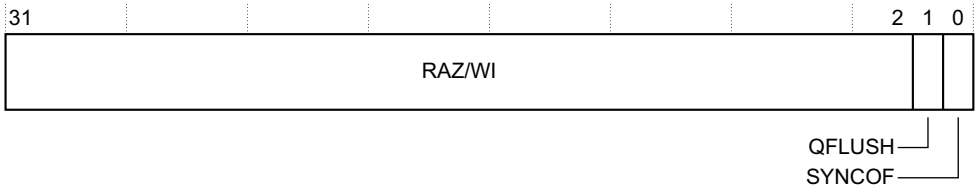

Figure 3-6 TRCAUXCTLR bit assignments

Table 3-16 shows the TRCAUXCTLR bit assignments.

Table 3-16 TRCAUXCTLR bit assignments

Bits	Name	Function
[31:2]	-	RAZ/WI
[1]	QFLUSH	Always respond immediately to AFREADY. No interaction with FIFO draining, even in WFI state.
[0]	SYNCOF	Force an overflow if synchronization is not completed when second synchronization is due.

3.4.6 Event Control 0 Register

The TRCEVENTCTL0R characteristics are:

Purpose Controls the tracing of events in the trace stream. The events also drive the external outputs from the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-7 shows the TRCEVENTCTL0R bit assignments.

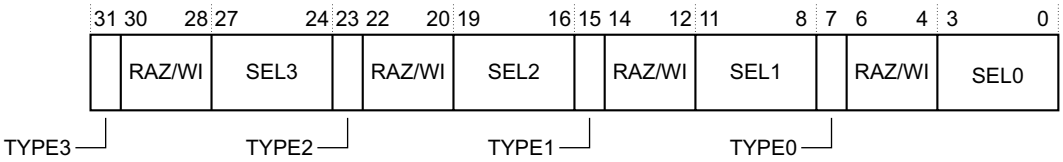

Figure 3-7 TRCEVENTCTL0R bit assignments

Table 3-17 shows the TRCEVENTCTL0R bit assignments.

Table 3-17 TRCEVENTCTL0R bit assignments

Bits	Name	Function
[31]	TYPE3	Selects the resource type for event 3: 0 Single selected resource. 1 Boolean combined resource pair.
[30:28]	-	RAZ/WI
[27:24]	SEL3	Selects the resource number, based on the value of TYPE3: When TYPE3 is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE3 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

Table 3-17 TRCEVENTCTL0R bit assignments (continued)

Bits	Name	Function
[23]	TYPE2	Selects the resource type for event 2: 0 Single selected resource. 1 Boolean combined resource pair.
[22:20]	-	RAZ/WI
[19:16]	SEL2	Selects the resource number, based on the value of TYPE2: When TYPE2 is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE2 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
[15]	TYPE1	Selects the resource type for event 1: 0 Single selected resource. 1 Boolean combined resource pair.
[14:12]	-	RAZ/WI
[11:8]	SEL1	Selects the resource number, based on the value of TYPE1: When TYPE1 is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE1 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
[7]	TYPE0	Selects the resource type for event 0: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	SEL0	Selects the resource number, based on the value of TYPE0: When TYPE0 is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE0 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.7 Event Control 1 Register

The TRCEVENTCTL1R characteristics are:

Purpose Controls the how the events selected by TRCEVENTCTL0R behave. See *Event Control 0 Register* on page 3-17.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-8 shows the TRCEVENTCTL1R bit assignments.

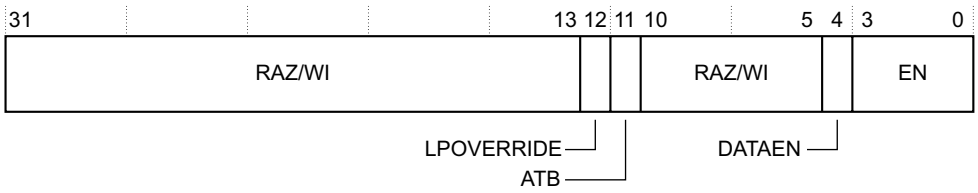

Figure 3-8 TRCEVENTCTL1R bit assignments

Table 3-18 shows the TRCEVENTCTL1R bit assignments.

Table 3-18 TRCEVENTCTL1R bit assignments

Bits	Name	Function
[31:13]	-	RAZ/WI
[12]	LPOVERRIDE	Low power state behavior override: 0 Low power state behavior unaffected. 1 Low power state behavior overridden. The resources and Event trace generation are unaffected by entry to a low power state.
[11]	ATB	ATB trigger enable: 0 ATB trigger disabled. 1 ATB trigger enabled.
[10:5]	-	RAZ/WI
[4]	DATAEN	Enables generation of an event element in the data trace stream when the selected event occurs: 0 Event does not cause an event element. 1 Event causes an event element.
[3:0]	EN	One bit per event, to enable generation of an event element in the instruction trace stream when the selected event occurs: 0 Event does not cause an event element. 1 Event causes an event element.

3.4.8 Stall Control Register

The TRCSTALLCTLR characteristics are:

Purpose Enables the ETM-R7 to stall the Cortex-R7 MPCore processor if the ETM-R7 FIFO overflows.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-9 shows the TRCSTALLCTLR bit assignments.

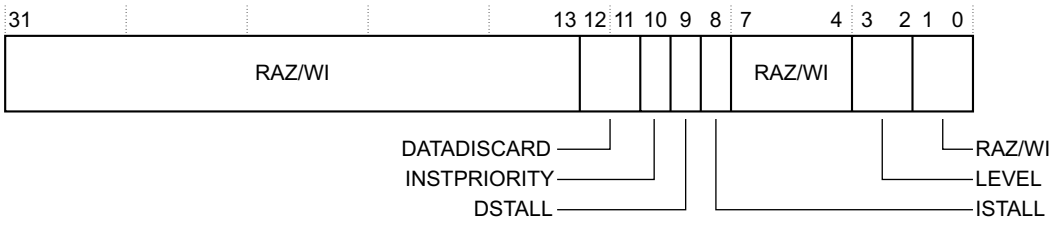

Figure 3-9 TRCSTALLCTLR bit assignments

Table 3-19 shows the TRCSTALLCTLR bit assignments.

Table 3-19 TRCSTALLCTLR bit assignments

Bits	Name	Function
[31:13]	-	RAZ/WI
[12:11]	DATADISCARD	Sets the priority of data trace components, enabling the ETM-R7 to discard some data if the data trace buffer space is less than LEVEL: `b00` Discard no data. `b01` Discard loaded data transfers. `b10` Discard stored data transfers. `b11` Discard both loaded and stored data transfers.
[10]	INSTPRIORITY	Prioritize instruction trace if instruction trace buffer space is less than LEVEL: `0` Do not prioritize instruction trace. `1` Prioritize instruction trace.
[9]	DSTALL	Stall processor based on data trace buffer space: `0` Do not stall processor. `1` Stall processor if data trace buffer space is less than LEVEL.
[8]	ISTALL	Stall processor based on instruction trace buffer space: `0` Do not stall processor. `1` Stall processor if instruction trace buffer space is less than LEVEL.
[7:4]	-	RAZ/WI
[3:2]	LEVEL	Threshold at which stalling becomes active. This provides four levels. This level can be varied to optimize the level of invasion caused by stalling, balanced against the risk of a FIFO overflow: `b00` Lowest level, where zero invasion occurs. `b11` Highest level, where the most invasion occurs to reduce the risk of overflow.
[1:0]	-	RAZ/WI

3.4.9 Global Timestamp Control Register

The TRCTSCTLR characteristics are:

Purpose Controls the insertion of global timestamps into the trace streams. A timestamp is always inserted into the instruction trace stream, and also in the data trace stream if any data tracing is enabled.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-10 shows the TRCTSCTLR bit assignments.

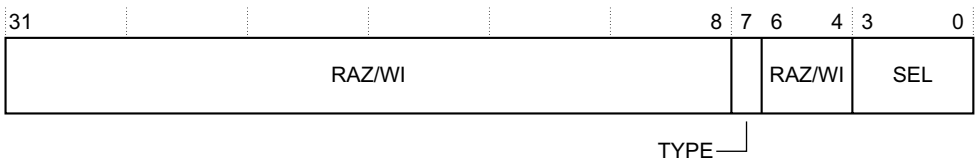

Figure 3-10 TRCTSCTLR bit assignments

Table 3-20 shows the TRCTSCTLR bit assignments.

Table 3-20 TRCTSCTLR bit assignments

Bits	Name	Function
[31:8]	-	RAZ/WI
[7]	TYPE	Selects the resource type: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	SEL	Selects the resource number, based on the value of TYPE: When TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.10 Synchronization Period Register

The TRCSYNCPR characteristics are:

Purpose Specifies the period of synchronization of the trace streams. TRCSYNCPR defines a number of bytes of trace between requests for synchronization. This value is always a power of two.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-11 shows the TRCSYNCPR bit assignments.

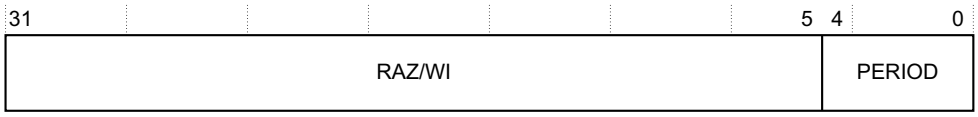

Figure 3-11 TRCSYNCPR bit assignments

Table 3-21 shows the TRCSYNCPR bit assignments.

Table 3-21 TRCSYNCPR bit assignments

Bits	Name	Function
[31:5]	-	RAZ/WI
[4:0]	PERIOD	Defines the number of bytes of trace between synchronization requests as a total of the number of bytes generated by both the instruction and data streams. The number of bytes is 2^N where N is the value of this field: • A value of zero disables these periodic synchronization requests, but does not disable other synchronization requests. • The minimum value that can be programmed, other than zero, is 8, providing a minimum synchronization period of 256 bytes. • The maximum value is 20, providing a maximum synchronization period of 2^{20} bytes.

3.4.11 Cycle Count Control Register

The TRCCCCTLR characteristics are:

Purpose Sets the threshold value for cycle counting.

Usage constraints Writing a value of all zeroes is UNPREDICTABLE when instruction trace cycle counting is enabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-12 shows the TRCCCCTLR bit assignments.

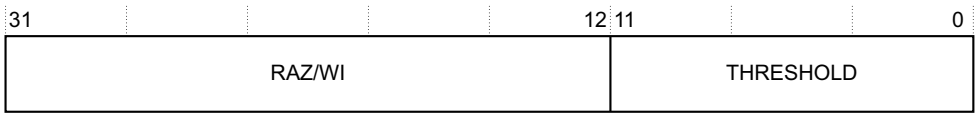

Figure 3-12 TRCCCCTLR bit assignments

Table 3-22 shows the TRCCCCTLR bit assignments.

Table 3-22 TRCCCCTLR bit assignments

Bits	Name	Function
[31:12]	-	RAZ/WI
[11:0]	THRESHOLD	Instruction trace cycle count threshold.

3.4.12 Branch Broadcast Control Register

The TRCBBCTLR characteristics are:

Purpose Controls how branch broadcasting behaves, and enables branch broadcasting to be enabled for certain memory regions.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-13 shows the TRCBBCTLR bit assignments.

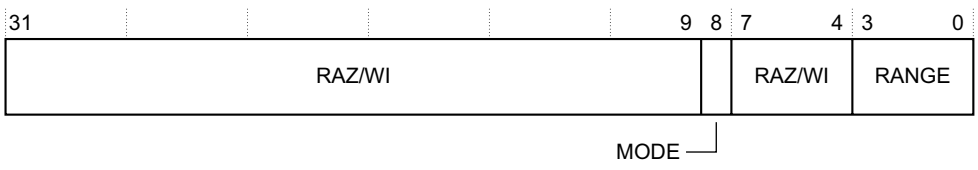

Figure 3-13 TRCBBCTLR bit assignments

Table 3-23 shows the TRCBBCTLR bit assignments.

Table 3-23 TRCBBCTLR bit assignments

Bits	Name	Function
[31:9]	-	RAZ/WI
[8]	MODE	Selects mode: `0` Exclude mode. The Address Range Comparators defined by the RANGE field indicate address ranges where branch broadcasting is not enabled. Selecting no ranges results in branch broadcasting being enabled over the whole memory map. `1` Include mode. The Address Range Comparators defined by the RANGE field indicate address ranges where branch broadcasting is enabled. Setting RANGE to all zeroes is UNPREDICTABLE when in Include mode.
[7:4]	-	RAZ/WI
[3:0]	RANGE	Selects Address Range Comparators to control where branch broadcasting is enabled. One bit is provided for each implemented Address Range Comparator.

3.4.13 Trace ID Register

The TRCTRACEIDR characteristics are:

Purpose Sets the trace ID on the trace bus. Controls two trace IDs, one for instruction trace and one for data trace.

Usage constraints In a CoreSight system, writing of reserved trace ID values, `0x00` and `0x70-0x7F`, is UNPREDICTABLE.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-2 on page 3-8.

Figure 3-14 shows the TRCTRACEIDR bit assignments.

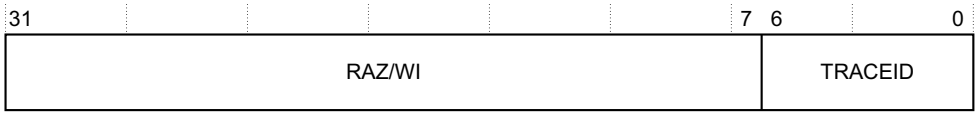

Figure 3-14 TRCTRACEIDR bit assignments

Table 3-24 shows the TRCTRACEIDR bit assignments.

Table 3-24 TRCTRACEIDR bit assignments

Bits	Name	Function
[31:7]	-	RAZ/WI
[6:0]	TRACEID	Trace ID value. When only instruction tracing is enabled, this provides the trace ID. When data tracing is enabled, this field must be written with bit[0] set to 0. The instruction and data trace streams use adjacent trace ID values: • The instruction trace stream uses the trace ID {[6:1],0}. • The data value trace stream uses the trace ID {[6:1],1}. When data tracing is not enabled, bit[0] can be set to any value.

3.4.14 ViewInst Main Control Register

The TRCVICTLR characteristics are:

Purpose Controls instruction trace filtering.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-9.

Figure 3-15 shows the TRCVICTLR bit assignments.

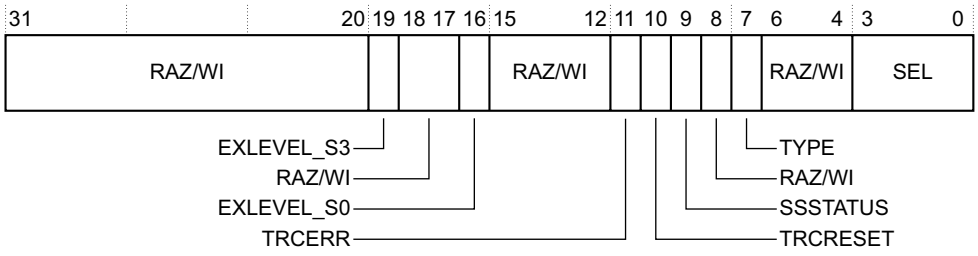

Figure 3-15 TRCVICTLR bit assignments

Table 3-25 shows the TRCVICTLR bit assignments.

Table 3-25 TRCVICTLR bit assignments

Bits	Value	Function
[31:20]	-	RAZ/WI
[19]	EXLEVEL_S3	Disables tracing in the specified exception level in Secure state for exception level 3. 0 Enable ViewInst in this exception level. 1 Disable ViewInst in this exception level.
[18:17]	-	RAZ/WI
[16]	EXLEVEL_S0	Disables tracing in the specified exception level in Secure state for exception level 0. 0 Enable ViewInst in this exception level. 1 Disable ViewInst in this exception level.
[15:12]	-	RAZ/WI
[11]	TRCERR	Selects whether a system error exception must always be traced: 0 System error exception is traced only if the instruction or exception immediately before the system error exception is traced. 1 System error exception is always traced regardless of the value of ViewInst.
[10]	TRCRESET	Selects whether a reset exception must always be traced: 0 Reset exception is traced only if the instruction or exception immediately before the reset exception is traced. 1 Reset exception is always traced regardless of the value of ViewInst.
[9]	SSSTATUS	Indicates the current status of the start/stop logic: 0 Start/stop logic is in the stopped state. 1 Start/stop logic is in the started state.
[8]	-	RAZ/WI

Table 3-25 TRCVICTLR bit assignments (continued)

Bits	Value	Function
[7]	TYPE	Selects the resource type: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	SEL	Selects the resource number, based on the value of TYPE: When TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.15 ViewInst Include/Exclude Control Register

The TRCVIIECTLR characteristics are:

Purpose Defines the address range comparators that control the ViewInst Include/Exclude control.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-9.

Figure 3-16 shows the TRCVIIECTLR bit assignments.

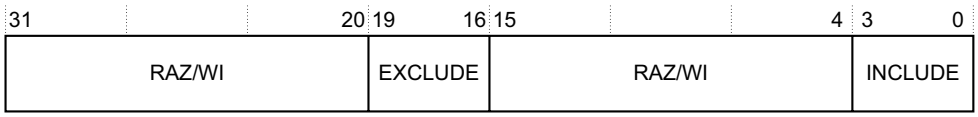

Figure 3-16 TRCVIIECTLR bit assignments

Table 3-26 shows the TRCVIIECTLR bit assignments.

Table 3-26 TRCVIIECTLR bit assignments

Bits	Name	Function
[31:20]	-	RAZ/WI
[19:16]	EXCLUDE	Defines the address range comparators for ViewInst exclude control. One bit is provided for each implemented Address Range Comparator.
[15:4]	-	RAZ/WI
[3:0]	INCLUDE	Defines the address range comparators for ViewInst include control. Selecting no include comparators indicates that all instructions must be included. The exclude control indicates which ranges must be excluded. One bit is provided for each implemented Address Range Comparator.

3.4.16 ViewInst Start/Stop Control Register

The TRCVISSCTLR characteristics are:

Purpose Defines the single address comparators that control the ViewInst Start/Stop logic.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-9.

Figure 3-17 shows the TRCVISSCTLR bit assignments.

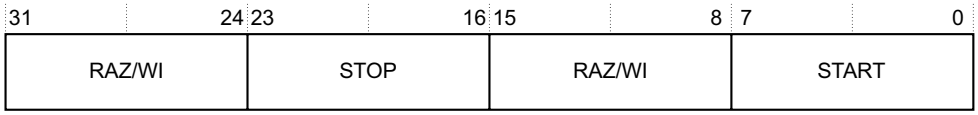

Figure 3-17 TRCVISSCTLR bit assignments

Table 3-27 shows the TRCVISSCTLR bit assignments.

Table 3-27 TRCVISSCTLR bit assignments

Bits	Name	Function
[31:24]	-	RAZ/WI
[23:16]	STOP	Defines the single address comparators to stop trace with the ViewInst Start/Stop control. One bit is provided for each implemented single address comparator.
[15:8]	-	RAZ/WI
[7:0]	START	Defines the single address comparators to start trace with the ViewInst Start/Stop control. One bit is provided for each implemented single address comparator.

3.4.17 ViewData Main Control Register

The TRCVDCTLR characteristics are:

Purpose Controls data trace filtering.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-9.

Figure 3-18 shows the TRCVDCTLR bit assignments.

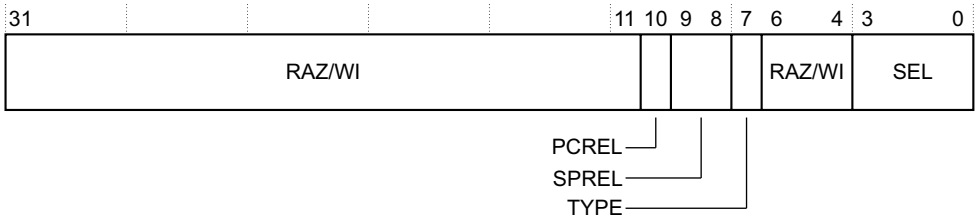

Figure 3-18 TRCVDCTLR bit assignments

Table 3-28 shows the TRCVDCTLR bit assignments.

Table 3-28 TRCVDCTLR bit assignments

Bits	Name	Function
[31:11]	-	RAZ/WI
[10]	PCREL	Controls tracing of data for transfers that are relative to the *Program Counter* (PC): 0 Tracing of PC-relative transfers is unaffected. 1 Do not trace either the address or value portions of PC-relative transfers.
[9:8]	SPREL	Controls tracing of data for transfers that are relative to the *Stack Pointer* (SP): b00 Tracing of SP-relative transfers is unaffected. b01 Reserved. b10 Do not trace the address portion of SP-relative transfers. A P1 data address element is generated if data value tracing is enabled. b11 Do not trace either the address or value portions of SP-relative transfers.
[7]	TYPE	Selects the resource type: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	SEL	Selects the resource number, based on the value of TYPE: When TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.18 ViewData Include/Exclude Single Address Comparator Register

The TRCVDSACCTLR characteristics are:

Purpose Defines the single address comparators that control the ViewData Include/Exclude control.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-9.

Figure 3-19 shows the TRCVDSACCTLR bit assignments.

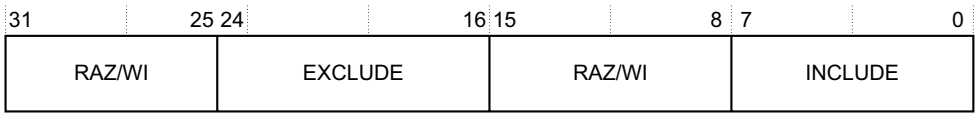

Figure 3-19 TRCVDSACCTLR bit assignments

Table 3-29 shows the TRCVDSACCTLR bit assignments.

Table 3-29 TRCVDSACCTLR bit assignments

Bits	Name	Function
[31:25]	-	RAZ/WI
[24:16]	EXCLUDE	Defines the single address comparators for ViewData exclude control. One bit is provided for each implemented address comparator.
[15:8]	-	RAZ/WI
[7:0]	INCLUDE	Defines the single address comparators for ViewData include control. One bit is provided for each implemented address comparator.

3.4.19 ViewData Include/Exclude Address Range Comparator Register

The TRCVDARCCTLR characteristics are:

Purpose Defines the address range comparators that control the ViewData Include/Exclude control.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-3 on page 3-9.

Figure 3-20 shows the TRCVDARCCTLR bit assignments.

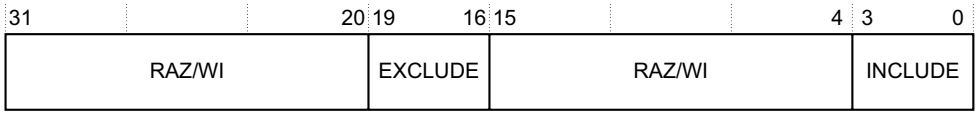

Figure 3-20 TRCVDARCCTLR bit assignments

Table 3-30 shows the TRCVDARCCTLR bit assignments.

Table 3-30 TRCVDARCCTLR bit assignments

Bits	Name	Function
[31:20]	-	RAZ/WI
[19:16]	EXCLUDE	Defines the address range comparators for ViewData exclude control. One bit is provided for each implemented address range comparator.
[15:4]	-	RAZ/WI
[3:0]	INCLUDE	Defines the address range comparators for ViewData include control. One bit is provided for each implemented address range comparator.

3.4.20 Sequencer State Transition Control Registers 0-2

The TRCSEQEVRn characteristics are:

Purpose Defines the sequencer transitions that progress to the next state or backwards to the previous state. The ETM-R7 implements a sequencer state machine with up to four states.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-21 shows the TRCSEQEVRn bit assignments.

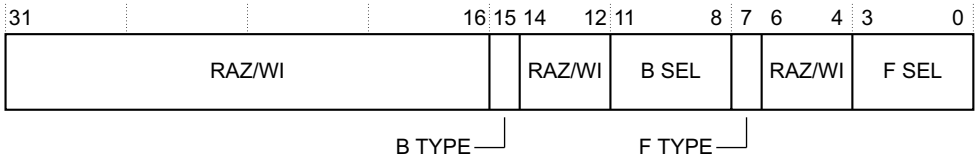

Figure 3-21 TRCSEQEVRn bit assignments

Table 3-31 shows the TRCSEQEVRn bit assignments.

Table 3-31 TRCSEQEVRn bit assignments

Bits	Name	Function
[31:16]	-	RAZ/WI
[15]	B TYPE	Selects the resource type to move backwards to this state from the next state: 0 Single selected resource. 1 Boolean combined resource pair.
[14:12]	-	RAZ/WI
[11:8]	B SEL	Selects the resource number, based on the value of B TYPE: When B TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When B TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
[7]	F TYPE	Selects the resource type to move forwards from this state to the next state: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	F SEL	Selects the resource number, based on the value of F TYPE: When F TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When F TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.21 Sequencer Reset Control Register

The TRCSEQRSTEVR characteristics are:

Purpose Resets the sequencer to state 0.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-22 shows the TRCSEQRSTEVR bit assignments.

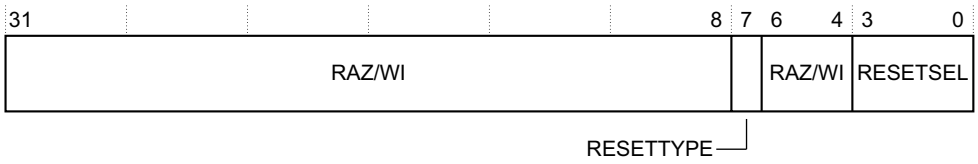

Figure 3-22 TRCSEQRSTEVR bit assignments

Table 3-32 shows the TRCSEQRSTEVR bit assignments.

Table 3-32 TRCSEQRSTEVR bit assignments

Bits	Name	Function
[31:8]	-	RAZ/WI
[7]	RESETTYPE	Selects the resource type to move back to state 0: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	RESETSEL	Selects the resource number, based on the value of RESETTYPE: When RESETTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When RESETTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.22 Sequencer State Register

The TRCSEQSTR characteristics are:

Purpose Holds the value of the current state of the sequencer.

Usage constraints
- Can only be written when the ETM-R7 is disabled.
- Must be programmed with an initial value when programming the sequencer.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-23 shows the TRCSEQSTR bit assignments.

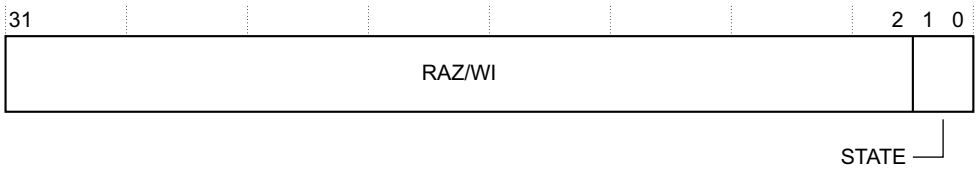

Figure 3-23 TRCSEQSTR bit assignments

Table 3-33 shows the TRCSEQSTR bit assignments.

Table 3-33 TRCSEQSTR bit assignments

Bits	Name	Function
[31:2]	-	RAZ/WI
[1:0]	STATE	Current sequencer state: b00 State 0. b01 State 1. b10 State 2. b11 State 3.

3.4.23 External Input Select Register

The TRCEXTINSELR characteristics are:

Purpose Controls the selectors that choose an external input as a resource in the ETM-R7.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-24 shows the TRCEXTINSELR bit assignments.

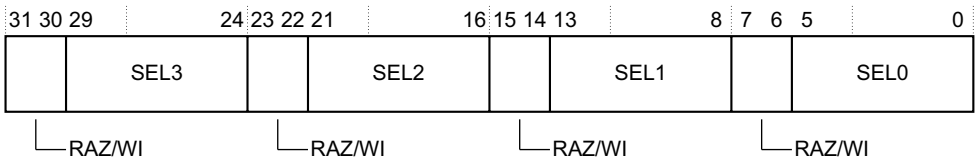

Figure 3-24 TRCEXTINSELR bit assignments

Table 3-34 shows the TRCEXTINSELR bit assignments.

Table 3-34 TRCEXTINSELR bit assignments

Bits	Name	Function
[31:30]	-	RAZ/WI
[29:24]	SEL3	Selects an event from the external input bus for External Input Resource 3.
[23:22]	-	RAZ/WI
[21:16]	SEL2	Selects an event from the external input bus for External Input Resource 2.
[15:14]	-	RAZ/WI
[13:8]	SEL1	Selects an event from the external input bus for External Input Resource 1.
[7:6]	-	RAZ/WI
[5:0]	SEL0	Selects an event from the external input bus for External Input Resource 0.

3.4.24 Counter Reload Value Registers 0-1

The TRCCNTRLDVRn characteristics are:

Purpose Defines the reload value for the counter.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-25 shows the TRCCNTRLDVRn bit assignments.

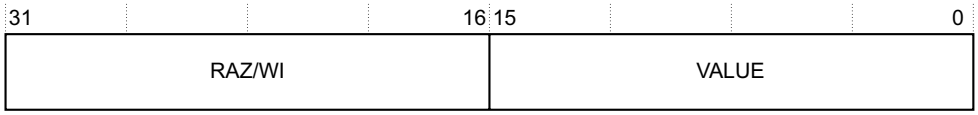

Figure 3-25 TRCCNTRLDVRn bit assignments

Table 3-35 shows the TRCCNTRLDVRn bit assignments.

Table 3-35 TRCCNTRLDVRn bit assignments

Bits	Value	Function
[31:16]	-	RAZ/WI
[15:0]	VALUE	Defines the reload value for the counter. This value is loaded into the counter each time the reload event occurs.

3.4.25 Counter Control Register 0

The TRCCNTCTLR0 characteristics are:

Purpose Controls the counter.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-26 shows the TRCCNTCTLR0 bit assignments.

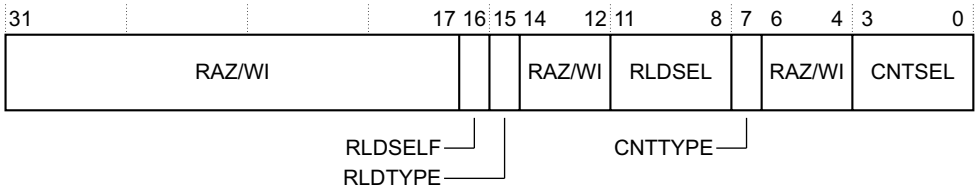

Figure 3-26 TRCCNTCTLR0 bit assignments

Table 3-36 shows the TRCCNTCTLR0 bit assignments.

Table 3-36 TRCCNTCTLR0 bit assignments

Bits	Name	Function
[31:17]	-	RAZ/WI
[16]	RLDSELF	Defines whether the counter reloads when it reaches zero: 0 The counter does not reload when it reaches zero. The counter only reloads based on RLDTYPE and RLDSEL. 1 The counter reloads when it reaches zero and the resource selected by CNTTYPE and CNTSEL is also active. The counter also reloads based on RLDTYPE and RLDSEL.
[15]	RLDTYPE	Selects the resource type for the reload: 0 Single selected resource. 1 Boolean combined resource pair.
[14:12]	-	RAZ/WI
[11:8]	RLDSEL	Selects the resource number, based on the value of RLDTYPE: When RLDTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When RLDTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
[7]	CNTTYPE	Selects the resource type for the counter: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	CNTSEL	Selects the resource number, based on the value of CNTTYPE: When CNTTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When CNTTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.26 Counter Control Register 1

The TRCCNTCTLR1 characteristics are:

Purpose Controls the counter.

Usage constraints Can only be written when the ETM-R7 is disabled.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-27 shows the TRCCNTCTLR1 bit assignments.

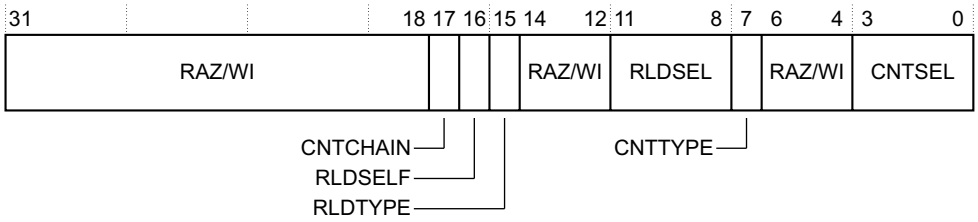

Figure 3-27 TRCCNTCTLR1 bit assignments

Table 3-37 shows the TRCCNTCTLR1 bit assignments.

Table 3-37 TRCCNTCTLR1 bit assignments

Bits	Name	Function
[31:18]	-	RAZ/WI
[17]	CNTCHAIN	Defines whether the counter decrements when the counter reloads. This enables two counters to be used in combination to provide a larger counter: 0 The counter operates independently from the counter. The counter only decrements based on CNTTYPE and CNTSEL. 1 The counter decrements when the counter reloads. The counter also decrements when the resource selected by CNTTYPE and CNTSEL is active.
[16]	RLDSELF	Defines whether the counter reloads when it reaches zero: 0 The counter does not reload when it reaches zero. The counter only reloads based on RLDTYPE and RLDSEL. 1 The counter reloads when it is zero and the resource selected by CNTTYPE and CNTSEL is also active. The counter also reloads based on RLDTYPE and RLDSEL.
[15]	RLDTYPE	Selects the resource type for the reload: 0 Single selected resource. 1 Boolean combined resource pair.
[14:12]	-	RAZ/WI
[11:8]	RLDSEL	Selects the resource number, based on the value of RLDTYPE: When RLDTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When RLDTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
[7]	CNTTYPE	Selects the resource type for the counter: 0 Single selected resource. 1 Boolean combined resource pair.
[6:4]	-	RAZ/WI
[3:0]	CNTSEL	Selects the resource number, based on the value of CNTTYPE: When CNTTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When CNTTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

3.4.27 Counter Value Registers 0-1

The TRCCNTVRn characteristics are:

Purpose Contains the current counter value.

Usage constraints
- Can only be written when the ETM-R7 is disabled.
- Must be programmed with an initial value when programming the counter.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-4 on page 3-9.

Figure 3-28 on page 3-35 shows the TRCCNTVRn bit assignments.

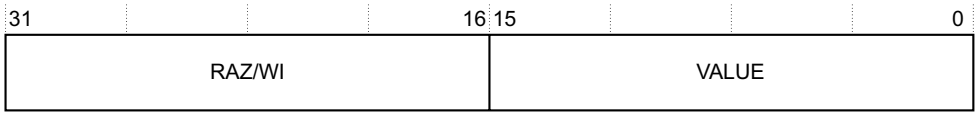

Figure 3-28 TRCCNTVRn bit assignments

Table 3-38 shows the TRCCNTVRn bit assignments.

Table 3-38 TRCCNTVRn bit assignments

Bits	Value	Function
[31:16]	-	RAZ/WI
[15:0]	VALUE	Contains the current counter value.

3.4.28 ID Register 8-13

The TRCIDR8-13 characteristics are:

Purpose Indicate information about the trace stream that is required to analyze the trace.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-29 shows the TRCIDR8 bit assignments.

Figure 3-29 TRCIDR8 bit assignments

Table 3-39 shows the TRCIDR8 bit assignments.

Table 3-39 TRCIDR8 bit assignments

Bits	Name	Function
[31:0]	MAXSPEC	Indicates the maximum speculation depth of the instruction trace stream. This is the maximum number of P0 elements that have not been committed in the trace stream at any one time. This field reads as `0x00000040` (64).

Figure 3-30 shows the TRCIDR9 bit assignments.

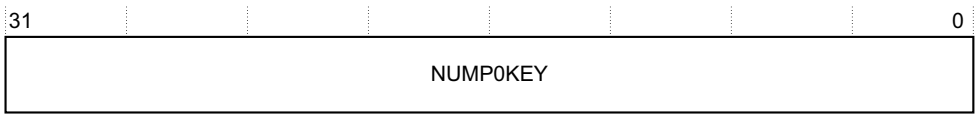

Figure 3-30 TRCIDR9 bit assignments

Table 3-40 shows the TRCIDR9 bit assignments.

Table 3-40 TRCIDR9 bit assignments

Bits	Name	Function
[31:0]	NUMP0KEY	Indicates the number of P0 right-hand keys that are used. This field reads as `0x00000040` (64).

Figure 3-31 shows the TRCIDR10 bit assignments.

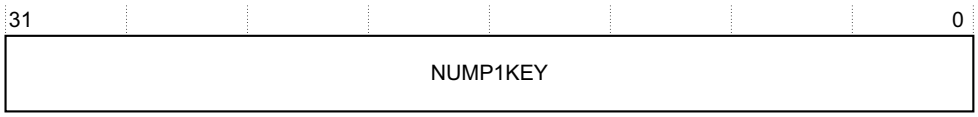

Figure 3-31 TRCIDR10 bit assignments

Table 3-41 shows the TRCIDR10 bit assignments.

Table 3-41 TRCIDR10 bit assignments

Bits	Name	Function
[31:0]	NUMP1KEY	Indicates the total number of P1 right-hand keys, including normal and special keys. This field reads as `0x00000040` (64 keys).

Figure 3-32 shows the TRCIDR11 bit assignments.

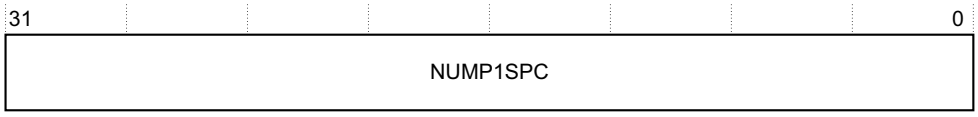

Figure 3-32 TRCIDR11 bit assignments

Table 3-42 shows the TRCIDR11 bit assignments.

Table 3-42 TRCIDR11 bit assignments

Bits	Name	Function
[31:0]	NUMP1SPC	Indicates the number of special P1 right-hand keys. This field reads as `0x00000011` (17 keys).

Figure 3-33 shows the TRCIDR12 bit assignments.

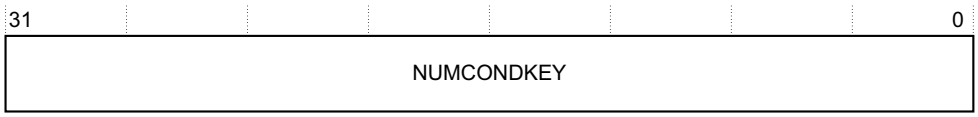

Figure 3-33 TRCIDR12 bit assignments

Table 3-43 shows the TRCIDR12 bit assignments.

Table 3-43 TRCIDR12 bit assignments

Bits	Name	Function
[31:0]	NUMCONDKEY	Indicates the total number of conditional instruction right-hand keys, including normal and special keys. This field reads as `0x00000020` (32).

Figure 3-34 shows the TRCIDR13 bit assignments.

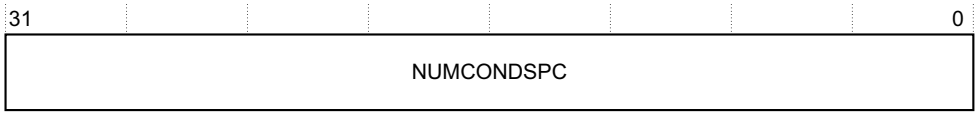

Figure 3-34 TRCIDR13 bit assignments

Table 3-44 shows the TRCIDR13 bit assignments.

Table 3-44 TRCIDR13 bit assignments

Bits	Name	Function
[31:0]	NUMCONDSPC	This indicates the number of special conditional instruction right-hand keys. There are no special conditional keys, so this field reads as 0.

3.4.29 Implementation Specific Register 0

The TRCIMSPEC0 characteristics are:

Purpose Shows the presence of any IMPLEMENTATION SPECIFIC features, and enables any features that are provided.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-35 shows the TRCIMSPEC0 bit assignments.

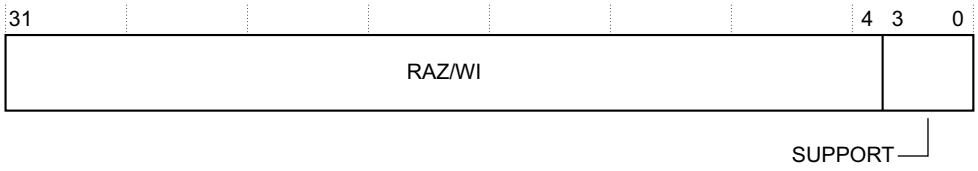

Figure 3-35 TRCIMSPEC0 bit assignments

Table 3-45 shows the TRCIMSPEC0 bit assignments.

Table 3-45 TRCIMSPEC0 bit assignments

Bits	Name	Function
[31:4]	-	RAZ/WI
[3:0]	SUPPORT	Set to 0. No IMPLEMENTATION SPECIFIC extensions are supported.

3.4.30 ID Register 0

The TRCIDR0 characteristics are:

Purpose Indicates the tracing capabilities of the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-36 shows the TRCIDR0 bit assignments.

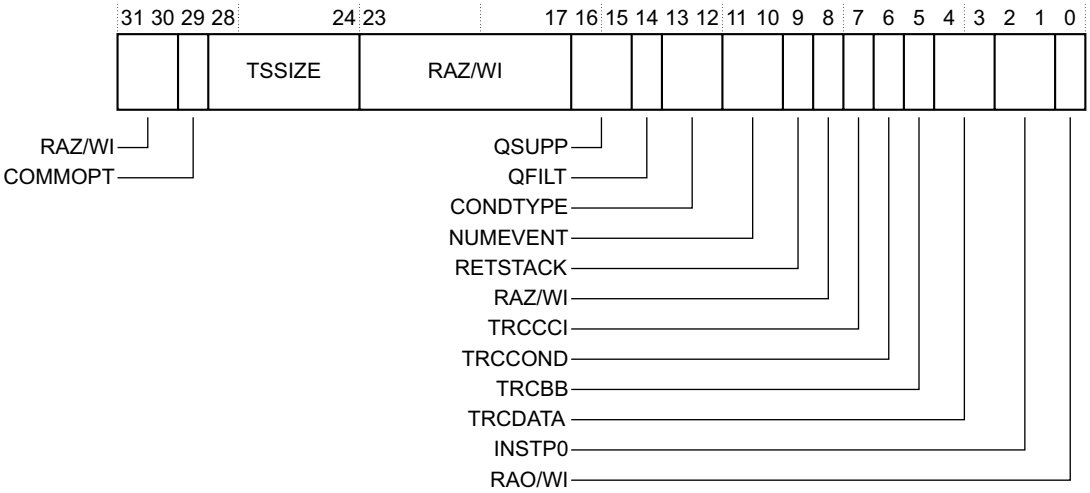

Figure 3-36 TRCIDR0 bit assignments

Table 3-46 shows the TRCIDR0 bit assignments.

Table 3-46 TRCIDR0 bit assignments

Bits	Name	Function
[31:30]	-	RAZ/WI
[29]	COMMOPT	Indicates the meaning of the commit field in some packets: `b0` Commit mode 0.
[28:24]	TSSIZE	Global timestamp size. Driven from external **TSSIZE** pin: `b00110` Maximum of 48-bit global timestamp implemented. **TSSIZE** is LOW. `b01000` Maximum of 64-bit global timestamp implemented. **TSSIZE** is HIGH. Other values are Reserved.
[23:17]	-	RAZ/WI
[16:15]	QSUPP	Indicates Q element support: `b00` Q elements not supported.
[14]	QFILT	Indicates Q element filtering support: `b0` Q element filtering not supported.
[13:12]	CONDTYPE	Indicates how conditional results are traced: `b01` Full CPSR traced.

Table 3-46 TRCIDR0 bit assignments (continued)

Bits	Name	Function
[11:10]	NUMEVENT	Number of events supported in the trace, minus 1: b11 Four events supported.
[9]	RETSTACK	Return stack support: 1 Return stack implemented.
[8]	-	RAZ/WI
[7]	TRCCCI	Support for cycle counting in the instruction trace: 1 Cycle counting in the instruction trace is implemented.
[6]	TRCCOND	Support for conditional instruction tracing: 1 Conditional instruction tracing is implemented.
[5]	TRCBB	Support for branch broadcast tracing: 1 Branch broadcast tracing is implemented.
[4:3]	TRCDATA	Support for tracing of data: b11 Tracing of data addresses and data values is implemented.
[2:1]	INSTP0	Support for tracing of load and store instructions as P0 elements: b11 Tracing of load and store instructions as P0 elements is implemented.
[0]	-	RAO/WI

3.4.31 ID Register 1

The TRCIDR1 characteristics are:

Purpose Indicates the basic architecture of the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-37 shows the TRCIDR1 bit assignments.

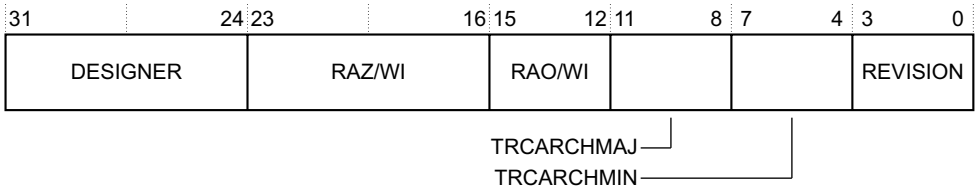

Figure 3-37 TRCIDR1 bit assignments

Table 3-47 shows the TRCIDR1 bit assignments.

Table 3-47 TRCIDR1 bit assignments

Bits	Name	Function
[31:24]	DESIGNER	Indicates the designer of the trace unit: 0x41 ASCII code for A, indicating ARM.
[23:16]	-	RAZ/WI
[15:12]	-	RAO/WI
[11:8]	TRCARCHMAJ	Major trace unit architecture version number: b0100 ETMv4.
[7:4]	TRCARCHMIN	Minor trace unit architecture version number: b0000 Minor revision 0.
[3:0]	REVISION	Implementation revision number: b0001 Implementation revision 1.

3.4.32 ID Register 2

The TRCIDR2 characteristics are:

Purpose Indicates the maximum sizes of certain aspects of items in the trace.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-38 shows the TRCIDR2 bit assignments.

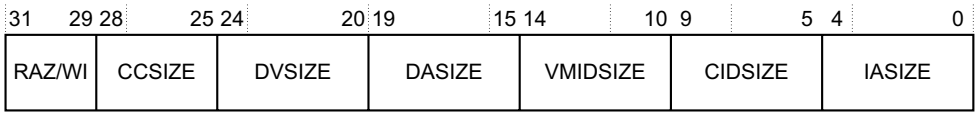

Figure 3-38 TRCIDR2 bit assignments

Table 3-48 shows the TRCIDR2 bit assignments.

Table 3-48 TRCIDR2 bit assignments

Bits	Name	Function
[31:29]	-	RAZ/WI
[28:25]	CCSIZE	Indicates the size of the cycle counter in bits minus 12: b0000 Cycle count is 12 bits.
[24:20]	DVSIZE	Data value size in bytes: b00100 Maximum of 32-bit data value size.
[19:15]	DASIZE	Data address size in bytes: b00100 Maximum of 32-bit address size.

Table 3-48 TRCIDR2 bit assignments (continued)

Bits	Name	Function
[14:10]	VMIDSIZE	Virtual Machine ID size: b00000 Virtual Machine ID tracing not implemented.
[9:5]	CIDSIZE	Context ID size in bytes: b00100 Maximum of 32-bit Context ID size.
[4:0]	IASIZE	Instruction address size in bytes: b00100 Maximum of 32-bit address size.

3.4.33 ID Register 3

The TRCIDR3 characteristics are:

Purpose Indicates certain aspects of the ETM-R7 configuration.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-39 shows the TRCIDR3 bit assignments.

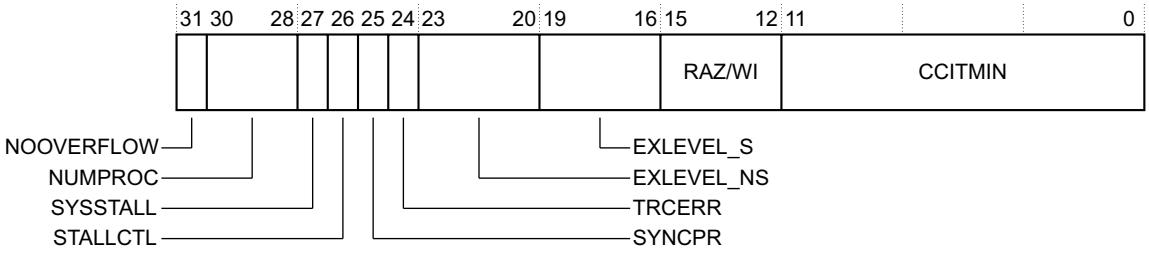

Figure 3-39 TRCIDR3 bit assignments

Table 3-49 shows the TRCIDR3 bit assignments.

Table 3-49 TRCIDR3 bit assignments

Bits	Name	Function
[31]	NOOVERFLOW	Indicates whether TRCSTALLCTLR.NOOVERFLOW is implemented: 0 NOOVERFLOW is not implemented.
[30:28]	NUMPROC	Number of processors available for tracing minus 1, indicating 1-8 processors. This describes the largest valid value which can be written to TRCPROCSELR.
[27]	SYSSTALL	System support for stall control of the processor. This is driven from the ETM **SYSSTALL** input pin, reflecting the system implementation: 0 System does not support stall control of the processor. 1 System supports stall control of the processor. This field is used in conjunction with STALLCTL. Only when both SYSSTALL and STALLCTL are b1 does the system support stalling of the processor.

Table 3-49 TRCIDR3 bit assignments (continued)

Bits	Name	Function
[26]	STALLCTL	Stall control support: 1 TRCSTALLCTLR is implemented. This field is used in conjunction with SYSSTALL.
[25]	SYNCPR	Synchronization period support: 0 TRCSYNCPR is read-write.
[24]	TRCERR	Indicates whether TRCVICTLR.TRCERR is implemented: 1 TRCERR is implemented.
[23:20]	EXLEVEL_NS	Exception levels implemented in Non-Secure state. One bit for each exception level 0-3. b0000 No Non-Secure exception levels are implemented.
[19:16]	EXLEVEL_S	Exception levels implemented in Secure state. One bit for each exception level 0-3. b1001 Secure exception levels EL0 and EL3 are implemented.
[15:12]	-	RAZ/WI
[11:0]	CCITMIN	Instruction trace cycle counting minimum threshold: 0x4 Minimum threshold is 4.

3.4.34 ID Register 4

The TRCIDR4 characteristics are:

Purpose Indicates the resources available in the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-40 shows the TRCIDR4 bit assignments.

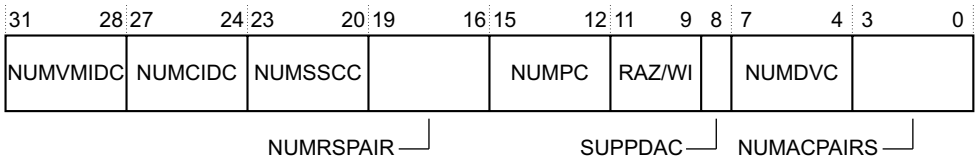

Figure 3-40 TRCIDR4 bit assignments

Table 3-50 shows the TRCIDR4 bit assignments.

Table 3-50 TRCIDR4 bit assignments

Bits	Name	Function
[31:28]	NUMVMIDC	Number of *Virtual Machine ID* (VMID) comparators implemented: `b0000` VMID comparators are not implemented.
[27:24]	NUMCIDC	Number of Context ID comparators implemented: `b0001` One Context ID comparator is implemented.
[23:20]	NUMSSCC	Number of Single-Shot comparator controls implemented: `b0010` Two Single-Shot comparator controls are implemented.
[19:16]	NUMRSPAIR	Number of resource selection pairs implemented: `b0111` Eight resource selection pairs are implemented. The first is not counted.
[15:12]	NUMPC	Number of processor comparator inputs implemented: `b0000` Processor comparator inputs are not implemented.
[11:9]	-	RAZ/WI
[8]	SUPPDAC	Data address comparisons implemented: 1 Data address comparisons are supported.
[7:4]	NUMDVC	Number of data value comparators implemented: `b0010` Two data value comparators are implemented.
[3:0]	NUMACPAIRS	Number of address comparator pairs implemented: `b0100` Four address comparator pairs are implemented.

3.4.35 ID Register 5

The TRCIDR5 characteristics are:

Purpose Indicates the resources available in the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-41 shows the TRCIDR5 bit assignments.

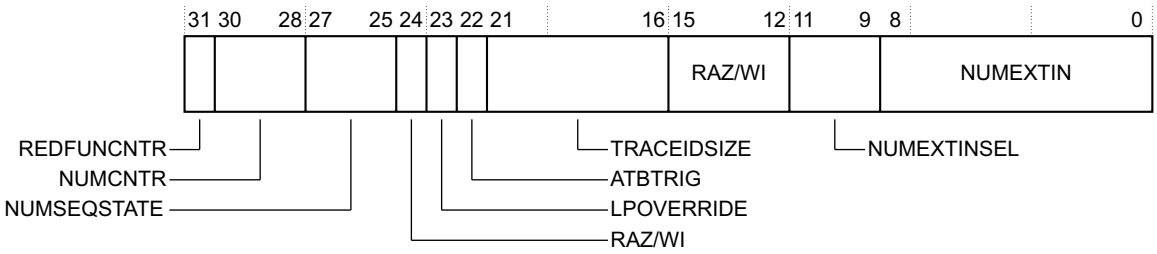

Figure 3-41 TRCIDR5 bit assignments

Table 3-51 shows the TRCIDR5 bit assignments.

Table 3-51 TRCIDR5 bit assignments

Bits	Name	Function
[31]	REDFUNCNTR	Reduced Function Counter implemented: 0 Reduced Function Counter not implemented.
[30:28]	NUMCNTR	Number of counters implemented: b010 Two counters implemented.
[27:25]	NUMSEQSTATE	Number of sequencer states implemented: b100 Four sequencer states implemented.
[24]	-	RAZ/WI
[23]	LPOVERRIDE	Low power state override support: 1 Low power state override support implemented.
[22]	ATBTRIG	ATB trigger support: 1 ATB trigger support implemented.
[21:16]	TRACEIDSIZE	Number of bits of trace ID: 0x07 Seven-bit trace ID implemented.
[15:12]	-	RAZ/WI
[11:9]	NUMEXTINSEL	Number of external input selectors implemented: b100 Four external input selectors implemented.
[8:0]	NUMEXTIN	Number of external inputs implemented: 0x40 64 external inputs implemented.

3.4.36 Resource Selection Registers 2-16

The TRCRSCTLRn characteristics are:

Purpose Controls the trace resources.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-5 on page 3-10.

Figure 3-42 shows the TRCRSCTLRn bit assignments.

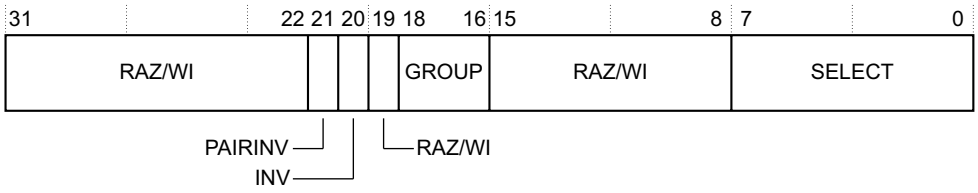

Figure 3-42 TRCRSCTLRn bit assignments

Table 3-52 shows the TRCRSCTLRn bit assignments.

Table 3-52 TRCRSCTLRn bit assignments

Bits	Name	Function
[31:22]	-	RAZ/WI
[21]	PAIRINV	Inverts the result of a combined pair of resources. This bit is only implemented on the lower register for a pair of resource selectors.
[20]	INV	Inverts the selected resources: 0 Resource is not inverted. 1 Resource is inverted.
[19]	-	RAZ/WI
[18:16]	GROUP	Selects a group of resources.
[15:8]	-	RAZ/WI
[7:0]	SELECT	Selects one or more resources from the desired group. One bit is provided per resource from the group.

3.4.37 Single-Shot Comparator Control Registers 0-1

The TRCSSCCRn characteristics are:

Purpose Controls the single-shot comparators.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-7 on page 3-10.

Figure 3-43 shows the TRCSSCCRn bit assignments.

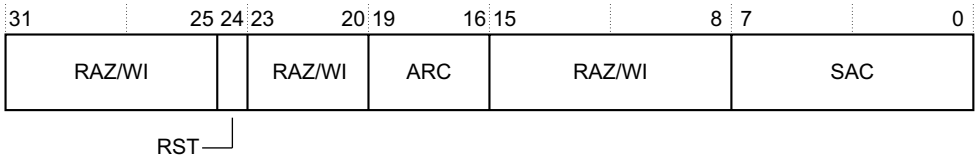

Figure 3-43 TRCSSCCRn bit assignments

Table 3-53 shows the TRCSSCCRn bit assignments.

Table 3-53 TRCSSCCRn bit assignments

Bits	Name	Function
[31:25]	-	RAZ/WI
[24]	RST	Enables the single-shot comparator resource to be reset when it occurs, to enable another comparator match to be detected: 1 Reset enabled. Multiple matches can occur.
[23:20]	-	RAZ/WI

Table 3-53 TRCSSCCRn bit assignments (continued)

Bits	Name	Function
[19:16]	ARC	Selects one or more address range comparators for single-shot control. One bit is provided for each implemented address range comparator.
[15:8]	-	RAZ/WI
[7:0]	SAC	Selects one or more single address comparators for single-shot control. One bit is provided for each implemented single address comparator.

3.4.38 Single-Shot Comparator Status Registers 0-1

The TRCSSCSRn characteristics are:

Purpose Indicates the status of the single-shot comparators:
- TRCSSCSR0 is sensitive to instruction addresses.
- TRCSSCSR1 is sensitive to data addresses and values.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-7 on page 3-10.

Figure 3-44 shows the TRCSSCSRn bit assignments.

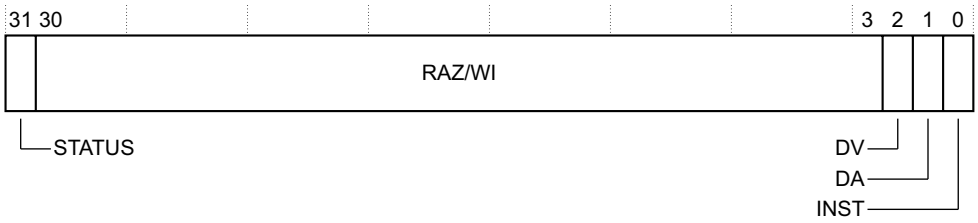

Figure 3-44 TRCSSCSRn bit assignments

Table 3-54 shows the TRCSSCSR0 bit assignments.

Table 3-54 TRCSSCSR0 bit assignments

Bits	Name	Function
[31]	STATUS	Single-shot status. This indicates whether any of the selected comparators have matched: 0 Match has not occurred. 1 Match has occurred at least once. When programming the ETM-R7, if TRCSSCCRn.RST is b0, the STATUS bit must be explicitly written to 0 to enable this single-shot comparator control.
[30:3}	-	RAZ/WI

Table 3-54 TRCSSCSR0 bit assignments (continued)

Bits	Name	Function
[2]	DV	Data value comparator support: 0 Single-shot data value comparisons not supported.
[1]	DA	Data address comparator support: 0 Single-shot data address comparisons not supported.
[0]	INST	Instruction address comparator support: 1 Single-shot instruction address comparisons supported.

Table 3-55 shows the TRCSSCSR1 bit assignments.

Table 3-55 TRCSSCSR1 bit assignments

Bits	Name	Function
[31]	STATUS	Single-shot status. This indicates whether any of the selected comparators have matched: 0 Match has not occurred. 1 Match has occurred at least once. When programming the ETM-R7, this bit must be explicitly written to 0 to enable this single-shot comparator control.
[30:3}	-	RAZ/WI
[2]	DV	Data value comparator support: 1 Single-shot data value comparisons supported.
[1]	DA	Data address comparator support: 1 Single-shot data address comparisons supported.
[0]	INST	Instruction address comparator support: 0 Single-shot instruction address comparisons not supported.

3.4.39 OS Lock Access Register

The TRCOSLAR characteristics are:

Purpose Sets and clears the OS Lock, to lock out external debugger accesses to the ETM-R7 registers.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-11.

Figure 3-45 shows the TRCOSLAR bit assignments.

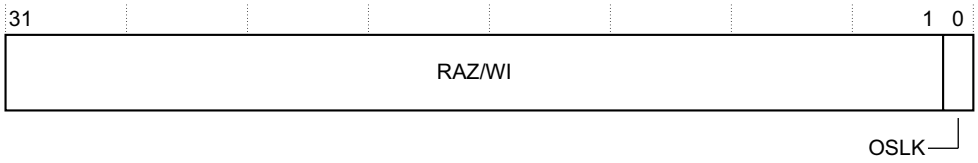

Figure 3-45 TRCOSLAR bit assignments

Table 3-56 shows the TRCOSLAR bit assignments.

Table 3-56 TRCOSLAR bit assignments

Bits	Name	Function
[31:1]	-	RAZ/WI
[0]	OSLK	OS Lock key value: 0 Unlock the OS Lock. 1 Lock the OS Lock.

3.4.40 OS Lock Status Register

The TRCOSLSR characteristics are:

Purpose Returns the status of the OS Lock.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-11.

Figure 3-45 on page 3-47 shows the TRCOSLSR bit assignments.

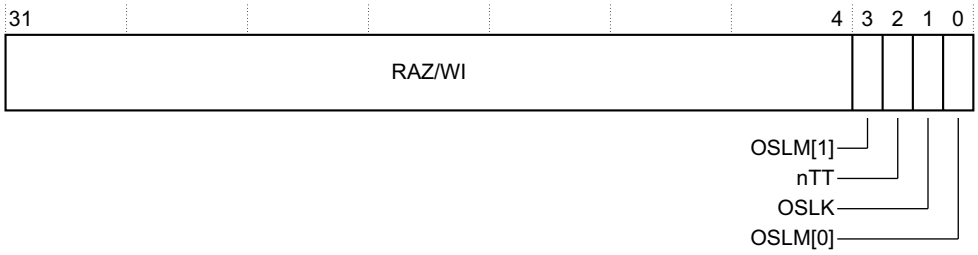

Figure 3-46 TRCOSLSR bit assignments

Table 3-56 shows the TRCOSLSR bit assignments.

Table 3-57 TRCOSLSR bit assignments

Bits	Name	Function
[31:4]	-	RAZ/WI
[3]	OSLM[1]	OS Lock model [1] bit. This bit is combined with OSLM[0] to form a two-bit field that indicates the OS Lock model is implemented. The value of this field is always 0b10, indicating that the OS Lock is implemented.
[2]	nTT	This bit is RAZ, which indicates that software must perform a 32-bit write to update the TRCOSLAR.
[1]	OSLK	OS Lock status bit: 0 OS Lock is unlocked. 1 OS Lock is locked.
[0]	OSLM[0]	OS Lock model [0] bit. This bit is combined with OSLM[1] to form a two-bit field that indicates the OS Lock model is implemented. The value of this field is always 0b10, indicating that the OS Lock is implemented.

3.4.41 Power Down Control Register

The TRCPDCR characteristics are:

Purpose Request to the system power controller to keep the ETM-R7 powered up.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-11.

Figure 3-47 shows the TRCPDCR bit assignments.

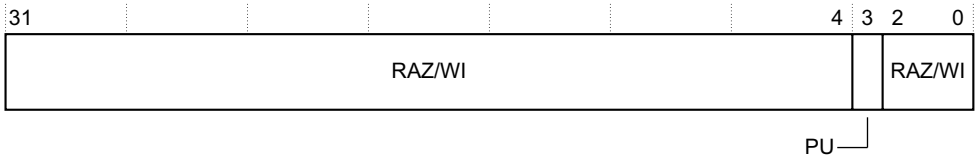

Figure 3-47 TRCPDCR bit assignments

Table 3-58 shows the TRCPDCR bit assignments.

Table 3-58 TRCPDCR bit assignments

Bits	Name	Function
[31:4]	-	RAZ/WI
[3]	PU	Power up request, to request that power to the ETM-R7 and access to the trace registers is maintained: 0 Power not requested. 1 Power requested. This bit is reset to 0 on a trace unit reset.
[2:0]	-	RAZ/WI

3.4.42 Power Down Status Register

The TRCPDSR characteristics are:

Purpose Indicates the power down status of the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-8 on page 3-11.

Figure 3-48 on page 3-50 shows the TRCPDSR bit assignments.

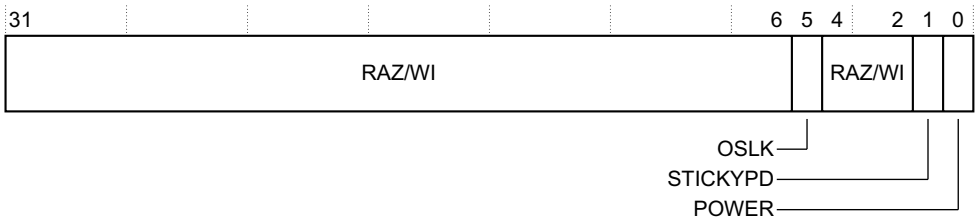

Figure 3-48 TRCPDSR bit assignments

Table 3-59 shows the TRCPDSR bit assignments.

Table 3-59 TRCPDSR bit assignments

Bits	Name	Function
[31:6]	-	RAZ/WI
[5]	OSLK	OS lock status.
[4:2]	-	RAZ/WI
[1]	STICKYPD	Sticky power down state. `0` Trace register power has not been removed since the TRCPDSR was last read. `1` Trace register power has been removed since the TRCPDSR was last read. This bit is set to 1 when power to the ETM-R7 registers is removed, to indicate that programming state has been lost. It is cleared after a read of the TRCPDSR.
[0]	POWER	Indicates the ETM-R7 is powered: `1` ETM-R7 is powered. All registers are accessible. If a system implementation allows the ETM to be powered off independently of the debug power domain, the system must handle accesses to the ETM appropriately.

3.4.43 Address Comparator Value Registers 0-7

The TRCACVRn characteristics are:

Purpose Indicates the address for the data address comparators.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-11.

Figure 3-49 shows the TRCACVRn bit assignments.

Figure 3-49 TRCACVRn bit assignments

Table 3-60 shows the TRCACVRn bit assignments.

Table 3-60 TRCACVRn bit assignments

Bits	Name	Function
[31:0]	ADDRESS	The address value to compare against.

3.4.44 Address Comparator Access Type Registers 0-7

The TRCACATRn characteristics are:

Purpose Controls the access for the data address comparators.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-11.

Figure 3-50 shows the TRCACATR0 bit assignments.

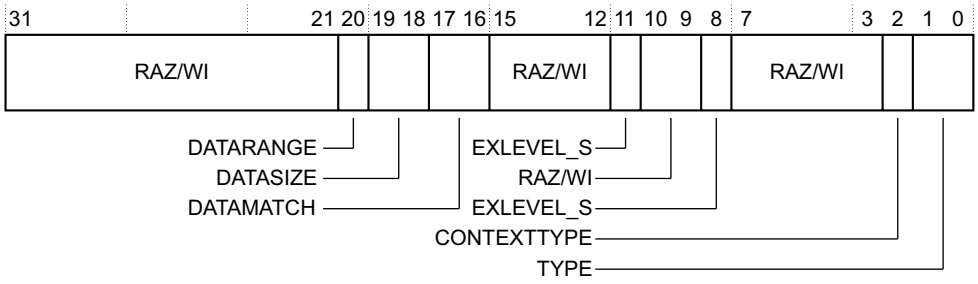

Figure 3-50 TRCACATR0 bit assignments

Table 3-61 shows the TRCACATR0 bit assignments.

Table 3-61 TRCACATR0 bit assignments

Bits	Name	Function
[31:21]	-	RAZ/WI
[20]	DATARANGE	Data value comparison range control, to select whether the data value comparison is made against the single address comparator or the address range comparator: `0` Only the single address comparator matches. `1` Only the address range comparator matches.
[19:18]	DATASIZE	Data value comparison size control: `b00` Byte size. `b01` Halfword size. `b10` Word size. `b11` Doubleword size.
[17:16]	DATAMATCH	Data value comparison control: `b01` Comparator matches only if the data value comparison matches. `b11` Comparator matches only if the data value comparison does not match.
[15:12]	-	RAZ/WI

Table 3-61 TRCACATR0 bit assignments (continued)

Bits	Name	Function
[11]	EXLEVEL_S	Indicates whether the comparator matches in exception level 3 in Secure state: 1 The comparator must not match in this exception level.
[10:9]	-	RAZ/WI
[8]	EXLEVEL_S	Indicates whether the comparator matches in exception level 0 in Secure state: 1 The comparator must not match in this exception level.
[7:3]	-	RAZ/WI
[2]	CONTEXTTYPE	Indicates whether the context comparator is used in the comparison: 0 Use no context comparators. 1 Use the Context ID comparator.
[1:0]	TYPE	The type of comparison: b00 Instruction address. b01 Data load address. b10 Data store address. b11 Data load or store address.

Note

TRCACATR2 is functionally identical to TRCACATR0.

Figure 3-50 on page 3-51 shows the TRCACATR1 bit assignments.

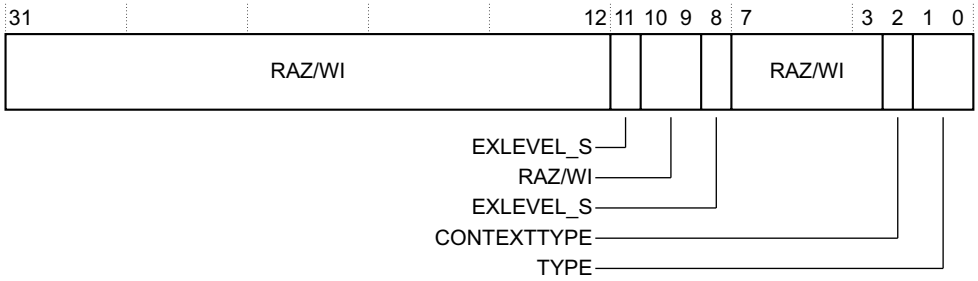

Figure 3-51 TRCACATR1 bit assignments

Table 3-61 on page 3-51 shows the TRCACATR1 bit assignments.

Table 3-62 TRCACATR1 bit assignments

Bits	Name	Function
[31:12]	-	RAZ/WI
[11]	EXLEVEL_S	Indicates whether the comparator matches in exception level 3 in Secure state: 1 The comparator must not match in this exception level.
[10:9]	-	RAZ/WI
[8]	EXLEVEL_S	Indicates whether the comparator matches in exception level 0 in Secure state: 1 The comparator must not match in this exception level.

Table 3-62 TRCACATR1 bit assignments (continued)

Bits	Name	Function
[7:3]	-	RAZ/WI
[2]	CONTEXTTYPE	Indicates whether the context comparator is used in the comparison: 0 Use no context comparators. 1 Use the Context ID comparator.
[1:0]	TYPE	The type of comparison: b00 Instruction address. b01 Data load address. b10 Data store address. b11 Data load or store address.

Note

TRCACATR3-7 are functionally identical to TRCACATR1.

3.4.45 Data Value Comparator Value Registers 0-1

The TRCDVCVRn characteristics are:

Purpose Indicates the value for the data value comparators.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-11.

Figure 3-52 shows the TRCDVCVRn bit assignments.

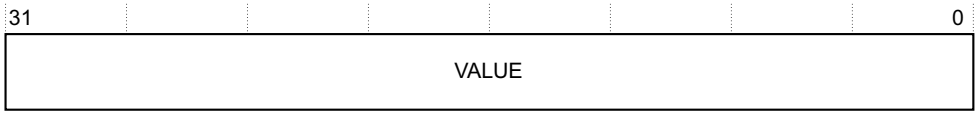

Figure 3-52 TRCDVCVRn bit assignments

Table 3-63 shows the TRCDVCVRn bit assignments.

Table 3-63 TRCDVCVRn bit assignments

Bits	Name	Function
[31:0]	VALUE	The data value to compare against.

3.4.46 Data Value Comparator Mask Registers 0-1

The TRCDVCMRn characteristics are:

Purpose Controls the mask value for the data value comparators.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-11.

Figure 3-53 shows the TRCDVCMRn bit assignments.

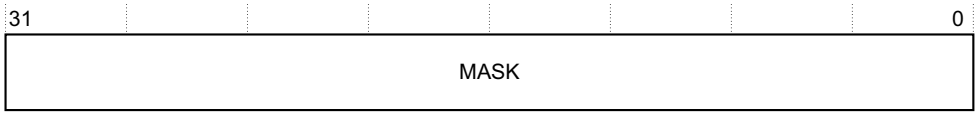

Figure 3-53 TRCDVCMRn bit assignments

Table 3-64 shows the TRCDVCMRn bit assignments.

Table 3-64 TRCDVCMRn bit assignments

Bits	Name	Function
[31:0]	MASK	The mask value to apply to the data value comparison.

3.4.47 Context ID Comparator Value Register 0

The TRCCIDCVR0 characteristics are:

Purpose Indicates the value for the context ID comparators.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-11.

Figure 3-54 shows the TRCCIDCVR0 bit assignments.

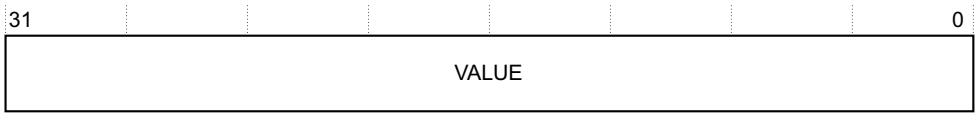

Figure 3-54 TRCCIDCVR0 bit assignments

Table 3-65 shows the TRCCIDCVR0 bit assignments.

Table 3-65 TRCCIDCVR0 bit assignments

Bits	Value	Function
[31:0]	VALUE	The Context ID value to compare with the current Context ID.

3.4.48 Context ID Comparator Control Register 0

The TRCCIDCCTLR0 characteristics are:

Purpose Controls the mask value for the context ID comparators.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-9 on page 3-11.

Figure 3-55 shows the TRCCIDCCTLR0 bit assignments.

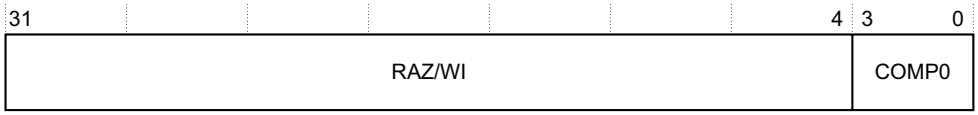

Figure 3-55 TRCCIDCCTLR0 bit assignments

Table 3-66 shows the TRCCIDCCTLR0 bit assignments.

Table 3-66 TRCCIDCCTLR0 bit assignments

Bits	Name	Function
[31:4]	-	RAZ/WI
[3:0]	COMP0	The mask value to apply to the Context ID comparator.

3.4.49 Integration Mode Control Register

The TRCITCTRL characteristics are:

Purpose Enables topology detection or integration testing, by putting the ETM-R7 into integration mode.

Usage constraints ARM recommends that you perform a debug reset after using integration mode.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-56 shows the TRCITCTRL bit assignments.

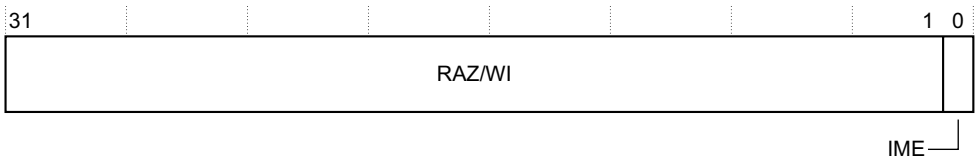

Figure 3-56 TRCITCTRL bit assignments

Table 3-67 shows the TRCITCTRL bit assignments.

Table 3-67 TRCPRGCTLR bit assignments

Bits	Name	Function
[31:1]	-	RAZ/WI
[0]	IME	Integration mode enable: 0 ETM-R7 is not in integration mode. This is the reset value. 1 ETM-R7 is in integration mode.

3.4.50 Claim Tag Set Register

The TRCCLAIMSET characteristics are:

Purpose Sets bits in the claim tag and determines the number of claim tag bits implemented.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-57 shows the TRCCLAIMSET bit assignments.

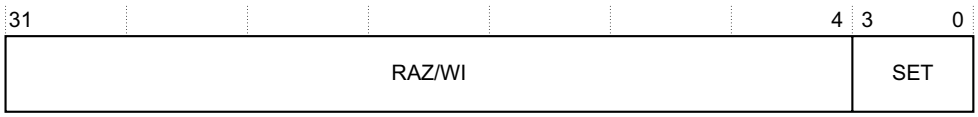

Figure 3-57 TRCCLAIMSET bit assignments

Table 3-68 shows the TRCCLAIMSET bit assignments.

Table 3-68 TRCCLAIMSET bit assignments

Bits	Name	Function
[31:4]	-	RAZ/WI
[3:0]	SET	On reads, for each bit: 0 Claim tag bit is not implemented. 1 Claim tag bit is implemented. On writes, for each bit: 0 Has no effect. 1 Sets the relevant bit of the claim tag.

3.4.51 Claim Tag Clear Register

The TRCCLAIMCLR characteristics are:

Purpose Clears bits in the claim tag and determines the current value of the claim tag.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-58 shows the TRCCLAIMCLR bit assignments.

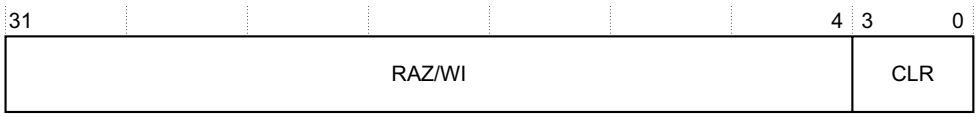

Figure 3-58 TRCCLAIMCLR bit assignments

Table 3-69 shows the TRCCLAIMCLR bit assignments.

Table 3-69 TRCCLAIMCLR bit assignments

Bits	Name	Function
[31:4]	-	RAZ/WI
[3:0]	CLR	On reads, for each bit: 0 Claim tag bit is not set. 1 Claim tag bit is set. On writes, for each bit: 0 Has no effect. 1 Clears the relevant bit of the claim tag.

3.4.52 Device Affinity Register

The TRCDEVAFF0 characteristics are:

Purpose Enables the ETM-R7 to determine which processor in the Cortex-R7 MPCore processor the component relates to.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-59 shows the TRCDEVAFF0 bit assignments.

Figure 3-59 TRCDEVAFF0 bit assignments

Table 3-70 shows the TRCDEVAFF0 bit assignments.

Table 3-70 TRCDEVAFF0 bit assignments

Bits	Name	Function
[31]	-	Indicates the register uses the new multiprocessor format. This is always 1.
[30]	U bit	Multiprocessing Extensions: Set to 0 Processor is part of a multiprocessor cluster.
[29:12]	Reserved	SBZ.
[11:8]	Cluster ID	Value read in **CLUSTERID** configuration pins. It identifies a Cortex-R7 processor in a system with more than one Cortex-R7 processor present.
[7:2]	Reserved	SBZ.
[1:0]	CPU ID	Indicates the processor number in the Cortex-R7 MPCore configuration: 0x0 Processor 0. 0x1 Processor 1.

3.4.53 Software Lock Access Register

The TRCLAR characteristics are:

Purpose Controls access to registers using the memory-mapped interface.

When the software lock is set, write accesses using the memory-mapped interface to all ETM-R7 registers are ignored except for write accesses to the TRCLAR.

When the software lock is set, read accesses of TRCPDSR do not change the TRCPDSR.STICKYPD bit. Read accesses of all other registers are not affected.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-60 shows the TRCLAR bit assignments.

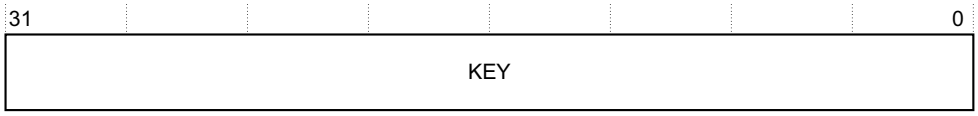

Figure 3-60 TRCLAR bit assignments

Table 3-71 shows the TRCLAR bit assignments.

Table 3-71 TRCLAR bit assignments

Bits	Name	Function
[31:0]	KEY	Software lock key value: 0xC5ACCE55 Clear the software lock. All other write values set the software lock.

3.4.54 Software Lock Status Register

The TRCLSR characteristics are:

Purpose Determines if the software lock is implemented, and indicates the current status of the software lock.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-61 on page 3-59 shows the TRCLSR bit assignments.

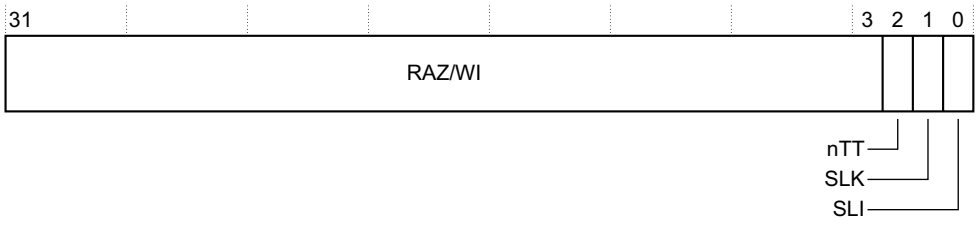

Figure 3-61 TRCLSR bit assignments

Table 3-72 shows the TRCLSR bit assignments.

Table 3-72 TRCLSR bit assignments

Bits	Name	Function
[31:3]	-	RAZ/WI
[2]	nTT	Indicates size of TRCLAR: 0 TRCLAR is always 32 bits.
[1]	SLK	Software lock status: 0 Software lock is clear. 1 Software lock is set.
[0]	SLI	Indicates whether the software lock is implemented on this interface. 1 Software lock is implemented on this interface.

3.4.55 Authentication Status Register

The TRCAUTHSTATUS characteristics are:

Purpose Indicates the current level of tracing permitted by the system.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-62 shows the TRCAUTHSTATUS bit assignments.

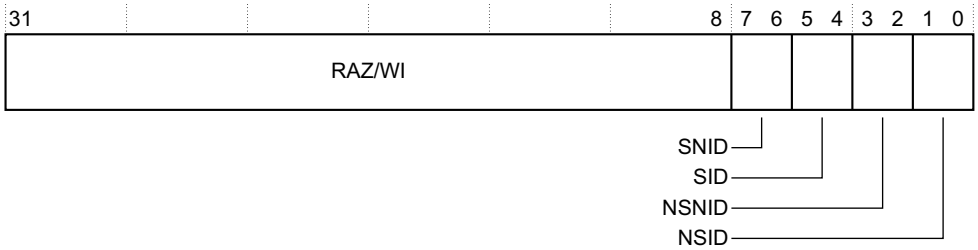

Figure 3-62 TRCAUTHSTATUS bit assignments

Table 3-73 shows the TRCAUTHSTATUS bit assignments.

Table 3-73 TRCAUTHSTATUS bit assignments

Bits	Name	Function
[31:8]	-	RAZ/WI
[7:6]	SNID	Secure Non-Invasive Debug: b10 Secure Non-Invasive Debug implemented but disabled. b11 Secure Non-Invasive Debug implemented and enabled.
[5:4]	SID	Secure Invasive Debug: b10 Secure Invasive Debug implemented but disabled. b11 Secure Invasive Debug implemented and enabled.
[3:2]	NSNID	Non-Secure Non-Invasive Debug: b00 Non-Secure Non-Invasive Debug not implemented.
[1:0]	NSID	Non-Secure Invasive Debug: b00 Non-Secure Invasive Debug not implemented.

3.4.56 Device Architecture Register

The TRCDEVARCH characteristics are:

Purpose Identifies the ETM-R7 as an ETMv4 component.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-64 on page 3-61 shows the TRCDEVARCH bit assignments.

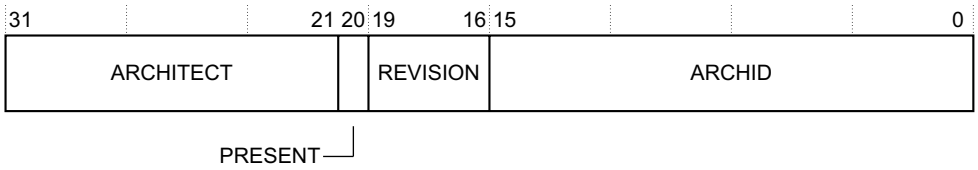

Figure 3-63 TRCDEVARCH bit assignments

Table 3-75 on page 3-61 shows the TRCDEVARCH bit assignments.

Table 3-74 TRCDEVARCH bit assignments

Bits	Name	Function
[31:21]	ARCHITECT	Defines the architect of the component: 0x43B ARM.

Table 3-74 TRCDEVARCH bit assignments (continued)

Bits	Name	Function
[20]	PRESENT	Indicates the presence of this register: `b1` Register is present.
[19:16]	REVISION	Architecture revision: `b0000` Architecture revision 0.
[15:0]	ARCHID	Architecture ID: `0x4A13` ETMv4 component.

3.4.57 Device ID Register

The TRCDEVID characteristics are:

Purpose Indicates the capabilities of the ETM-R7.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-64 shows the TRCDEVID bit assignments.

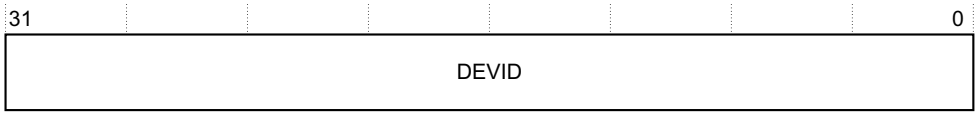

Figure 3-64 TRCDEVID bit assignments

Table 3-75 shows the TRCDEVID bit assignments.

Table 3-75 TRCDEVID bit assignments

Bits	Name	Function
[31:0]	DEVID	RAZ. There are no component-defined capabilities.

3.4.58 Device Type Register

The TRCDEVTYPE characteristics are:

Purpose Indicates the type of the component.

Usage constraints There are no usage constraints.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-65 on page 3-62 shows the TRCDEVTYPE bit assignments.

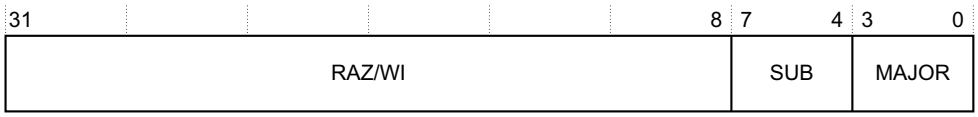

Figure 3-65 TRCDEVTYPE bit assignments

Table 3-76 shows the TRCDEVTYPE bit assignments.

Table 3-76 TRCDEVTYPE bit assignments

Bits	Name	Function
[31:8]	-	RAZ/WI
[7:4]	SUB	The sub-type of the component: `b0001` Processor trace.
[3:0]	MAJOR	The main type of the component: `b0011` Trace source.

3.4.59 Peripheral Identification Registers

The TRCPIDR0-7 characteristics are:

Purpose Provides the standard Peripheral ID required by all CoreSight components. See the *Embedded Trace Macrocell Architecture Specification ETMv4* for more information

Usage constraints Only bits[7:0] of each register are used. This means that TRCPIDR0-7 define a single 64-bit *Peripheral ID*, as Figure 3-66 shows.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-66 shows the mapping between TRCPIDR0-7 and the single 64-bit *Peripheral ID* value.

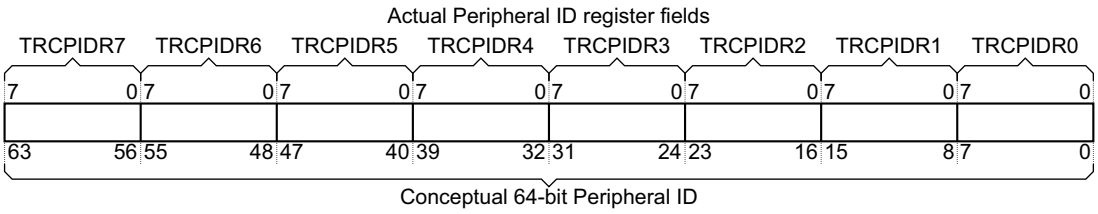

Figure 3-66 Mapping between TRCPIDR0-7 and the Peripheral ID value

Figure 3-67 on page 3-63 shows the Peripheral ID bit assignments in the single conceptual Peripheral ID register.

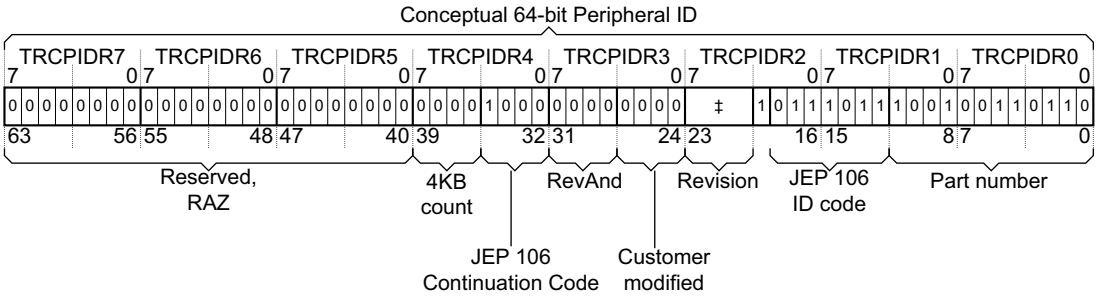

Figure 3-67 Peripheral ID fields

Table 3-77 shows the values of the fields when reading this set of registers. The *Embedded Trace Macrocell Architecture Specification ETMv4* gives more information about many of these fields.

Table 3-77 TCRPIDR0-7 bit assignments

Register	Register number	Register offset	Bits	Value	Description
TRCPIDR7	0x3F7	0xFDC	[31:8]	-	Unused, read undefined.
			[7:0]	0x00	Reserved for future use, RAZ.
TRCPIDR6	0x3F6	0xFD8	[31:8]	-	Unused, read undefined.
			[7:0]	0x00	Reserved for future use, RAZ.
TRCPIDR5	0x3F5	0xFD4	[31:8]	-	Unused, read undefined.
			[7:0]	0x00	Reserved for future use, RAZ.
TRCPIDR4	0x3F4	0xFD0	[31:8]	-	Unused, read undefined.
			[7:4]	0x0	n, where 2^n is number of 4KB blocks used.
			[3:0]	0x4	JEP 106 continuation code.
TRCPIDR3	0x3FB	0xFEC	[31:8]	-	Unused, read undefined.
			[7:4]	0x0	RevAnd (at top level). Manufacturer revision number.
			[3:0]	0x0	Customer Modified. 0x0 indicates from ARM.
TRCPIDR2	0x3FA	0xFE8	[31:8]	-	Unused, read undefined.
			[7:4]	a	Revision Number of Peripheral. This value is the same as the Implementation revision field of the TRCIDR, see *ID Register 1* on page 3-39.
			[3]	1	Always 1. Indicates that a JEDEC assigned value is used.
			[2:0]	b011	JEP 106 identity code [6:4].

Table 3-77 TCRPIDR0-7 bit assignments (continued)

Register	Register number	Register offset	Bits	Value	Description
TRCPIDR1	0x3F9	0xFE4	[31:8]	-	Unused, read undefined.
			[7:4]	b1011	JEP 106 identity code [3:0]
			[3:0]	0x9	Part Number[11:8]. Upper *Binary Coded Decimal* (BCD) value of Device Number.
TRCPIDR0	0x3F8	0xFE0	[31:8]	-	Unused, read undefined.
			[7:0]	0x36	Part Number [7:0]. Middle and Lower BCD value of Device Number.

a. See the Description column for details.

Note

In Table 3-77 on page 3-63, the *Peripheral Identification Registers* on page 3-62 are listed in order of register name, from most significant (TRCPIDR7) to least significant (TRCPIDR0). This does not match the order of the register offsets. Similarly, in Table 3-78 on page 3-65 the *Component Identification Registers* are listed in order of register name, from most significant (TRCCIDR3) to least significant (TRCCIDR0).

3.4.60 Component Identification Registers

The TRCCIDR0-3 characteristics are:

Purpose Identifies the ETM as a CoreSight component. For more information, see the *Embedded Trace Macrocell Architecture Specification ETMv4*.

Usage constraints Only bits[7:0] of each register are used. This means that TRCCIDR0-3 define a single 32-bit Component ID, as Figure 3-68 shows.

Configurations Available in all configurations.

Attributes See the register summary in Table 3-1 on page 3-5 and Table 3-11 on page 3-12.

Figure 3-68 shows the mapping between TRCCIDR0-3 and the single 64-bit *Component ID* value.

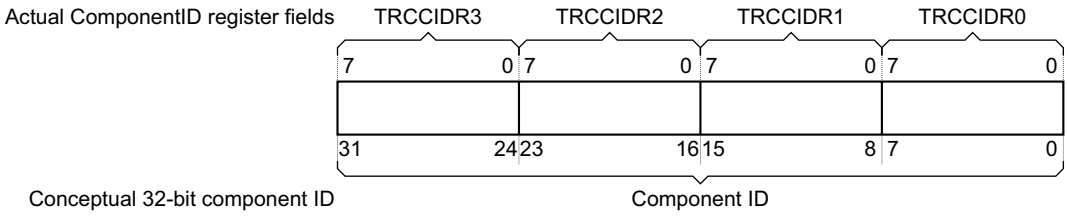

Figure 3-68 Mapping between TRCCIDR0-3 and the Component ID value

Table 3-78 shows the Component ID bit assignments in the single conceptual Component ID register.

Table 3-78 TRCCIDR0-3 bit assignments

Register	Register number	Register offset	Bits	Value	Description
TRCCIDR3	0x3FF	0xFFC	[31:8]	-	Unused, read undefined.
			[7:0]	0xB1	Component identifier, bits [31:24].
TRCCIDR2	0x3FE	0xFF8	[31:8]	-	Unused, read undefined.
			[7:0]	0x05	Component identifier, bits [23:16].
TRCCIDR1	0x3FD	0xFF4	[31:8]	-	Unused, read undefined.
			[7:4]	0x9	Component class (component identifier, bits [15:12]).
			[3:0]	0x0	Component identifier, bits [11:8].
TRCCIDR0	0x3FC	0xFF0	[31:8]	-	Unused, read undefined.
			[7:0]	0x0D	Component identifier, bits [7:0].

3.4.61 Integration Test Registers

The following subsections describe the Integration Test Registers. To access these registers you must first set bit [0] of the *Integration Mode Control Register* on page 3-55 to 1.

- You can use the write-only Integration Test Registers to set the outputs of some of the ETM signals. Table 3-79 shows the signals that can be controlled in this way.
- You can use the read-only Integration Test Registers to read the state of some of the ETM input signals. Table 3-80 on page 3-66 shows the signals that can be read in this way.

See the *Embedded Trace Macrocell Architecture Specification ETMv4* for details of TRCITCTRL.

Table 3-79 Output signals that the Integration Test Registers can control

Signal	Register	Bits	Register description
AFREADYMD	TRCITDATBOUTR	[1]	See *Integration Data ATB Out Register* on page 3-71
AFREADYMI	TRCITIATBOUTR	[1]	See *Integration Instruction ATB Out Register* on page 3-72
ATBYTESMD[2:0]	TRCITDATBOUTR	[10:8]	See *Integration Data ATB Out Register* on page 3-71
ATBYTESMI[1:0]	TRCITIATBOUTR	[9:8]	See *Integration Instruction ATB Out Register* on page 3-72
ATDATAMD[63, 55, 47, 39, 31, 23, 15, 7, 0]	TRCITDDATAR	[8:0]	See *Integration Data ATB Data Register* on page 3-69
ATDATAMI[31, 23, 15, 7, 0]	TRCITIDATAR	[4:0]	See *Integration Instruction ATB Data Register* on page 3-69
ATIDMD[6:0]	TRCITATBIDR	[6:0]	See *Integration ATB Identification Register* on page 3-68
ATIDMI[6:0]	TRCITATBIDR	[6:0]	See *Integration ATB Identification Register* on page 3-68
ATVALIDMD	TRCITDATBOUTR	[0]	See *Integration Data ATB Out Register* on page 3-71

Table 3-79 Output signals that the Integration Test Registers can control (continued)

Signal	Register	Bits	Register description
ATVALIDMI	TRCITIATBOUTR	[0]	See *Integration Instruction ATB Out Register* on page 3-72
ETMACTIVE	TRCITMISCOUTR	[5]	See *Integration Miscellaneous Outputs Register*
ETMEXTOUT[3:0]	TRCITMISCOUTR	[11:8]	See *Integration Miscellaneous Outputs Register*

Table 3-80 Input signals that the Integration Test Registers can read

Signal	Register	Bits	Register description
AFVALIDMD	TRCITDATBINR	[1]	See *Integration Data ATB In Register* on page 3-70
ATREADYMD	TRCITDATBINR	[0]	See *Integration Data ATB In Register* on page 3-70
AFVALIDMI	TRCITIATBINR	[1]	See *Integration Instruction ATB In Register* on page 3-71
ATREADYMI	TRCITIATBINR	[0]	See *Integration Instruction ATB In Register* on page 3-71
CPUACTIVE	TRCITMISCINR	[4]	See *Integration Miscellaneous Inputs Register* on page 3-67
DBGACK	TRCITMISCINR	[5]	See *Integration Miscellaneous Inputs Register* on page 3-67
ETMEVENT[3:0]	TRCITMISCINR	[3:0]	See *Integration Miscellaneous Inputs Register* on page 3-67

Using the Integration Test Registers

The *Cortex-R7 MPCore Integration Manual* gives a full description of the use of the Integration Test Registers to check integration. In brief:

When bit[0] of TRCITCTRL is set to 1:

- Values written to the write-only integration test registers map onto the specified outputs of the macrocell. For example, writing `0x3` TRCITMISCOUTR[11:8] causes **ETMEXTOUT[3:0]** to take the value `0x3`.
- Values read from the read-only integration test registers correspond to the values of the specified inputs of the macrocell. For example, if you read TRCITMISCINR[3:0] you obtain the value of **ETMEXTIN[3:0]**.

When bit[0] of TRCITCTRL is set to 0:

- Reading an Integration Test Register returns an UNPREDICTABLE value.
- The effect of attempting to write to an Integration Test Register, other than the read-only Integration Test Registers, is UNPREDICTABLE.

Note

You must not attempt to write to an Integration Test Register unless you have set bit[0] of TRCITCTRL to 1.

Integration Miscellaneous Outputs Register

The TRCITMISCOUTR characteristics are:

Purpose Sets the state of the output pins shown in Table 3-81 on page 3-67.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-79 on page 3-65.

Figure 3-69 shows the TRCITMISCOUTR bit assignments.

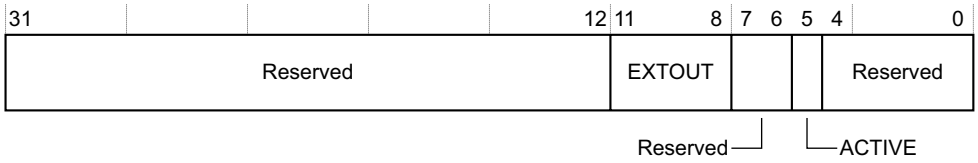

Figure 3-69 TRCITMISCOUTR bit assignments

Table 3-81 shows the TRCITMISCOUTR bit assignments.

Table 3-81 TRCITMISCOUTR bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero.
[11:8]	EXTOUT	Drives the **ETMEXTOUT[3:0]** output pins[a].
[7:6]	-	Reserved. Write as zero.
[5]	ACTIVE	Drives the **ETMACTIVE** output pin[a].
[4:0]	-	Reserved. Write as zero.

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITMISCOUTR bit values correspond to the physical state of the output pins.

Integration Miscellaneous Inputs Register

The TRCITMISCINR characteristics are:

Purpose Reads the state of the input pins shown in Table 3-82 on page 3-68.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-80 on page 3-66.

Figure 3-70 on page 3-68 shows the TRCITMISCINR bit assignments.

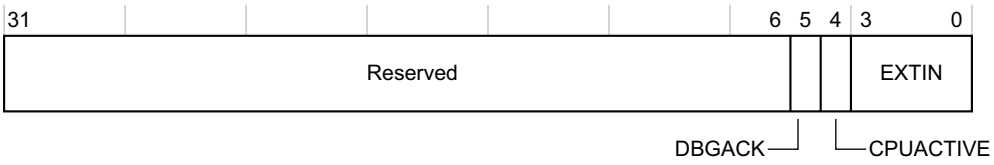

Figure 3-70 TRCITMISCINR bit assignments

Table 3-82 shows the TRCITMISCINR bit assignments.

Table 3-82 TRCITMISCINR bit assignments

Bits	Name	Function
[31:6]	-	Reserved. Read undefined.
[5]	DBGACK	Returns the value of the **DBGACK** input pin[a].
[4]	CPUACTIVE	Returns the value of the **CPUACTIVE** input pin[a].
[3:0]	EXTIN	Returns the value of the **ETMEVENT[3:0]** input pins[a].

a. When an input pin is LOW, the corresponding register bit is 0.
When an input pin is HIGH, the corresponding register bit is 1.
The TRCITMISCINR bit values always correspond to the physical state of the input pins.

Integration ATB Identification Register

The TRCITATBIDR characteristics are:

Purpose Sets the state of output pins shown in Table 3-83.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-79 on page 3-65.

Figure 3-71 shows the TRCITATBIDR bit assignments.

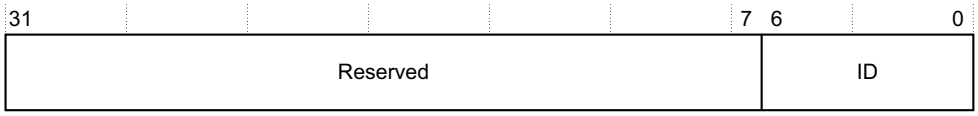

Figure 3-71 TRCITATBIDR bit assignments

Table 3-83 shows the TRCITATBIDR bit assignments.

Table 3-83 TRCITATBIDR bit assignments

Bits	Name	Function
[31:7]	-	Reserved. Read undefined.
[6:0]	ID	Drives the **ATIDMD[6:0]** and **ATIDMI[6:0]** output pins[a].

a. Bits[6:1] drive both **ATIDMD[6:1]** and **ATIDMI[6:1]**. Bit 0] drives **ATIDMI[0]**.
When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
ATIDMD[0] is always driven HIGH.
The TRCITATBIDR bit values correspond to the physical state of the output pins.

Integration Data ATB Data Register

The TRCITDDATAR characteristics are:

Purpose Sets the state of the **ATDATAMD** output pins shown in Table 3-84.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-79 on page 3-65.

Figure 3-72 shows the TRCITDDATAR bit assignments.

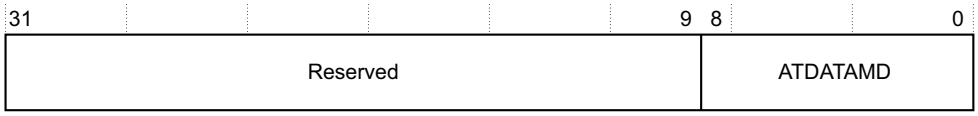

Figure 3-72 TRCITDDATAR bit assignments

Table 3-84 shows the TRCITDDATAR bit assignments.

Table 3-84 TRCITDDATAR bit assignments

Bits	Name	Function
[31:9]	-	Reserved. Write as zero.
[8:0]	ATDATAMD	Drives the **ATDATAMD[63, 55, 47, 39, 31, 23, 15, 7, 0]** output pins[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITDDATAR bit values correspond to the physical state of the output pins.

Integration Instruction ATB Data Register

The TRCITIDATAR characteristics are:

Purpose Sets the state of the **ATDATAMI** output pins shown in Table 3-85 on page 3-70.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-79 on page 3-65.

Figure 3-73 shows the TRCITIDATAR bit assignments.

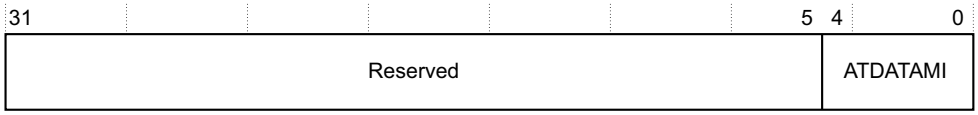

Figure 3-73 TRCITIDATAR bit assignments

Table 3-85 shows the TRCITIDATAR bit assignments.

Table 3-85 TRCITIDATAR bit assignments

Bits	Name	Function
[31:5]	-	Reserved. Write as zero.
[4:0]	ATDATAMI	Drives the **ATDATAMI[31, 23, 15, 7, 0]** output pins[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITIDATAR bit values correspond to the physical state of the output pins.

Integration Data ATB In Register

The TRCITDATBINR characteristics are:

Purpose Reads the state of the input pins shown in Table 3-86.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-80 on page 3-66.

Figure 3-74 shows the TRCITDATBINR bit assignments.

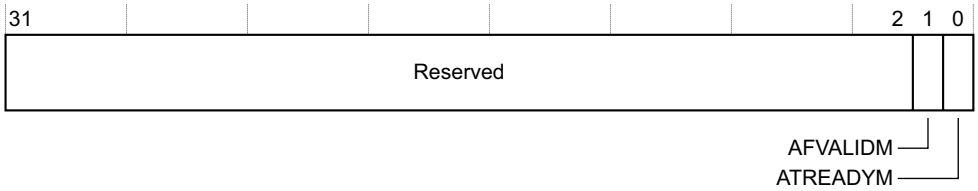

Figure 3-74 TRCITDATBINR bit assignments

Table 3-86 shows the TRCITDATBINR bit assignments.

Table 3-86 TRCITDATBINR bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Read undefined.
[1]	AFVALIDM	Returns the value of the **AFVALIDMD** input pin[a].
[0]	ATREADYM	Returns the value of the **ATREADYMD** input pin[a].

a. When an input pin is LOW, the corresponding register bit is 0.
When an input pin is HIGH, the corresponding register bit is 1.
The TRCITDATBINR bit values always correspond to the physical state of the input pins.

Integration Instruction ATB In Register

The TRCITIATBINR characteristics are:

Purpose Reads the state of the input pins shown in Table 3-87.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-80 on page 3-66.

Figure 3-75 shows the TRCITIATBINR bit assignments.

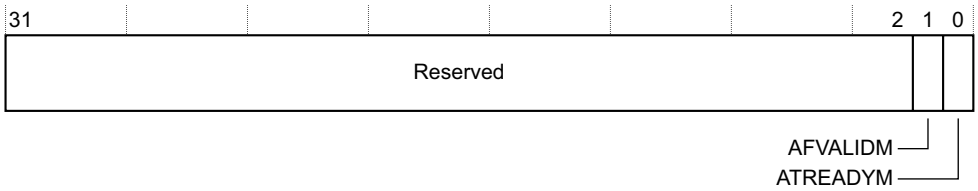

Figure 3-75 TRCITIATBINR bit assignments

Table 3-87 shows the TRCITIATBINR bit assignments.

Table 3-87 TRCITIATBINR bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Read undefined.
[1]	AFVALIDM	Returns the value of the **AFVALIDMI** input pin[a].
[0]	ATREADYM	Returns the value of the **ATREADYMI** input pin[a].

a. When an input pin is LOW, the corresponding register bit is 0.
When an input pin is HIGH, the corresponding register bit is 1.
The TRCITIATBINR bit values always correspond to the physical state of the input pins.

Integration Data ATB Out Register

The TRCITDATBOUTR characteristics are:

Purpose Sets the state of the output pins shown in Table 3-88 on page 3-72.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-79 on page 3-65.

Figure 3-76 shows the TRCITDATBOUTR bit assignments.

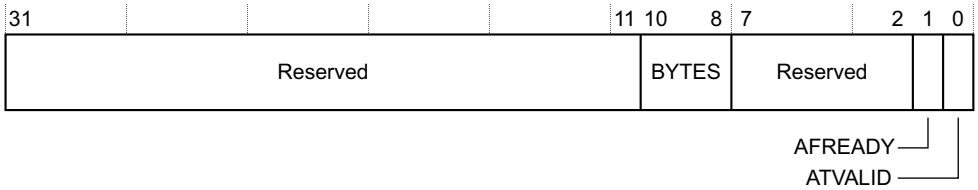

Figure 3-76 TRCITDATBOUTR bit assignments

Table 3-88 shows the TRCITDATBOUTR bit assignments.

Table 3-88 TRCITDATBOUTR bit assignments

Bits	Name	Function
[31:11]	-	Reserved. Read undefined.
[10:8]	BYTES	Drives the **ATBYTESMD[2:0]** output pins[a].
[7:2]	-	Reserved. Read undefined.
[1]	AFREADY	Drives the **AFREADYMD** output pin[a].
[0]	ATVALID	Drives the **ATVALIDMD** output pin[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITDATBOUTR bit values always correspond to the physical state of the output pins.

Integration Instruction ATB Out Register

The TRCITIATBOUTR characteristics are:

Purpose Sets the state of the output pins shown in Table 3-89 on page 3-73.

Usage constraints
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

Configurations Available in all configurations.

Attributes See the register summaries in Table 3-1 on page 3-5, Table 3-10 on page 3-11, and Table 3-79 on page 3-65.

Figure 3-77 shows the TRCITIATBOUTR bit assignments.

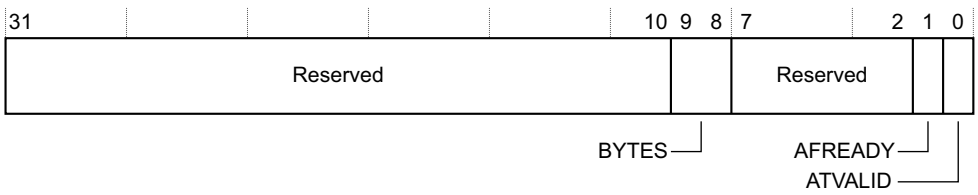

Figure 3-77 TRCITIATBOUTR bit assignments

Table 3-89 shows the TRCITIATBOUTR bit assignments.

Table 3-89 TRCITIATBOUTR bit assignments

Bits	Name	Function
[31:10]	-	Reserved. Read undefined.
[9:8]	BYTES	Drives the **ATBYTESMI[1:0]** output pins[a].
[7:2]	-	Reserved. Read undefined.
[1]	AFREADY	Drives the **AFREADYMI** output pin[a].
[0]	ATVALID	Drives the **ATVALIDMI** output pin[a].

a. When a bit is set to 0, the corresponding output pin is LOW.
When a bit is set to 1, the corresponding output pin is HIGH.
The TRCITIATBOUTR bit values always correspond to the physical state of the output pins.

Appendix A
Signal Descriptions

This appendix describes the signals used in the macrocell. It contains the following sections:

A.1 Signal descriptions

Table A-1 shows the ETM-R7 signals in alphabetical order. The signals listed here are at the ETM level, within the Cortex-R7 MPCore processor top level. See the *Cortex-R7 MPCore Technical Reference Manual* for a list of top-level signals. The following sections show the signal directions for each of the interfaces. See the *Cortex-R7 MPCore Integration Manual* for information about signals and connectivity.

Table A-1 ETM-R7 signals

Signal name	Description
AFREADYMD	*ATB interface* on page A-7
AFREADYMI	*ATB interface* on page A-7
AFVALIDMD	*ATB interface* on page A-7
AFVALIDMI	*ATB interface* on page A-7
ATBYTESMD[2:0]	*ATB interface* on page A-7
ATBYTESMI[1:0]	*ATB interface* on page A-7
ATDATAMD[63:0]	*ATB interface* on page A-7
ATDATAMI[31:0]	*ATB interface* on page A-7
ATIDMD[6:0]	*ATB interface* on page A-7
ATIDMI[6:0]	*ATB interface* on page A-7
ATREADYMD	*ATB interface* on page A-7
ATREADYMI	*ATB interface* on page A-7
ATVALIDMD	*ATB interface* on page A-7
ATVALIDMI	*ATB interface* on page A-7
CLK	*Clocks and resets* on page A-4
CPUACTIVE	*Processor trace interface* on page A-5
DBGACK	*Processor trace interface* on page A-5
DFTSE	*Test interface* on page A-9
ETMACTIVE	*Processor trace interface* on page A-5
ETMBACK	*Processor trace interface* on page A-5
ETMBUS[321:0]	*Processor trace interface* on page A-5
ETMEVENT[63:0]	*Miscellaneous signals* on page A-8
ETMEXTOUT[3:0]	*Miscellaneous signals* on page A-8
ETMIFEN	*Processor trace interface* on page A-5
ETMIFVALID	*Processor trace interface* on page A-5
ETMPWRUPREQ	*Miscellaneous signals* on page A-8
NIDEN	*Miscellaneous signals* on page A-8
nRESET	*Clocks and resets* on page A-4

Table A-1 ETM-R7 signals (continued)

Signal name	Description
NUMPROC[2:0]	*Miscellaneous signals* on page A-8
PADDRDBG[11:2]	*APB interface* on page A-6
PADDRDBG31	*APB interface* on page A-6
PENABLEDBG	*APB interface* on page A-6
PRDATADBG[31:0]	*APB interface* on page A-6
PREADYDBG	*APB interface* on page A-6
PROCSEL[2:0]	*Miscellaneous signals* on page A-8
PSELDBG	*APB interface* on page A-6
PSLVERRDBG	*APB interface* on page A-6
PWDATADBG[31:0]	*APB interface* on page A-6
PWRITEDBG	*APB interface* on page A-6
SYNCREQD	*ATB interface* on page A-7
SYNCREQI	*ATB interface* on page A-7
SYSSTALL	*Miscellaneous signals* on page A-8
TSSIZE	*Miscellaneous signals* on page A-8
TSVALUE[63:0]	*Miscellaneous signals* on page A-8

A.2 Clocks and resets

Table A-2 shows the clock and reset signals.

Table A-2 Clock and reset signals

Signal name	Type	Source/destination	Description
CLK	Input	Clock source	This is the clock for the ETM-R7.
nRESET	Input		Debug reset. Resets programmers model as specified in the *Embedded Trace Macrocell Architecture Specification ETMv4*.

A.3 Processor trace interface

Table A-3 shows the trace interface signals from the Cortex-R7 MPCore processor.

Table A-3 Processor trace interface signals

Signal name	Type	Source/destination	Description
ETMBUS[321:0]	Input	Processor	Combined ETM interface channel.
ETMIFVALID	Input		Core active, interface stable.
ETMIFEN	Output		Power control for processor ETM interface.
ETMBACK	Output		Configurable output to stall processor.
DBGACK	Input		Processor is in debug state.
CPUACTIVE	Input		Processor is not in WFI/WFE or other low power state.

A.4 APB interface

Table A-4 shows the APB signals.

Table A-4 APB signals

Signal name	Type	Source/destination	Description
PADDRDBG[11:2]	Input	Debug APB interconnect	Debug APB Address Bus.
PADDRDBG31	Input		Originates as an output signal from the *Debug Access Por*t (DAP): • **PADDRDBG31** at logic 1 indicates an access from hardware (JTAG). • **PADDRDBG31** at logic 0 indicates an access from software.
PENABLEDBG	Input		The Debug APB interface is enabled for a transfer.
PSELDBG	Input		Debug APB slave select signal.
PREADYDBG	Output		Used to extend Debug APB transfers.
PRDATADBG[31:0]	Output		Debug APB read data.
PWDATADBG[31:0]	Input		Debug APB write data.
PWRITEDBG	Input		Debug APB transfer direction: 0 = Read 1 = Write.
PSLVERRDBG	Output		Debug APB error response.

A.5 ATB interface

Table A-5 shows the ATB signals for instruction trace.

Table A-5 ATB signals for instruction trace

Signal name	Type	Source/destination	Description
AFREADYMI	Output	CoreSight trace system	ATB interface FIFO flush finished.
AFVALIDMI	Input		ATB interface FIFO flush request.
ATBYTESMI[1:0]	Output		Size of **ATDATA**.
ATDATAMI[31:0]	Output		ATB interface data.
ATIDMI[6:0]	Output		ATB interface trace source ID.
ATREADYMI	Input		**ATDATA** can be accepted.
ATVALIDMI	Output		ATB interface data valid.
SYNCREQI	Input		Synchronization request from instruction trace sink.

Table A-6 shows the ATB signals for data trace.

Table A-6 ATB signals for data trace

Signal name	Type	Source/destination	Description
AFREADYMD	Output	CoreSight trace system	ATB interface FIFO flush finished.
AFVALIDMD	Input		ATB interface FIFO flush request.
ATBYTESMD[2:0]	Output		Size of **ATDATA**.
ATDATAMD[63:0]	Output		ATB interface data.
ATIDMD[6:0]	Output		ATB interface trace source ID.
ATREADYMD	Input		**ATDATA** can be accepted.
ATVALIDMD	Output		ATB interface data valid.
SYNCREQD	Input		Synchronization request from data trace sink.

A.6 Miscellaneous signals

Table A-7 shows the miscellaneous signals.

Table A-7 Miscellaneous signals

Signal name	Type	Source/destination	Description
PROCSEL[2:0]	Output	Trace multiplexor, if present	Where an ETM is shared between multiple processors, this signal controls the multiplexor. The value is driven from bits[2:0] of the *Processor Select Control Register* on page 3-13.
NUMPROC[2:0]	Input	Tie off	Where an ETM is shared between multiple processors, this signal specifies the number of processors the ETM can trace. It must be tied to the number of processors sharing the ETM minus 1. These signals determine the value of bits[30:28] in the *ID Register 3* on page 3-41.
NIDEN	Input	System	Non-invasive debug enable. When HIGH (1), indicates that non-invasive debug is enabled.
ETMACTIVE	Output	Processor	Trace is being output.
ETMEVENT[63:0]	Input	PMU and CTI	External input resources.
ETMEXTOUT[3:0]	Output	CTI	External outputs.
SYSSTALL	Input	Tie off	System supports stalling of the processor by the ETM.
ETMPWRUPREQ	Output	System power control	Request to maintain power to ETM.
TSSIZE	Input	Tie off	When HIGH (1), timestamp is 64 bit. When LOW (0), timestamp is 48 bit.
TSVALUE[63:0]	Input	CoreSight system	Timestamp value.
CLUSTERID[3:0]	Input	System	Value read in the Cluster ID field, bits[11:8], of the Cortex-R7 *Multiprocessor Affinity Register* (MPIDR).
CPUID	Input	System	Value read in the CPU ID field, bit[0], of the MPIDR in the connected processor.

A.7 Test interface

Table A-8 shows the scan chain signal.

Table A-8 Test signal

Signal name	Type	Source/destination	Description
DFTSE	Input	Tester	Scan enable DFT signal.

Appendix B
Revisions

This appendix describes the technical changes between released issues of this book.

Table B-1 Issue A

Change	Location	Affects
First release	-	-

Table B-2 Differences between issue A and issue B

Change	Location	Affects
Added Data FIFO	Table 1-1 on page 1-5	All revisions
Added description of synchronization	*Synchronization* on page 2-11	All revisions
Updated value of MAXSPEC field in TRCIDR8	Table 3-1 on page 3-5 and Table 3-39 on page 3-35	r0p1
Updated value of NUMP0KEY field in TRCIDR9	Table 3-1 on page 3-5 and Table 3-40 on page 3-36	r0p1
Updated value of REVISION field and reset value for TRCIDR1	Table 3-1 on page 3-5 and Table 3-47 on page 3-40	r0p1
Added description of TRCOSLSR	Table 3-1 on page 3-5, Table 3-8 on page 3-11, and *OS Lock Status Register* on page 3-48	All revisions
Clarified coverage of ETM signals	*Signal descriptions* on page A-2	All revisions