Juno r2 ARM® Development Platform SoC

Revision: r2p0

Technical Overview

ARM®

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Juno r2 ARM Development Platform SoC
Technical Overview

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
10 July 2014	A	Non-Confidential	First release, for r0p0
01 May 2015	B	Non-Confidential	Second release, for r1p0
16 December 2015	C	Non-Confidential	Third release, for r2p0

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Product Status

The information in this document is final, that is for a developed product.

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Contents

Juno r2 ARM Development Platform SoC Technical Overview

Preface

This preface introduces the *Juno ARM® Development Platform SoC Technical Overview*. It contains the following sections:

About this book

This book is for the *Juno ARM Development Platform* (ADP) SoC. It provides a high-level overview of the ADP.

Product revision status

The r*m*p*n* identifier indicates the revision status of the product described in this book, for example, r0p0, where:

r*m* Identifies the major revision of the product, for example, r0.

p*n* Identifies the minor revision or modification status of the product, for example, p0.

Intended audience

This book is written for software engineers who want to work with an ARM® reference platform. It describes the high-level functionality of the ADP SoC.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the ADP SoC, a description of its features, and the components that it contains.

Chapter 2 *Hardware Functional Description*

Read this for a description of the major hardware interfaces, the hardware components of the ADP, and how they operate.

Chapter 3 *Software Functional Description*

Read this for a description of the ADP software.

Appendix A *Hardware Components*

Read this for a detailed description of the hardware components that the ADP SoC and the motherboard contain.

Appendix B *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

The *ARM Glossary* is available on the ARM Infocenter at `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html`.

Conventions

Conventions that this book can use are described in:

- *Typographical conventions*.
- *Timing diagrams*.
- *Signals* on page viii.

Typographical conventions

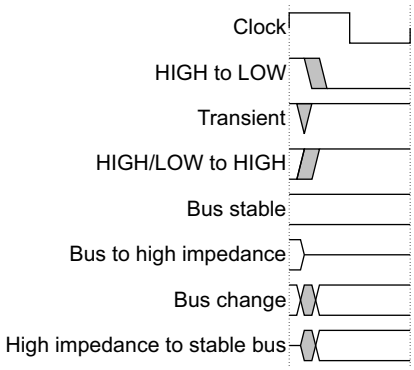
The following table describes the typographical conventions:

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace`	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace` *`italic`*	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions* on page vii. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter, http://infocenter.arm.com for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *Juno r2 ARM® Development Platform SoC Technical Reference Manual* (ARM DDI 0515)
  http://infocenter.arm.com/help/topic/com.arm.doc.ddi0515-/index.html.
- *ARM® Versatile™ Express Juno r2 Development Platform (V2M-Juno r2) Technical Reference Manual* (ARM 100114)
  http://infocenter.arm.com/help/topic/com.arm.doc.100114_0200_00_en/index.html.
- *Juno ARM® Development Platform Getting Started Guide* (ARM DUI 0928)
  http://infocenter.arm.com/help/topic/com.arm.doc.dui0928-/index.html.
- *ARM® Juno System Profiler Technical Reference Manual* (ARM DDI 0520).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- The title.
- The number, ARM DTO 0038C.
- The page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Note

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Chapter 1
Introduction

This chapter introduces the *Juno r2 ARM® Development Platform* (ADP) SoC. It contains the following section:

1.1 Purpose

The ADP SoC is a development platform for:

- ARMv8 AArch64 and AArch32 compute.
- big.LITTLE™ *Multi-Processing* (MP).
- *Graphics Processing Unit* (GPU) compute.
- 3D Graphics.
- Control and management of:
  - Security.
  - Power.
  - Thermal.

The ADP SoC enables you to develop software and tooling for ARMv8 AArch64 and AArch32.

1.2 Components

The ADP SoC consists of the following:

- A standalone development motherboard, ARM® Versatile™ Express Juno Development Platform V2M-Juno r2, instantiating the ADP SoC fabricated in TSMC28HPM.
- A *Software Development Kit* (SDK) that supports each hardware platform and contains the following:
  - ADP AArch64 firmware with standardized *Application Programming Interfaces* (APIs).
  - AArch64 Linux kernel with big.LITTLE MP support.
  - AArch32 and AArch64 Linux user space example.
- DS-5 tool support.

The processor clusters contain the following fully coherent processor clusters:

- Dual core Cortex®-A72 processor cluster.
- Quad core Cortex-A53 processor cluster.

The GPU cluster contains an I/O-coherent Mali™-T624 Series GPU.

The compute platform also contains a Cortex-M3 *System Control Processor* (SCP) for power control and thermal management.

External interfaces include:

- External memory capability includes DDR3-1600 dual channel striped memories.
- USB2 and a custom SoC to *Field Programmable Gate Array* (FPGA) prototyping extension interface.
- A *Peripheral Component Interconnect Express* (PCIe) Gen2.0 four lanes, Root Port, and PHY, that has both I/O coherent and non-coherent modes.

1.3 Software development

The ADP delivers heterogeneous compute to software developers including big.LITTLE64 and *General-Purpose computing on Graphics Processing Units* (GPGPU) compute, for example:

- OpenCL.
- Direct Compute.
- OpenGL-ES.
- Direct-X graphics.
- *Trusted Execution Environment* (TEE) integration.
- Advanced power control and thermal management.

1.4 Compliance

The ADP conforms to ARM *Platform Design Documents* (PDDs) and white paper guidance documents, in particular, the following:

- *Server Base System Architecture – Level1* (ARM-EPM-030514).
- *Trusted Base System Architecture 1* (ARM DEN 0007).
- *Trusted Board Boot Requirements* (ARM DEN 0006).
- *Power State Coordination Interface* (ARM DEN 0022).
- *Principles of ARM® Memory Maps White Paper* (ARM DEN 0001).

This document provides a technical overview of the ADP design and associated software deliverables for the platform.

Chapter 2
Hardware Functional Description

This chapter describes the functionality of the *Juno r2 ARM® Development Platform* (ADP) SoC hardware.

It contains the following sections:

2.1 Functional overview

Figure 2-1 shows a block diagram of the ADP SoC.

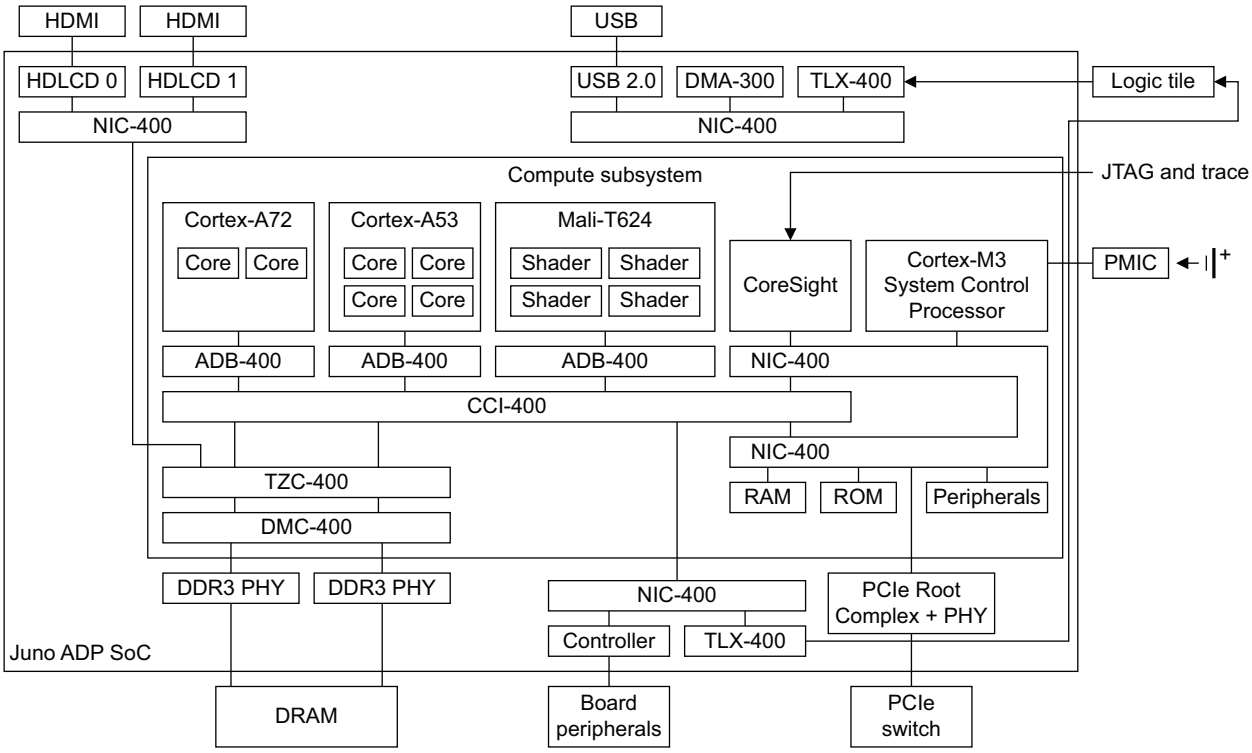

Figure 2-1 ADP SoC block diagram

The main components are as follows:

- *Cortex-A72 processor cluster subsystem* on page 2-3.
- *Cortex-A53 processor cluster subsystem* on page 2-3.
- *Graphics subsystem* on page 2-3.
- *System Control Processor (SCP) subsystem* on page 2-4.
- *Interconnects and on-system memory* on page 2-4.
- *System Memory Management Unit (SMMU)* on page 2-4.
- *Generic Interrupt Controller (GIC)* on page 2-4.
- *Memory subsystem* on page 2-5.
- *Peripheral Component Interconnect Express (PCIe)* on page 2-5.
- *USB 2.0 Enhanced Host Controller Interface (EHCI)* on page 2-5.
- *Direct Memory Access (DMA)* on page 2-5.
- *High Definition Liquid Crystal Display (HDLCD) controllers* on page 2-5.
- *Static Memory Controller (SMC)* on page 2-6.
- *Universal Asynchronous Receiver-Transmitter (UART)* on page 2-6.
- *I2C* on page 2-6.
- *Thin Links SoC to FPGA prototyping interface* on page 2-6.
- *CoreSight™* on page 2-6.

2.1.1 Cortex-A72 processor cluster subsystem

The Cortex®-A72 processor subsystem consists of the following:

- ARMv8 dual core Cortex-A72 cluster that is configured with an AMBA®4 ACE interface and 2MB L2 cache.
- ARM® CoreLink™ ADB-400 AMBA® Domain Bridge to enable *Dynamic Voltage and Frequency Scaling* (DVFS).

2.1.2 Cortex-A53 processor cluster subsystem

The Cortex-A53 processor subsystem consists of the following:

- ARMv8 quad core Cortex-A53 cluster that is configured with an AMBA4 ACE interface and 1MB L2 cache.
- CoreLink ADB-400 asynchronous bridge to enable DFVS.

2.1.3 Graphics subsystem

The Mali™-T624 Series *Graphics Processing Unit* (GPU) is a high-performance hardware accelerator for 2D and 3D graphics. The GPU subsystem consists of the following:

- Mali-T624 Series GPU containing:
  - Four shader cores.
  - A hierarchical tiler.
  - A *Power-Management Unit* (PMU).
- A job manager that distributes workloads to the four shader cores.
- A *Memory-Management Unit* (MMU) that performs address translation of data reads and writes from components in the system.
- A CoreLink ADB-400 asynchronous bridge to enable DFVS.

The Mali-T624 Series GPU is configured with 128KB L2 RAM and an AMBA4 ACE-Lite interface.

The GPU and its associated software are compatible with the following graphics standards:

- OpenGL ES 1.1 and 2.0.
- OpenCL 1.1 full profile.
- EGL 1.4.
- Renderscipt compute.
- DirectX 11 feature level 9_1, 9_3 through DX9 DDI, including Direct3D.
- DirectX 11 full-feature through DX10/11 DDI:
  - Direct3D.
  - DirectCompute.

2.1.4 *System Control Processor* (SCP) subsystem

A Cortex-M3 processor controls and manages the SoC. The SCP:

- Controls clocks and resets.
- Is responsible for power state transitions for the power regions in the SoC.
- Has direct control over the *Power-Management Integrated Circuit* (PMIC) on the board.

The *Operating System* (OS) can send power-management commands to the SCP using a hardware *Message Handling Unit* (MHU).

2.1.5 Interconnects and on-system memory

The ADP contains a CoreLink CCI-400 Cache Coherent Interconnect that provides:

- Full coherency between the processor clusters.
- I/O coherency between the GPU and processor clusters.

A 128-bit I/O coherent slave and master interface is extended from the coherent interconnect using CoreLink NIC-400 Network Interconnect components and connected to peripherals such as *Direct Memory Access* (DMA) and interchip interconnect.

The following static RAMs are instantiated for the application processors:

- 128KB trusted.
- 16KB non-trusted.

The following ROMs are instantiated for the application processors:

- 128KB trusted.
- 16KB non-trusted.

The ROM code is fully committed at the time of manufacture. However, it is possible to override the internal code of both ROMs for development and debug purposes.

2.1.6 *System Memory Management Unit* (SMMU)

Individual ARM CoreLink MMU-401 System Memory Management Unit or ARM CoreLink MMU-400 System Memory Management Unit components connect all non-processor masters such as the following, to the ARM CoreLink CCI-400 Cache Coherent Interconnect and ARM CoreLink NIC-400 Network Interconnect components:

- Graphics subsystem.
- *Universal Serial Bus* (USB).
- DMA.
- Debug subsystem.

These SMMUs implement stage 2 address translations, that translates an *Intermediate Physical Address* (IPA) to a *Physical Address* (PA).

2.1.7 *Generic Interrupt Controller* (GIC)

The ADP ARM CoreLink GIC-400 Generic Interrupt Controller complies with the GICv2m architecture. GICv2m includes a message-based interrupt feature that is necessary to handle *Message Signaled Interrupts* (MSIs).

GICv2m enables MSIs to set GICv2 *Shared Peripheral Interrupts* (SPIs) to pending. The GICv2m provides a similar mechanism to the message-based interrupt features added in GICv3.

The ADP SoC is compliant to level 1 of the Server Base System Architecture specification. See *Compliance* on page 1-5.

2.1.8 Memory subsystem

The memory subsystem contains an ARM CoreLink DMC-400 Dynamic Memory Controller that interfaces with external DDR memory using a dual 32-bit DDR3 PHY. The PHY supports both DDR3, and DDR3L and operates to 1600MT/s.

An ARM CoreLink TZC-400 TrustZone™ Address Space Controller exists at the interface of the DMC-400 to the system. The TZC-400 enables the trusted OS to define multiple regions within the DDR memory that have different security access permissions.

2.1.9 *Peripheral Component Interconnect Express* (PCIe)

The ADP includes a 4-lane PCIe Root Port capable of operating at up to 5GTps per lane. The Root Port supports high-bandwidth connectivity with external peripherals such as SATA disk controllers and Gigabit Ethernet NIC. The PCIe Root Port and PHY are integrated on the chip.

2.1.10 USB 2.0 *Enhanced Host Controller Interface* (EHCI)

The ADP SoC instantiates a bus mastered USB 2.0 *Enhanced Host Controller Interface* (EHCI) host controller for attaching peripherals such as keyboard, mouse, and flash drive to the system. The EHCI operates with native OS drivers and supports the following available speeds:

- Low speed.
- Full speed.
- Hi speed.

USB 2.0 supports data rates of 480Mbps. The host controller is on the SoC. It is connected to a USB PHY on the board through the 60MHz 12-pin *UTMI+ Low Pin Interface* (ULPI) *Single Data Rate* (SDR) interface[1]. The USB controller is configured to provide one OHCI controller and one EHCI controller. Debug is an optional feature in EHCI but the ADP does not support it.

The USB 2.0 controller supports 64-bit EHCI addressing capability therefore supports *Large Physical Address Extension* (LPAE) and 64-bit *Operating Systems* (OSs).

2.1.11 *Direct Memory Access* (DMA)

The ADP SoC includes a system ARM CoreLink DMA-330 DMA Controller. You can use the *Direct Memory Access* (DMA) controller to transfer data:

- Within memory.
- Between memory and peripherals.

2.1.12 *High Definition Liquid Crystal Display* (HDLCD) controllers

The ADP SoC includes two independent *High Definition Liquid Crystal Display* (HDLCD) controllers. The HDLCD controllers can run from:

- An HDLCD clock that is generated by an on-chip PLL.
- A shared clock that is fed directly from outside through the input pad.

This scheme enables both displays to run at high resolution, and you can switch either or both of the displays to low-resolution mode, such as VGA, if necessary. The ADP includes a single HDLCD PLL and it is not possible to run both displays at different high-resolution modes. The achievable frame rate of *Full-High Definition* (FHD) is 60fps.

An I^2S controller supplies audio, and the output serves the two *High Definition Multimedia Interface* (HDMI) connectors that are on the board.

1. *USB 2.0 Transceiver Macrocell Interface* (UTMI).

2.1.13 *Static Memory Controller* (SMC)

The ADP includes an SMC-354 *Static Memory Controller* (SMC) to provide access to a 64MB off-chip NOR flash. The interface also provides access to off-chip peripherals such as *Non-Volatile* (NV) counter for anti-replay protection, Secure keypad input, and *Real Time Counter* (RTC) instantiated within a *Field Programmable Gate Array* (FPGA).

2.1.14 *Universal Asynchronous Receiver-Transmitter* (UART)

The ADP SoC provides Secure and Non-secure *Universal Asynchronous Receiver-Transmitter*s (UARTs), PL011s, for:

- Firmware logs and interactive firmware shell.
- Debugging the OS kernel.

Both serial ports operate at up to 115200Bd.

2.1.15 I^2C

The ADP SoC includes the following I^2C controllers:

1. I^2C controller that is only accessible from the SCP and used for PMIC control.
2. I^2C controller that is mapped in the application processor area and used for board functions such as:
   - HDMI controller configuration.
   - *Small Outline Dual In-line Memory Module* (SODIMM) discovery.
3. I^2C controller that is mapped in the application processor area and used exclusively for trusted user input from a keypad.

2.1.16 Thin Links SoC to FPGA prototyping interface

The ADP contains an ARM CoreLink TLX-400 Network Interconnect Thin Links component. An AXI expansion interface covers both master and slave interfaces for prototyping and driver development for external components such as GPU and I/O peripherals. The Thin Links expansion interface supports 40-bit addressing, QoS, and I/O coherency. The interface supports the following bandwidths:

Juno r2 SoC master interface

- Forward direction, that is, from the Juno r2 SoC to the FPGA: 68Mbps.
- Reverse direction, that is, from the FPGA to the Juno r2 SoC: 78Mbps.

Juno r2 SoC slave interface

- Forward direction, that is, from the FPGA to the Juno r2 SoC: 246Mbps.
- Reverse direction, that is, from the Juno r2 SoC to the FPGA: 305Mbps.

2.1.17 CoreSight™

ARM CoreSight™ technology provides debug and trace capability and includes an enhanced capability for extracting bandwidth and latency measurements from the system.

2.2 *Trusted Execution Environment* (TEE)

The ADP provides a software development environment to enable the development of a trusted OS.

Specifically, the following peripherals are instantiated:

- *Trusted entropy sources*.
- *Trusted key storage*.
- *Non-Volatile (NV) counter*.
- *Non-invasive attack prevention*.

2.2.1 Trusted entropy sources

Two trusted entropy sources are instantiated.

2.2.2 Trusted key storage

The *Trusted Board Boot Requirements* (TBBR) PDD defines a set of cryptographic keys to store in *One Time Programmable* (OTP) or eFuse memory. The ADP does not instantiate an OTP or eFuse macro. Instead, keys are tied in hardware, using registers that TIE cells drive, to a default and fixed value. These keys are as follows:

- 128-bit *Hardware Unique Key* (HUK).
- 256-bit *Endorsement Key* (EK).
- 256-bit Hash of the *Root Of Trusted Public Key* (ROTPK).

Note

The optional *Secret Symmetric Key* (SSK) is not implemented.

2.2.3 *Non-Volatile* (NV) counter

The *Trusted Base System Architecture* (TBSA) PDD defines a series of NV counters that retain state even when the SoC has been powered down. For the purposes of the development platform, the trusted and non-trusted counters are tied to the limit of increment:

31 For the trusted counter.

223 For the non-trusted counter.

The 232 state anti-replay counter exists through implementation in an external FPGA and you can access it by using a Secure I^2C access.

2.2.4 Non-invasive attack prevention

The ADP does not instantiate peripherals to prevent non-invasive attacks such as glitch or brown-out detection.

2.3 Power control and thermal management

This section contains the following subsections:

- *Voltage domains*.
- *Power-gated regions* on page 2-9.
- *Sensor-based power-management* on page 2-9.

2.3.1 Voltage domains

The following core voltage domains exist on the ADP SoC:

VA72 Core supply to the dual core Cortex-A72 cluster. 0.8-1.0V. Switchable on the board.

VA53 Core supply to the quad core Cortex-A53 cluster. 0.8-1.0V. Switchable on the board.

VGPU Core supply to the Mali-T624 Series GPU. 0.8-0.9V. Switchable on the board.

VSYSTOP Main 0.9V supply to the SoC top-level, including peripherals such as USB, top-level logic, and the CoreSight subsystem. Switchable on the board.

VAON Always on 0.9V supply to the SCP subsystem, Debug Access Ports, and the digital side of the *General Purpose Input and Output* (GPIO).

The ADP contains asynchronous clock domains that fully support DVFS of the Cortex-A72 cluster, Cortex-A53 cluster, and the GPU. Figure 2-2 on page 2-9 shows the ADP voltage domains.

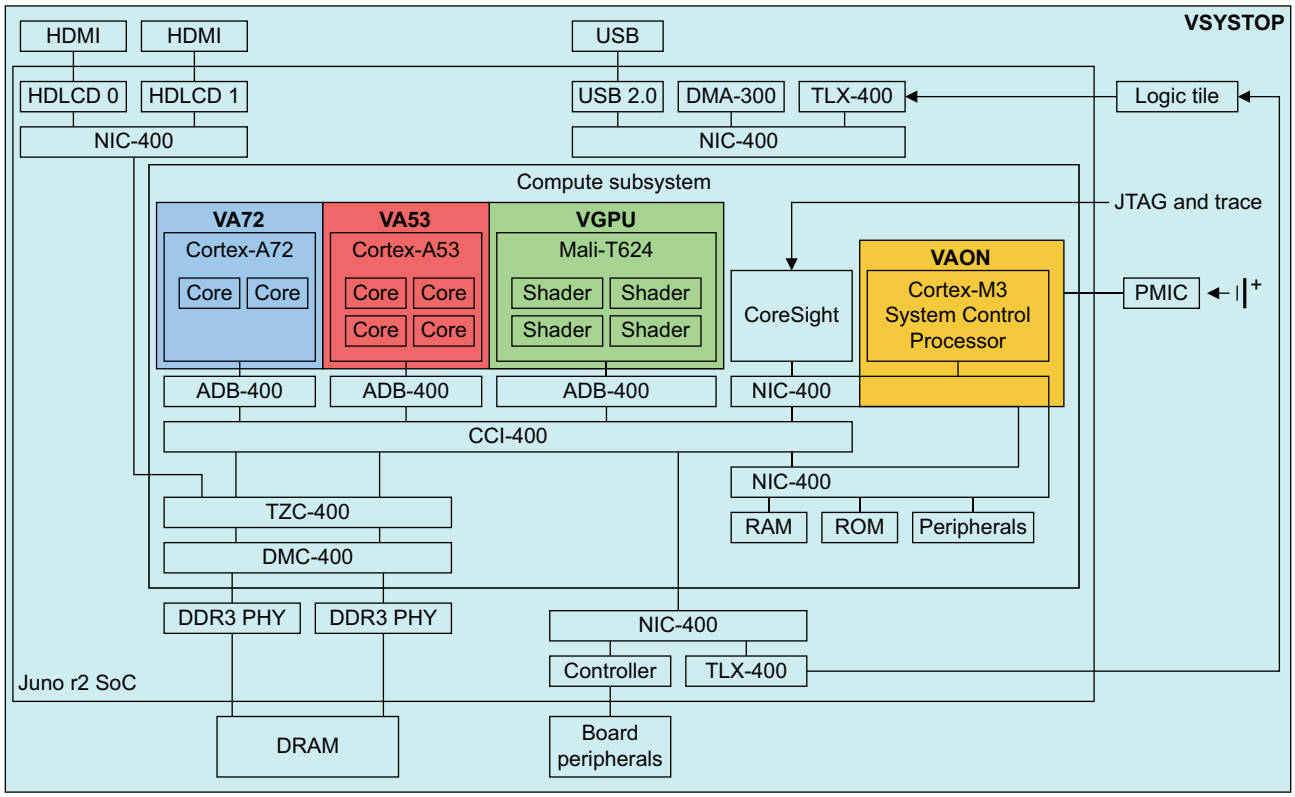

Figure 2-2 ADP voltage domains

2.3.2 Power-gated regions

The ADP contains the following gated power components:

- The two Cortex-A72 cores, the *Snoop Control Unit* (SCU), and the L2 can be power-gated separately.
- The four Cortex-A53 cores, the SCU, and the L2 can be power-gated separately. The *Embedded Trace Macrocell* (ETM) is not separately gated.

The GPU has no provision for individual power-gating of each shader core.

2.3.3 Sensor-based power-management

Sensor-based power-management provides feedback to the SCP and application processors to enable real-time thermal management. *Power, Voltage, Temperature* (PVT) monitors are instantiated at key locations in the ADP, such as physically close to the GPU and Cortex-A72 processor clusters. Unique SQ adjustment parameters for each device support sensor calibration.

2.4 ADP motherboard specification

The ADP motherboard includes the following hardware:

- PMIC.
- *Ball Grid Array* (BGA), BGA-1156, instantiating an ADP SoC.
- Dual HDMI Controllers.
- Two DDR3-1600, 800MHz, providing 8GB of memory.
- USB 2.0 PHY and USB hub.
- A *Peripheral Component Interconnect Express* (PCIe) Gen2.0 four lanes, Root Port, and PHY, that has both I/O coherent and non-coherent modes.
- NOR Flash, 64MB, two banks of 32MB.
- Two RS232 UARTs.
- I/O component FPGA providing:
  - Secure I^2C anti-replay counters.
  - Battery-backed *Real Time Clock* (RTC).
  - Secure keyboard and keypad socket.
- ARM CoreSight Interfaces, *Joint Test Action Group* (JTAG), and trace.

Figure 2-3 on page 2-11 shows a block diagram of the ADP board.

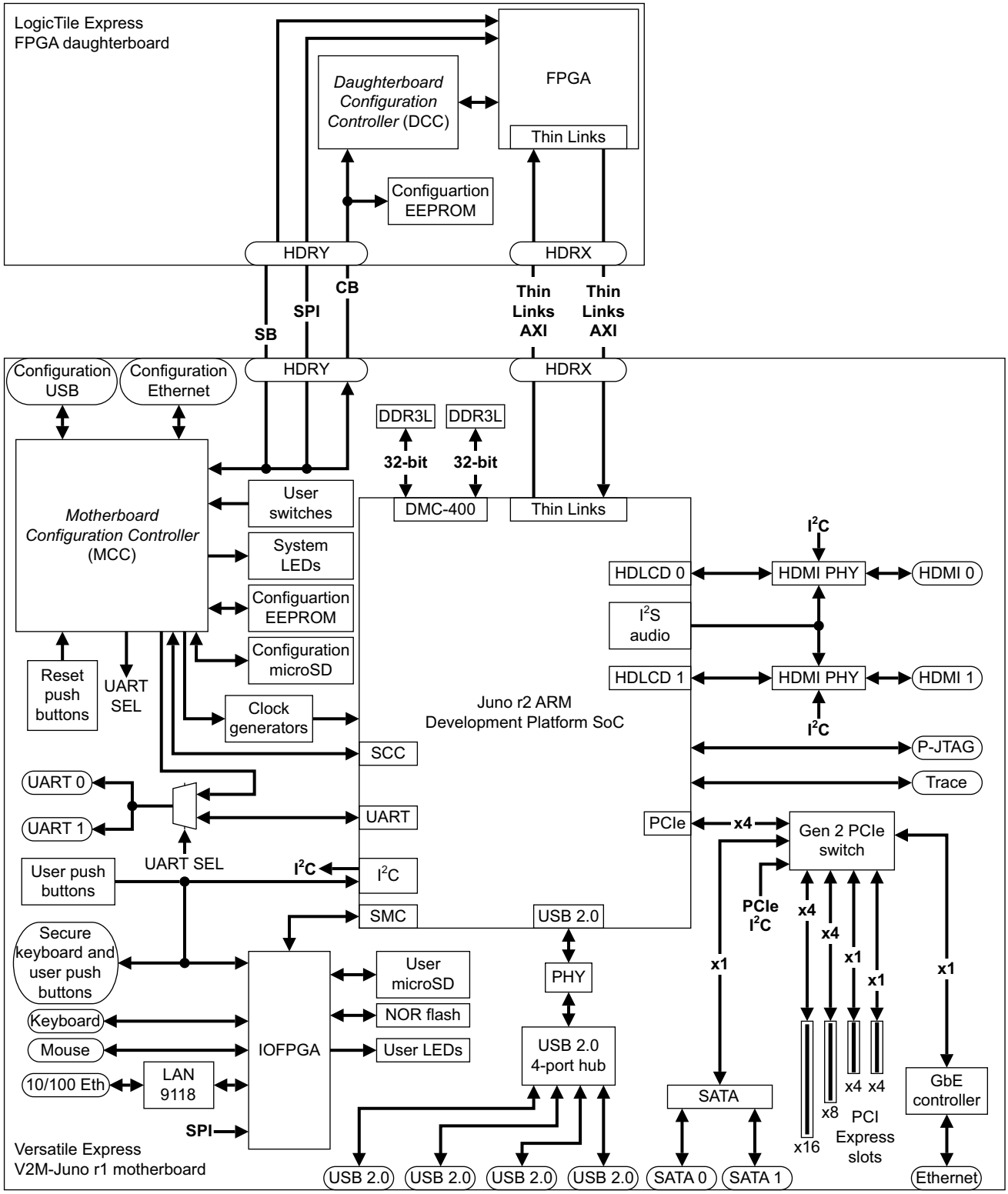

Figure 2-3 ADP board block diagram

Chapter 3
Software Functional Description

This chapter contains links to information about the *Juno ARM® Development Platform* (ADP) SoC software.

- The following website describes the Juno r2 software stacks:
  https://community.arm.com/groups/arm-development-platforms
- The *Juno ARM® Development Platform Getting Started Guide* in the following location describes the firmware:
  http://infocenter.arm.com/help/topic/com.arm.doc.dui0928-/index.html

Appendix A
Hardware Components

This chapter describes the *Juno r2 ARM Development Platform* (ADP) SoC hardware. It contains the following sections:

A.1 ADP SoC

The ADP SoC includes the following hardware:

- Dual core Cortex®-A72 processor cluster.
- Quad core Cortex-A53 processor cluster.
- Mali™-T624 Series GPU with four shader cores.
- *System Control Processor* (SCP) based on a Cortex-M3 processor.
- CoreLink™ CCI-400 Cache Coherent Interconnect.
- CoreLink NIC-400 Network Interconnect.
- CoreLink MMU-401 System Memory Management Unit.
- CoreLink MMU-400 System Memory Management Unit.
- CoreLink GIC-400 Generic Interrupt Controller.
- CoreLink DMC-400 DDR3 Dynamic Memory Controller.
- CoreLink DMA-330.
- Dual 32-bit DDR3, two × 1600MT/s.
- Dual ARM HDLCD display controllers, 1920 × 1080 at 60fps, with single I^2S with four stereo channels.
- Bus mastered EHCI USB2 host controller, 480Mbps, *UTMI+ Low Pin Interface* (ULPI) interface to off-chip PHY[1].
- CoreLink SMC-354 Static Memory Controller, 64MB NOR flash, and board peripherals.
- UART, two × PL011.
- I^2C, high-speed mode, 3.4Mb/s.
- PVT sensor subsystem.
- Security peripherals, RNG, NV counters, fuses, 32KHz oscillator.
- AXI master and slave SoC to FPGA interface based on CoreLink TLX-400, Thin Links technology.

1. *USB 2.0 Transceiver Macrocell Interface* (UTMI).

A.2 ADP motherboard

See *ADP motherboard specification* on page 2-10.

Appendix B
Revisions

This appendix describes the technical changes between released issues of this book.

Table B-1 Issue A

Change	Location	Affects
First release.	-	-

Table B-2 Differences between issue A and issue B

Change	Location	Affects
Replaced the PL352 component with the PL354 component.	Throughout the document.	r1p0
Updated references to the board, and board documentation, to Juno r1 and V2M-Juno r1.	Throughout the document.	r1p0
Added PCIe information.	• *ADP SoC block diagram* on page 2-2. • *Peripheral Component Interconnect Express (PCIe)* on page 2-5. • *ADP motherboard specification* on page 2-10. • *ADP board block diagram* on page 2-11.	r1p0
Updated Thin Links speed values.	*Thin Links SoC to FPGA prototyping interface* on page 2-6.	r1p0
Updated voltage values.	*Voltage domains* on page 2-8.	r1p0
Removed SODIMM.	*ADP motherboard specification* on page 2-10	r1p0

Table B-3 Differences between issue B and issue C

Change	Location	Affects
Changed the big processor from a Cortex®-A57 processor to a Cortex-A72 processor.	Throughout the document.	r2p0
Changed the voltage range of the Cortex-A53 processor.	*Voltage domains* on page 2-8	r2p0
Removed references to sockets where items are soldered.	*ADP motherboard specification* on page 2-10	r2p0
Removed the contents of the *Software Functional Description* chapter and replaced with links to: • The *ARM® Development Platforms* section of the *ARM Connected Community* website. • The *Juno ARM® Development Platform Getting Started Guide* on the ARM® Infocenter, http://infocenter.arm.com.	Chapter 3 *Software Functional Description*	r2p0