AMBA Design Kit (BP010)
Errata Notice

This document contains all errata known at the date of issue in releases up to and including revision r3p0 of AMBA Design Kit (ADK) -Perpetual

© Copyright ARM Limited 2008. All rights reserved.

Proprietary notice

Words and logos marked with ® or ™ are registered trademarks or trademarks of ARM Limited in the EU and other countries, except as otherwise stated below in this proprietary notice. Other brands and names mentioned herein may be the trademarks of their respective owners.

Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder.

The product described in this document is subject to continuous developments and improvements. All particulars of the product and its use contained in this document are given by ARM Limited in good faith. However, all warranties implied or expressed, including but not limited to implied warranties of merchantability, or fitness for purpose, are excluded.

This document is intended only to assist the reader in the use of the product. ARM Limited shall not be liable for any loss or damage arising from the use of any information in this document, or any error or omission in such information, or any incorrect use of the product.

Document confidentiality status

This document is Non Confidential.

Web address

http://www.arm.com/

© Copyright ARM Limited 2008. All rights reserved.

Feedback on the product

If you have any comments or suggestions about this product, contact your supplier giving:

- The product name
- A concise explanation of your comments.

Feedback on this document

If you have any comments on about this document, please send email to mailto:errata@arm.com giving:

- The document title
- The documents number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

© Copyright ARM Limited 2008. All rights reserved.

Contents

© Copyright ARM Limited 2008. All rights reserved.

Introduction

Scope

This document describes errata categorised by level of severity. Each description includes:

- the current status of the defect
- where the implementation deviates from the specification and the conditions under which erroneous behavior occurs
- the implications of the erratum with respect to typical applications
- the application and limitations of a 'work-around' where possible

Categorisation of Errata

Errata recorded in this document are split into three levels of severity:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

© Copyright ARM Limited 2008. All rights reserved.

Change Control

09 Jul 2008: Changes in Document v3

Page	Status	ID	Cat	Summary
19	New	551220	Cat 2	Bus-matrix CLI --connectivity command
18	New	543724	Cat 2	Command line interface support

18 Apr 2008: Changes in Document v2

Page	Status	ID	Cat	Summary
16	New	502136	Cat 2	Bus Matrix RTL render failure
17	New	504319	Cat 2	Bus Matrix RTL renders incorrectly

11 Aug 2007: Changes in Document v1

Page	Status	ID	Cat	Summary
9	New	331256	Cat 2	Downsizer64: AHB protocol error when translating 64-bit INCR16 bursts
21	New	340342	Cat 3	Location of perl in bus matrix script
20	New	338355	Cat 3	Clarification of Ahb2LiteSyncDn functionality
11	New	337443	Cat 2	Incorrect mask generation in 64 bit SyncUpBridge and SyncDnBridge
15	New	350856	Cat 2	BusMatrix InputStage.v missing sensitivity list items
13	New	338354	Cat 2	Arbiter3.v NextHmastLock logic reorder required
25	New	369515	Doc	Incorrect file location in DUI0183A User Guide
24	New	338353	Doc	Installation assumes $MODELTECH_ROOT is defined
23	New	326332	Doc	ARM DUI 0183D - User Guide: SDF back-annotation not supported in ADK
22	New	319007	Doc	TRM ARM DDI 0243A

© Copyright ARM Limited 2008. All rights reserved.

Errata Summary Table

The errata associated with this product affect product versions as below.

A cell shown thus **X** indicates that the defect affects the revision shown at the top of that column.

ID	Cat	Summary of Erratum	r2p0-00bet0	r3p0-00rel0	r3p0-00rel1	r3p0-00rel3
319007	Doc	TRM ARM DDI 0243A	X			
326332	Doc	ARM DUI 0183D - User Guide: SDF back-annotation not supported in ADK	X			
338353	Doc	Installation assumes $MODELTECH_ROOT is defined	X			
369515	Doc	Incorrect file location in DUI0183A User Guide	X			
331256	Cat 2	Downsizer64: AHB protocol error when translating 64-bit INCR16 bursts	X	X	X	X
337443	Cat 2	Incorrect mask generation in 64 bit SyncUpBridge and SyncDnBridge	X			
338354	Cat 2	Arbiter3.v NextHmastLock logic reorder required	X	X	X	X
350856	Cat 2	BusMatrix InputStage.v missing sensitivity list items	X			
502136	Cat 2	Bus Matrix RTL render failure			X	
504319	Cat 2	Bus Matrix RTL renders incorrectly			X	
543724	Cat 2	Command line interface support				X
551220	Cat 2	Bus-matrix CLI --connectivity command		X	X	X
338355	Cat 3	Clarification of Ahb2LiteSyncDn functionality	X			
340342	Cat 3	Location of perl in bus matrix script	X			

© Copyright ARM Limited 2008. All rights reserved.

Errata - Category 1

There are no Errata in this Category

© Copyright ARM Limited 2008. All rights reserved.

Errata - Category 2

331256: Downsizer64: AHB protocol error when translating 64-bit INCR16 bursts

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r2p0-00bet0,r3p0-00rel0,r3p0-00rel1,r3p0-00rel3, Open.

Description

The Downsizer translates an incoming 64-bit INCR16 burst into two outgoing 32-bit INCR16 bursts. The boundary detection logic used to insert a NONSEQ (non-sequential) transfer at the start of the second 32-bit INCR16 burst is incorrect: it uses the same calculation as is used for WRAP16 bursts, and so the NONSEQ transfer for the second 32-bit INCR16 burst is inserted when the address crosses the wrap boundary for a 64-bit WRAP16 (i.e. when the address is divisible by 0x80).

For example:

- a 64-bit INCR16 burst to address 0x1000 will be translated into a single 32-bit INCR16 burst, but which is 32 transfers long

- a 64-bit INCR16 burst to address 0x428 will be translated into two 32-bit INCR16 bursts, but the first will be 22 transfers long, and the second will be 10 transfers long

Therefore, this causes an AHB protocol violation on the 32-bit bus when translating any 64-bit INCR16 (unless the start address is divisible by 0x40 but not 0x80).

Note: The address generation for the 32-bit INCR16 bursts is not affected - the correct addresses are accessed

Note: Translation of 64-bit WRAP16 bursts is not affected - these are implemented correctly

Implications

This erratum is only applicable when the Downsizer is included in a system where a 64-bit INCR16 transfer can be generated and addressed to a slave which is accessed via the Downsizer.

If all slaves and/or AHB layers accessed via the Downsizer do not make use of the HBURST information of an AHB transfer then there is no effect from this erratum.

If an AHB layer accessed via the Downsizer uses HBURST information for (e.g.) arbitration purposes, then that layer may behave in an unpredictable manner when presented with a 32-bit INCR16 burst which continues for more than 16 transfers. You will need to check the components instantiated in your system for details.

If an AHB slave accessed via the Downsizer uses HBURST information for (e.g.) internal arbitration purposes, then that slave may behave in an unpredictable manner when presented with a 32-bit INCR16 burst which continues for more than 16 transfers. You will need to check the components instantiated in your system for details.

© Copyright ARM Limited 2008. All rights reserved.

Workaround

The translation of 64-bit INCR16 bursts can be forced to use 32-bit INCR (as opposed to INCR16) bursts. INCR allows bursts of arbitrary length, and so the protocol error is removed. To do this, edit process p_burst_map so that HBURSTmapped is set to INCR:

Change from:

```
`BUR_INCR16 : begin
 HBURSTmapped = `BUR_INCR16;
```

To:

```
`BUR_INCR16 : begin
 HBURSTmapped = `BUR_INCR;
```


© Copyright ARM Limited 2008. All rights reserved.

337443: Incorrect mask generation in 64 bit SyncUpBridge and SyncDnBridge

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

The 64 bit SyncUp and SyncDn bridges do not correctly implement WRAP16 address alignment for DoubleWord bursts as the WrapMask logic treats Word and DWord identically, resulting in BUSY cycle having wrong HADDR value at wrap point.

Implications

Due to the incorrect generation of a mask, the HADDRM address value may be incorrectly generated.

Workaround

The following files need to be modified:

- design\Ahb2AhbSyncDn\verilog\rtl_source\Ahb2LiteSyncDn64.v
- design\Ahb2AhbSyncDn\verilog\rtl_source\Ahb2LiteSyncUp64.v

For each file the code is currently as below:

```
`BUR_WRAP4 : begin
    case (iHSIZEM)
      `SZ_BYTE  : WrapMask  = 6'b111100;
      `SZ_HALF  : WrapMask  = 6'b111000;
      `SZ_WORD  : WrapMask  = 6'b110000;
      `SZ_DWORD : WrapMask  = 6'b100000;
      default   : WrapMask  = 6'b000000;
    endcase
  end
`BUR_WRAP8 : begin
    case (iHSIZEM)
      `SZ_BYTE  : WrapMask  = 6'b111000;
      `SZ_HALF  : WrapMask  = 6'b110000;
      `SZ_WORD  : WrapMask  = 6'b100000;
      `SZ_DWORD : WrapMask  = 6'b000000;
      default   : WrapMask  = 6'b000000;
    endcase
  end
`BUR_WRAP16 : begin
    case (iHSIZEM)
      `SZ_BYTE  : WrapMask  = 6'b110000;
      `SZ_HALF  : WrapMask  = 6'b100000;
```


© Copyright ARM Limited 2008. All rights reserved.

```
            `SZ_WORD  : WrapMask  = 6'b000000;
            `SZ_DWORD : WrapMask  = 6'b000000;
            default   : WrapMask  = 6'b000000;
          endcase
        end
```

and should be changed to:

```
      `BUR_WRAP4 : begin
          case (iHSIZEM)
            `SZ_BYTE  : WrapMask  = 7'b1111100;
            `SZ_HALF  : WrapMask  = 7'b1111000;
            `SZ_WORD  : WrapMask  = 7'b1110000;
            `SZ_DWORD : WrapMask  = 7'b1100000;
            default   : WrapMask  = 7'b1100000;
          endcase
        end
      `BUR_WRAP8 : begin
          case (iHSIZEM)
            `SZ_BYTE  : WrapMask  = 7'b1111000;
            `SZ_HALF  : WrapMask  = 7'b1110000;
            `SZ_WORD  : WrapMask  = 7'b1100000;
            `SZ_DWORD : WrapMask  = 7'b1000000;
            default   : WrapMask  = 7'b1000000;
          endcase
        end
      `BUR_WRAP16 : begin
          case (iHSIZEM)
            `SZ_BYTE  : WrapMask  = 7'b1110000;
            `SZ_HALF  : WrapMask  = 7'b1100000;
            `SZ_WORD  : WrapMask  = 7'b1000000;
            `SZ_DWORD : WrapMask  = 7'b0000000;
            default   : WrapMask  = 7'b0000000;
          endcase
        end
```


© Copyright ARM Limited 2008. All rights reserved.

338354: Arbiter3.v NextHmastLock logic reorder required

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r2p0-00bet0,r3p0-00rel0,r3p0-00rel1,r3p0-00rel3, Open.

Description

If a master asserts HLOCK before starting a new burst, at the same time as the data phase access from the same master's previous transfer returns a SPLIT response, the existing Arbiter design incorrectly prioritises the assertion of HLOCK over the receipt of a SPLIT response, and keeps this master granted for one additional clock cycle.

This allows the master to perform one further transfer before it does see that it is no longer granted, contrary to the AMBA 2 AHB specification requirements.

A SPLIT response requires the arbiter to remove HGRANT from that master immediately, and to keep the master not granted until such times as the slave which generated the SPLIT response signals the master can be re-granted by asserting the relevant HSPLIT bus bit.

The correct behaviour from the arbiter design would be to ignore the new assertion of HLOCK from the current master as soon as it samples HRESP=SPLIT, and to remove HGRANT immediately so that the master does not perform any further accesses.

Implications

The master which has just received a SPLIT response will remain granted on the bus for an additional transfer, contrary to the AMBA 2 AHB specification.

The SPLIT response tells the master to re-attempt the transfer which has just failed, so this extra transfer the master is granted for is likely to be repeating the original failed transfer to the original slave.

When a slave gives a SPLIT response to a master it will not expect any further requests from that specific master, so the slave, and therefore system behaviour following this additional illegal transfer is undefined, and could cause the slave or system to fail.

Workaround

In file Arbiter3.v, found at design/ElementsAHB/verilog/rtl_source, lines 536-538 are as below:

```
((AddrMaster == DataMaster) &&
((HRESP == `RSP_SPLIT) || (HRESP == `RSP_RETRY)) &&
LockedData == 1'b0) ? 1'b0 :
```

These need to be moved above the previous element in the "assign" statement so that they are inserted at line 527.

The complete "assign NextHmastLock" statement should then look like the

following code...

```
assign NextHmastLock = ForceNoGrant ? 1'b0 :
```


© Copyright ARM Limited 2008. All rights reserved.

```
                        HREADY ? Lock :
// next line added to hold HMASTLOCK high
// during LOCKed BUSY or IDLE, problem was
// that 2nd next line meant BUSY/IDLE at end
// of LOCKed burst dropped HMASTLOCK
(iHMASTLOCK &&
  ((HTRANS == `TRN_IDLE) ||
   (HTRANS == `TRN_BUSY))
  ) ? 1'b1 :
                        ((AddrMaster == DataMaster) &&
                         ((HRESP == `RSP_SPLIT) || (HRESP == `RSP_RETRY)) &&
                         LockedData == 1'b0) ? 1'b0 :
// next line added to drive HMASTLOCK when
// IDLE->NSEQ when HREADY low and same
// master, problem when new master wanted
// LOCKed accesses, caused oscillations on
// HGRANT and HMASTLOCK, hence Grant=Addr
((GrantMaster == AddrMaster) &&
  ((HTRANS == `TRN_IDLE) ||
   (HTRANS == `TRN_BUSY))
  ) ? Lock :
                        iHMASTLOCK;
```


© Copyright ARM Limited 2008. All rights reserved.

350856: BusMatrix InputStage.v missing sensitivity list items

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

In file
`design/BusMatrix/verilog/rtlsource/InputStage.v`

There are 2 missing signals from the sensitivity list at line 283.

The signals are: HMASTERS and RegMaster.

The line reads:

```
always @ (PendTranReg or HSELS or HTRANSS or HADDRS or HWRITES or
            HSIZES or HBURSTS or HPROTS or HMASTLOCKS or RegAddr or
            RegWrite or RegSize or RegBurst or RegProt or RegMastlock)
```

and should read

```
always @ (PendTranReg or HSELS or HTRANSS or HADDRS or HWRITES or HSIZES or
            HBURSTS or HPROTS or HMASTERS or HMASTLOCKS or RegAddr or
            RegWrite or RegSize or RegBurst or RegProt or RegMaster or
RegMastlock)
```

Implications

With these signals not appearing in the RTL sensitivity list it could mean that the HMASTERM outputs of the BusMatrix would not be updated in the correct HCLK cycle. The design will synthesise to the correct logic, however in simulation the BusMatrix HMASTERM outputs wont be updated at the correct HCLK cycle.

Only system designs using the HMASTER signals coming out of the BusMatrix would be affected and only if the HMASTERS inputs change combinatorially slower than the other inputs to this process.

Workaround

Modify design/BusMatrix/verilog/rtlsource/InputStage.v as detailed above

© Copyright ARM Limited 2008. All rights reserved.

502136: Bus Matrix RTL render failure

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r3p0-00rel1, Fixed in r3p0-00rel3.

Description

When there are multiple masters/slaves and the arbitration scheme is set to round robin, if one or more of the master interfaces are sparsely connected to a single slave interface, the RTL generation scripts will fail.

Implications

If it has been possible to successfully run the render scripts, then this problem is not present and therefore there are no further implications.

Workaround

Use r3p0-00rel3 or later

© Copyright ARM Limited 2008. All rights reserved.

504319: Bus Matrix RTL renders incorrectly

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r3p0-00rel1, Fixed in r3p0-00rel3.

Description

Corner case configurations can cause the Bus Matrix render engine to produce invalid Verilog that will fail to load into a simulator.

Implications

If it has been possible to load the generated Verilog into a simulator, then this problem is not present and therefore there are no further implications.

Workaround

Use r3p0-00rel3 or later

© Copyright ARM Limited 2008. All rights reserved.

543724: Command line interface support

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r3p0-00rel3, Open.

Description

In version 1.77 of BuildBusMatrix.pl, the command-line method of design entry can malfunction.

For example:

```
./BuildBusMatrix.pl --inports=2 --outports=2 --connectivity='SI0=MI{1}:SI1=MI{0,1}' \
--verbose --overwrite
```

It has the following effects:

1. Warnings from Perl about variable initialisation and pattern match failure.

2. The Verilog of the matrix decoder does not render correctly.

The defect is fixed in file version 1.79.

Implications

None

Workaround

Either revert back to a previous release of ADK or use AMBA Designer to configure the AHB Bus Matrix. Alternately contact support for Patch BP010_20080527_01.

© Copyright ARM Limited 2008. All rights reserved.

551220: Bus-matrix CLI --connectivity command

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 2, Present in: r3p0-00rel0,r3p0-00rel1,r3p0-00rel3, Open.

Description

When using the command line interface to render an AHB Bus Matrix it is possible that a parsing error will result in an incorrectly connected matrix. In the example below, port 0 is should be connected but is incorrectly omitted.

```
  BuildBusMatrix.pl --inports=2 --outports=2 --connectivity='SI0=MI{0,1}:SI1=MI{0,1}' --
verbose --overwrite
```

This is only a concern when specifying connectivity using the `--connectivity=` argument

Implications

The AHB Bus Matrix may be generated without the expected connectivity to port 0. This should be obvious from the error messages generated as below

```
Interface <portID> has no connectivity mapping and is isolated!
```

Workaround

Either use AMBA Designer to render the AHB bus Matrix or include a backslash in front of each set of braces.

```
  BuildBusMatrix.pl --inports=2 --outports=2 --connectivity='SI0=MI{0,1}:SI1=MI{0,1}' --
verbose --overwrite
```

would therefore become

```
  BuildBusMatrix.pl --inports=2 --outports=2 --connectivity='SI0=MI\{0,1}:SI1=MI\{0,1}' --
verbose --overwrite
```


© Copyright ARM Limited 2008. All rights reserved.

Errata - Category 3

338355: Clarification of Ahb2LiteSyncDn functionality

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 3, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

Inline comments in the RTL of the Ahb2LiteSyncDn module within the Ahb2AhbSyncDn bridge are unclear. A clarification is below:

The Ahb2LiteSyncDn module inside this Bridge implements an AHB Master on the destination AHB bus, and it has been designed to continue a fixed length burst when an ERROR is seen.

Implications

None

Workaround

None

© Copyright ARM Limited 2008. All rights reserved.

340342: Location of perl in bus matrix script

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Cat 3, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

The file BuildBusMatrix.pl at design\BusMatrix\verilog specifies the location of Perl as:

```
#!/usr/local/bin/perl -w
```

It should be noted that this location may not be correct in some installations.

If Perl is installed at a different location, the file should be modified accordingly.

Implications

The incorrect Perl location will prevent the script from running correctly.

Workaround

Place a link at /usr/local/bin/perl pointing to your installation of the perl executable

© Copyright ARM Limited 2008. All rights reserved.

Errata - Documentation

319007: TRM ARM DDI 0243A

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Doc, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

In the ADK Technical Reference Manual, section 3.8.6, the signal descriptions refer to HREADYMx.

In the RTL, this signal is actually named HREADYMUXMx.

Implications

None

Workaround

None

© Copyright ARM Limited 2008. All rights reserved.

326332: ARM DUI 0183D - User Guide: SDF back-annotation not supported in ADK

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Doc, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

The AMBA Design Kit User Guide, ARM DUI 0183A, section 2.3.5 on page 9 should be deleted.

Running the integration tests on the synthesized netlist with SDF back-annotation is not supported in ADK.

Implications

None

Workaround

None

© Copyright ARM Limited 2008. All rights reserved.

338353: Installation assumes $MODELTECH_ROOT is defined

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Doc, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

The ADK installation assumes the presence of an environment variable $MODELTECH_ROOT.

Implications

It is not possible to initiate the simulation environment without this variable correctly set

Workaround

If this is not set in the Modelsim tools installation, it will need to be manually set to `$MODEL_TECH/..`

© Copyright ARM Limited 2008. All rights reserved.

369515: Incorrect file location in DUI0183A User Guide

Status

Affects: product AMBA Design Kit (ADK) -Perpetual.

Fault status: Doc, Present in: r2p0-00bet0, Fixed in r3p0-00rel0.

Description

The "AMBA Design Kit User Guide" (ARM DUI 0183A) page 2-6 refers to a file:
`$ADK/design/TBEasy_FRBM/frbmtests/IntegrationTest.fri`

This should instead be
`$ADK/design/TBEasy_FRBM/integration/frbmtests/IntegrationTest.fri`

Implications

None

Workaround

None

© Copyright ARM Limited 2008. All rights reserved.

Errata – Driver Software

There are no Errata in this Category

© Copyright ARM Limited 2008. All rights reserved.