PrimeCell® Infrastructure AMBA™ 2 AHB™ to AMBA 3 AXI™ Bridges (BP136)

Revision: r0p1

Technical Overview

ARM®

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Release Information

The following changes have been made to this book.

Change History

Date	Issue	Confidentiality	Change
16 May 2005	A	NonConfidential	First release for r0p0
08 Februrary 2006	B	NonConfidential	Update for r0p1, sideband signal information and minor corrections.

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

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PrimeCell Infrastructure AMBA 2 AHB to AMBA 3 AXI Bridges (BP136) Technical Overview

Chapter 1
PrimeCell® Infrastructure AMBA™ 2 AHB™ to AMBA 3 AXI™ Bridges (BP136)

This technical overview describes the functionality of the AHB to AXI bridges in the following sections:

1.1 About the AHB to AXI bridges

The AMBA™ 2 AHB™ to AMBA 3 AXI™ bridges enable AHB masters to communicate with AXI slaves or interconnects if the clock and reset signals are common. The bridge is available in three variants to support the following interfaces:

- ARM11 AHB-Lite master bus
- AHB master bus
- post-decoder AHB slave bus.

The bridges share the following features:

- 64-bit or 32-bit data bus width
- single active transaction
- transaction control information is preserved between bus domains
- fixed-length AHB bursts are converted into AXI bursts of the same length
- undefined-length bursts are converted into single transfers
- minimal latency overhead, assuming that the AXI slave accepts and presents data/response with zero wait states:
  - read latency overhead = 1+0+0, initial, inter-beat, last beat
  - write latency overhead = 0+0+1.
- **AxPROT[1]** is tied low to make the bridge secure
- common clock and reset domains
- HDL code is supplied as Verilog
- area is approximately 1000 NAND2X1 gate equivalents.

Figure 1 shows a typical AHB to AXI bridge used in its simplest configuration.

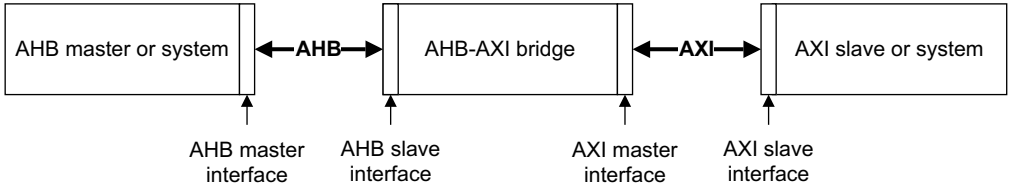

Figure 1-1 Figure 1 AHB to AXI bridge

1.1.1 AXI master interface attributes

Table 1-1 lists the AXI master interface attributes.

Table 1-1 AXI master interface attributes

Attribute	Description	Value
Combined issuing capability	The maximum number of active transactions that a master can generate	1
Write ID capability	The maximum number of different **AWID** values that a master can generate for all active write transactions at any one time	1
Write ID width	The number of bits in the **AWID**, **WID**, and **BID** buses	0
Read ID capability	The maximum number of different **ARID** values that a master can generate for all active read transactions at any one time	1
Read ID width	The number of bits in the **ARID** and **RID** buses	0

1.2 Functional description

The following sections provide a brief functional description of each bridge type:

- ARM11 AHB-Lite master bus to AXI
- AHB master bus to AXI
- AHB slave bus to AXI on page 6.

1.2.1 ARM11 AHB-Lite master bus to AXI

The ARM11 AHB-Lite to AXI bridge, `A11AhbLiteMToAxi`, enables an ARM11 AHB-Lite master to connect to an AXI slave or interconnect. ARM11 AHB-Lite masters support AHB-Lite with the additional features of unaligned accesses, exclusive accesses, and extended caching control information.

The AXI protocol supports all these features, and so they are preserved across the bridge. The bridge does not modify data paths, so you must route these directly between the AHB and AXI domains. Figure 1-2 shows an example application.

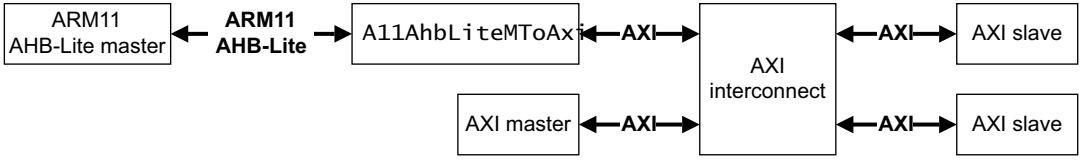

Figure 1-2 ARM11 AHB-Lite master to AXI interconnect example

1.2.2 AHB master bus to AXI

Figure 3 shows how the AHB master bus to AXI bridge, `AhbMToAxi`, enables a full AHB master to connect to an AXI slave or interconnect.

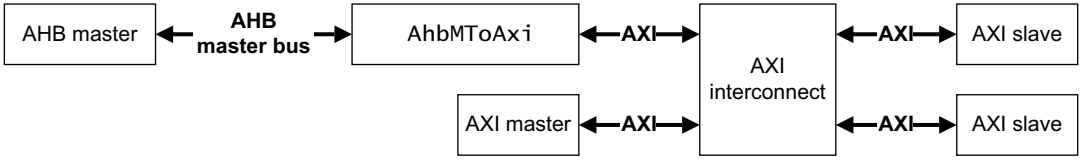

Figure 1-3 AHB master to AXI interconnect example

1.2.3 AHB slave bus to AXI

The AHB slave bus to AXI bridge, `AhbSToAxi`, enables an AHB subsystem to connect to an AXI slave or interconnect. The AHB slave bus is the post-decoder bus that includes **HREADY**, **HREADYOUT**, and **HSEL**. Figure 4 shows an example application.

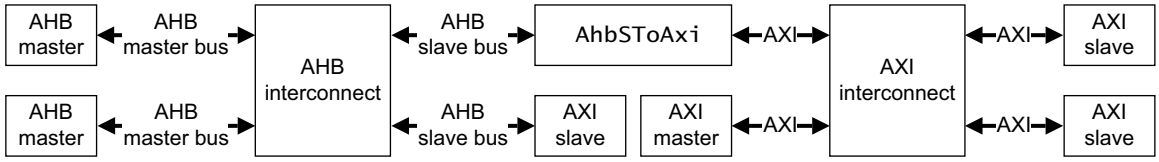

Figure 1-4 AHB slave to AXI interconnect example

The *PrimeCell Infrastructure AMBA 2 AHB to AMBA 3 AXI Bridges (BP136) Design Manual* describes how you can connect an AHB-Lite master to the `AhbSToAxi` by tying off certain AHB signals, and setting a parameter.

1.3 Physical data

Physical data is provided in:

- *AC characteristics*
- *Gate count*

1.3.1 AC characteristics

The AHB to AXI bridges are structured so that all AXI outputs are registered except the data buses. The data buses bypass the bridge. The AHB outputs, HRESP and HREADY, are combinatorial from AXI inputs. If you require timing isolation between the AHB and AXI domains, use separate isolating bridges or registers on either the AHB or AXI buses. It is usually more efficient on the AXI bus, where you can use a register slice, PrimeCell Infrastructure AMBA 3 AXI Register Slice (BP130), to register the AXI inputs.

The AHB to AXI bridge conforms to the following timing parameters:

- All inputs are valid at 60% of the clock cycle.
- AXI outputs are valid within 20% of the clock cycle.
- AHB outputs are valid within 75% of the clock cycle. The budget for the combinatorial logic is 15% of the cycle.

The timing characteristics are confirmed by performing synthesis on the block using the slow-slow process point of the Artisan SAGE HS library for the TSMC CL013G process at a target speed of 200MHz.

1.3.2 Gate count

Table 3 lists the estimated gate counts in the library that *AC characteristics* specifies.

Table 1-2 Gate counts

Bridge	Approximate NAND2X1 equivalents
ARM11 AHB-Lite master to AXI	1200
AHB master bus to AXI	1100
AHB slave bus to AXI	1200

Note

The gate count estimate does not include scan logic.

1.4 Signal descriptions

The AHB to AXI bridge signals are standard AMBA AXI and AHB signals. These are described in:

- the *AMBA AXI Protocol Specification*
- the *AMBA Specification*.

Note

User signals are provided as sideband signals to the standard AXI and AHB interfaces.

The following figures show the connections:

- Figure 1-5 on page 1-8 shows the ARM11 AHB-Lite master bus to AXI bridge signal connections
- Figure 1-6 on page 1-9 shows the AHB master bus to AXI bridge signal connections
- Figure 1-7 on page 1-10 shows the AHB slave bus to AXI bridge signal connections.

Note

In the three figures, **DATA_MAX** is the maximum high index of the data bus vectors, for example, 63 or 31, depending on the bus widths. A calculated parameter, STRB_MAX, controls the strobe bus width.

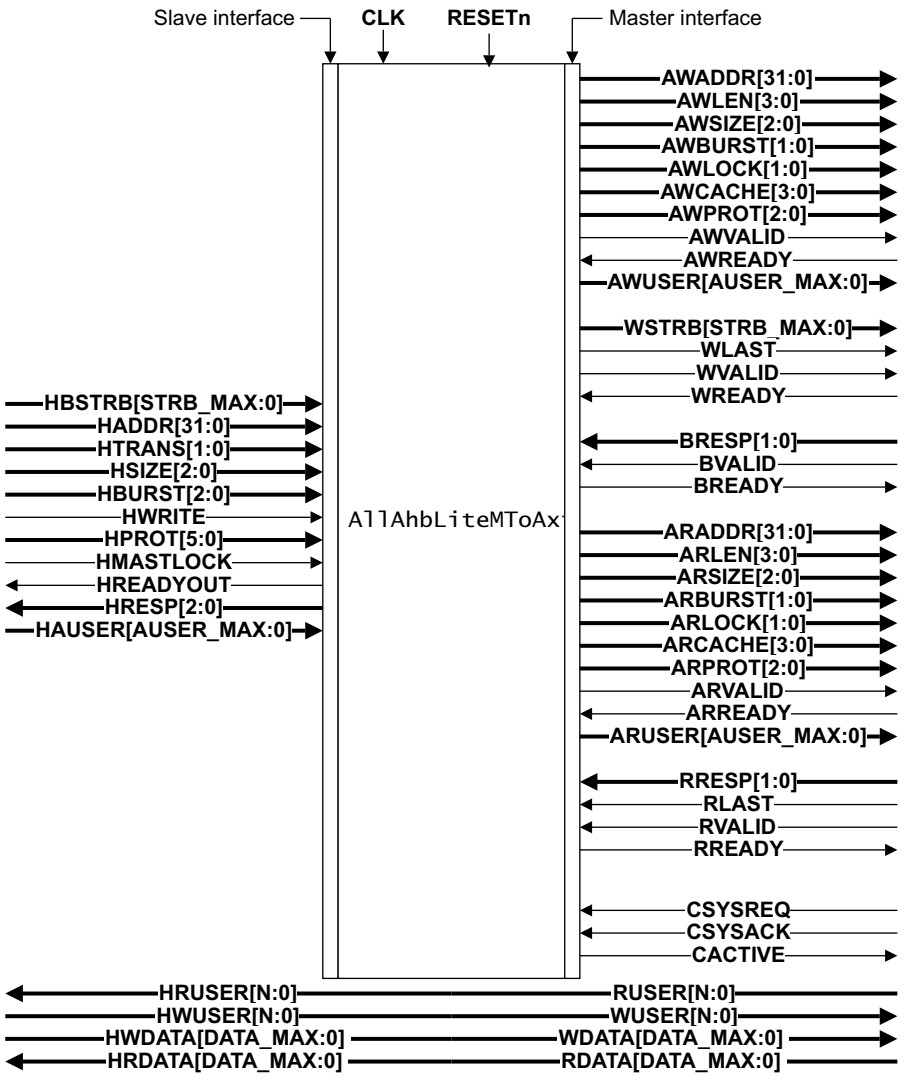

Figure 1-5 ARM11 AHB-Lite master bus to AXI bridge signal connections

Note

- The value of N in the bus widths is not defined in the bridge.
- The **HWUSER**, **HRUSER**, **WUSER**, **RUSER**, **RDATA**, **WDATA**, **HRDATA**, and **HWDATA** signals all bypass the bridge.

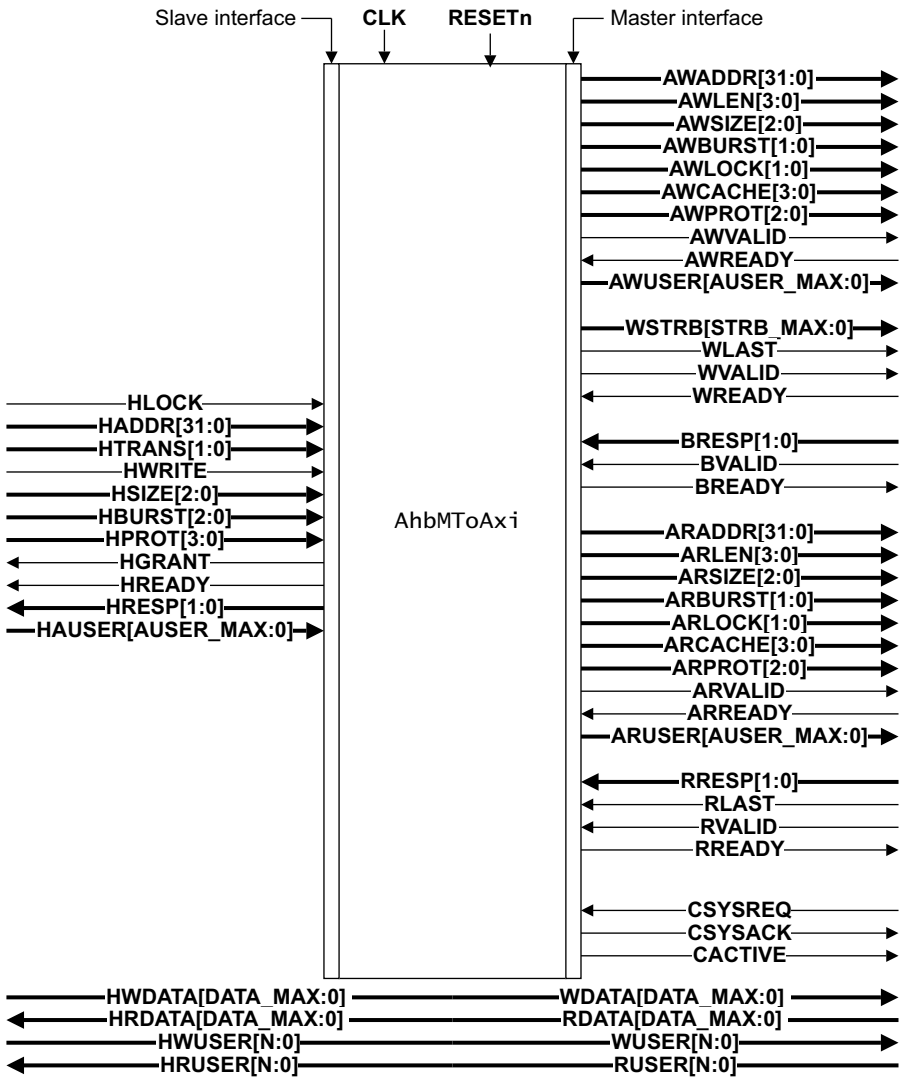

Figure 1-6 AHB master bus to AXI bridge signal connections

Note

- The value of N in the bus widths is not defined in the bridge.
- The **HWUSER**, **HRUSER**, **WUSER**, **RUSER**, **RDATA**, **WDATA**, **HRDATA**, and **HWDATA** signals all bypass the bridge.

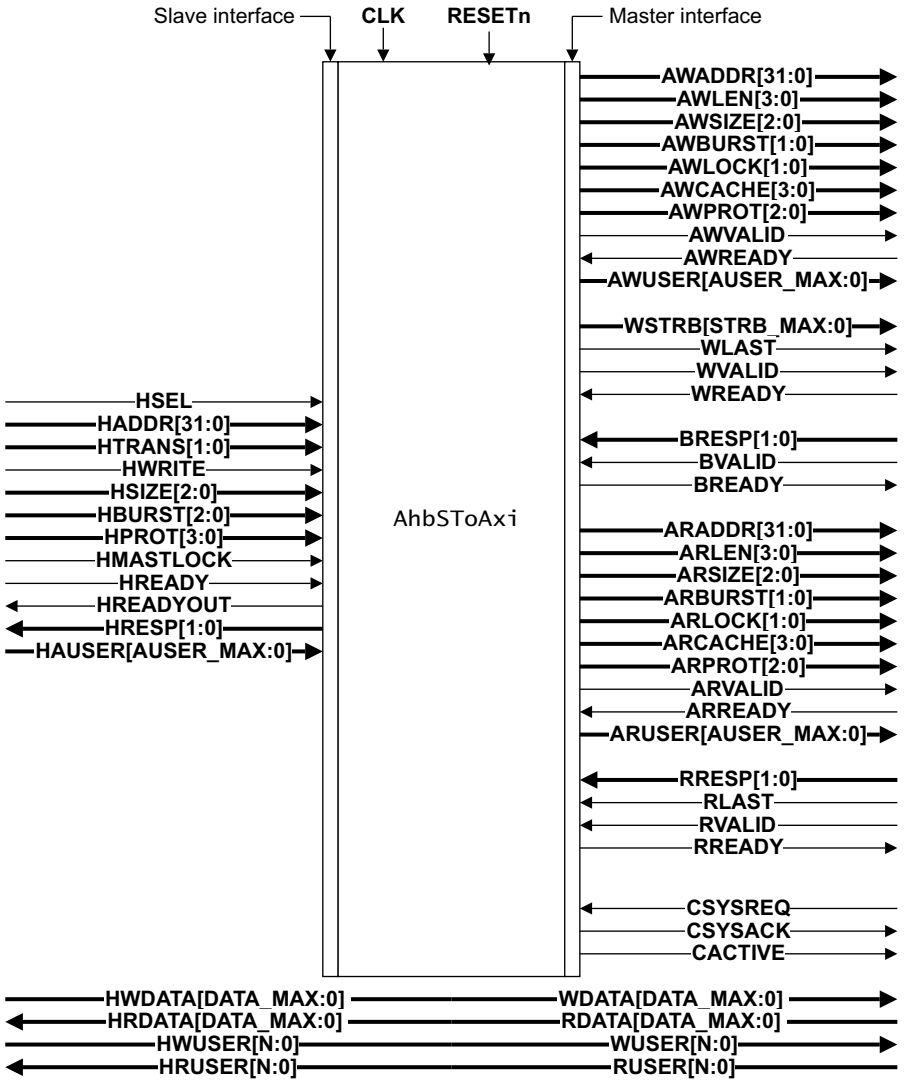

Figure 1-7 AHB slave bus to AXI bridge signal connections

Note

- The value of N in the bus widths is not defined in the bridge.
- The **HWUSER**, **HRUSER**, **WUSER**, **RUSER**, **RDATA**, **WDATA**, **HRDATA**, and **HWDATA** signals all bypass the bridge.

