Arm Neoverse N2 Automotive Reference Design

Revision: r0p0

Hardware Technical Overview

Non-Confidential

Issue 01

107916

Arm Neoverse N2 Automotive
Hardware Technical Overview

Release information

Document history

Issue	Date	Confidentiality	Change
0000-01	25-JAN-2023	Non-Confidential	Initial release for r0p0

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(LES-PRE-20349)

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Inclusive language commitment

Arm values inclusive communities. Arm recognizes that we and our industry have used language that can be offensive. Arm strives to lead the industry and create change.

Contents

1. Introduction

1.1. Product revision status

The rxpy identifier indicates the revision status of the product described in this book, for example, r1p2, where:

rx identifies the major revision of the product, for example, r1.

py identifies the minor revision or modification status of the product, for example, p2.

1.2. Intended audience

The document is intended for software, hardware, and system engineers who are planning to evaluate and use the Neoverse™ N2 Automotive Reference stack and would like to understand the architecture of the Neoverse™ N2 Automotive Reference Design which is the underlying hardware of the stack.

1.3. Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: https**://developer.arm.com/glossary.**

Typographical conventions

Convention	Use
italic	Citations.
bold	Interface elements, such as menu names. Terms in descriptive lists, where appropriate.
`monospace`	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace` **`bold`**	Language keywords when used outside example code.
`monospace underline`	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

Convention	Use
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Terms that have specific technical meanings as defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.
Caution	Recommendations. Not following these recommendations might lead to system failure or damage.
Warning	Requirements for the system. Not following these requirements might result in system failure or damage.
Danger	Requirements for the system. Not following these requirements will result in system failure or damage.
Note	An important piece of information that needs your attention.
Tip	A useful tip that might make it easier, better, or faster to perform a task.
Remember	A reminder of something important that relates to the information you are reading.

Danger

1.4. Useful resources

This document contains information that is specific to this product. See the following resources for other relevant information.

- Arm Non-Confidential documents are available on developer.arm.com/documentation. Each document link in the tables below provides direct access to the online version of the document.
- Arm Confidential documents are available to licensees only through the product package.

Arm products	Document ID	Confidentiality

Arm architecture and specifications	Document ID	Confidentiality
Arm Neoverse N2 reference design Technical Overview	102337_0000_04_en	*Non-Confidential*

Non-Arm resources	Document ID	Organization

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Adobe PDF reader products can be downloaded at **http://www.adobe.com**.

2. Overview

The document describes the underlying hardware architecture of the Neoverse™ N2 Automotive Reference Stack.

The document is intended for software, hardware, and system engineers who are planning to evaluate and use the Neoverse™ N2 Automotive Reference stack. The emphasis is to understand the hardware architecture of the Neoverse™ N2 Automotive Reference design.

Neoverse™ N2 Automotive reference design (RD-N2-Automotive) introduces the concept of a high-performance Application Processor (Primary Compute) system augmented with a Cortex-R based safety island. The safety Island is for scenarios where additional system safety monitoring is required. The Reference Design also includes a Runtime Security Subsystem used for Secure boot services used by the different elements.

Neoverse™ N2 reference design (RD-N2) represents the Primary Compute subsystem to be augmented. RD-N2-Automotive is developed incrementally on top of RD-N2.

This document must be read together with the Arm Neoverse™ N2 reference design (RD-N2) Technical Overview. It highlights the overall system topology and only describes the incremental updates on functions and programming models of RD-N2.

3. System Topology

RD-N2-Automotive consists of four main subsystems.

3.1. Subsystems in RD-N2-Automotive

They are:

- Runtime Security Subsystem
  - New in RD-N2-Automotive
- Cortex-R82 based safety island subsystem
  - New in RD-N2-Automotive
- System Control Processor subsystem
  - Originally part of RD-N2
- Primary compute subsystem
  - Originally part of RD-N2
  - New NIC450 Switch(es) added

3.2. System architecture

In RD-N2 technical overview, the system is partitioned into functional blocks. The following figure intends to keep the RD-N2 functional blocks and adds the allocation them into the four subsystems in RD-N2-Automotive.

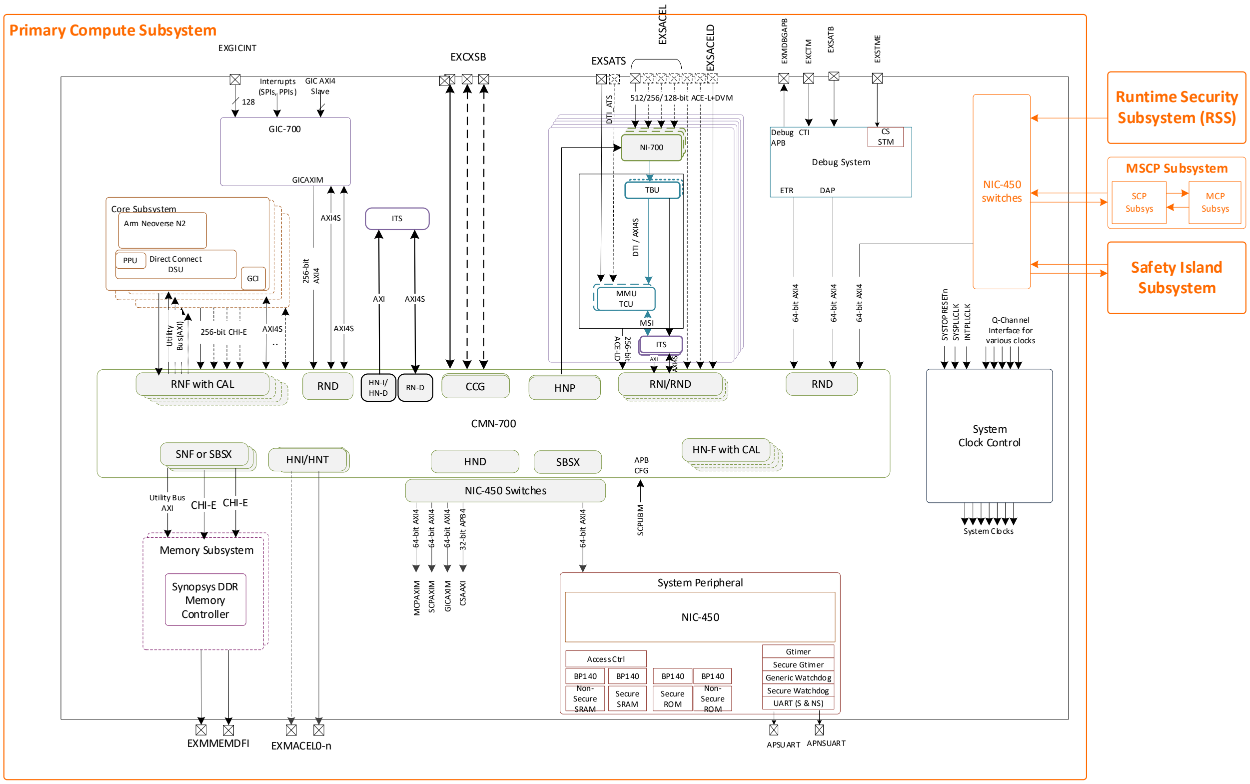

Figure 3-1 RD-N2-Automotive System Topology

4. Functional Description

This section describes the additional functions introduced in RD-N2-Automotive comparing to RD-N2.

4.1. Power Domain updates

All the newly added components including RSS and the safety island subsystem are added in the AONTOP power domain.

PD_CPU<n> power domains are not changed.

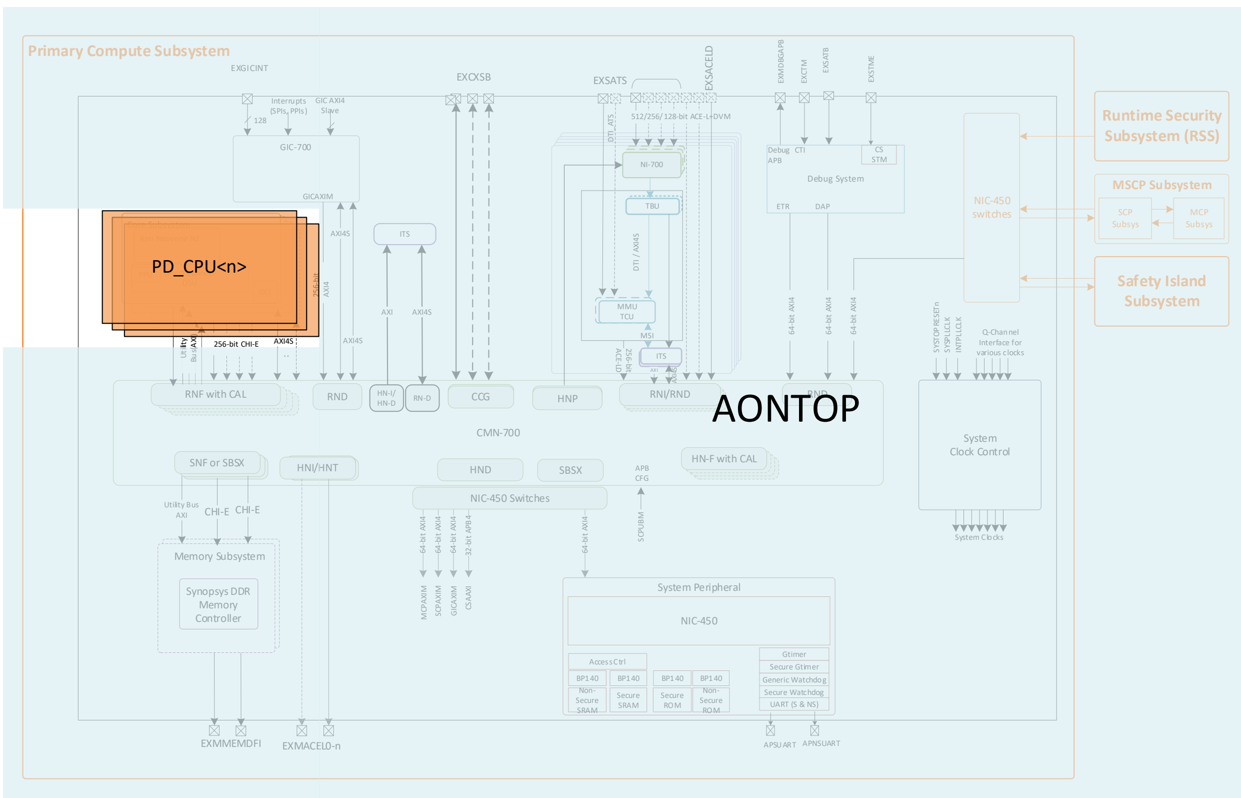

Figure 4-1 Updated Power Domains

4.2. Clocks updates

The newly added RSS, the safety island subsystem and the NIC 450 switch will use same SYSPLLCLK as source clock and run synchronously.

4.3. Reset Domain updates

RSS and the safety island subsystem have separate reset domains.

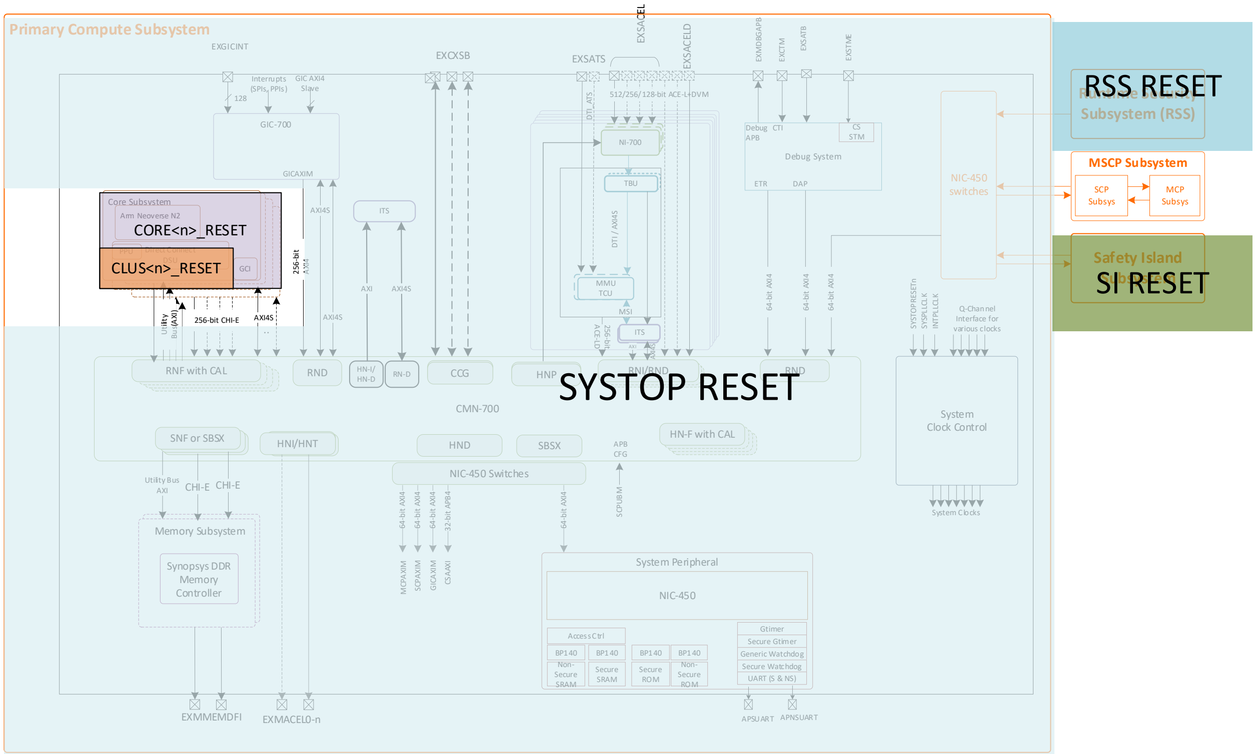

Figure 4-2 Updated Reset Domains

RSS and the safety island subsystem have separate reset domains.

4.4. System Boot

With the additions of two new subsystems, the boot flow of RD-N2-Automotive is different to RD-N2.

The details of the booting flow from software perspective can be found in the software documentation https://rd-n2-automotive.docs.arm.com.

RD-N2-Automotive supports the secure boot.

Note

Note that in RD-N2-Automotive, MCP in MSCP subsystem is not used therefore not described in boot flow.

To support secure boot, the compute subsystem additionally provides:

- RSS designed to function as root of Trust
-

4.4.1. Boot flow overview

This section provides an overview of the boot flow.

To boot-up, the assumption is that the compute subsystem must be supplied with voltage and input clocks before the `RSSRESETn` is de-asserted:

1. RSS comes out of reset and start booting from its boot ROM.
2. RSS loads SCP boot image from external flash to boot RAM of SCP.
3. RSS authenticates the SCP boot image.
4. RSS powers up SCP.
5. SCP comes out of reset and start booting from its boot RAM.
6. SCP completes booting and informs RSS via MHU.
7. RSS loads boot image of safety island from external flash to the boot RAM of the safety island.
8. RSS authenticates the boot image of the safety island.

   Steps 7-8 are repeated for each of the additional safety island clusters, if present.
9. RSS requests SCP to power on safety island.
10. SCP power on safety island.
11. Safety Island informs RSS that booting is complete.
12. RSS loads AP_BL1 boot image of the first core in Primary Compute to boot RAM of Primary Compute.
13. RSS authenticates the AP_BL1 boot image.
14. RSS request SCP to power on first core in Primary Compute
15. The powered-up core starts booting from boot RAM of Primary compute and execute AP_BL1.

Note

The software architecture defines the rest of the software boot flow steps.

4.5. Security

RSS is the root of trust therefore treated as inherently Trusted and Secure.

SI is treated as non-secure with respect to the rest of the system.

4.6. MHU based inter-subsystem communication

MHU components are required to enable MHU-based inter-subsystem communications. With the addition of RSS and safety island subsystem, more MHU components are added in the RD-N2-Automotive.

MHU components are considered part of the system peripherals in each subsystem and have their programming register space in the corresponding memory maps.

Figure 4-3 Additional MHUs comparing to RD-N2 shows the additional MHU components in each subsystem.

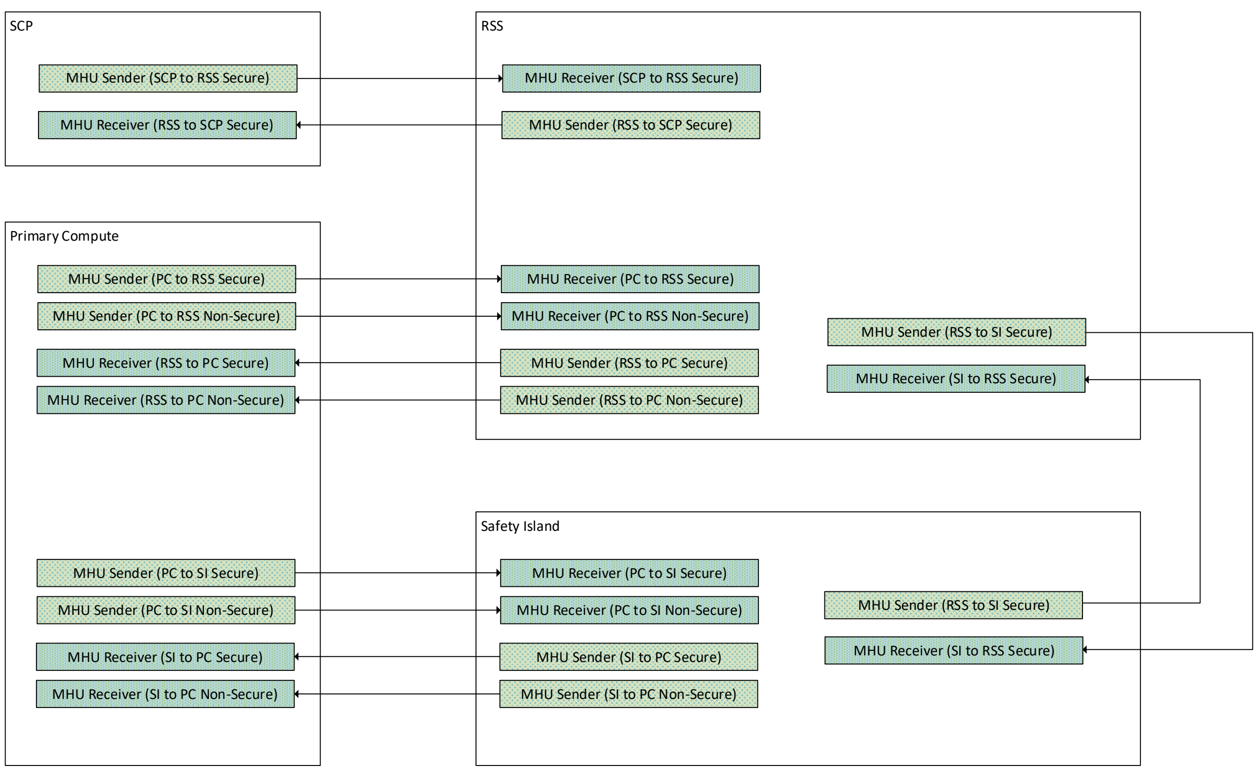

Figure 4-3 Additional MHUs comparing to RD-N2

5. Programming Model

This section describes the updates to the RD-N2 programming model.

5.1. About the Programming Model

The updates of the programming model contain:

1. Addition of MHU components.
2. Additional access from SCP to safety island for power control

5.2. Memory Maps

The memory maps are the updates to the RD-N2 memory maps so only the updated entries are shown for each subsystem.

5.2.1. Primary Compute Memory Map update

This table lists all the updated entries with respect to the RD-N2 AP Memory Map.

Table 1 Primary Compute Memory Map Update

Start address	End address	Size	Description	Access Control
0x00_2AA2_0000	0x00_2AA2_FFFF	64 KB	PC->RSS Non-secure MHU Send frame	Non-Secure
0x00_2AA3_0000	0x00_2AA3_FFFF	64 KB	RSS->PC Non-secure MHU Receive frame	Non-Secure
0x00_2AA4_0000	0x00_2AA4_FFFF	64 KB	PC->RSS secure MHU Send frame	Secure
0x00_2AA5_0000	0x00_2AA5_FFFF	64 KB	RSS->PC secure MHU Receive frame	Secure
0x00_2AAA_0000	0x00_2AAA_FFFF	64 KB	AP->SI CL0 Non-secure MHU send frame	Non-Secure
0x00_2AAB_0000	0x00_2AAB_FFFF	64 KB	SI CL0->AP Non-secure MHU Receive frame	Non-Secure

Start address	End address	Size	Description	Access Control
0x00_2AAC_0000	0x00_2AAC_FFFF	64 KB	AP->SI CL0 Secure MHU send frame	Secure
0x00_2AAD_0000	0x00_2AAD_FFFF	64 KB	SI CL0->AP Secure MHU Receive frame	Secure

5.2.2. SCP Memory Map update

Table 2 SCP Memory Map update only

Start address	End address	Size	Description	Access Control
0x4582_0000	0x4582_FFFF	64 KB	SCP -> RSS Secure MHU Send Frame	Secure
0x4583_0000	0x4583_FFFF	64 KB	RSS -> SCP Secure MHU Receive Frame	Secure
0x5008_0000	0x5008_FFFF	64 KB	Safety island power control register Targeting address on SI memory map is (0x00_2A60_0000 to 0x00_2A60_FFFF)	Secure
0x5600_0000	0x563F_FFFF	4 MB	Safety Island Utility Bus of R82 cluster. Targeting address on SI memory map is (0x00_2800_0000 to 0x00_283F_FFFF)	Secure
0x5800_0000	0x5FFF_FFFF	128 MB	NVM in Safety island Memory map. Targeting address on SI memory map is (0x00_6000_0000 to 0x00_67FF_FFFF)	Secure

5.2.3. MHU register description

Same with RD-N2 Technical Overview.

Please refer to RD-N2 section 7.4.7

5.2.4. MHU in RSS memory map

Table 3 MHU register locations in RSS Memory Map

Start address	End address	Size	Description	Access Control
0x4010_8000	0x4010_8FFF	4KB	RSS to PC Secure Send Frame	Secure
0x4010_9000	0x4010_8FFF	4KB	PC to RSS Secure Receive Frame	Secure
0x4010_A000	0x4010_AFFF	4KB	RSS to PC Non-Secure Send Frame	Non-Secure
0x4010_B000	0x4010_BFFF	4KB	PC to RSS Non-Secure Receive Frame	Non-Secure
0x4010_C000	0x4010_CFFF	4KB	RSS to SCP Secure Send Frame	Secure
0x4010_D000	0x4010_DFFF	4KB	SCP to RSS Secure Receive Frame	Secure
0x4011_0000	0x4011_0FFF	4KB	RSS to SI Secure Send Frame	Secure
0x4011_1000	0x4011_1FFF	4KB	SI to RSS Secure Receive Frame	Secure

5.2.5. MHU in SI memory map

Table 4 MHU register locations in SI Memory Map

Start address	End address	Size	Description	Access Control
0x00_2AA3_0000	0x00_2AA3_FFFF	64KB	SI_PC_0_MHUV2_RCV_S	Secure
0x00_2AA2_0000	0x00_2AA2_FFFF	64KB	SI_PC_0_MHUV2_SEND_S	Secure
0x00_2AA1_0000	0x00_2AA1_FFFF	64KB	SI_RSS_0_MHUV2_RCV_S	Secure
0x00_2AA0_0000	0x00_2AA0_FFFF	64KB	SI_RSS_0_MHUV2_SEND_S	Secure
0x00_2A93_0000	0x00_2A93_FFFF	64KB	SI_PC_0_MHUV2_RCV_NS	Non-Secure
0x00_2A92_0000	0x00_2A92_FFFF	64KB	SI_PC_0_MHUV2_SEND_NS	Non-Secure

5.3. Interrupt Maps

The interrupts maps are the updates to the RD-N2 interrupts maps so only the updated entries are shown for each subsystem.

5.3.1. Primary Compute Interrupt Map update

This table lists all the updated entries with respect to the RD-N2 AP Interrupt Map.

Table 5 Primary Compute Interrupt Map updates

Interrupt ID (offset from CHIP_START_INTID)	Interrupt Name	Description	Trigger	Polarity
33	RSS2APMHU_NS	RSS to PC MHU Non-Secure Interrupt from the receiver frame	Level	Active-HIGH
34	RSS2APMHU_S	RSS to PC MHU Secure Interrupt from the receiver frame	Level	Active-HIGH
35	SICL02APMHU_NS	SI to PC MHU Non-Secure Interrupt from the receiver frame	Level	Active-HIGH
36	SICL02APMHU_S	SI to PC MHU Secure Interrupt from the receiver frame	Level	Active-HIGH

5.3.2. SCP Interrupt Map update

Table 6 SCP Interrupt Map update

Interrupt ID	Interrupt Name	Description	Trigger	Polarity
85	RSS2SCP MHU Secure Int	RSS2SCP MHU Secure Interrupt	Level	ACTIVE-High
86	RSS2SCP MHU Non-secure Int	RSS2SCP MHU Non-Secure Interrupt	Level	ACTIVE-High

Appendix A. Revisions

This appendix describes the technical changes between released issues of this document.

Table A-1: Issue 01

Change	Location

Table A-2: Differences between issue 01 and issue 02

Change	Location