ARM®

RealView® Development Suite Glossary

The items in this glossary are listed in alphabetical order, with any symbols and numerics appearing at the end.

AAPCS *See* Procedure Call Standard for the ARM® Architecture.

ABI for the ARM Architecture (base standard) (BSABI)
The ABI for the ARM Architecture is a collection of specifications, some open and some specific to ARM architecture, that regulate the inter-operation of binary code in a range of ARM architecture-based execution environments. The base standard specifies those aspects of code generation that must be standardized to support inter-operation and is aimed at authors and vendors of C and C++ compilers, linkers, and runtime libraries.

Adaptive clocking A technique used by RealView ICE where it sends out a clock signal and then waits for the returned clock before generating the next clock pulse. The technique enables the RealView ICE run control unit to adapt to differing signal drive capabilities and differing cable lengths.

ADS *See* ARM Developer Suite™.

Advanced Microcontroller Bus Architecture (AMBA®)
On-chip communications standard for high-performance 32-bit and 16-bit embedded microcontrollers.

AMBA *See* Advanced Microcontroller Bus Architecture.

Angel A debug monitor that enables you to develop and debug applications running on hardware that is based on an ARM architecture-based processor. Angel can debug applications running in either ARM state or Thumb state.

armar The ARM librarian.

armasm The ARM assembler.

armcc The ARM C compiler.

ARM Advanced SIMD Extension

ARM Advanced SIMD Extension is an optional component of ARMv7 architecture. It is a 64/128 bit hybrid SIMD technology targeted at advanced media and signal processing applications and embedded processors. It is implemented as part of the ARM core, but has its own execution pipelines and a register bank that is distinct from the ARM core register bank.

ARM Advanced SIMD Extension supports integer, fixed-point, and single-precision floating-point SIMD operations. These instructions are available in both ARM and Thumb-2.

ARM Advanced SIMD Extension is also known as *ARM NEON Technology* (NEON™).

ARM Developer Suite (ADS)

A suite of software development applications, together with supporting documentation and examples, that enable you to write and debug applications for the ARM family of *RISC* processors. ADS is superseded by RealView Development Suite (RVDS).

See also RealView Development Suite.

ARM eXtended Debugger (AXD)

The *ARM eXtended Debugger* (AXD) is a single-processor debugger that runs on Windows platforms. AXD supports Multi-ICE and RealView ARMulator ISS debug targets with legacy ARM7 and ARM9 core modules.

See also ARM Symbolic Debugger, Multi-ICE®, RealView ARMulator® ISS, *and* RealView Debugger.

ARM instruction A word that encodes an operation for an ARM processor operating in ARM state. ARM instructions must be word-aligned.

See also Thumb® instruction, Thumb-2 instruction, *and* Thumb-2EE instruction.

armlink The ARM linker.

ARM MultiTrace™ External collection unit for ARM Real-Time Trace.

ARM state A processor that is executing ARM instructions is operating in ARM state. The processor switches to Thumb state (and to recognizing Thumb instructions) when directed to do so by a state-changing instruction such as `BX`, `BLX`.

See also Jazelle® state, Thumb state, *and* ThumbEE state.

ARM Symbolic Debugger (armsd)
A command-line debugger that runs on all supported platforms. armsd supports only RealView ARMulator ISS debug targets with legacy ARM7™ and ARM9™ core modules.

See also ARM eXtended Debugger, RealView ARMulator ISS, *and* RealView Debugger.

AXD *See* ARM eXtended Debugger.

Big-endian In the context of the ARM architecture, big-endian is defined as the memory organization in which the least significant byte of a word is at a higher address than the most significant byte.

See also Little-endian.

Board file RealView Debugger uses this term to refer to the top-level configuration file, normally called `rvdebug.brd`, that references one or more other configuration files. A board file contains the connection-level settings and references to any *Board/Chip Definition* (BCD) files assigned to a connection.

Board/Chip Definition (BCD) file
In the context of RealView Debugger, a BCD file enables you to define the memory map and memory mapped registers for a target development board or processor. Various BCD files are provided with RVDS for ARM development boards (for example `AP.bcd`) and processor core modules (for example `CM940T.bcd`).

Breakpoint unit In the context of RealView Debugger, a unit within a Chained breakpoint that combines with other breakpoint units to create a complex breakpoint.

See also Chained breakpoint.

BSABI *See* ABI for the ARM Architecture (base standard).

Canonical Frame Address (CFA)
In DWARF, this is an address on the stack specifying where the call frame of an interrupted function is located.

Captive thread Captive threads are all threads that can be brought under the control of RealView Development Suite. Special threads, called non-captive threads, are essential to the operation of *Running System Debug* (RSD) and so are not under debugger control. Non-captive threads are grayed out in the GUI.

See also Running System Debug.

CFA *See* Canonical Frame Address.

Chained breakpoint In the context of RealView Debugger, a complex breakpoint that comprises multiple breakpoint units.

See also Breakpoint unit.

Chained tracepoint In the context of RealView Debugger, a complex tracepoint that comprises multiple tracepoint units.

See also Tracepoint unit.

CodeWarrior IDE for RVDS
The ARM Limited version of the CodeWarrior *Integrated Development Environment* (IDE) provided with RealView Development Suite. It includes settings panels and stationery specific to the ARM development tools provided with RVDS.

Conditional breakpoint
A breakpoint that has one or more condition qualifiers assigned. The breakpoint is activated when all assigned conditions are met, and either stops or continues execution depending on the action qualifiers that are assigned. The condition normally references the values of program variables that are in scope at the breakpoint location.

See also Data breakpoint, Hardware breakpoint, Instruction breakpoint, Software breakpoint, *and* Unconditional breakpoint.

Core module In the context of the ARM Integrator™, an add-on development board that contains an ARM architecture-based processor and local memory. Core modules can run stand-alone, or can be stacked onto Integrator motherboards.

See also Integrator.

CPSR *See* Current Processor Status Register.

Current Processor Status Register (CPSR)
A register containing the current state of control bits and flags.

See also Saved Processor Status Register.

Data breakpoint A breakpoint that activates when a given location is accessed in a specific way. The breakpoint can also check for a specific data value being access at the given location, if required.

See also Conditional breakpoint, Hardware breakpoint, Instruction breakpoint, Software breakpoint, *and* Unconditional breakpoint.

DCC *See* Debug Communications Channel.

Debug Agent (DA) The Debug Agent resides on the target to provide target-side support for *Running System Debug* (RSD) in RealView Debugger. The Debug Agent can be a thread or built into the RTOS. The Debug Agent and RealView Development Suite communicate with

each other using the *Debug Communications Channel* (DCC). This enables data to be passed between the debugger and the target using the ICE interface, without stopping the program or entering debug state.

See also Running System Debug *and* Debug Communications Channel.

Debug Communications Channel (DCC)
A debug communications channel enables data to be passed between RealView Development Suite and the EmbeddedICE logic on the target using the JTAG interface, without stopping the program flow or entering debug state.

Deprecated A deprecated option or feature is one that you are strongly discouraged from using. Deprecated options and features are to be removed in future versions of the product.

Doubleword In the context of the ARM architecture, a 64-bit unit of information. Contents are taken as being an unsigned integer unless otherwise stated.

DWARF Debug With Arbitrary Record Format.

ELF Executable and Linking Format.

Embedded assembler
Embedded assembler is assembler code that is included in a function, and is separate from other C or C++ functions.

Embedded Trace Buffer™ (ETB™)
The Embedded Trace Buffer provides logic inside the core that extends the information capture functionality of the Embedded Trace Macrocell.

Embedded Trace Macrocell™ (ETM)
A block of logic, embedded in the hardware, that is connected to the address, data, and status signals of the processor. It broadcasts branch addresses, and data and status information in a compressed protocol through the trace port. It contains the resources used to trigger and filter the trace output.

EmbeddedICE® logic
The EmbeddedICE logic is an on-chip logic block that provides TAP-based debug support for ARM architecture-based processors. It is accessed through the TAP controller on the ARM architecture-based processor using the JTAG interface.

See also IEEE1149.1.

Emulator In the context of target connection hardware, an emulator provides an interface to the pins of a real core (emulating the pins to the external world) and enables you to control or manipulate signals on those pins.

ETB *See* Embedded Trace Buffer.

ETM *See* Embedded Trace Macrocell.

ETV *See* Extended Target Visibility.

Execution vehicle Part of the debug target interface, execution vehicles process requests from the client tools to the target.

Execution view The address of regions and sections after the image has been loaded into memory and started execution.

Extended Target Visibility (ETV)
Extended Target Visibility enables RealView Development Suite to access features of the underlying target, such as chip-level details provided by the hardware manufacturer or SoC designer.

Filtering In the context of RealView Debugger Trace, a facility that enables you to refine the results of a trace capture that has already been performed in RealView Debugger. This is useful if you want to refine your area of interest within the display.

FIQ Fast Interrupt.

fromelf The ARM image conversion utility. This accepts ELF format input files and converts them to a variety of output formats. `fromelf` can also generate text information about the input image, such as code and data size.

GCC GNU Compiler Collection.

GDB GNU Debugger.

GPIO General Purpose Input/Output.

Halfword In the context of the ARM architecture, defined as a 16-bit unit of information. Contents are taken as being an unsigned integer unless otherwise stated.

Halted System Debug (HSD)
Usually used for OS aware debugging, *Halted System Debug* (HSD) means that a target can only be debugged when it is not running. Any target must be stopped before carrying out any analysis of the system. With the target stopped, RealView Debugger presents OS awareness information by reading and interpreting target memory.

See also Running System Debug.

Hardware breakpoint

A breakpoint that is implemented using non-intrusive additional hardware. Hardware breakpoints are the only method of halting execution when the location is in *Read Only Memory* (ROM) or Flash. Using a hardware breakpoint often results in the processor halting completely. This is usually undesirable for a real-time system.

See also Conditional breakpoint, Data breakpoint, Instruction breakpoint, Software breakpoint, *and* Unconditional breakpoint.

Hint instruction A hint instruction provides information to the hardware that the hardware can take advantage of. An implementation can choose whether to implement hint instructions or not. If they are not implemented, they execute as `NOP`.

HSD *See* Halted System Debug.

ICE Extension Unit A hardware extension to the EmbeddedICE logic that provides more breakpoint units.

IEEE 1149.1 The IEEE Standard that defines TAP. Commonly (but incorrectly) referred to as JTAG.

Image An executable file that can be loaded onto a processor for execution.

A binary execution file that can be loaded onto a processor and given a thread of execution. An image can have multiple threads. An image is related to the processor that is running the default thread for the image.

Immediate values Values that are encoded directly in the instruction and used as numeric data when the instruction is executed. Many ARM and Thumb instructions enable small numeric values to be encoded as immediate values within the instruction that operates on them.

Implementation defined
In the context of the ARM architecture, this means that the behavior is not architecturally defined, but must be defined and documented by individual implementations.

In-Circuit Emulator A device enabling access to and modification of the signals of a circuit while that circuit is operating.

Input section Contains code or initialized data or describes a fragment of memory that must be set to zero before the application starts.

Instruction breakpoint
A location in the image containing an instruction that, if executed, activates a breakpoint. The breakpoint activation can be delayed by assigning condition qualifiers, and subsequent execution of the image is determined by any actions assigned to the breakpoint.

See also Conditional breakpoint, Data breakpoint, Hardware breakpoint, Software breakpoint, *and* Unconditional breakpoint.

Instruction Register (IR)
When referring to a TAP controller, a register that controls the operation of the TAP.

Instruction Set System Model (ISSM)
In the context of RealView Development Suite, a set of models that simulate the ARM Cortex™ family of processors. These models are provided with RealView Development Suite.

Integrator A range of ARM hardware development platforms. Core modules are available that contain the processor and local memory.

Interworking A method of working that enables branches between ARM and Thumb code.

IRQ Interrupt Request.

ISSM *See* Instruction Set System Model.

IT block A block of up to four instructions following the 16-bit Thumb-2 *If-Then* (`IT`) instruction. Each instruction in the block is conditional. The conditions for the instructions are either all the same, or some can be the inverse of others.

Jazelle The Jazelle architecture extends the existing ARM architecture to enable direct execution of selected JVM (Java Virtual Machine) opcodes.

Jazelle state A processor that is executing Jazelle bytecode instructions is operating in Jazelle state.

See also ARM state, Thumb state, *and* ThumbEE state.

JTAG Joint Test Action Group.

JTAG interface unit In the context of ARM tools, a protocol converter that converts low-level commands from RealView Development Suite into JTAG signals to the processor, for example to the EmbeddedICE logic and the ETM.

Little-endian In the context of the ARM architecture, little-endian is defined as the memory organization in which the most significant byte of a word is at a higher address than the least significant byte.

See also Big-endian.

Load view The address of regions and sections when the image has been loaded into memory but has not yet started execution.

LVDS Low Voltage Digital Signaling.

MaxSim™ Explorer MaxSim Explorer is part of the ARM MaxSim toolset that can be used for fast modeling, simulation and debugging of complex System-on-Chip (SoC) designs. System and processor models created with the MaxSim tools can be debugged with MaxSim Explorer in conjunction with RealView Debugger.

Memory hint In the context of the ARM architecture, a memory hint instruction enables a programmer to provide advance information to memory systems about future memory accesses, without actually loading or storing any data.

Monitor mode In the context of TrustZone®, an ARM mode that is responsible for switching the core between the Secure and Normal state. Do not confuse Monitor mode with *Monitor debug-mode*.

See also Normal world, Normal state, Secure state, Secure world, *and* TrustZone.

MPCore An integrated Symmetric Multiprocessor system (SMP) delivered as a traditional uniprocessor core. The chip contains up to four ARM1136J-S™ based CPUs with cache coherency.

MPU Multi-Processor Unit.

Multi-ICE A JTAG-based tool for debugging embedded systems. Multi-ICE must be purchased as separate product.

MultiTrace Works in conjunction with ARM Multi-ICE to provide real-time trace functionality for software running in leading edge System-on-Chip devices with deeply embedded processor cores. The MultiTrace hardware must be purchased as a separate product.

NEON *See* ARM Advanced SIMD Extension.

Normal state In the context of TrustZone, the processor is in Normal state if the *Secure Configuration Register* (SCR) NS-bit is 1, and the processor is in any mode other than Monitor mode. The core cannot access the Secure world.

See also Monitor mode, Normal world, Secure state, Secure world, *and* TrustZone.

Normal world In the context of TrustZone, all the hardware, both core and system, that is accessible when the core is in Normal state.

See also Monitor mode, Normal state, Secure state, Secure world, *and* TrustZone.

Output section A contiguous sequence of input sections that have the same RO, RW, or ZI attributes. The sections are grouped together in larger fragments called regions. The regions are grouped together into the final executable image.

See also Region.

PC Program Counter.

PCH *See* Precompiled Header.

Precompiled Header (PCH)
A header file that is precompiled. This avoids the compiler having to compile the file each time it is included by source files.

Procedure Call Standard for the ARM Architecture (AAPCS)
Procedure Call Standard for the ARM Architecture defines how registers and the stack will be used for subroutine calls.

Processor Status Register (PSR)
A register containing various control bits and flags.

See also Current Processor Status Register *and* Saved Processor Status Register.

Profiling In the context of RealView Debugger Trace, the accumulation of statistics during execution of a program being debugged, to measure performance or to determine critical areas of code.

Program Counter (PC)
In the context of the ARM architecture, integer register R15.

Program image *See* Image.

Program Status Register (PSR)
Contains some information about the current program and some information about the current processor. Also referred to as Current PSR (CPSR), to emphasize the distinction between it and the Saved PSR (SPSR). The SPSR holds the value the PSR had when the current function was called, and which will be restored when control is returned.

An Enhanced Program Status Register (EPSR) contains an additional bit (the Q bit, signifying saturation) used by some ARM architecture-based processors, including the ARM9E.

PSR *See* Processor Status Register

PU Protection Unit.

RDI *See* Remote Debug Interface.

Read-Only Position Independent (ROPI)
In the context of the ARM architecture, code or read-only data that can be placed at any address.

Read Write Position Independent (RWPI)
In the context of the ARM architecture, read/write data addresses that can be changed at runtime.

RealMonitor A small program that, when integrated into your target application or *Real-Time Operating System* (RTOS), enables you to observe and debug your target while parts of your application continue to run.

RealView ARMulator ISS (RVISS)
One of the ARM simulators supplied with RealView Development Suite.

RVISS is a collection of programs that simulate the instruction sets and architecture of various ARM processors. This provides instruction-accurate simulation and enables ARM and Thumb executable programs to be run on non-native hardware.

RVISS provides modules that model:

- the ARM processor core
- the memory used by the processor.

There are alternative predefined models for each of these parts. However, you can create your own models if a supplied model does not meet your requirements.

See also RealView Simulator Broker.

RealView Compilation Tools (RVCT)
RealView Compilation Tools is a suite of tools, together with supporting documentation and examples, that enables you to write and build applications for the ARM family of *RISC* processors.

RealView Simulator Broker
RealView Simulator Broker is an execution vehicle that enables you to connect to RVISS simulator targets on your local system, or on a remote system. It also enables you to make multiple connections to the simulator.

See also RealView ARMulator ISS.

RealView Debugger The latest debugger software from ARM Limited that enables you to make use of a debug agent in order to examine and control the execution of software running on a debug target. RealView Debugger is supplied in both Windows, Red Hat Linux, and Sun Solaris versions.

RealView Debugger Trace
Part of the RealView Development Suite product that extends the debugging capability with the addition of real-time program and data tracing. It is available from the RealView Debugger Code window.

RealView Development Suite (RVDS)
The latest suite of software development applications, together with supporting documentation and examples, that enable you to write and debug applications for the ARM family of *RISC* processors.

See also ARM Developer Suite.

RealView ICE (RVI) A JTAG-based debug solution to debug software running on ARM architecture-based processors. RealView ICE must be purchased as a separate product.

RealView Trace (RVT)
Works in conjunction with ARM RealView ICE to provide real-time trace functionality for software running in leading edge System-on-Chip devices with deeply embedded processor cores. The RealView Trace hardware must be purchased as a separate product.

Region In an image, a region is a contiguous sequence of one to three output sections (RO, RW, and ZI). A region typically maps onto a physical memory device, such as ROM, RAM, or peripheral.

See also Root region.

Remote Debug Interface (RDI)
The *Remote Debug Interface* (RDI) is an ARM standard procedural interface between a debugger and the debug agent. RDI gives the debugger a uniform way to communicate with:

- a debug monitor running on hardware that is based on an ARM architecture-based processor accessed through a communication link (for example, Angel)
- a debug agent controlling an ARM architecture-based processor through hardware debug support (for example, Multi-ICE).

Remote_A Remote_A is a software protocol converter and configuration interface. It converts between the RDI 1.5 software interface of a debugger and the Angel Debug Protocol used by Angel targets. It can communicate over a serial or Ethernet interface.

ROPI *See* Read-Only Position Independent.

Root region In an image, regions having the same load and execution address. A non-root region is a region that must be copied from its load address to its execution address.

RSD *See* Running System Debug.

Running System Debug (RSD)
Used for OS-aware debugging, *Running System Debug* (RSD) means that a target can be debugged when it is running. This means that the debug target does not have to be stopped before carrying out any analysis of the system. RSD gives access to the application using a *Debug Agent* (DA) that resides on the target. The Debug Agent is scheduled along with other tasks in the system.

See also Debug Agent *and* Halted System Debug.

RVCT *See* RealView Compilation Tools.

RVDS *See* RealView Development Suite.

RVISS *See* RealView ARMulator ISS.

RVT *See* RealView Trace.

RWPI *See* Read Write Position Independent.

Saved Processor Status Register (SPSR)
A register that holds a copy of what was in the Current Processor Status Register before the most recent exception. Each exception mode has its own SPSR.

Scatter-loading Assigning the address and grouping of code and data sections individually rather than using single large blocks.

SDT *See* Software Development Toolkit.

Section In the context of applications targeted at ARM architecture-based processors, a block of software code or data for an Image.

See also Input section *and* Output section.

Secure state In the context of TrustZone, the processor is in Secure state if the *Secure Configuration Register* (SCR) NS-bit is 0, or the processor is in Monitor mode. The core can access both the Secure and Normal worlds.

See also Monitor mode, Normal state, Normal world, Secure world, *and* TrustZone.

Secure World In the context of TrustZone, all the hardware, both core and system, that is only accessible when the core is in Secure state.

See also Monitor mode, Normal state, Normal world, Secure state, *and* TrustZone.

Semihosting A mechanism whereby the target communicates I/O requests made in the application code to the host system, rather than attempting to support the I/O itself.

Supervisor Call (SVC)
An instruction that causes the processor to call a programmer-specified subroutine. Used by the ARM standard C library to handle semihosting. This replaces *software interrupt* (SWI).

Simple tracepoint A type of tracepoint that enables you to set trigger points, trace start and end points, or trace ranges for memory and data accesses.

See also Tracepoints.

Simulator In the context of the ARM tools, a simulator executes non-native instructions in software (simulating a core).

See also Instruction Set System Model, RealView ARMulator ISS.

Software breakpoint A breakpoint that is implemented by replacing an instruction in memory with one that causes the processor to take exceptional action. Because instruction memory must be altered software breakpoints cannot be used where instructions are stored in read-only memory. Using software breakpoints can enable interrupt processing to continue during the breakpoint, making them more suitable for use in real-time systems.

See also Conditional breakpoint, Data breakpoint, Hardware breakpoint, Instruction breakpoint, Software breakpoint, *and* Unconditional breakpoint.

Software Development Toolkit (SDT)
An ARM product, now superseded by ADS and RVCT.

SPSR Saved Program Status Register.

See also Program Status Register.

Stack Pointer (SP) Integer register R13.

SVC *See* Supervisor Call.

SWI *See* Supervisor Call.

TAP *See* Test Access Port.

TAP Controller Logic on a device which enables access to some or all of that device for test purposes. The circuit functionality is defined in IEEE1149.1.

See also Test Access Port *and* IEEE1149.1.

TAPOp The name of the interface API between the Multi-ICE Server and its clients.

Target Access In the context of RealView Debugger, the access point to the Target Vehicle used as the interface between RealView Debugger and the target hardware.

Target Vehicle Target vehicles provide RealView Development Suite with a standard interface to disparate targets so that the debugger can connect easily to new target types without having to make changes to the debugger core software.

TCM Tightly Coupled Memory.

TDI Test Data Input.

TDO Test Data Output.

Thumb instruction One halfword or two halfwords that encode an operation for an ARM architecture-based processor operating in Thumb state. Thumb instructions must be halfword-aligned.

See also ARM instruction, Thumb-2 instruction, *and* Thumb-2EE instruction.

Thumb state A processor that is executing Thumb instructions is operating in Thumb state. The processor switches to ARM state (and to recognizing ARM instructions) when directed to do so by a state-changing instruction such as `BX`, `BLX`.

See also ARM state, Jazelle state, *and* ThumbEE state.

Thumb-2 instruction Thumb-2 is a major enhancement of the Thumb instruction set, and is defined by ARMv6T2 and ARMv7M architectures. Thumb-2 provides almost exactly the same functionality as the ARM instruction set. It has both 16-bit and 32-bit instructions, and achieves performance similar to ARM code, but with code density similar to Thumb code.

See also ARM instruction, Thumb instruction, *and* Thumb-2EE instruction.

Thumb-2EE instruction
Thumb-2 Execution Environment (Thumb-2EE) is defined by ARMv7 architecture. The Thumb-2EE instruction set is based on Thumb-2, with some changes and additions to make it a better target for dynamically generated code, that is, code compiled on the device either shortly before or during execution.

See also ARM instruction, Thumb instruction, *and* Thumb-2 instruction.

ThumbEE state A processor that is executing Thumb-2EE instructions is operating in ThumbEE state. In this state, the instruction set is almost identical to the Thumb instruction set. However, some instructions have modified behavior, some instructions are not available, and some new instructions become available.

See also ARM state, Jazelle state, *and* Thumb state.

Tracepoint A tracepoint can be set on a line of source code, a line of assembly code, or a memory address. In RealView Development Suite, you can set a variety of tracepoints to determine exactly what program information is traced.

Tracepoint unit In the context of RealView Debugger, a unit within a Chained tracepoint that combines with other tracepoint units to create a complex tracepoint.

See also Chained tracepoint.

Trigger In the context of breakpoints, a trigger is the action of noticing that the breakpoint has been reached by the target and that any associated conditions are met.

In the context of tracing, a trigger is an event that instructs the debugger to stop collecting trace and display the trace information around the trigger position, without halting the processor. The exact information that is displayed depends on the position of the trigger within the buffer.

TrustZone ARM technology-optimized software that provides a secure execution environment to enable trusted programs and data to be separated from the operating system and applications.

See also Monitor mode, Normal state, Normal world, Secure state, *and* Secure world.

Unconditional breakpoint
A breakpoint that does not have a conditional qualifier assigned. The breakpoint activates immediately it is hit, but subsequent image execution is determined by any actions assigned to the breakpoint.

See also Conditional breakpoint, Data breakpoint, Hardware breakpoint, Instruction breakpoint, Software breakpoint, *and* Unconditional breakpoint.

Undefined In the context of the ARM architecture, an attempt to execute an undefined instruction causes an Undefined Instruction exception.

Unpredictable In the context of the ARM architecture, the result of an unpredictable instruction cannot be relied upon. Unpredictable instructions or results must not represent security holes. Unpredictable instructions must not halt or hang the processor, or any parts of the system.

Vector Floating Point (VFP)
A standard for floating-point coprocessors where several data values can be processed by a single instruction.

Veneer In the context of the ARM architecture, a small block of code used with subroutine calls when there is a requirement to change processor state or branch to an address that cannot be reached in the current processor state.

VFP *See* Vector Floating Point.

VLSI Very Large Scale Integration.

Watch In RealView Debugger, a watch is a variable or expression that you require the debugger to display at every step or breakpoint so that you can see how its value changes. The Watch pane is part of the RealView Debugger Code window. It displays the watchpoints you have defined.

Watchpoint In RealView Development Suite, this is a hardware breakpoint.

Word In the context of the ARM architecture, a word holds a value held in four contiguous bytes. A 32-bit unit of information. Contents are taken as being an unsigned integer unless otherwise stated.

