Release notes for System Registers for Arm A-profile Architecture

2025-03

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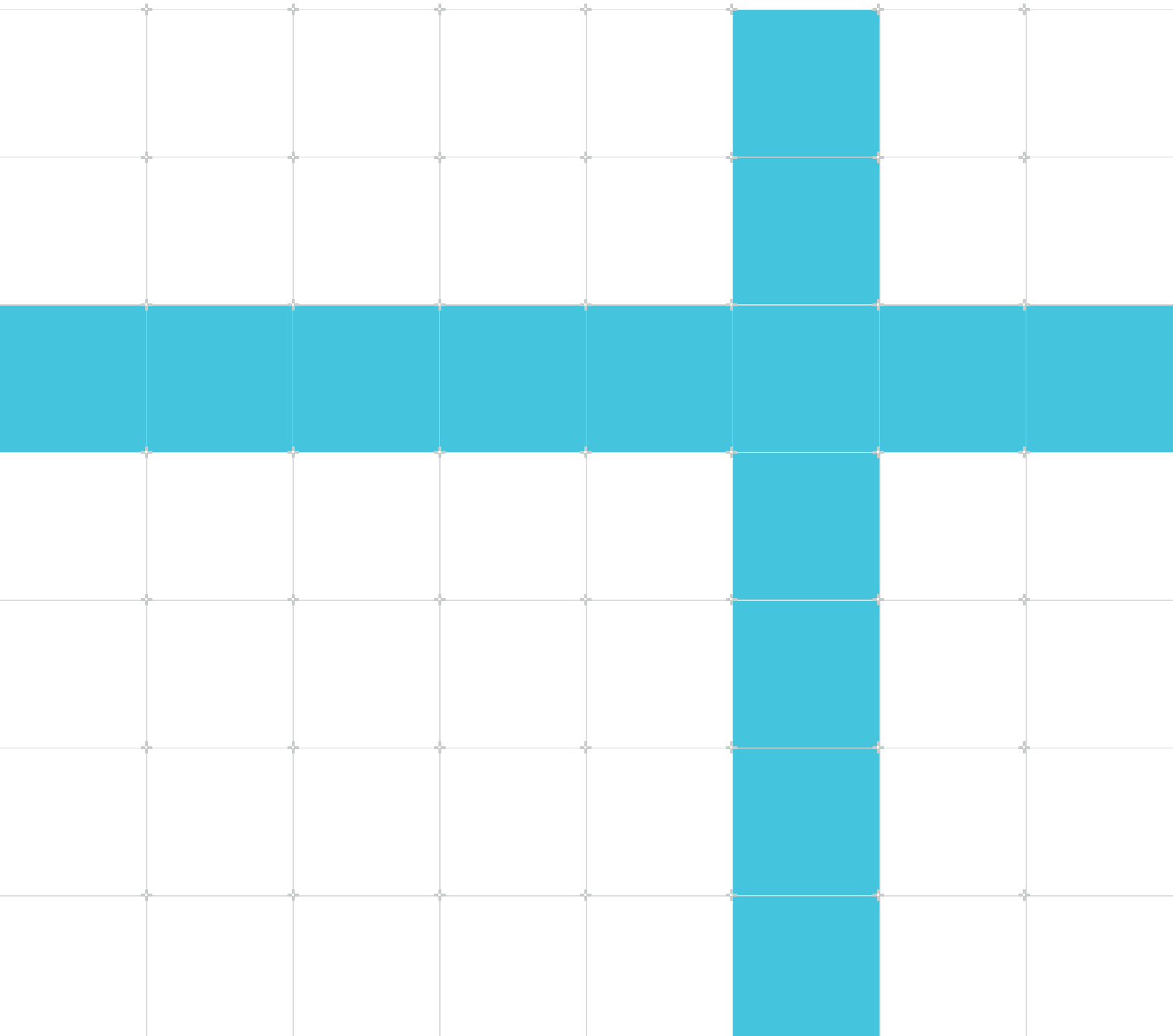

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Release information

Document history

Issue	Date	Confidentiality	Change
2024_25-01	26 March 2025	Non-Confidential	2025-03 release
2024_12-01	17 December 2024	Non-Confidential	2024-12 release
2024_09-01	30 September 2024	Non-Confidential	2024-09 release
2024_06-01	5 July 2024	Non-Confidential	2024-06 release
2024_03-01	27 March 2024	Non-Confidential	2024-03 release
2023_12-01	19 December 2023	Non-Confidential	2023-12 release
2023_09-01	29 September 2023	Non-Confidential	2023-09 release

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1. Release notes for System Register XML for A-Profile Architecture (2025-03)

The information relating to the 2024 Extensions is at Alpha quality. Alpha quality means that most major features of the specification are described in this release, but some features and details might be missing. The information relating to the rest of the A-profile Architecture is at Beta quality. Beta quality means that all major features of the specification are described, but some details might be missing.

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Change history

- The memory-mapped register ERRGSR is now an array of registers ERRGSR<m>.
- DBGDOSLSR.OSLM field is updated to indicate it is IMPLEMENTATION DEFINED.
- CNTVOFF_EL2 description is corrected to refer to the virtual counter.
- PMZR.F0 description is corrected to indicate the fine grained-trap HDFGWTR2_EL2.nPMICNTR_EL0 affects the access to the field.
- The description of the ID_AA64ISAR2_EL1.RPRES field is updated to clarify that it only affects single-precision reciprocal and reciprocal square root instructions.
- SCTLR_EL1.UCI is updated to include instructions added by FEAT_OCCMO.
- The access text of the DC Invalidate by address instructions that refers to access at EL0 has been corrected to require write access permission to the Virtual Address.
- GIC ICV register pages that include ICC encodings are corrected to be identical to the ICC encoding accessors in the ICC register pages.
- The field HCR_EL2.MIOCNCE is deprecated and made Reserved, **RES0**.
- External registers ERRCRICR2, ERRERICR2, and ERRFHICR2 are updated to indicate they are all 32-bit registers.
- The description of the ISS encoding in ESR_EL1, ESR_EL2 and ESR_EL3 are corrected to include instructions introduced by FEAT_PAuth_LR.
- TCR_ELx value constraints on FEAT_D128 are removed.
- Generic timer accessor conditions that test SCR_EL3.ECVEn=='1' are updated to also test for EL3.
- The description of the ERRPIDR4.SIZE field is corrected to include FEAT_RASSAv2.
- The configuration of the external PMZR_EL0 register is corrected to indicate that it is present when FEAT_PMUv3_EXT32 is implemented.

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- The condition on SCR_EL3.TID5 is updated to be FEAT_IDTE3 and FEAT_MTE2.
- Instruction cache maintenance behavior when CTR_EL0.DIC is 1 is clarified.
- The SMIDR_EL1 description in field NSMC, is corrected to read SMCUs instead of SCMUs.
- The EDSCR.RW description is corrected to remove the incorrect Exception Levels and state the correct ones when the current Security State is implemented and enabled.
- The access text of the GICx_ICACTIVER<n>{E} registers has been updated to include a statement about writes becoming visible within a finite time. The access text of the GICx_ISACTIVER<n>{E} registers has also been clarified to write, that after reading back the value written, a subsequent deactivate generated by the CPU interface is ordered after the write to the registers.
- The PnCH field descriptions in TCR_EL3, TCR2_EL1 and TCR2_EL2 are corrected to remove the incorrect descriptions for the Protected bit and Contiguous bit.
- The field description for RGSR_EL1.SEED is corrected to indicate that it is used for generating values returned by the function RandomTag().
- The HCR_EL2 description in the field HCD, is corrected to apply to EL2 and EL1.
- In TCR_EL1.E0PD1, the TTBR0_EL1 is corrected to TTBR1_EL1 when FEAT_E0PD is implemented.
- The field descriptions in SMCR_EL{1,2}.FA64 are corrected to account for HCR_EL2.{E2H,TGE} and to align with the function IsFullA64Enabled().
- PMPCSCTL accessors are updated to remove the reference to the function AllowExternalPMUAccess().
- The description of the HCR_EL2.TPCP field is updated to clarify that trapping applies only to instructions that are capable of being trapped, rather than assuming all specified instructions are always trapped.
- Inconsistent use of terminology when referring to ESR_ELx.EC is updated to refer to EC syndrome value.
- The description of HCRX_EL2.MCE2 is updated to remove references to behavior when HCR_EL2.TGE is 1.

Many simple clarifications and corrections are also present, but are too small to be listed here. Some minor formatting changes are suppressed and not highlighted in the diff output.

Known issues

All issues identified in the below list will be fixed in a future release.

- Accessibility for RAS registers will be relaxed to remove traps when there is a minimal RASv2 implementation.
- The description of PMSIDR_EL1.FDS will be updated to say the feature FEAT_SPE_FDS is not mandatory if PMSIDR_EL1.LDS is 0.
- Corresponding SET and CLR registers will be mapped to each other.
- MPAMBW2_EL2.{TRAP_MPAMBWIDR_EL1, TRAP_MPAMBW0_EL1, TRAP_MPAMBW1_EL1, TRAP_MPAMBWSM_EL1} trap fields will be renamed {nTRAP_MPAMBWIDR_EL1,

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nTRAP_MPAMBW0_EL1, nTRAP_MPAMBW1_EL1, nTRAP_MPAMBWSM_EL1}. MPAMBW3_EL3.TRAPLOWER trap field will be renamed nTRAPLOWER.

- MPAMBWIDR_EL1.{US_INT,US_FRAC} will be deleted.
- Bits 43:40 of GPTBR_EL3 will be an extension to the BADDR field.
- The PMEVTYPER<n>_EL0.MT field description will be clarified to describe whether cycles are counted when the event is true for any of, all of, or the sum across all affected PEs.
- ID_AA64PFR0_EL1.RAS will be updated to remove the requirement to implement RAS System Architecture.

Potential Upcoming Changes

Arm is constantly exploring ways to make the architecture presentation precise and clear. Towards this, the following changes are expected in future releases:

- Accessibility of unimplemented registers in indexed register arrays will be improved.
- Accessibility for memory mapped accesses to registers will be improved.
- Accessibility when there is a width mismatch between the accessor and the register will be improved.
- Configurability details will be captured more formally to define features, acceptable feature choices, and mapping of features to ID registers.

The details of the architecture are presented in pseudocode in Architecture Specification Language (ASL). Arm is defining a new version of the Architecture Specification Language, ASL1, to improve and expand the capabilities of the language. Please see https://developer.arm.com/Architectures/Architecture%20Specification%20Language for details on this language. Arm will be publishing an equivalent release in ASL1 format later in 2025.

Intention and quality statements for all ArmARM architecture releases

The intention and scope of the Architecture releases is to describe changes from the existing architecture to the next release. The quality of the architecture releases refers to the accuracy and completeness of the changes described in the specifications.

The intention and scope of the XML releases is to describe the content and behavior of the registers, system registers, instructions, pseudocode and features of the architecture in full, for human readers in a way that enables correct information for the current or any previous release can be deduced. The quality of the XML releases refers to the accuracy and completeness of the content to a human reader.

The intention and scope of the JSON releases is to describe aspects of the XML releases in a structured, machine readable format. The content of the architectural content will be approximately equivalent to the corresponding XML release. However there are some aspects of the architecture which cannot yet be represented in a machine readable format.

The intention and scope of the Schema for the JSON releases is to describe the syntax and format of the json files used in the json releases. The schema is still under development and is subject to change.

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