ARM®

PrimeCell® Infrastructure AMBA™ 3 AXI™ Downwards-synchronizing Bridge (BP133) Revision: r0p0 **Technical Overview**

This technical overview describes the functionality of the AXI downwards-synchronizing bridge in the following sections:

1 Preliminary material

1.1 Release information

Changes to this document are listed in Table 1.

Table 1 Change history

Date	Issue	Change
29 November 2004	A	First issue for r0p0

1.2 Proprietary notice

1.3 Confidentiality status

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1.4 Product status

The information in this document is final, that is for a developed product.

1.5 Web address

`http://www.arm.com`

2 About the AXI downwards-synchronizing bridge

The AXI downwards-synchronizing bridge, SyncDnAxi, enables a fast AXI clock domain to communicate with a slower one using a common clock select.

Figure 1 shows SyncDnAxi used in a system where an AXI master is running at 200MHz and an AXI slave is running at 100MHz.

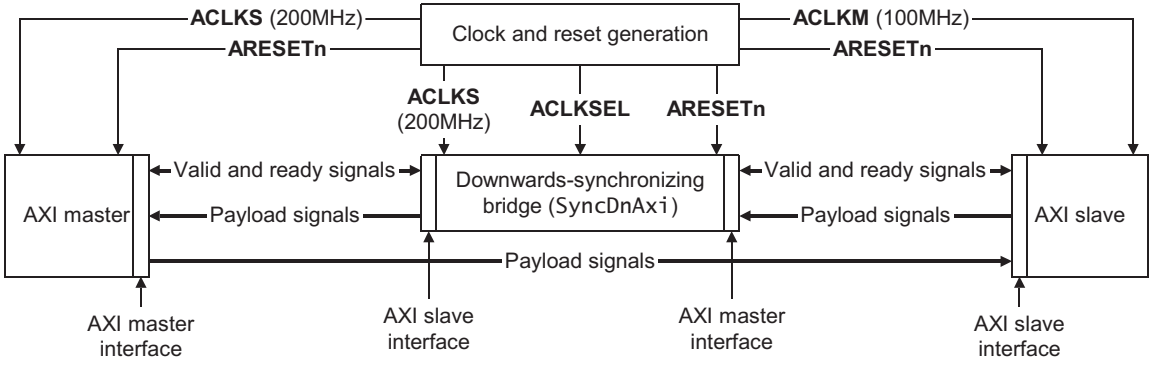

Figure 1 Downwards-synchronizing bridge block diagram

The SyncDnAxi n:1 bridge has the following features:

- n:1 clock synchronizing using a common clock select input where n is an integer greater than or equal to one
- **CSYSREQ**, **CSYSACK**, and **CACTIVE** are synchronized on the low-power interface
- synchronizes the channel flow control signals on the AXI interface:
  - **AW** Write address channel.
  - **W** Write data channel.
  - **B** Write response channel.
  - **AR** Read address channel.
  - **R** Read data channel.
- only the handshake signals are synchronized on the write address, write, and read address channels
- buffered synchronization of the write response and read channels
- the HDL code is supplied as Verilog.

3 Functional description

Figure 2 shows a block diagram of the major internal component blocks.

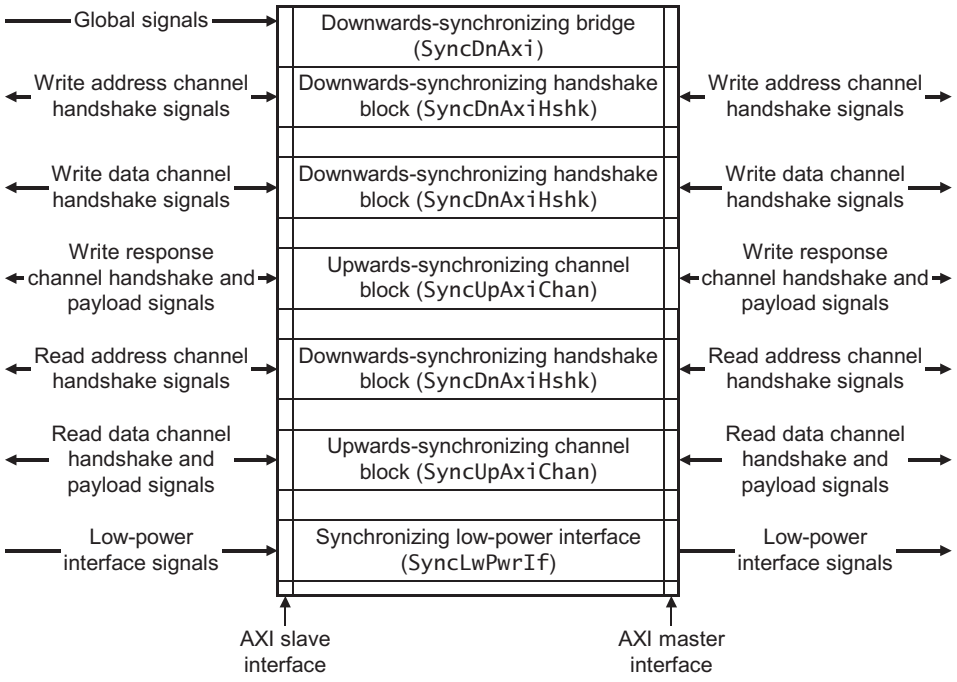

Figure 2 AXI downwards-synchronizing bridge components

The major internal component blocks are:

`SyncDnAxiHshk`

This is an AXI downwards-synchronizing handshake block. The inputs and outputs are not registered. The block synchronizes the valid and ready signal handshakes in a system where the transfer source component is clocked at a higher frequency than the transfer destination component. The clock domains must be synchronously related so that the clock select occurs over the coincidental rising edges.

The `SyncDnAxiHshk` block is used for the AXI channels shown in Figure 2.

`SyncUpAxiChan`

This is an AXI upwards-synchronizing channel block. The inputs and outputs are not registered. The block synchronizes the valid and ready signal handshakes in a system where the transfer source component is

clocked at a lower frequency than the transfer destination component. A zero latency buffer is used to synchronize the write response and read channels. The clock domains must be synchronously related so that the clock select occurs over the coincidental rising edges.

The `SyncUpAxiHshk` block is used for the AXI channels shown in Figure 2 on page 4.

`SyncLwPwrIf`

The AXI low-power signaling mechanism provides a coherent control method for a system-level power-down mode.

For systems that require multiple related clock domains, a low-power mode-aware component can sit in a different clock domain to that of the system low-power controller. The synchronizing low-power interface, `SyncDnLwPwrIf`, ensures that transfers across these boundaries can complete. The interface retimes the **CSYSREQ**, **CSYSACK**, and **CACTIVE** signals between the clock domains. All low-power channel signals are retimed to supply a definite timing point for implementation, and to ensure satisfactory synchronization in both domains.

See the *AMBA AXI Protocol Specification* for more information.

3.1 Interface attributes

The master and slave interface attributes for the AXI downwards-synchronizing bridge are described in:

- Table 2
- Table 3 on page 6.

Table 2 Master interface attributes

Attribute	Description	Value
Write ID capability	The maximum number of different **AWID** values that a master can generate for all active write transactions at any one time	Master-dependent
Write ID width	The number of bits in the **AWID** and **WID** buses.	Master-dependent
Write issuing capability	The maximum number of active write transactions that a master can generate.	Master-dependent

Table 2 Master interface attributes (continued)

Attribute	Description	Value
Read ID capability	The maximum number of different **ARID** values that a master can generate for all active read transactions at any one time.	Master-dependent
Read ID width	The number of bits in the **ARID** bus.	Master-dependent
Read issuing capability	The maximum number of active read transactions that a master can generate.	Master-dependent

Table 3 Slave interface attributes

Attribute	Description	Value
Write acceptance capability	The maximum number of active write transactions that a slave can accept.	Slave-dependent
Read acceptance capability	The maximum number of active read transactions that a slave can accept.	Slave-dependent
Write interleave depth	The number of active write transactions for which the slave can receive data. This is counted from the earliest transaction.	Slave-dependent
Read data reorder depth	The number of active read transactions for which a slave may transmit data. This is counted from the earliest transaction.	Slave-dependent

Note

Master-dependent and slave-dependent used in the Value column of Table 2 on page 5 and Table 3 mean that the bridge adopts the attribute value of the master or slave that the relevant interface is connected to.

4 Physical data

This section describes:

- *AC characteristics*
- *Gate count*.

4.1 AC characteristics

The downwards-synchronizing bridge adheres to the following timing guidelines. The figures refer to the percentage of clock cycle allowed for each function:

- inputs to registers must be valid for 40% prior to the rising edge of the fast clock
- outputs from registers must be valid for 20% after the rising edge of the fast clock
- combinatorial paths must not take longer than 10% of the complete fast clock cycle.

Note

If the component is used only for clock ratios > 1:1, you can relax these constraints accordingly.

Timing characteristics are confirmed by performing synthesis on the block using the slow-slow process point of the Artisan SAGE HS library for the TSMC CL013G process at a target speed of 200MHz.

4.2 Gate count

Total gate count is approximately 1190 NAND2x1 equivalent gates with respect to the library described in *AC characteristics*.

Note

The gate count estimate does not include scan logic.

5 Signal descriptions

Figure 3 shows the AXI downwards-synchronizing bridge signal connections.

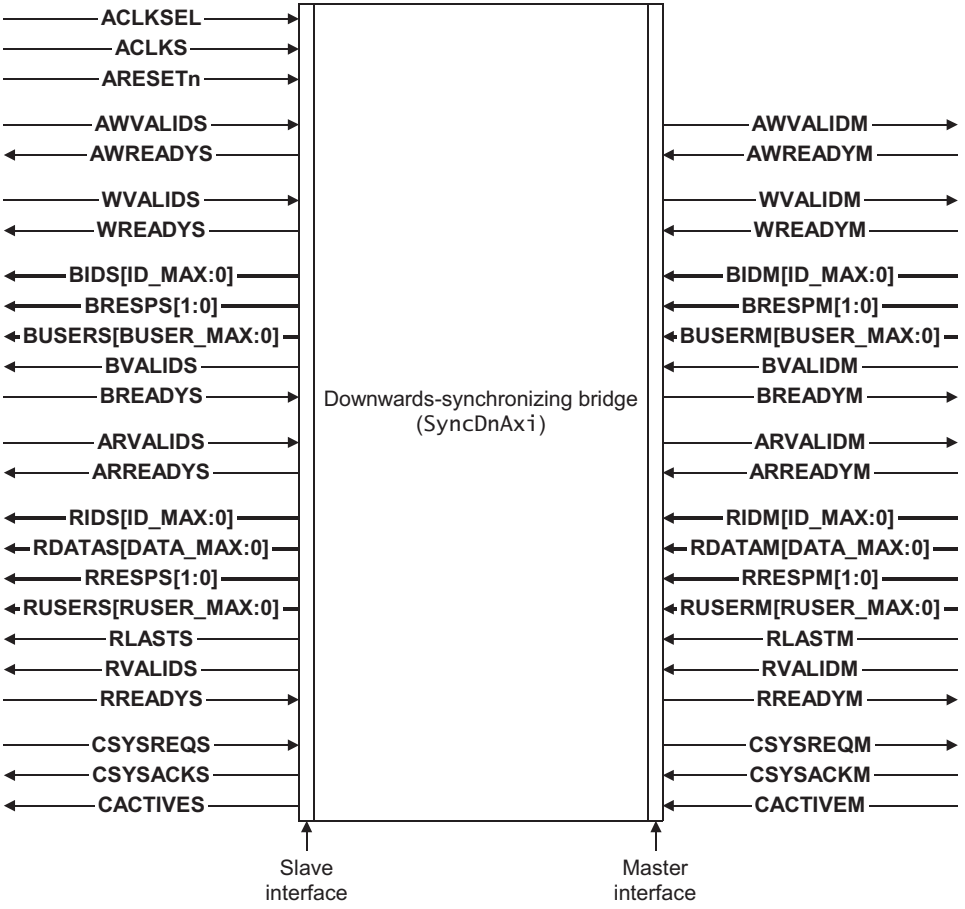

Figure 3 Downwards-synchronizing bridge signal connections

Note

In Figure 3:

- The read channel, write channel, and low-power interface signals are standard AMBA AXI signals as described in the *AMBA AXI Protocol Specification*. The signal names are appended with:
  - — the letter **M** for signals that connect to the component master interface
  - — the letter **S** for signals that connect to the component slave interface.

- The scan signals are not shown.

Table 4 lists the non-standard AXI and scan signals.

Table 4 Non-standard signals

Name	Type	Source/ destination	Description
ACLKS	Input	Clock source	Clock signal from the faster clock domain
ACLKSEL	Input	Clock source	Select signal that indicates the relationship between the fast and slow clocks
SCANENABLE	Input	Scan logic	Scan mode enable
SCANINACLKS	Input	Scan logic	Scan chain clock input
SCANOUTACLKS	Output	Scan logic	Scan chain clock output

